

**CORA, Model :COR152-US, Utility Board
Assembly # 111551774C**

REVISIONS			
REV	ECN	DATE	CHECKED

SEE CPI MRP DATABASE FOR CHANGE HISTORY AFTER INITIAL DESIGN RELEASE

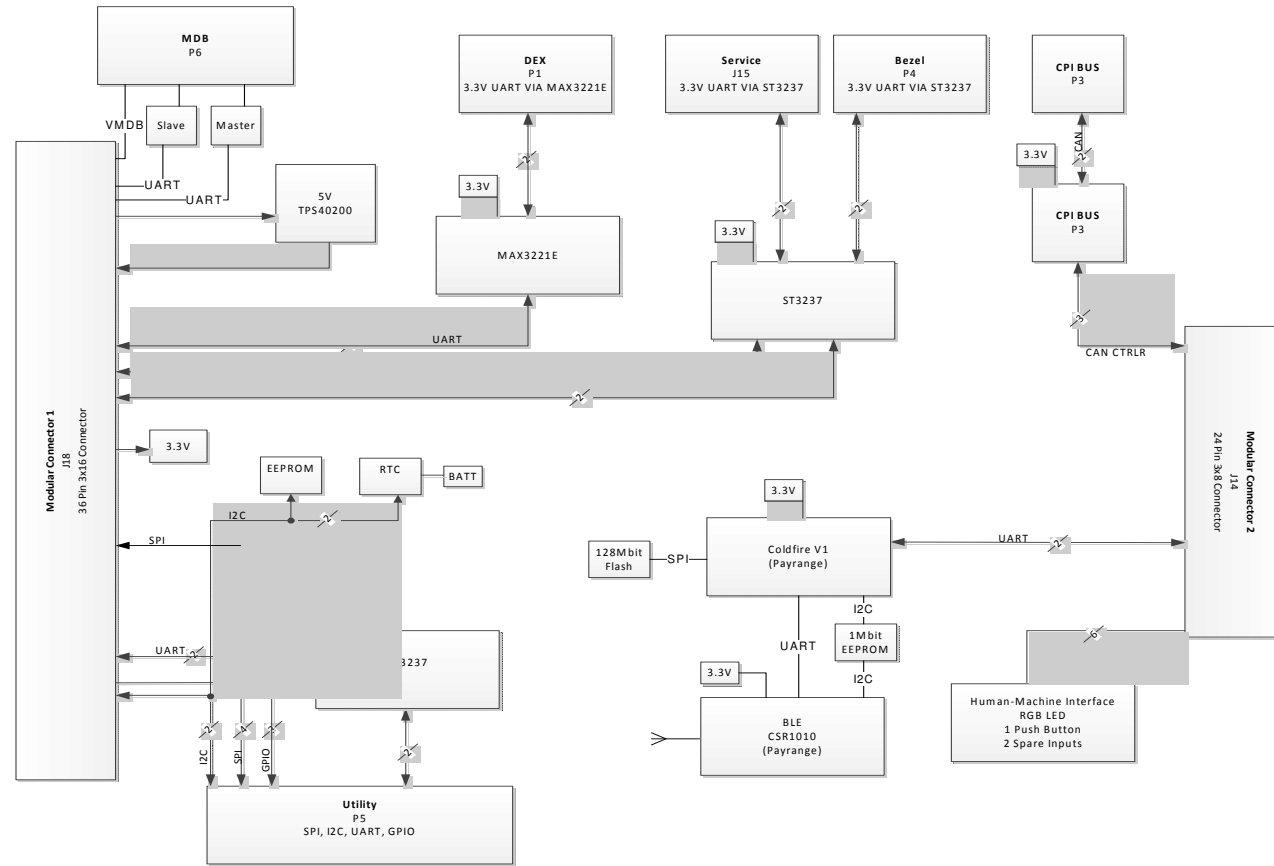
Applicable Site(s) : MVN
 Alliance MDB+PayRange Utility PCBA Hardware Design
 Subject : Document

REF : 300002382C
 ECN : ISSUE G1
 Page : 1 of 1



Title : Alliance MDB+PayRange Utility PCBA Hardware Design Document
 Number : 300002382C
 Issue : G1
 Date : September 12, 2018
 Authors : M. Perreca
 File : 300002382Cg1 Hardware Design Document.doc

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MECHANICAL PARTS



CIRCUIT DESIGN NOTEBOOK

LAST REVISED
 DATE: 9/19/2018
 TIME: 8:51:59 AM

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	<p>DRAWN: Mike Perreca</p> <p>CHECKED: Tony Radice</p>		<p>TITLE: Alliance MDB+PayRange Utility PCB Block Diagram</p>
	<p>PROJECT ENGINEER: Tony Radice</p>	<p>DATE: -</p>	<p>SIZE: C</p> <p>DESIGN CENTER: MVN</p> <p>DOC CL: CD</p> <p>DWG NO.: 300002382C</p> <p>REV: G1</p>
	<p>SCALE: 1/1</p>	<p>VOLUME: (CUBIC MM)</p>	<p>SHEET 1 OF 10</p>

Revision History:

SK R1	11/2017	Initial Development - Project Alliance, Utility Variant "Conan"	MP
SK R2	1/2018	Corrected ColdFire Footprint	MP
SK R3	3/2018	Fixed AP/Vendo Dex Issues	MP
Y1	4/2018	Adjusted P6 to Navigator Pinout Added MDB Master Overvoltage Protection	MP

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Design Checklist

- PC Board Stackup
- 1 - S1 - (TOP) "Component" Layer; Signal 1
 - 2 - G1 - Ground Reference Layer;
 - 3 - P1 - Power Layer; (Floods Only)
 - 4 - S2 - (BOTTOM) Signal Layer

- Notes:
- 1: NO signal traces permitted on Ground layer or power layer
 - 2: Connections to ground (bypass caps) should minimize inductance.
ie: Use largest trace width b/t pad & via practical.
 - 3: Board should predominantly use RF Design Rules, especially in BLE region
 - 4: Gate drives for FETs should be run with floods, not traces.
 - 5: Nets with prefix "V" should be run with floods, not traces.
 - 6: Many Testpoints have the reference designator (TP) NOT Visible. They may be toggled to visible as required. This is done to reduce schematic clutter.

Utility Variant Table

PCB P/N	Code Name	Module Connection	MDB Slave	MDB Master	BLE	DEX	Bezel	Service	EEPROM	RTC	PayRange	CPI Bus		
300002382C	Conan	1x 36Pin 3Row 1x 24Pin 3Row	X	X	X	X	X	X	X	X	X	X		



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TITLE: Alliance MDB+PayRange Utility PCB Variant Table

SIZE: C	DESIGN CENTER: MVN	DOC CL: CD	DWG NO: 300002382C	REV: G1
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SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 2 OF 10

MDB Voltage for the 5V supply is through J18 Pins 25 and 26.
The Processor PCBAs shorts these two pins to complete the circuit
To prevent the supply from being on without the processor board installed

+5V Supply

<https://analogtools.ti.com/SwitcherPro/Main>
Input: VMin: 18, VMax: 50
VOut: 5 IOut: 5A Max Pulsed
Specify: TPS40200, NTF5116PL FET

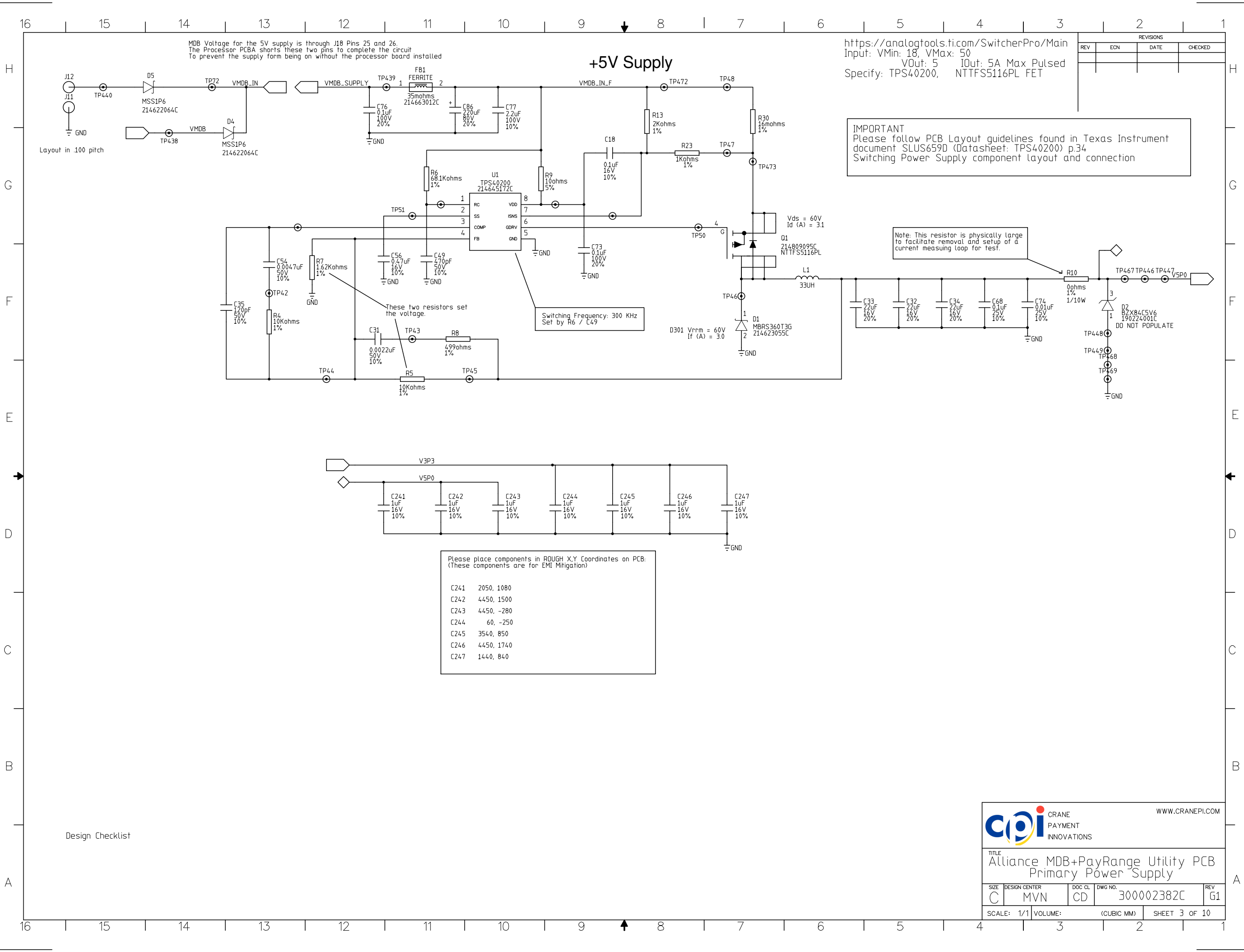
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IMPORTANT
Please follow PCB Layout guidelines found in Texas Instrument document SLUS659D (Datasheet: TPS40200) p.34
Switching Power Supply component layout and connection

Note: This resistor is physically large to facilitate removal and setup of a current measuring loop for test.

Switching Frequency: 300 KHz
Set by R6 / C49

These two resistors set the voltage.



Please place components in ROUGH X,Y Coordinates on PCB:
(These components are for EMI Mitigation)

C241	2050, 1080
C242	4450, 1500
C243	4450, -280
C244	60, -250
C245	3540, 850
C246	4450, 1740
C247	1440, 840

Design Checklist

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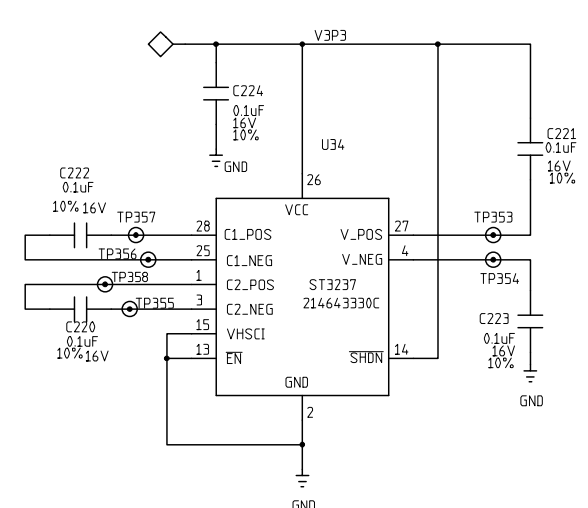
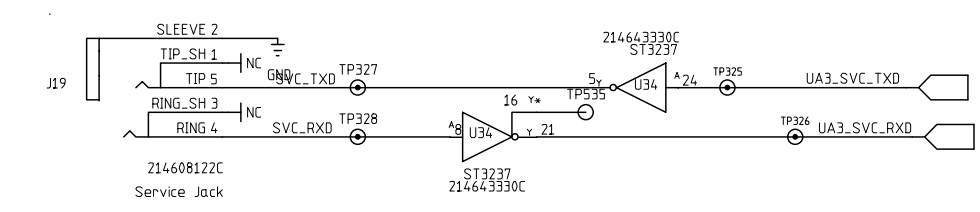
cpi CRANE PAYMENT INNOVATIONS

TITLE: Alliance MDB+PayRange Utility PCB Primary Power Supply

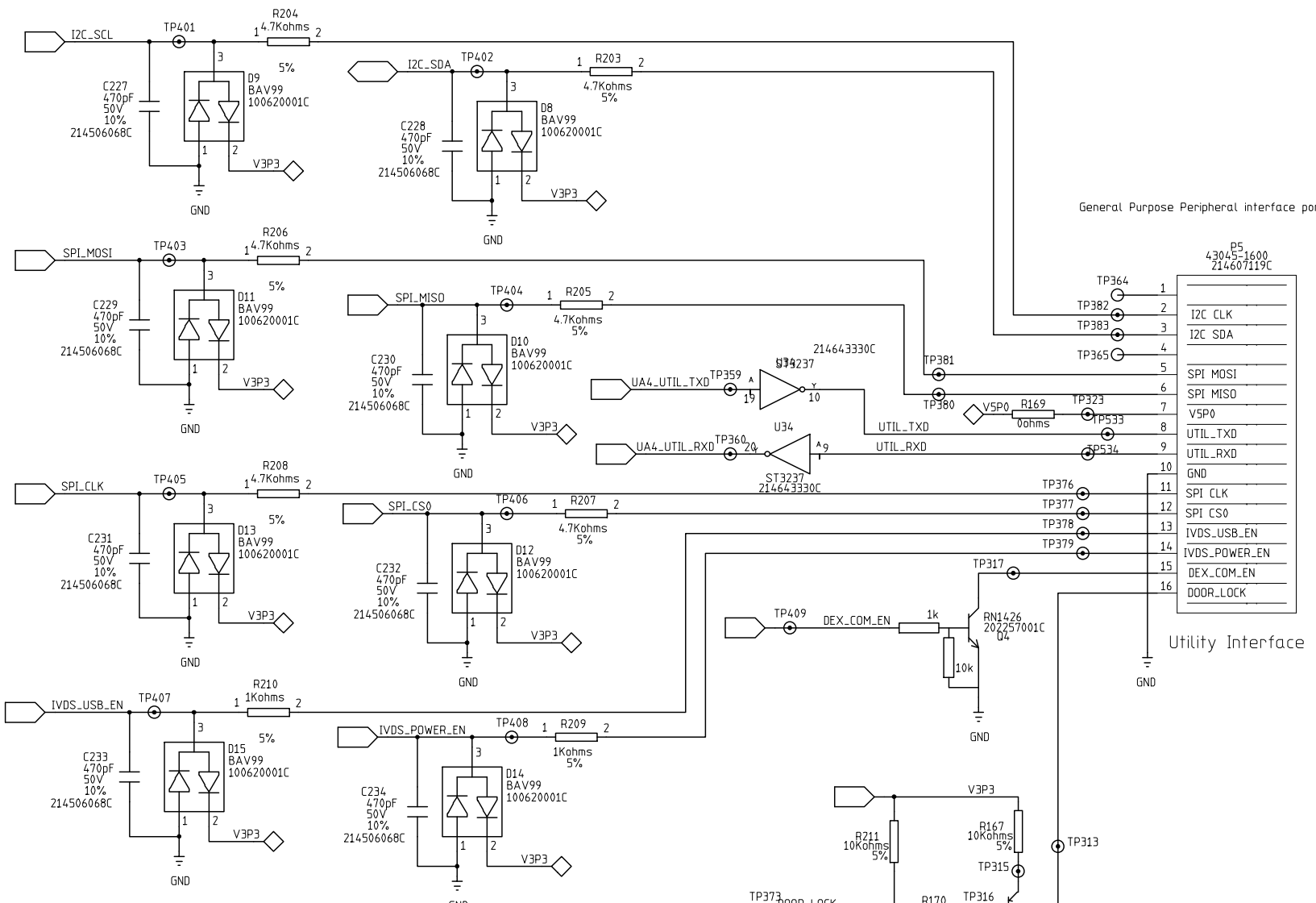
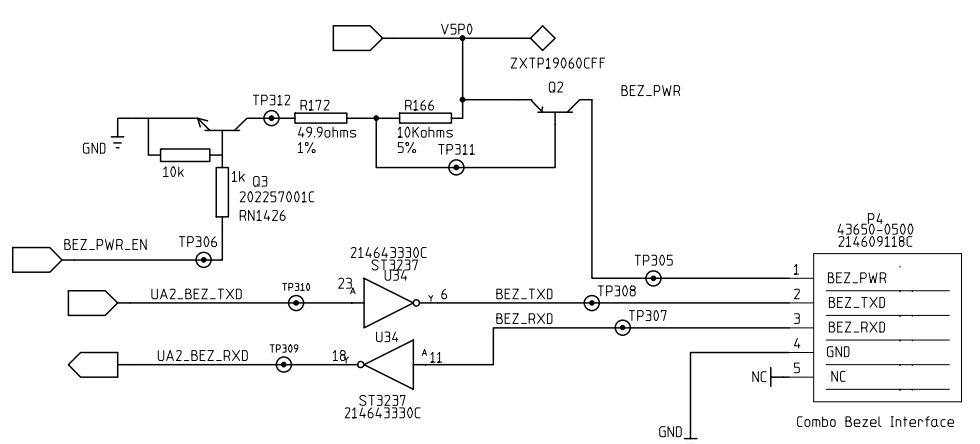
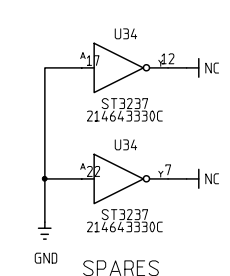
SIZE: C	DESIGN CENTER: MVN	DOC CL: CD	DWG NO: 300002382C	REV: G1
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SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 3 OF 10

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NOTE: ST3237 ESD Protection Level: 15KV



P5	
Pin	Signal
1	I2C CLK
2	I2C SDA
3	SPI MOSI
4	SPI MISO
5	V5P0
6	UTIL_TXD
7	UTIL_RXD
8	GND
9	SPI CLK
10	SPI CS0
11	IVDS_USB_EN
12	IVDS_POWER_EN
13	DEX_COM_EN
14	DOOR_LOCK

Design Checklist
(...)

GPIO Assignments	Notes
	Extern Power Supply Enable
13 GP2P4	IVDS USB Mode
14 GP2P5	IVDS Power Enable
15 GP2P6	NECTA Communications Enable
16 GP2P7	Door Lock

DATE: 8/3/2016
TIME: 2:17:35 PM

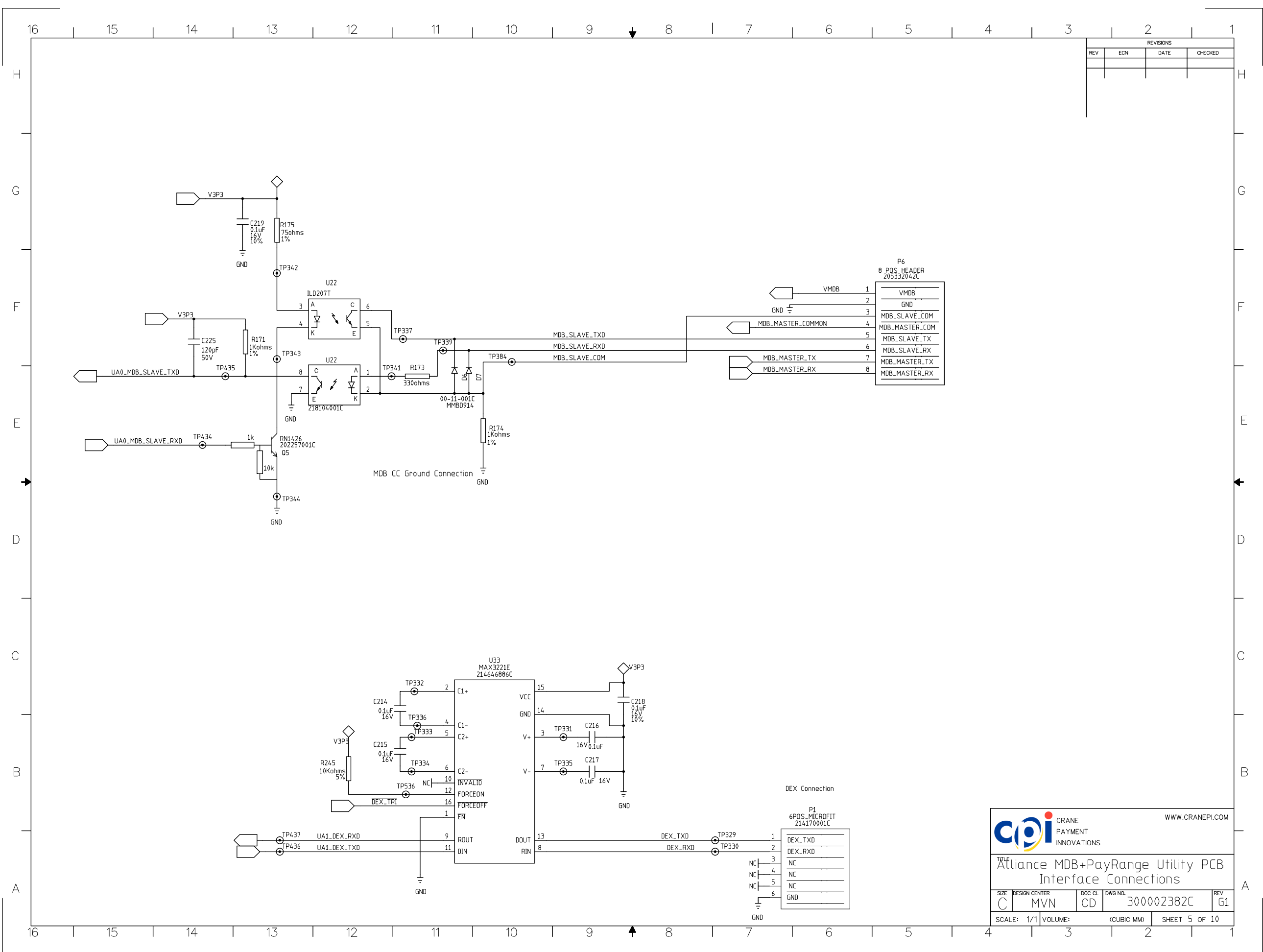
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TITLE: Alliance MDB + PayRange Utility PCB Interface Connections

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300002382C	G1

SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 4 OF 10



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P6
8 POS HEADER
205332042C

1	VMDB
2	GND
3	MDB_SLAVE_COM
4	MDB_MASTER_COMMON
5	MDB_SLAVE_TX
6	MDB_SLAVE_RX
7	MDB_MASTER_TX
8	MDB_MASTER_RX

DEX Connection

P1
6POS_MICROFIT
214170001C

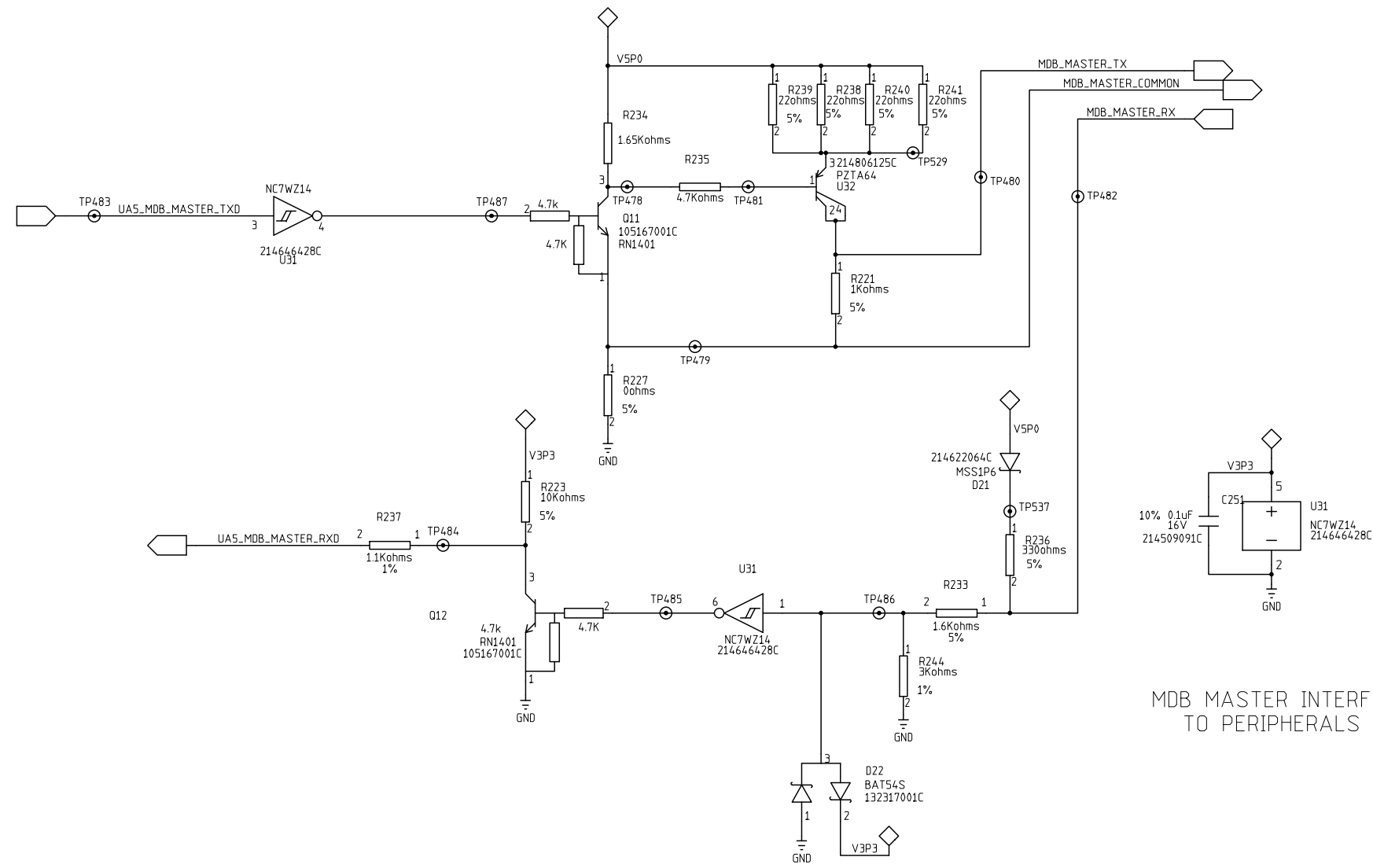
1	DEX_TXD
2	DEX_RXD
3	NC
4	NC
5	NC
6	GND

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Alliance MDB+PayRange Utility PCB Interface Connections

SIZE C	DESIGN CENTER MVN	DOC CL CD	DWG NO. 300002382C	REV G1
SCALE: 1/1		VOLUME: (CUBIC MM)		SHEET 5 OF 10

REVISIONS			
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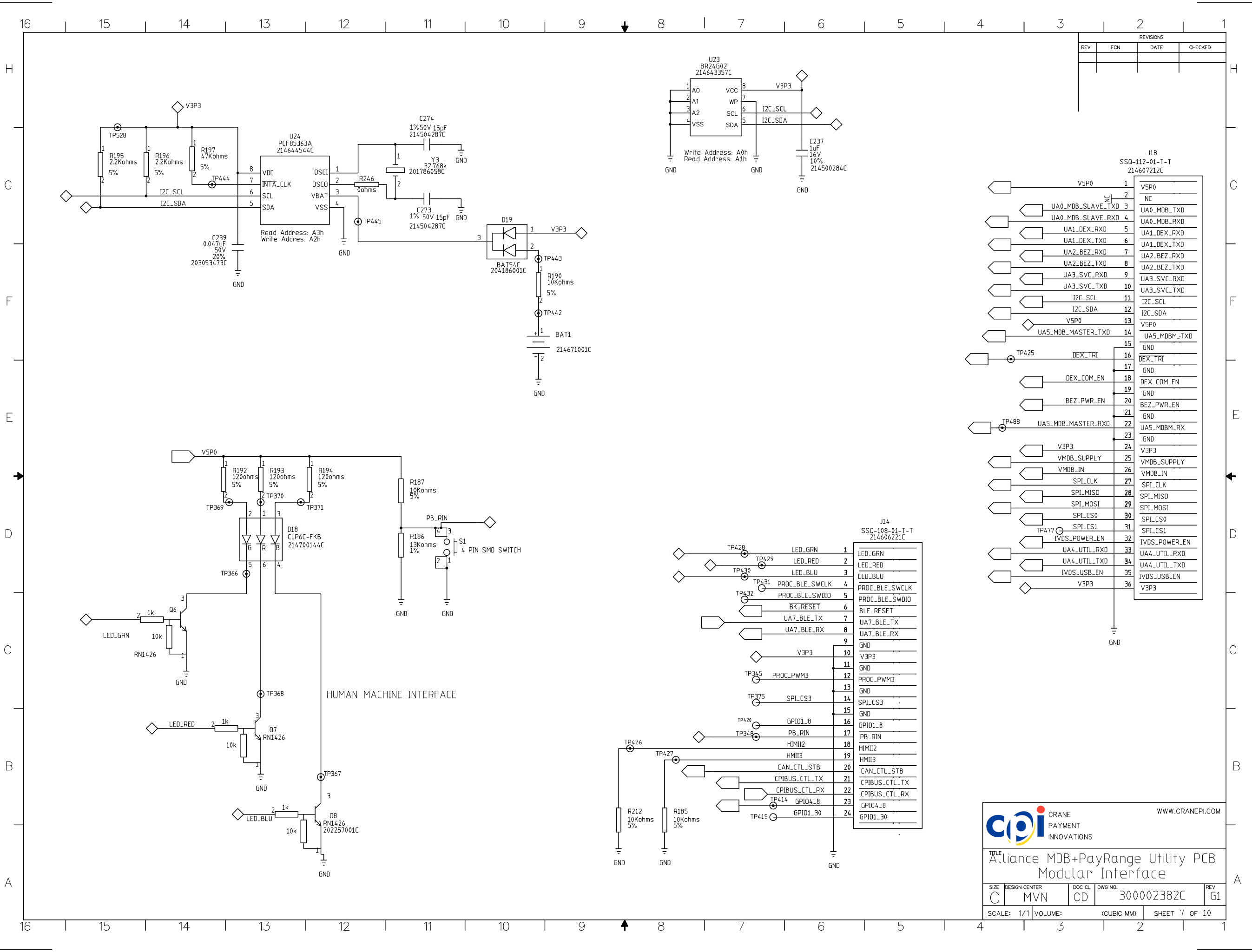
MDB MASTER INTERFACE TO PERIPHERALS


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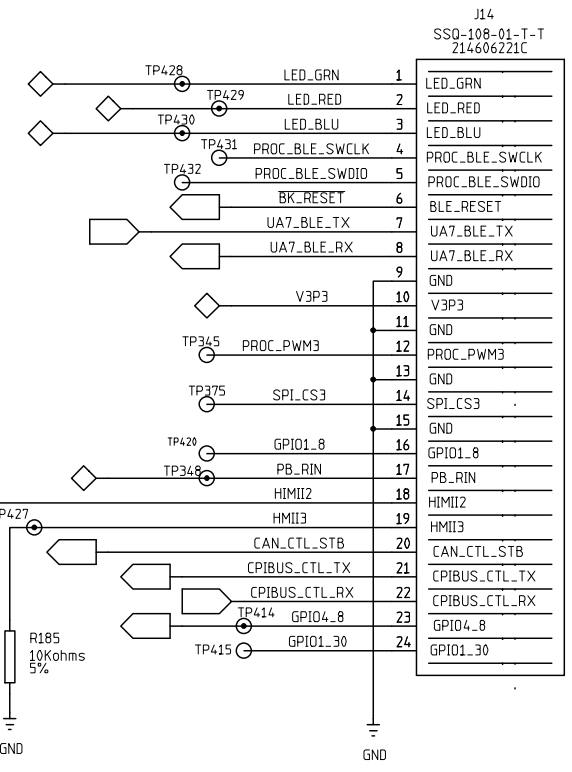
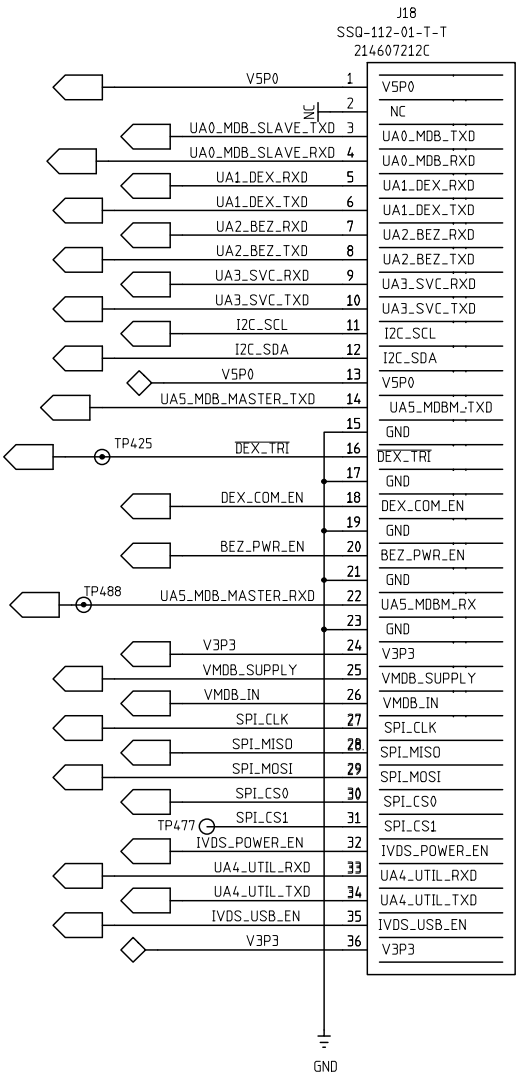
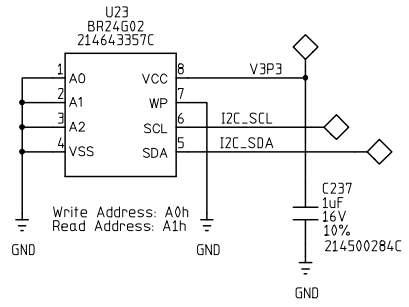
TITLE
 Alliance MDB+PayRange Utility PCB
 MDB Master Interface

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300002382C	G1

SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 6 OF 10



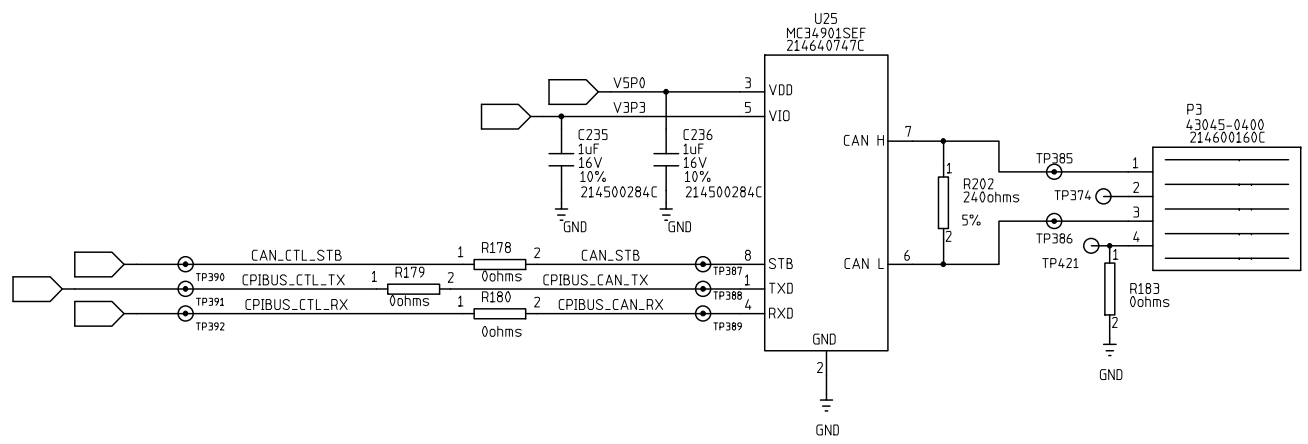
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 Alliance MDB+PayRange Utility PCB
 Modular Interface
 SIZE: C DESIGN CENTER: MVN DOC CL: CD DWG NO.: 300002382C REV: G1
 SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 7 OF 10

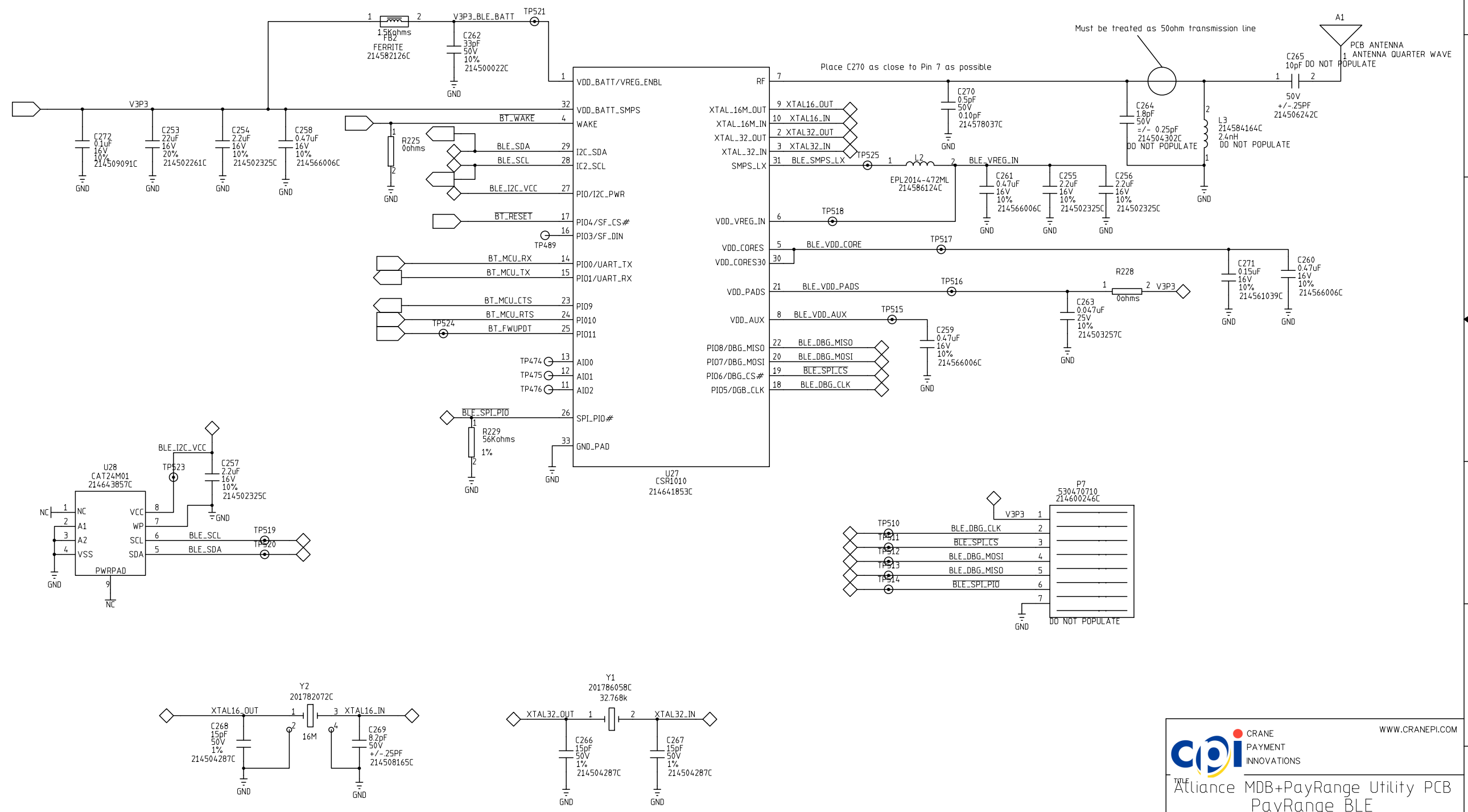
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CPI BUS CAN Option



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<p>ALLIANCE MDB+PayRange Utility PCB CPI Bus</p>			
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C	MVN	CD	300002382C
SCALE: 1/1		VOLUME:	REV
		(CUBIC MM)	G1
		SHEET 8 OF	10

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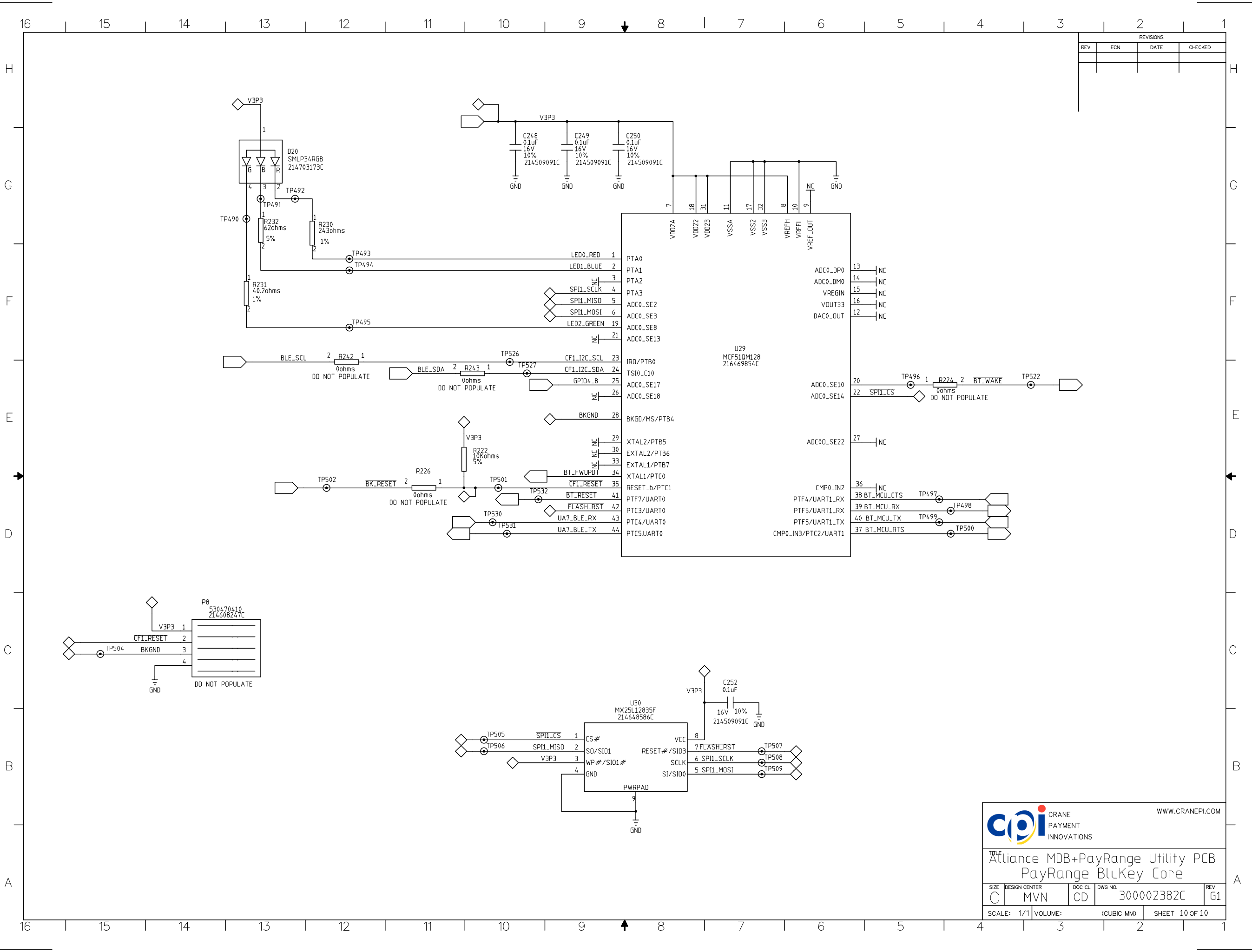
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PAYMENT INNOVATIONS

Alliance MDB+PayRange Utility PCB
PayRange BLE

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300002382C	G1

SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 9 OF 10

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FILE Alliance MDB+PayRange Utility PCB
 PayRange BluKey Core

SIZE	DESIGN CENTER	DOC CL	DWG NO.	REV
C	MVN	CD	300002382C	G1

SCALE: 1/1 VOLUME: (CUBIC MM) SHEET 10 OF 10