

Data Sheet		
Version 1.9		
Thursday, April	06, 2000	5

WT12-A



Copyright © 2000-2006 Bluegiga Technologies

All rights reserved.

Bluegiga Technologies assumes no responsibility for any errors, which may appear in this manual. Furthermore, Bluegiga Technologies reserves the right to alter the hardware, software, and/or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. Bluegiga Technologies' products are not authorized for use as critical components in life support devices or systems.

The WRAP is a registered trademark of Bluegiga Technologies

The *Bluetooth* trademark is owned by the *Bluetooth* SIG Inc., USA, and is licensed to Bluegiga Technologies.

All other trademarks listed herein are owned by their respective owners.

Contents:

1.	Devi	ice Features Overview
2.	Gene	eral Description5
2	.1 Phy	ysical Outlook5
2	.2 Blo	ock Diagram and Descriptions6
	2.2.1	BlueCore046
	2.2.2	Crystal7
	2.2.3	Flash7
	2.2.4	Balun/Filter
	2.2.5	Matching7
	2.2.6	Antenna7
	2.2.7	USB7
	2.2.8	Synchronous Serial Interface7
	2.2.9	UART7
	2.2.10	Audio PCM Interface7
	2.2.11	Programmable I/O7
	2.2.12	Reset7
	2.2.13	802.11 Coexistence Interface7
2	.3 Ap	plications8
3.	Phys	sical Layer Specifications9
4.	Gene	eral Specifications 10
5.	Elec	trical Charasteristics 12
6.	WT1	2 PIN description
7.	Foot	: print 15
8.	Phys	sical Dimensions17
9.	Phys	sical Interfaces 18
9	.1 UA	RT Interface
	9.1.1	UART Configuration While RESET is Active21
	9.1.2	UART Bypass Mode21

9.1.3	Current Consumption in UART Bypass Mode21
9.2 US	B Interface22
9.2.1	USB Data Connections
9.2.2	USB Pull-Up Resistor
9.2.3	Power Supply22
9.2.4	Self Powered Mode 22
9.2.5	Bus Powered Mode24
9.2.6	Suspend Current24
9.2.7	Detach and Wake-Up Signaling25
9.2.8	USB Driver
9.2.9	USB 1.1 Compliance
9.2.10	USB 2.0 Compatibility26
9.3 SP	I Interface
9.4 I/C	Parallel Ports
10. Rese	et 27
11. Soft	ware Stacks 27
11.1	iWRAP Stack
12. Cont	act Information 30

1. DEVICE FEATURES OVERVIEW

- Fully Qualified Bluetooth system v2.0 + EDR, CE and FCC
- Integrated chip antenna
- Industrial temperature range from -40°C to +85°C
- Enhanced Data Rate (EDR) compliant with v2.0.E.2 of specification for both 2Mbps and 3Mbps modulation modes
- RoHS Compliant
- Full Speed Bluetooth Operation with Full Piconet
- Scatternet Support
- USB version 2.0 compatible
- UART with bypass mode
- Support for 802.11 Coexistence
- 8Mbits Flash Memory

2. GENERAL DESCRIPTION

2.1 Physical Outlook



Figure 1: Physical outlook of WT12

Chip Matching antenna Balun & Filter UART SPI PC M BlueCore04 USB PIO RESET Śс +3.3V 8 MBit 26 MHz Flash Memory Crystal WRAP THOR WT12

2.2 Block Diagram and Descriptions

Figure 2: Block Diagram of WT12

2.2.1 BlueCore04

BlueCore4 is a single chip Bluetooth solution which implements the Bluetooth radio transceiver and also an on chip microcontroller. BlueCore4 implements Bluetooth® 2.0+EDR (Enhanced Data Rate) and it can deliver data rates up to 3 Mbps.

The microcontroller (MCU) on BlueCore04 acts as interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

BlueCore04 has 48Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

2.2.2 Crystal

The crystal oscillates at 26MHz.

2.2.3 Flash

Flash memory is used for storing the Bluetooth protocol stack and Virtual Machine applications. It can also to the optional external RAM for memory intensive applications.

2.2.4 Balun/Filter

Combined balun and filter changes the balanced input/output signal of the module to unbalanced signal of the monopole antenna. The filter is a band pass filter (ISM band).

2.2.5 Matching

Antenna matching components match the antenna to 50 Ohms.

2.2.6 Antenna

The antenna is ACX AT3216 chip antenna.

2.2.7 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. WT12 acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

2.2.8 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory.

2.2.9 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

2.2.10 Audio PCM Interface

The audio pulse code modulation (PCM) Interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

2.2.11 Programmable I/O

WT12 has a total of 6 digital programmable I/O terminals. These are controlled by firmware running on the device.

2.2.12 Reset

This can be used to reset WT12.

2.2.13 802.11 Coexistence Interface

Dedicated hardware is provided to implement a variety of coexistence schemes. Channel skipping AFH (Adaptive Frequency Hopping), priority signaling, channel signaling and host passing of channel instructions are all supported. The features are configured in firmware.

Since the details of some methods are proprietary (e.g. Intel WCS) please contact Bluegiga for details.

2.3 Applications

WT12 Bluetooth module is designed for:

- Hand held terminals
- Industrial devices
- Point-of-Sale systems
- PCs
- Personal Digital Assistants (PDAs)
- Computer Accessories
- Access Points
- Automotive Diagnostics Units

3. PHYSICAL LAYER SPECIFICATIONS

Item	Specification
Operating Frequency	2400 MHz to 2483.5 MHz (ISM-Band)
Carrier Spacing	1.0 MHz
Channels	79
Duplexing	TDD
Symbol Rate	1 Msymbol/s
	Binary one: Positive frequency deviation
TX Modulation Polarity	Binary zero: Negative frequency deviation
DV Data Out Polarity	F _c + dF: "H"
RX Data Out Polarity	F _c - dF: "L"

The common physical layer specifications are shown in the table below.

Table 1: Common physical layer specifications

4. GENERAL SPECIFICATIONS

Item	Specification
Supply voltage	3.3 V \pm 0.1 V regulated voltage. (Noise < 10 mV_{P-P})
Supply current	Maximum current in TX mode: 70.0mA Maximum current in RX mode: 70.0mA
Frequency range	2400 MHz 2483.5 MHz (ISM-Band)
Guard band	2 MHz < F < 3.5 MHz (Europe, Japan, USA)
Carrier frequency	2402 MHz 2480 MHz, F = 2402 + k MHz, k = 0 78
Modulation method	GFSK (1 Mbps), $\Pi/4$ DQPSK (2Mbps) and 8DQPSK (3Mbps)
Hopping	1600 hops/s, 1 MHz channel space
	GFSK:
	Asynchronous, 723.2 kbps / 57.6 kbps
	Synchronous: 433.9 kbps / 433.9 kbps
	П/4 DQPSK:
Maximum data rate	Asynchronous, 1448.5 kbps / 115.2 kbps
	Synchronous: 869.7 kbps / 869.7 kbps
	8DQPSK:
	Asynchronous, 2178.1 kbps / 177.2 kbps
	Synchronous: 1306.9 kbps / 1306.9 kbps
Receiving signal range	-82 to -20 dBm (Typical)
Receiver IF frequency	1.5 MHz (Center frequency)

Transmission power	Minimum: -119 dBm Maximum +1 +3 dBm
RF input impedance	50 Ω
Baseband crystal OSC	26 MHz
Output interfaces	6 GPIO, PCM, SPI, UART, USB
Operation temperature	-40°C +85°C
Storage temperature	-40°C +105°C
Compliance	Bluetooth specification, version 2.0 + EDR
USB specification	USB specification, version 1.2

Table 2: General specifications

5. ELECTRICAL CHARASTERISTICS

Rating	Min	Мах
Storage temperature	-40°C	+150°C

Table 3: Absolute Maximum Ratings

Operating conditions	Min	Мах
Operating Temperature Range:	-40°C	+85°C
Supply Voltage: VDD	3.2V	3.4V

Table 4: Recommended Operating Conditions

Digital terminals	Min	Тур	Max	Unit
Input voltage				
V_{IL} input logic level low (VDD=3.3V)	-0.4		+0.8	V
V_{IH} input logic level high	0.7VDD		VDD+0.1	V
Output voltage				
V_{OL} output logic level low (VDD=3.3V) (I _{o =} 3.0mA)			0.2	V
V_{OL} output logic level high (VDD=3.3V) ($I_{o} = -3.0mA$)	VDD-0.2			V

 Table 5: Input/Output Terminal Characteristics

6. WT12 PIN DESCRIPTION

The PIN description of WT12 is shown in the table below.

No.	Pin name	I/O	Description
1	GND	GND	Ground
2	3V3	VDD	Power supply connection
3	PIO2	I/O	Programmable I/O lines
4	PIO3	I/O	Programmable I/O lines
5	NRTS	0	UART RTS (internal pull-up, active low)
6	RXD	Ι	UART RX (internal pull down)
7	РСМО	0	Synchronous 8 kbps data out (internal Pull down)
8	USB_D+	A	USB data plus (Internal 22 ohm serial resistor)
9	USB_D-	А	USB data minus (Internal 22 ohm serial resistor)
10	NCTS	Ι	UART CTS (internal pull down, active low)
11	PCMI	Ι	Synchronous 8 kbps data in (internal pull-down)
12	РСМС	I/O	Synchronous data clock (internal pull-down)
13	PCMS	I/O	Synchronous data strobe (internal pull-down)
14	GND	GND	Ground
15	GND	GND	Ground
16	3V3	VDD	Power supply connection
17	RES	Ι	Reset input (active high)

-	1		· · · · · · · · · · · · · · · · · · ·
18	PIO6	I/O	Programmable I/O lines
19	PIO7	I/O	Programmable I/O lines
20	PIO4	I/O	Programmable I/O lines
21	NCSB	I	Chip selection for SPI (internal pull up, active low)
22	SCLK	I/O	SPI Clock (internal pull down)
23	MISO	0	SPI data output (pull down)
24	MOSI	Ι	SPI data input (pull down)
25	PIO5	I/O	Programmable I/O lines
26	TXD	0	UART TX (internal pull up)
27	NC	-	NC, not used in WT12-A module
28	GND	GND	Ground
29	GND	GND	Ground
30	NC	NC	Not used in WT12-A module
31	GND	GND	Ground

Table 6: WT1	2 PIN configuratior	n
---------------------	---------------------	---

Notes: Voltage level of input (I), output (O) and input/output (I/O) pins is 3.3V.

7. FOOT PRINT

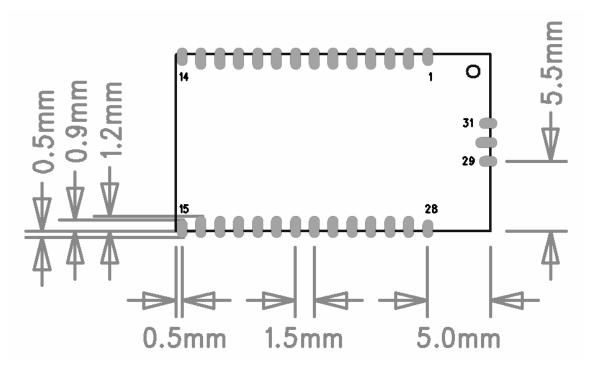


Figure 3: WT12 foot print and dimension

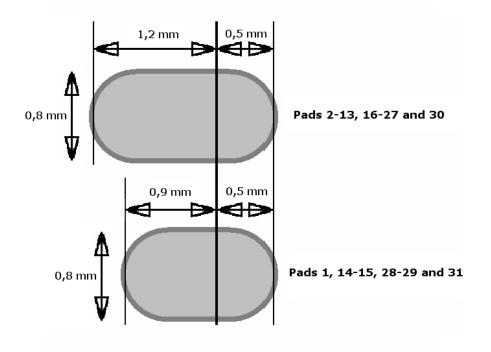


Figure 4: WT12 pad dimensions

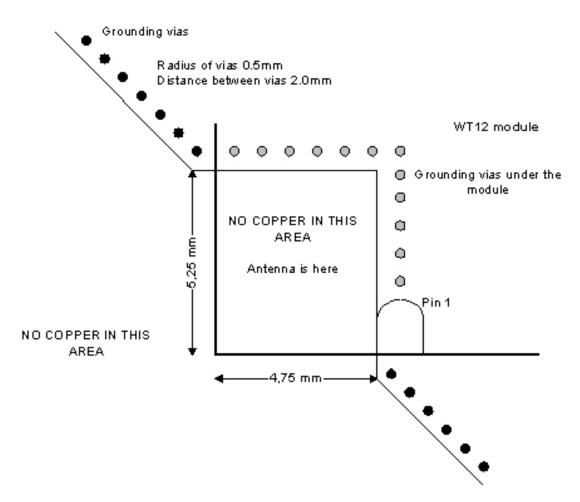


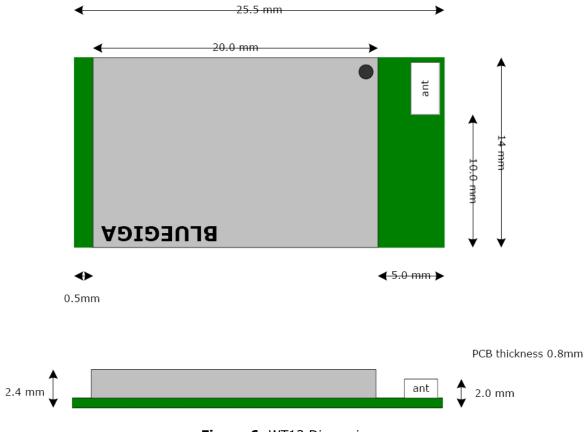
Figure 5: PCB design around ACX antenna

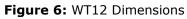
Figure four above illustrates how PCB design around the antenna of WT12 should be made. The most important thing is that there is no copper (ground plane or traces) underneath or in the close proximity of the ACX antenna.

It's also very important to have grounding vias all the way in the border between ground plane and free space, as illustrated with black and gray dots in figure 4. This prevents the RF signal for reflecting back to the PCB and signal lines over there.

For more information, please refer to the WT12 design guide and design references.

8. PHYSICAL DIMENSIONS





9. PHYSICAL INTERFACES

9.1 UART Interface

WT12 Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 standard¹.

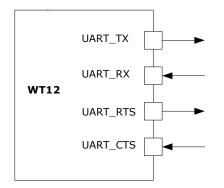


Figure 7: WT12 UART interface

Four signals are used to implement the UART function, as shown in Figure 11.12. When WT12 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signaling levels of 0V and VDD_PADS.

UART configuration parameters, such as Baud rate and packet format, are set using iWRAP software.

Notes:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

1. Uses RS232 protocol but voltage levels are 0V to VDD_USB, (requires external RS232 transceiver chip)

Parameter		Possible values
Baud rate	Minimum	1200 baud (d2%Error)
		9600 baud (d1%Error)
	Maximum	3.0Mbaud (d1%Error)
Flow control		RTS/CTS, none

Parity	None, Odd, Even
Number of stop bits	1 or 2
Bits per channel	8

Figure 8: Possible UART settings

The UART interface is capable of resetting WT12 upon reception of a break signal. A Break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure below If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialize the system to a known state. Also, WT12 can emit a Break character that may be used to wake the Host.



Figure 9: Break signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 15 shows a list of commonly used Baud rates and their associated values for the Persistent Store Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any Baud rate within the supported range can be set in the Persistent Store Key according to the formula in Equation below.

Baud Rate = <u>PSKEY_UART_BAUD_RATE</u> 0.004096

Figure 10: Baud rate calculation formula

	Persistent		
Baud rate	Нех	Dec	Error
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2765800	0x2c3d	11325	0.00%

Table 7: UART baud rates and error values

9.1.1 UART Configuration While RESET is Active

The UART interface for WT12 while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when WT12reset is deasserted and the firmware begins to run.

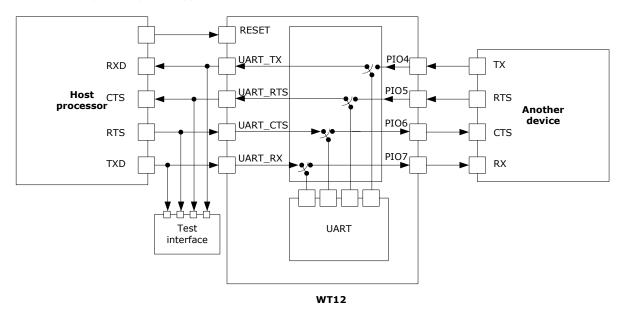
9.1.2 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on WT12 can be used. The default state of WT12 after reset is de-asserted, this is for the host UART bus to be connected to the WT12 UART, thereby allowing communication to WT12 via the UART.

In order to apply the UART bypass mode, a BCCMD command will be issued to WT12 upon this, it will switch the bypass to PIO[7:4] as shown in Figure 6. Once the bypass mode has been invoked, WT12 will enter the deep sleep state indefinitely.

In order to re-establish communication with WT12, the chip must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.





9.1.3 Current Consumption in UART Bypass Mode

The current consumption for a device in UART Bypass Mode is equal to the values quoted for a device in standby mode.

9.2 USB Interface

WT12 USB devices contain a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth v2.0 + EDR specification or alternatively can appear as a set of endpoint appropriate to USB audio devices such as speakers.

As USB is a Master/Slave oriented system (in common with other USB peripherals), WT12 only supports USB Slave operation.

9.2.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the WT12 and therefore have low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors are included with USB_DP / USB_DN and the cable.

9.2.2 USB Pull-Up Resistor

WT12 features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when

WT12 is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device. The USB internal pull-up is implemented as a current source, and is compliant with Section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15k: r5% pull-down resistor (in the hub/host) when VDD =3.3V. This presents a Therein resistance to the host of at least 9000hms. Alternatively, an external 1.5k: pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

9.2.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

9.2.4 Self Powered Mode

In self powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design for, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to WT12 via a resistor network (Rvb1 and Rvb2), so WT12 can detect when VBUS is powered up. WT12 will not pull USB_DP high when VBUS is off.

Self powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5K 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self powered mode. The internal pull-up in WT12 is only suitable for bus powered USB devices i.e. dongles.

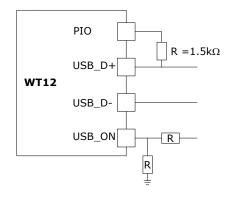


Figure 12: USB in self powered mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

In self powered mode $\mathsf{PSKEY_USB_PIO_PULLUP}$ must be set to match with the PIO selected.

Note:

USB_ON is shared with WT12 PIO terminals (PIO2-PIO7).

9.2.5 Bus Powered Mode

In bus powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. WT12 negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For WT12 Bluetooth applications, it is recommended that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without fold back or limiting. In bus powered mode, WT12 requests 100mA during enumeration.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB specification v1.1, Section 7.2.4.1). Some applications may require soft start circuitry to limit inrush current if more than 10pF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of WT12 will result in reduced receive sensitivity and a distorted RF transmit signal.

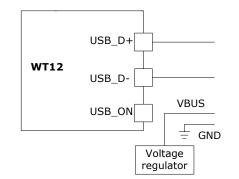


Figure 13: USB in bus powered mode

In bus powered mode PSKEY_USB_PIO_PULLUP must be set to 16 for internal pull-up (default configuration in WT12).

9.2.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB Suspend mode. While in USB Suspend, bus powered devices must not draw more than 0.5mA from USB VBUS (self powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100uA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by WT12. The entire circuit must be able to enter the suspend mode. (For more details on USB Suspend, see separate CSR documentation).

9.2.7 Detach and Wake-Up Signaling

WT12 can provide out-of-band signaling to a host controller by using the control lines called 'USB_DETACH' and 'USB_WAKE_UP'. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding WT12 into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes WT12 to put USB_DN and USB_DP in high impedance state and turned off the pull-up resistor on D+. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, WT12 will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable), and cannot be sent while WT12 is effectively disconnected from the bus.

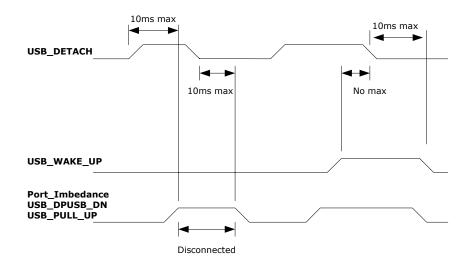


Figure 14: USB_DETACH and USB_WAKE_UP Signal

9.2.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between WT12 and Bluetooth software running on the host computer. Suitable drivers are available from www.bluegiga.com/techforum/.

9.2.9 USB 1.1 Compliance

WT12 is qualified to the USB specification v1.1, details of which are available from <u>http://www.usb.org</u>. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labeling.

Although WT12 meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed

USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plug fest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification 2.0 (Chapter 7) electrical requirements.

9.2.10 USB 2.0 Compatibility

WT12 is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

9.3 SPI Interface

The synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory. SPI interface is connected using the MOSI, MISO, CSB and CLK pins.

9.4 I/O Parallel Ports

The Parallel Input Output (PIO) Port is a general-purpose I/O interface to WT12. The port consists of six programmable, bi-directional I/O lines, PIO[2:7].

Programmable I/O lines can be accessed either via an embedded application running on WT12 or via private channel or manufacturer-specific HCI commands.

All PIO lines are configured as inputs with weak pull downs at reset.

PIO[2] / USB_PULL_UP (1)

This is a multifunction terminal. The function depends on whether WT12 is a USB or UART capable version. On UART versions, this terminal is a programmable I/O. On USB versions, it can drive a pull-up resistor on USB_D+. For application using external RAM this terminal may be programmed for chip select.

PIO[3] / USB_WAKE_UP (1)

This is a multifunction terminal. On UART versions of WT12 this terminal is a programmable I/O. On USB versions, its function is selected by setting the Persistent Store Key PSKEY_USB_PIO_WAKEUP (0x2cf) either as a programmable I/O or as a USB_WAKE_UP function.

PIO[4] / USB_ON (1)

This is a multifunction terminal. On UART versions of WT12 this terminal is a programmable I/O. On USB versions, the USB_ON function is also selectable.

PIO[5] / USB_DETACH (1)

This is a multifunction terminal. On UART versions of WT12 this terminal is a programmable I/O. On USB versions, the USB_DETACH function is also selectable.

PIO[6] / CLK_REQ

This is multifunction terminal, its function is determined by Persistent Store Keys. Using PSKEY_CLOCK_REQUEST_ENABLE, (0x246) this terminal can be configured to be low when WT12 is in deep sleep and high when a clock is required. The clock must be supplied within 4ms of the rising edge of PIO[6] to avoid losing timing accuracy in certain Bluetooth operating modes.

PIO[7]

Programmable I/O terminal.

10. RESET

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period **greater than 5ms**.

11. SOFTWARE STACKS

WT12 is supplied with Bluetooth v2.0 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.

The WT12 software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

11.1 iWRAP Stack

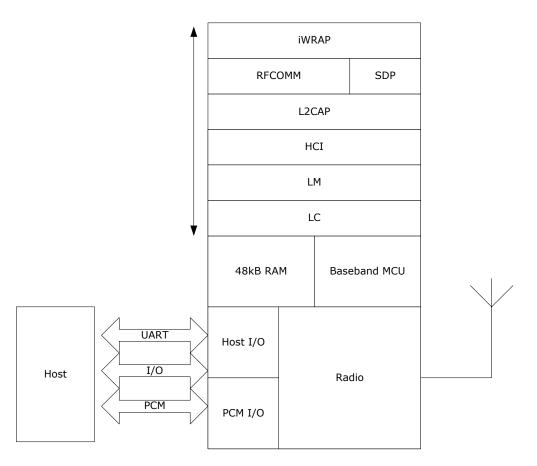


Figure 15: WRAP THOR VM Stack

In figure above, the iWRAP software solution is described. In this version of the stack firmware shown no host processor is required to run the Bluetooth protocol stack. All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The host processor interfaces to iWRAP software via one or more of the physical interfaces which are also shown in the figure above. The most common interfacing is done via UART interface using the ASCII commands supported by the iWRAP software. With these ASCII commands the user can access Bluetooth functionality without paying any attention to the complexity which lies in the Bluetooth protocol stack.

The user may write applications code to run on the host processor to control iWRAP software with ASCII commands and to develop Bluetooth powered applications.

Notes:

More details of iWRAP software and it's features can be found from *iWRAP User Guide* which can be downloaded from <u>www.bluegiga.com</u>.

12. FCC STATEMENT

Federal Communications Commission (FCC) Statement

15.21

You are cautioned that changes or modifications not expressly approved by the part responsible for compliance could void the user's authority to operate the equipment.

15.105(b)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help.

Operation is subject to the following two conditions:

1) this device may not cause interference and

2) this device must accept any interference, including interference that may cause undesired operation of the device.

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Note:

The end product shall has the words "Contains Transmitter Module FCC ID: QOQWT12"

13. CONTACT INFORMATION

Sales:

<u>sales@bluegiga.com</u>

Technical support: <u>support@bluegiga.com</u> <u>http://www.bluegiga.com/techforum/</u>

Orders:

orders@bluegiga.com

Head Office / Finland

Phone: +358-9-4355 060 Fax: +358-9-4355 0660

Street Address:

Sinikalliontie 11 02630 ESPOO FINLAND

Postal address:

P.O. BOX 120 02631 ESPOO, FINLAND

Sales Office / USA

Phone: (781) 556-1039

Bluegiga Technologies, Inc. 99 Derby Street, Suite 200 Hingham, MA 02043