User manual

Product references
Product code: **TELEMACO/RC2015/ERMETE**
Product description: Telematics platform for data acquisition “Telemaco,RC2015,Ermete”

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0.5	15/10/15	M. Freguglia		Added warnings in installation paragraph

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1. Overview

This document contains the specifications for installation and use of the product named Telemaco, RC2015 or Ermete depending on commercialization brand.
Below are described:

- the components of the system and the most common options
- the placement of the connectors and pinouts
- the specifications of connection and use of the devices connected to the system
- the features and specifications of use of internal peripherals
- the container and the characteristics of mounting and assembly

2. System Components

2.1. Box

The box constitutes the processing unit and the interface with the world; it is equipped with:

- plastic housing with fixing brackets for mounting on vehicle
- automotive connector for connectivity to the world
- dedicated connectors for connectivity with administrator or technical operator
- connectors for antennas (GPS, WiFi, GSM and BT)
- internal connectors for other options and debugging

2.2. Options and expansions

The system is usually accompanied by the following options:

- antennas or trivalent antenna
- wiring for the automotive connector

2.3. Declaration

DMD Computers declares that the Telemaco, RC2015 or Ermete is

- compliant to the regulations of mechanical resistance:
  - EN 60068-2-64:2012
  - ISO 16750-3:2012
  - EN 60068-2-27:2012
  - IVECO STD. 18-2252
- compliant to the regulations of electromagnetic compatibility (CE/99/05) and further modification
- compliant with UN ECE R10 (CE/28/2006) for "automotive" aspects
- compliant to the Iveco rules (STD 18-2252)

3. External connections

The box is provided to the outside of the following connectors:

- Vehicle side
  - 1 automotive connector MULTILOCK double section
  - 1 SMA connector for GPS antenna
  - 1 SMA-R antenna WiFi
  - 1 SMA antenna for GSM
  - 1 SMA-R BT antenna
- User side
  - 1 jack plug for auxiliary power
  - 1 USB 2.0 host connector (single port)
  - 2 USB 2.0 host connector (double port)
  - 1 USB 2.0 device
  - 1 HDMI connector
  - 1 Ethernet 10/100/1000 connector
  - 1 SIM holder
  - 1 µSD holder (optional)

3.1. Vehicle side

Figure 1 shows the vehicle side view of the box.
The figure shows the numbering of the connectors, as described in the following paragraphs.

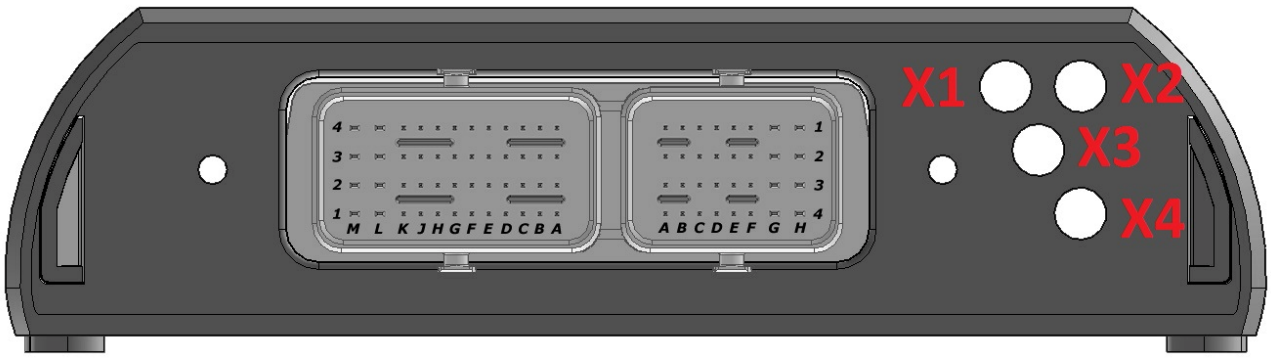


Figure 1: vehicle side view

- X1: SMA-R connector for BT antenna
- X2: SMA-R connector for WiFi antenna
- X3: SMA connector for GPS antenna
- X4: SMA connector for GSM antenna

3.1.1. Automotive connector

The main connector is an automotive connector MULTILOCK double section with 80 pins.
The image of the connector and pin numbering is shown in Figure 2.

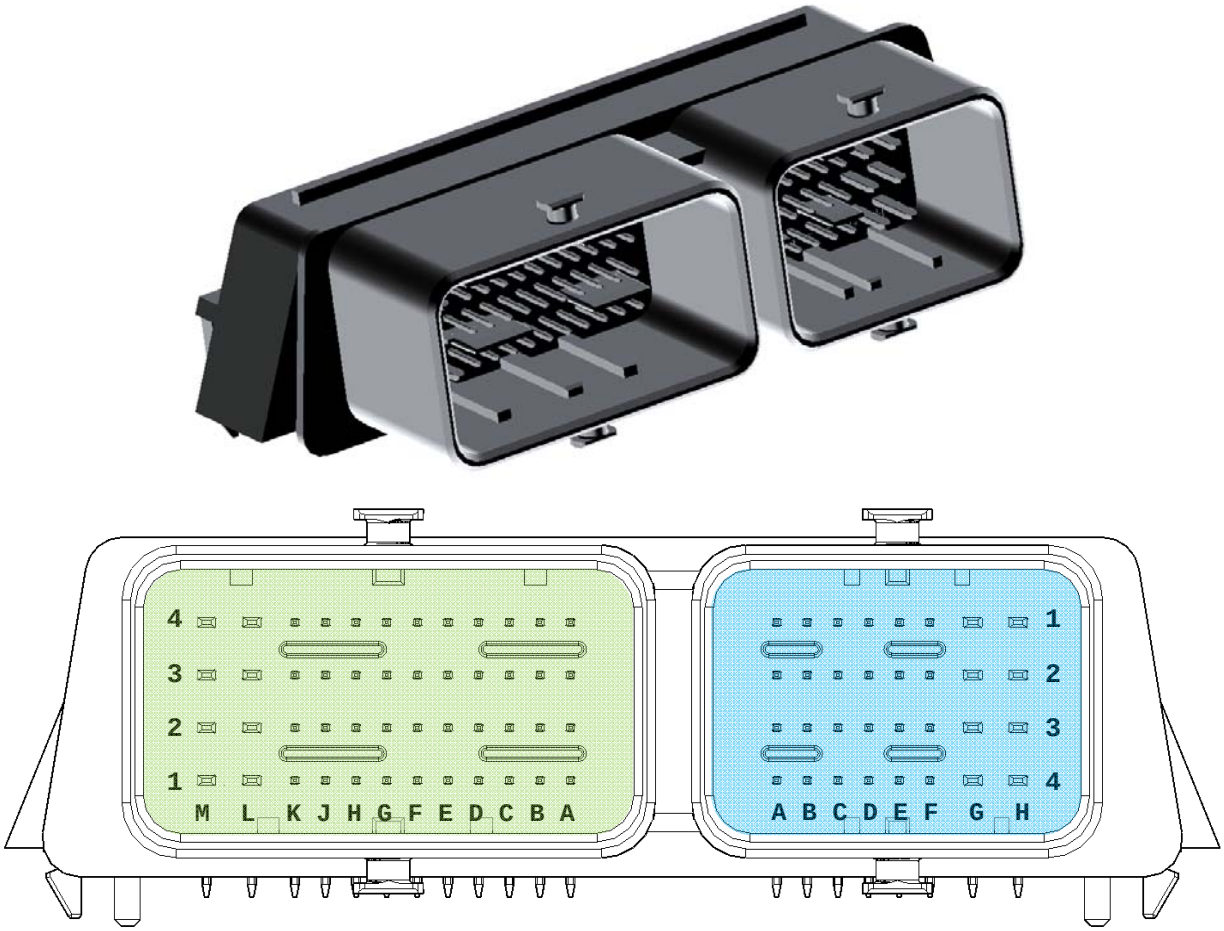


Figure 2: main connector

The assignment of the signals is summarized, for the left section with 48 pins, in Table 1.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1A	GND_RF	2A	LAN_RX-	3A	GND	4A	WU_IN1
1B	GND	2B	LAN_RX+	3B	RS232c_RI	4B	DIG_IO8
1C	CAN4H	2C	LAN_TX-	3C	RS232c_DCD	4C	DIG_IO7
1D	CAN4L	2D	LAN_TX+	3D	RS232c_CTS	4D	DIG_IO6
1E	CAN3H	2E	USB_GND	3E	RS232c_RX	4E	DIG_IO5
1F	CAN3L	2F	USB_DM	3F	RS232c_DTR	4F	DIG_IO4
1G	CAN1L	2G	USB_DP	3G	RS232c_RTS	4G	DIG_IO3
1H	CAN1H	2H	USB_VCC	3H	RS232c_TX	4H	DIG_IO2
1J	CAN2H	2J	RS485_N	3J	RS232c_DSR	4J	DIG_IO1
1K	CAN2L	2K	RS485_P	3K	GND	4K	GND
1L	MIC_GND	2L	DIG-OUT2	3L	WU_IN2	4L	WU_IN3
1M	MIC_IN	2M	DIG-OUT1	3M	PWR	4M	PWR_GND

Table 1: main connector pinout, left section (48 pins)

The assignment of the signals is summarized, for the right section with 32 pins, in Table 2.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1A	EXP_1	2A	EXP_9	3A	RS232r_TX	4A	CAN5L
1B	EXP_2	2B	EXP_10	3B	RS232r_RX	4B	CAN5H
1C	EXP_3	2C	EXP_11	3C	GND	4C	CAN6L
1D	EXP_4	2D	EXP_12	3D	K1	4D	CAN6H
1E	EXP_5	2E	EXP_13	3E	K2	4E	CANBH
1F	EXP_6	2F	EXP_14	3F	K3	4F	CANBL
1G	EXP_7	2G	EXP_15	3G	EXP_17	4G	GND
1H	EXP_8	2H	EXP_16	3H	EXP_18	4H	TACHO

Table 2: main connector pinout, right section (32 pins)

3.1.1.1. Main power - PWR and PWR_GND

The power supply of the system is automotive compliant.
The associated connector pins are PWR and PWR_GND.

	Min.	Typ.	Max.	
rated voltage	8	24	40	V
voltage protection			36	V
maximum continuous voltage			100	V
tolerated load-dump			200	V
current			7	A
short-circuit protection	n.a.			

Table 3: main power

The power supply accepts input voltages in the range of 8÷40V, is protected against reverse battery and load-dump and is capable of operating up to 100V persistent; under 8V it does not guarantee its proper operation, above 36V ($V_{PWRPROT}$) a protection circuit decouples the power supply from external battery and the system is powered from the backup battery.

3.1.1.2. Digital wake-up signals - WU_IN$_x$

They are 3 digital inputs, active high, that allow to wake up the system.
The associated connector pins are WU_IN$_x$.

	Min.	Typ.	Max.	
rated voltage	6		PWR	V
maximum continuous voltage			100	V
tolerated load-dump			200	V
impedance		100k		Ω
short-circuit protection	yes			

Table 4: digital wake-up signals

3.1.1.3. High-speed CAN lines - CAN$_x$L and CAN$_x$H

They are 6 high-speed CAN lines.
The associated connector pins are CAN$_x$L and CAN$_x$H.
The CAN1 line has wake-up capabilities.

		Min.	Typ.	Max.	
rated voltage dominant state	CANH	3	3.6	4.25	V
	CANL	0.5	1.4	1.75	V
rated voltage recessive state	CANH/L	2	2.5	3	V
maximum continuous voltage	CANH/L	-27		+40	V
tolerated load-dump	CANH/L	-200		+200	V
impedance			20k		Ω

		Min.	Typ.	Max.	
communication speed				1M	bps
short-circuit protection		yes			

Table 5: high-speed CAN lines

All the CAN lines are, by default, not terminated. However, with a simple soldering point, a 120Ω termination can be inserted.

3.1.1.4. Low-speed CAN lines - CANBL and CANBH

It is a low-speed and fault-tolerant CAN line.
The associated connector pins are CANBL and CANBH.

		Min.	Typ.	Max.	
rated voltage dominant state	CANH	3.6		5	V
	CANL	0		1.4	V
rated voltage recessive state	CANH	0		0.2	V
	CANL	4.8		5	V
maximum continuous voltage	CANH/L	-58		+58	V
tolerated load-dump	CANH/L	-200		+200	V
impedance			330k		Ω
communication speed				125k	bps
short-circuit protection		yes			

Table 6: low-speed CAN line

This CAN line is, by default, not terminated. However, with a simple soldering point, a 120Ω termination can be inserted.

3.1.1.5. High-speed K lines - K_x

They are 6 high-speed K lines.
The associated connector pins are K_x.

		Min.	Typ.	Max.	
rated voltage dominant state	TxD			0.2 x VPWR	V
rated voltage recessive state		0.95 x VPWR			V
rated voltage dominant state	RxD			0.35 x VPWR	V
rated voltage recessive state		0.65 x VPWR			
maximum continuous voltage		-16		+36	V
tolerated load-dump					V
impedance		500			Ω
communication speed				250k	bps
short-circuit protection		yes			

Table 7: high-speed K lines

The hot side of the K line is connected to the protected battery voltage VPWRPROT. If the vehicle battery is 24V, the pull-up on each line is 1kΩ; if the vehicle battery is 12V, the pull-up is 500Ω; the selection is done automatically by the power-management processor. On each line, a “boost” function is available; it allows to reach the maximum communication speed (up to 250kbps), even on lines long several meters.

3.1.1.6. Digital input/output - DIG_IO$_x$

They are 8 digital signals configurable, in HW, as inputs or outputs.
The default configuration provides 2 inputs and 6 outputs.

3.1.1.6.1. Inputs

They are 2 TTL compatible inputs but tolerant until the battery voltage.
The associated connector pins are DIG_IO1 and DIG_IO2.

	Min.	Typ.	Max.	
rated voltage	3		VPWR	V
maximum continuous voltage			100	V
tolerated load-dump			200	V
impedance	10k			Ω
short-circuit protection	yes			

Table 8: digital inputs

The 2 inputs include a pull-up that maintains a well-known logic level if the pins are left floating.

3.1.1.6.2. Outputs

They are 6 outputs capable of providing, on command, a voltage of 5V.
The associated connector pins are DIG_IO3÷DIG_IO8.

	Min.	Typ.	Max.	
rated voltage		5		V
maximum continuous voltage			15m	A
tolerated load-dump	-1		40	V
impedance				V
short-circuit protection	yes			

Table 9: digital outputs

The 6 outputs are able to supply 15mA ensuring 5V; if the load circuit tends to draw more power, a thermal protection intervenes and limits the current and the voltage available.
The same thermal protection ensures the protection against short-circuits; however, a prolonged state of thermal protection determines a stress condition in the device and this limits its operational life.

3.1.1.7. High-power digital outputs - DIG_OUT1 and DIG_OUT2

They are 2 high-side digital outputs, connected to the protected battery voltage VPWRPROT.
The associated connector pins are DIG_OUT1 and DIG_OUT2.

	Min.	Typ.	Max.	
rated voltage			VPWR	V
maximum continuous voltage			500m	A
tolerated load-dump			40	V
impedance				V
short-circuit protection	yes			

Table 10: high-power digital outputs

3.1.1.8. RS232 serial lines - RS232C_{XY} and RS232R_{XY}

They are 2 serial lines in standard RS232, one is complete with 8 wires, and the other is minimal with 2 wire.
The associated connector pins are RS232C_{XY} and RS232R_{XY}.

		Min.	Typ.	Max.	
rated voltage high level	TxD	5			V
rated voltage low level				-5	V
rated voltage high level	RxD			2.4	V
rated voltage low level		1.2			V
maximum continuous voltage	TxD	-13		13	V
tolerated load-dump					V
impedance		3k		7k	Ω
communication speed				1M	bps
short-circuit protection		only TxD to Ground			

Table 11: RS232 serial lines

3.1.1.9. RS2485 serial line - RS485$_x$

It is a serial line in standard RS485 with 2 wires.
The associated connector pins are RS485$_x$.

		Min.	Typ.	Max.	
differential voltage	TxD	1.5			V
hysteresis voltage	RxD		35m		V
maximum continuous voltage		-9		14	V
tolerated load-dump					V
impedance			120		Ω
communication speed				32M	bps
short-circuit protection		only to Ground			

Table 12: RS485 serial line

3.1.1.10. Ethernet line - LAN$_x$

It is a 10/100 Ethernet line.
The associated connector pins are LAN$_x$.

The electrical characteristics are compatible with the LAN specifications for 10/100Mbps

3.1.1.11. USB line - USB$_x$

It is a USB 2.0 host line.
The associated connector pins are USB$_x$.

The electrical characteristics are compatible with USB 2.0 specifications

3.1.1.12. Microphone line - MIC$_x$

It is a line for passive microphone.
The associated connector pins are MIC$_x$.

	Min.	Typ.	Max.	
rated voltage		1.8		V
maximum continuous voltage			2	V
tolerated load-dump				V
impedance		2k		Ω
programmable gain	-24		24	dB
SNR		91		dB
short-circuit protection	only to Ground			

Table 13: microphone line

The microphone input includes an internal 2.2kΩ bias pull-up.

3.1.1.13. Future expansion

They are 20 general purpose signals can be used for future expansion.
The associated connector pins are EXP$_x$.
They are available on the connector but are not "mapped" on any device.

3.1.2. SMA connector for GSM antenna – X4

X4 is an SMA male connector used for connection to a GSM antenna.
The connector is electrically connected to the module.
The antenna cable must be a female coaxial with 50Ω impedance.

3.1.3. SMA connector for GPS antenna – X3

X3 is a SMA female connector used for connection to a GPS antenna.
The connector is electrically connected to the module.
The antenna cable must be a female coaxial with 50Ω impedance.

3.1.4. SMA-R connector for WiFi antenna – X2

X2 is a male SMA-R connector used to connect with WiFi antenna.
The connector is electrically connected to the module.
The antenna cable must be a female coaxial with 50Ω impedance.

3.1.5. SMA-R connector for BT antenna – X1

X1 is a male SMA-R connector used to connect with WiFi antenna.
The connector is electrically connected to the module.
The antenna cable must be a female coaxial with 50Ω impedance

3.2. User side

Figure 3 shows the vehicle side view of the box.
The figure shows the numbering of the connectors, as described in the following paragraphs.

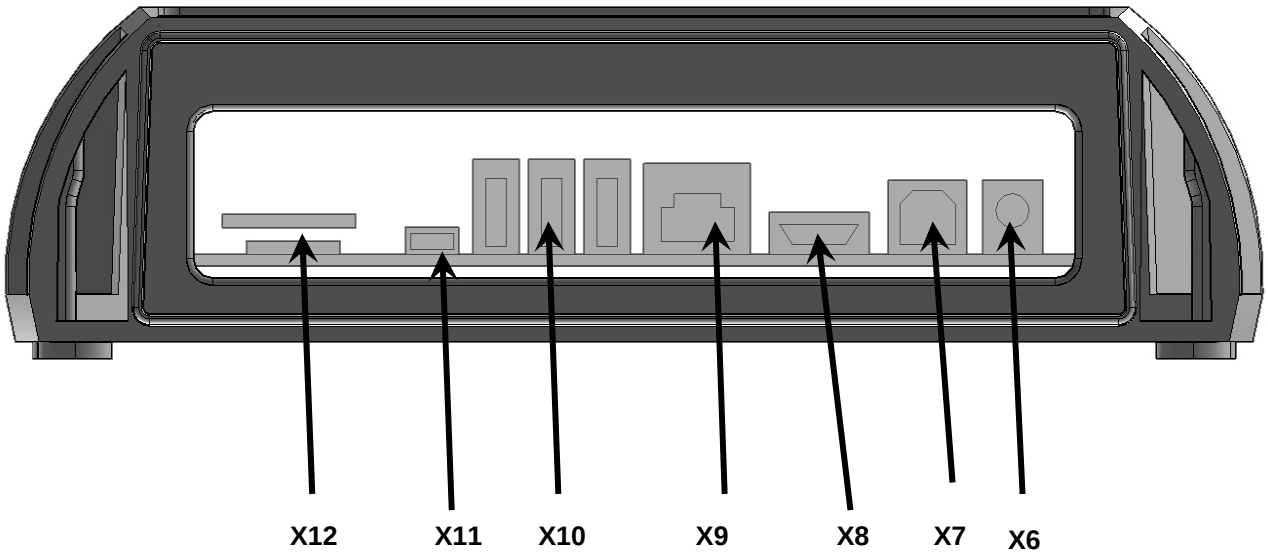


Figure 3: user side view

- X6: jack connector for auxiliary power supply
- X7: USB device connector
- X8: HDMI connector
- X9: Ethernet connector
- X10: USB host connector (three masters)
- X11: USB slave connector (console)
- X12: SIM (above) and µSD (below) holders

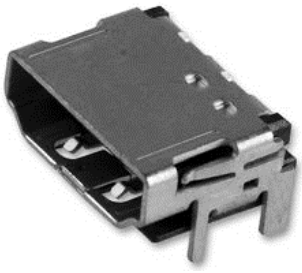
3.2.1. Jack connector for auxiliary power supply – X6

On the user side an auxiliary connector is available; it is compatible with the power jack of the laptop PC, allowing to power the system without being connected to the vehicle battery.
CAUTION: is strongly recommended to connect the auxiliary power supply only for use at the lab and do not connect anything to the auxiliary power supply if the system is already connected to the vehicle battery.

3.2.2. USB device connector – X7

On the user side a Type-B standard receptacle for USB 2.0 is available. This connector provides an USB OTG interface used in device mode. To avoid any problem of ground-shift, this USB channel is optically isolated. Even if used in device mode, the Remote Check cannot be powered by this connector.

3.2.3. HDMI connector – X8



On the user side a standard HDMI connector is available. The interface is compatible with the version 1.4 support a graphic full-HD @ 1920x1080 pixel.

3.2.4. Ethernet connector – X9

On the user side a standard RJ45 for 10/100/1000 Ethernet is available.

3.2.5. USB host connector (single) – X10

On the user side a Type-A standard single receptacle for USB 2.0 is available. This connector provides an USB interface used in device mode.

3.2.6. USB host connector (double) – X11

On the user side a Type-A standard double receptacle for USB 2.0 is available. This connector provides an USB interface used in device mode.

3.2.7. SIM e µSD holders – X12

On the user side 2 holders push-pull type are available. The upper support is for the SIM and the other is for µSD card.

4. Internal modules

4.1. Core module

This chapter defines the characteristics of a device, hereinafter referred as "core logic" or “core module”, intended to provide an embedded platform based on iMX6 Freescale ARM processor.
This platform integrates the processor, the DDR3 volatile memory bank, the on-chip MMC non-volatile memory bank for storage and the "physical layer" Ethernet for LAN connection. There is also a PMIC for the intelligent management of power supplies and operating states (off, sleep, idle, run).
All peripherals of the processor, described below, are available on 3 high density and high speed connectors.

4.1.1. Printed circuit board

Figure 4 shows the location of the elements on the circuit board of the core logic.

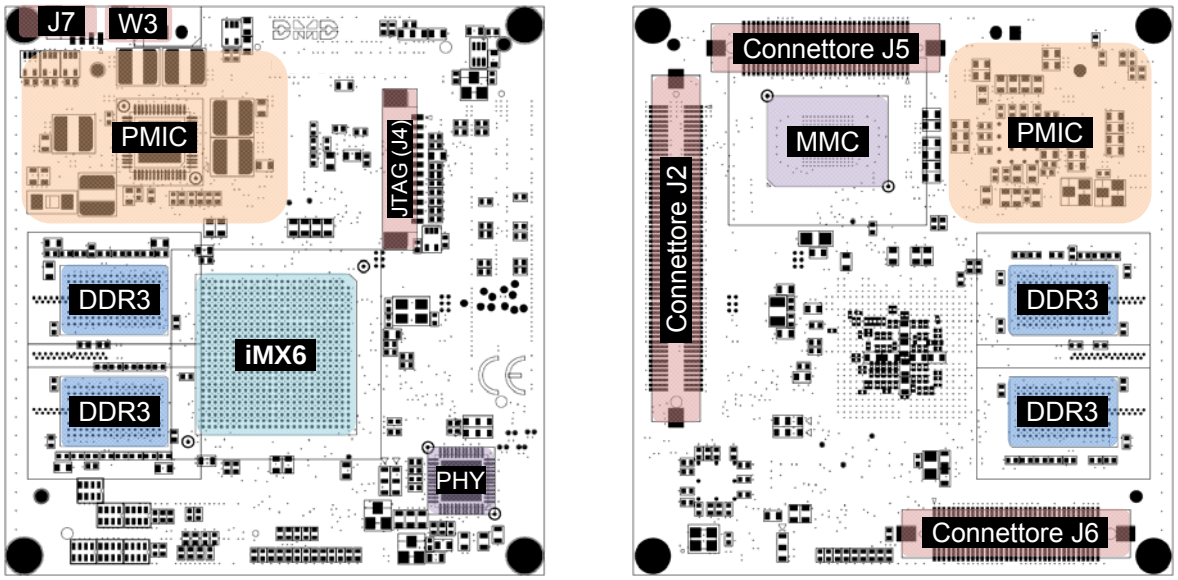


Figure 4: RC2core – component placement

The PCB is almost square and measures 71x75mm.
The left image is the upper side of the core logic, the right is the bottom side.
In case of quad/dual core, 4 banks of DDR3 RAM are installed, and in this case the memory bus is 64 bit wide. In case of single core, only 2 banks are installed and the access to the bus is 32 bit wide.

4.1.2. Boot configuration

The boot mode can be selected by mounting/dismounting appropriate resistances.
There are 3 main ways to boot, summarized in Table 14:

Boot mode	R32	R34
Boot from fuses	pull-down	pull-down
Boot from serial	pull-down	pull-up
Boot from board settings	pull-up	pull-down

Table 14: RC2core – boot modes

The boot from fuses requires that the fuses, internal to the processor, have been previously programmed; the programming of these fuses cannot be undone once performed.
Boot from serial executes a bootloader on UART1 and requires an appropriate programmer.

The boot form board setting is the default; at reset, the processor samples the logic state of some pin (ref. **Errore. L'origine riferimento non è stata trovata.**); these pins define the external boot device.

4.1.2.1. Boot from board settings

In this boot mode, the processor, after the reset, samples the state of some pins in order to determine the storage device boot. Because, after the reset, these pins become usable by the application, it is important that all devices connected to these pins, through the interface connectors, do not alter their state during reset.
Table 15 lists the sampled pin during the reset.

Signal	Connector	iMX6 pin	Reset level
SPI2_SS1	1 – pin 41	EIM_LBA	H
SPI2_SS0	1 – pin 40	EIM_RW	H
EIM_A16	3 – pin 26	EIM_A16	L
EIM_A17	3 – pin 20	EIM_A17	L
EIM_A18	3 – pin 23	EIM_A18	L
EIM_A19	3 – pin 22	EIM_A19	L
EIM_A20	3 – pin 16	EIM_A20	L
EIM_A21	3 – pin 24	EIM_A21	L
EIM_A23	3 – pin 18	EIM_A23	L
EIM_DA8	3 – pin 28	EIM_DA8	L
EIM_WAIT	3 – pin 21	EIM_WAIT	L

Table 15: RC2core – boot pins at reset

In theory, the processor can boot from many sources, including memories connected to the SPI and I^2C channels. However, the core logic excludes these possibilities, reducing the possible boot sources to channels SD3, SD4 (where the MMC is connected) and SATA.

4.1.2.1.1. Boot from SD

Boot from Secure Digital card is implemented if the card is plugged on the 3rd SD channel (SD3), available on connector J2. Table 16 summarizes how some resistors must be installed to boot from SD.

	R65	R64	R63	R75
1-bit boot	yes	no	no	no
4-bit bot				yes

Table 16: RC2core – boot from SD

4.1.2.1.2. Boot from MMC

Boot from Multimedia Card is implemented on the 4th SD channel (SD4), where an on-chip MMC is connected and available on connector J2. Table 17 summarizes how some resistors must be installed to boot from MMC.

	R65	R64	R63	R75
8-bit boot	yes	yes	yes	no

Table 17: RC2core – boot from MMC

4.1.2.1.3. Boot da SATA

Boot from SATA is implemented if the device is connected to the SATA channel, available on connector J2. Table 18 summarizes how some resistors must be installed to boot from SATA.

	R65	R64	R63	R75
Boot a 8bit	no	yes	no	-

Table 18: RC2core – boot from SATA

4.1.3. Pinout of the interface connectors

Below are described the pinout of the connectors interface between the core logic and the carrier board.
The following information is reported:

- Position: connector pin number
- Name: signal name
- Vdd: signal supply
- Direction: signal direction (from core logic point of view)
- iMX6 pin: iMX6's pin where the signal is connected/associated
- Description: short description of the signal

With regard to "Vdd" item, Table 19 summarizes the possible values of some "special power supply":

Vdd	Valore [V]
VDD_SYS	3.7 ÷ 4.4
LICELL	3.0 ÷ 4.4
VSNVS	~3.0

Table 19: RC2core – special power supply

Warning: there are some signs whose dynamics is not the "classic" 3.3V but only 1.8V. A level shifter may have to be provided on carrier board.

4.1.3.1. Connector J2

Table 20 lists the pinout of the connector J2, which provides most of the interfaces of core logic.

Pos.	Name	Vdd	Dir.	iMX6 pin	Description
1	VDD_SYS_4V2	VDD_SYS	IN	-	Main power supply
2	VDD_SYS_4V2	VDD_SYS	IN	-	Main power supply
3	VDD_SYS_4V2	VDD_SYS	IN	-	Main power supply
4	VDD_SYS_4V2	VDD_SYS	IN	-	Main power supply
5	P3V3_LICELL	LICELL	IN	-	Stand-by power supply
6	VDD_SYS_4V2	VDD_SYS	IN	-	Main power
7	PWRON	VSNVS	IN	-	Global reset (iMX6 and PMIC)
8	CPU-ONOFF	VSNVS	IN	ONOFF	Power On/Off
9	I2C2_SDA	3.3V	BI	KEY-ROW3	Data signal of 2nd I^2C channel
10	I2C3_SCL	3.3V	OUT	GPIO_3	Clock signal of 2nd I^2C channel
11	I2C2_SCL	3.3V	OUT	KEY_COL3	Clock signal of 3rd I^2C channel
12	I2C3_SDA	3.3V	BI	GPIO_6	Data signal of 3rd I^2C channel
13	POR_B	VSNVS	BI	POR_B	Processor reset
14	VDD_3V3	3.3V	OUT	-	PMIC SW2 power supply
15	CAN1_TX	3.3V	OUT	GPIO_7	TX signal of 1st CAN channel
16	CAN2_TX	3.3V	OUT	KEY_COL4	TX signal of 2nd CAN channel
17	CAN1_RX	3.3V	IN	GPIO_8	RX signal of 1st CAN channel
18	CAN2_RX	3.3V	IN	KEY_ROW4	RX signal of 2nd CAN channel
19	GND	-	-	-	Ground reference
20	GND	-	-	-	Ground reference
21	UART1_TX	1.8V	OUT	CSI0_DAT10	TX signal of 1st UART channel
22	UART1_RX	1.8V	IN	CSI0_DAT11	RX signal of 1st UART channel
23	UART4_RX	1.8V	IN	CSI0_DAT13	RX signal of 4th UART channel
24	UART4_TX	1.8V	OUT	CSI0_DAT12	TX signal of 4th UART channel
25	UART3_CTS	3.3V	IN	EIM_D23	CTS of 3rd UART channel
26	UART4_RTS	1.8V	OUT	CSI0_DAT16	RTS of 4th UART channel
27	UART3_TX	3.3V	OUT	EIM_D24	TX signal of 3rd UART channel
28	UART4_CTS	1.8V	IN	CSI0_DAT17	CTS of 4th UART channel
29	UART3_RX	3.3V	IN	EIM_D25	RX signal of 3rd UART channel
30	UART2_TX	3.3V	OUT	EIM_D26	TX signal of 2nd UART channel
31	UART3_RTS	3.3V	OUT	EIM_D31	RTS of 3rd UART channel

Pos.	Name	Vdd	Dir.	iMX6 pin	Description
32	UART2_RX	3.3V	IN	EIM_D27	RX signal of 2nd UART channel
33					
34					
35					
36					
37	SPI2_SCLK	3.3V	OUT	EIM_CS0	Clock signal of 2nd SPI channel
38	SPI2_MOSI	3.3V	OUT	EIM_CS1	MOSI signal of 2nd SPI channel
39	SPI2_MISO	3.3V	IN	EIM_OE	MISO signal of 2nd SPI channel
40	SPI2_SS0	3.3V	OUT	EIM_RW	Chip-select 0 of 2nd SPI channel
41	SPI2_SS1	3.3V	OUT	EIM_LBA	Chip-select 1 of 2nd SPI channel
42	GND	-	-	-	Ground reference
43	GND	-	-	-	Ground reference
44	USB_HOST_DN	5.0V	BI	USB_HOST_DN	Data- signal of USB host channel
45	USB_OTG_DN	5.0V	BI	USB_OTG_DN	Data- signal of USB OTG channel
46	USB_HOST_DP	5.0V	BI	USB_HOST_DP	Data+ signal of USB host channel
47	USB_OTG_DP	5.0V	BI	USB_OTG_DP	Data+ signal of USB OTG channel
48	GND	-	-	-	Ground reference
49	GND	-	-	-	Ground reference
50	VDD_USB_H	-	IN	USB_H1_VBUS	Power supply of USB host channel
51	VDD_USB_O	-	IN	USB_OTG_VBUS	Power supply of USB OTG channel
52	USB_OTG_ID	1.8V	IN	ENET_RX_ER	ID signal of USB OTG channel
53	USB_OTG_OC#	3.3V	IN	EIM_D21	Overcurrent flag of USB OTG channel
54	USB_OTG_PWR	3.3V	OUT	EIM_D22	Enable signal of USB OTG channel
55	USB_H1_OC#	3.3V	IN	EIM_D30	Overcurrent flag of USB host channel
56	USB_H1_PWR	1.8V	OUT	ENET_TXD1	Enable signal of USB host channel
57	USB_OTG_OK	1.8V	IN	ENET_RXD0	Feedback signal of USB OTG channel
58	GND	-	-	-	Ground reference
59	GND	-	-	-	Ground reference
60	PCIE_PWR_EN	3.3V	OUT	EIM_D19	Enable signal of PCIe channel
61	PCIE_RXM	1.35V	IN	PCIE_RXM	RX- signal of PCIe channel
62	PCIE_WAKE_B	3.3V	IN	CSI0_DATA_EN	Wake-up signal of PCIe channel
63	PCIE_RXP	1.35V	IN	PCIE_RXP	RX+ signal of PCIe channel
64	PCIE_RST_B	3.3V	OUT	GPIO_17	Reset signal of PCIe channel
65	GND	-	-	-	Ground reference
66	GND	-	-	-	Ground reference
67	PCIE_TXP	1.35V	OUT	PCIE_TXP	TX+ signal of PCIe channel
68	CLK1_P	1.35V	OUT	CLK1_P	CLK+ signal of PCIe channel
69	PCIE_TXM	1.35V	OUT	PCIE_TXM	TX- signal of PCIe channel
70	CLK1_N	1.35V	OUT	CLK1_N	CLK- signal of PCIe channel
71	GND	-	-	-	Ground reference
72	GND	-	-	-	Ground reference
73	SD3_DAT1	3.3V	BI	SD3_DAT1	Data1 signal of 3rd SD channel
74	SD3_DAT0	3.3V	BI	SD3_DAT0	Data0 signal of 3rd SD channel
75	SD3_DAT6	3.3V	BI	SD3_DAT6	Data6 signal of 3rd SD channel
76	SD3_CLK	3.3V	OUT	SD3_CLK	Clock signal of 3rd SD channel
77	SD3_DAT4	3.3V	BI	SD3_DAT4	Data4 signal of 3rd SD channel
78	SD3_DAT2	3.3V	BI	SD3_DAT2	Data2 signal of 3rd SD channel
79	SD3_DAT5	3.3V	BI	SD3_DAT5	Data5 signal of 3rd SD channel
80	SD3_DAT3	3.3V	BI	SD3_DAT3	Data3 signal of 3rd SD channel
81	SD3_CMD	3.3V	OUT	SD3_CMD	Command signal of 3rd SD channel
82	SD3_WP	3.3V	IN	NANDF_D1	Write-protect signal of 3rd SD channel
83	SD3_DAT7	3.3V	BI	SD3_DAT7	Data7 signal of 3rd SD channel
84	SD3_CD_B	3.3V	IN	NANDF_D0	Card-detect signal of 3rd SD channel
85	GND	-	-	-	Ground reference
86	GND	-	-	-	Ground reference

Pos.	Name	Vdd	Dir.	iMX6 pin	Description
87	SD2_DAT3	3.3V	BI	SD2_DAT3	Data3 signal of 2nd SD channel
88	SD2_DAT2	3.3V	BI	SD2_DAT2	Data2 signal of 2nd SD channel
89	SD2_DAT0	3.3V	BI	SD2_DAT0	Data0 signal of 2nd SD channel
90	SD2_DAT7	3.3V	BI	NANDF_D7	Data7 signal of 2nd SD channel
91	SD2_DAT4	3.3V	BI	NANDF_D4	Data4 signal of 2nd SD channel
92	SD2_CD_B	3.3V	IN	NANDF_D2	CardDetect signal of 2nd SD channel
93	SD2_DAT5	3.3V	BI	NANDF_D5	Data5 signal of 2nd SD channel
94	SD2_CLK	3.3V	OUT	SD2_CLK	Clock signal of 2nd SD channel
95	SD2_WP	3.3V	IN	NANDF_D3	WriteProtect signal of 2nd SD channel
96	SD2_DAT1	3.3V	BI	SD2_DAT1	Data1 signal of 2nd SD channel
97	SD2_DAT6	3.3V	BI	NANDF_D6	Data6 signal of 2nd SD channel
98	SD2_CMD	3.3V	OUT	SD2_CMD	Command signal of 2nd SD channel
99	GND	-	-	-	Ground reference
100	GND	-	-	-	Ground reference
101	SATA_TXM	1.35V	OUT	SATA_TXM	TX- signal of SATA channel
102	SATA_RXM	1.35V	IN	SATA_RXM	RX- signal of SATA channel
103	SATA_TXP	1.35V	OUT	SATA_TXP	TX+ signal of SATA channel
104	SATA_RXP	1.35V	IN	SATA_RXP	RX+ signal of SATA channel
105	GND	-	-	-	Ground reference
106	GND	-	-	-	Ground reference
107	GBE_MDI3-	3.3V	BI	-	Gigabit Ethernet –negative signal 4th pair
108	GBE_MDI1-	3.3V	BI	-	Gigabit Ethernet –negative signal 2nd pair
109	GBE_MDI3+	3.3V	BI	-	Gigabit Ethernet –positive signal 4th pair
110	GBE_MDI1+	3.3V	BI	-	Gigabit Ethernet –positive signal 2nd pair
111	GND	-	-	-	Ground reference
112	GND	-	-	-	Ground reference
113	GBE_MDI2-	3.3V	BI	-	Gigabit Ethernet –negative signal 3rd pair
114	GBE_MDI0-	3.3V	BI	-	Gigabit Ethernet –negative signal 1st pair
115	GBE_MDI2+	3.3V	BI	-	Gigabit Ethernet –positive signal 3rd pair
116	GBE_MDI0+	3.3V	BI	-	Gigabit Ethernet –positive signal 1st pair
117	GND	-	-	-	Ground reference
118	GND	-	-	-	Ground reference
119	GBE_LED1	3.3V	OUT	-	Gigabit Ethernet – led activity 1
120	GBE_LED2	3.3V	OUT	-	Gigabit Ethernet – led activity 2

Table 20: RC2core - J2 connector pinout

4.1.3.2. Connector J5

Table 21 lists the pinout of the connector J5.

Pos.	Name	Vdd	Dir.	iMX6 pin	Description
1	GND	-	-	-	Ground reference
2	GND	-	-	-	Ground reference
3	LVDS1_TX0_N	2.5V	OUT	LVDS1_TX0_N	TX- signal of 1st pair on 2nd LVDS channel
4	LVDS1_TX3_P	2.5V	OUT	LVDS1_TX3_P	TX+ signal of 4th pair on 2nd LVDS channel
5	LVDS1_TX0_P	2.5V	OUT	LVDS1_TX0_P	TX+ signal of 1st pair on 2nd LVDS channel
6	LVDS1_TX3_N	2.5V	OUT	LVDS1_TX3_N	TX- signal of 4th pair on 2nd LVDS channel
7	GND	-	-	-	Ground reference
8	GND	-	-	-	Ground reference
9	LVDS1_TX1_P	2.5V	OUT	LVDS1_TX1_P	TX+ signal of 2nd pair on 2nd LVDS channel
10	LVDS1_CLK_N	2.5V	OUT	LVDS1_CLK_N	CLK- signal of 2nd LVDS channel
11	LVDS1_TX1_N	2.5V	OUT	LVDS1_TX1_N	TX- signal of 2nd pair on 2nd LVDS channel
12	LVDS1_CLK_P	2.5V	OUT	LVDS1_CLK_P	CLK+ signal of 2nd LVDS channel
13	GND	-	-	-	Ground reference
14	GND	-	-	-	Ground reference

Pos.	Name	Vdd	Dir.	iMX6 pin	Description
15	LVDS0_TX0_N	2.5V	OUT	LVDS0_TX0_N	TX- signal of 1st pair on 1st LVDS channel
16	LVDS1_TX2_P	2.5V	OUT	LVDS1_TX2_P	TX+ signal of 3rd pair on 2nd LVDS channel
17	LVDS0_TX0_P	2.5V	OUT	LVDS0_TX0_P	TX+ signal of 1st pair on 1st LVDS channel
18	LVDS1_TX2_N	2.5V	OUT	LVDS1_TX2_N	TX- signal of 3rd pair on 2nd LVDS channel
19	GND	-	-	-	Ground reference
20	GND	-	-	-	Ground reference
21	LVDS0_CLK_N	2.5V	OUT	LVDS0_CLK_N	CLK- signal of 1st LVDS channel
22	LVDS0_TX3_N	2.5V	OUT	LVDS0_TX3_N	TX- signal of 4th pair on 1st LVDS channel
23	LVDS0_CLK_P	2.5V	OUT	LVDS0_CLK_P	CLK+ signal of 1st LVDS channel
24	LVDS0_TX3_P	2.5V	OUT	LVDS0_TX3_P	TX+ signal of 4th pair on 1st LVDS channel
25	GND	-	-	-	Ground reference
26	GND	-	-	-	Ground reference
27	LVDS0_TX1_N	2.5V	OUT	LVDS0_TX1_N	TX- signal of 2nd pair on 1st LVDS channel
28	LVDS0_TX2_N	2.5V	OUT	LVDS0_TX2_N	TX- signal of 3rd pair on 1st LVDS channel
29	LVDS0_TX1_P	2.5V	OUT	LVDS0_TX1_P	TX+ signal of 2nd pair on 1st LVDS channel
30	LVDS0_TX2_P	2.5V	OUT	LVDS0_TX2_P	TX+ signal of 3rd pair on 1st LVDS channel
31	GND	-	-	-	Ground reference
32	GND	-	-	-	Ground reference
33	NANDF_CS3	3.3V	BI	NANDF_CS3	General purpose IO
34	NANDF_CS2	3.3V	BI	NANDF_CS2	General purpose IO
35	NANDF_CLE	3.3V	BI	NANDF_CLE	General purpose IO
36	NANDF_ALE	3.3V	BI	NANDF_ALE	General purpose IO
37	GND	-	-	-	Ground reference
38	GND	-	-	-	Ground reference
39	MICROPHONE_DET	3.3V	IN	GPIO_9	Audio – microphone detection signal
40	GPIO_0_CLKO	3.3V	OUT	GPIO_0	Audio –clock signal
41	KEY_VOL_DN	3.3V	BI	GPIO_5	Audio – decrease volume control
42	CODEC_PWR_EN	3.3V	OUT	KEY_COL2	Audio – enable signal
43	KEY_VOL_UP	3.3V	BI	GPIO_4	Audio – increase volume control
44	AUD3_RXD	1.8V	IN	CSI0_DAT7	Audio – ADC digital audio data
45	AUD3_TXC	1.8V	OUT	CSI0_DAT4	Audio – bit clock
46	AUD3_TXD	1.8V	OUT	CSI0_DAT5	Audio – DAC digital audio data
47	AUD3_TXFS	1.8V	OUT	CSI0_DAT6	Audio – left / right clock
48	HEADPHONE_DET	3.3V	IN	SD3_RST	Audio – headphone detection signal
49	SD1_DAT3	1.8V	BI	SD1_DAT3	General purpose IO
50	I2C1_SDA	1.8V	BI	CSI0_DAT8	Data signal of 1st I2C channel
51	VDD_5V_PMIC	5.0V	OUT	-	PMIC SWBST power supply
52	I2C1_SCL	1.8V	OUT	CSI0_DAT9	Clock signal of 1st I2C channel
53	GND	-	-	-	Ground reference
54	GND	-	-	-	Ground reference
55	HDMI_D0P	1.35V	OUT	HDMI_D0P	D+ signal of 1st pair on HDMI channel
56	HDMI_CEC_IN	3.3V	IN	KEY_ROW2	CEC signal on HDMI channel
57	HDMI_D0M	1.35V	OUT	HDMI_D0M	D- signal of 1st pair on HDMI channel
58	HDMI_HPD	1.35V	OUT	HDMI_HPD	HDP signal on HDMI channel
59	GND	-	-	-	Ground reference
60	GND	-	-	-	Ground reference
61	HDMI_D1P	1.35V	OUT	HDMI_D1P	D+ signal of 2nd pair on HDMI channel
62	HDMI_D2P	1.35V	OUT	HDMI_D2P	D+ signal of 3rd pair on HDMI channel
63	HDMI_D1M	1.35V	OUT	HDMI_D1M	D- signal of 2nd pair on HDMI channel
64	HDMI_D2M	1.35V	OUT	HDMI_D2M	D- signal of 3rd pair on HDMI channel
65	GND	-	-	-	Ground reference
66	GND	-	-	-	Ground reference
67	HDMI_DDC_SCL	3.3V	OUT	KEY_COL3	Clock signal of I2C channel on HDMI channel
68	HDMI_CLKM	1.35V	OUT	HDMI_CLKM	CLK- signal on HDMI channel
69	HDMI_DDC_SDA	3.3V	IN	KEY-ROW3	Data signal of I2C channel on HDMI channel

Pos.	Name	Vdd	Dir.	iMX6 pin	Description
70	HDMI_CLKP	1.35V	OUT	HDMI_CLKP	CLK+ signal on HDMI channel

Table 21: RC2core – J5 connector pinout

4.1.3.3. Connector J6

Table 22 lists the pinout of the connector J6.

Pos.	Name	Vdd	Dir.	iMX6 pin	Description
1	GPIO_16	3.3V	BI	GPIO_16	General purpose IO
2	GPIO_19	3.3V	BI	GPIO_19	General purpose IO
3	GND	-	-	-	Ground reference
4	GPIO_2	3.3V	BI	GPIO_2	General purpose IO
5	UART5_TX	1.8V	OUT	CSI0_DAT14	TX signal of 5th UART channel
6	GND	-	-	-	Ground reference
7	UART5_CTS	1.8V	IN	CSI0_DAT19	CTS signal of 5th UART channel
8	UART5_RX	1.8V	IN	CSI0_DAT15	RX signal of 5th UART channel
9	GND	-	-	-	Ground reference
10	UART5_RTS	1.8V	OUT	CSI0_DAT18	RTS signal of 5th UART channel
11	ENET_TXD0	1.8V	BI	ENET_TXD0	General purpose IO
12	GND	-	-	-	Ground reference
13	EIM_BCLK	3.3V	BI	EIM_BCLK	General purpose IO
14	EIM_D16	3.3V	BI	EIM_D16	General purpose IO
15	EIM_D28	3.3V	BI	EIM_D28	General purpose IO
16	EIM_A20	3.3V	BI	EIM_A20	General purpose IO
17	NANDF_WP_B	3.3V	BI	NANDF_WP_B	General purpose IO
18	EIM_A23	3.3V	BI	EIM_A23	General purpose IO
19	NANDF_CS0	3.3V	BI	NANDF_CS0	General purpose IO
20	EIM_A17	3.3V	BI	EIM_A17	General purpose IO
21	EIM_WAIT	3.3V	BI	EIM_WAIT	General purpose IO
22	EIM_A19	3.3V	BI	EIM_A19	General purpose IO
23	EIM_A18	3.3V	BI	EIM_A18	General purpose IO
24	EIM_A21	3.3V	BI	EIM_A21	General purpose IO
25	NANDF_CS1	3.3V	BI	NANDF_CS1	General purpose IO
26	EIM_A16	3.3V	BI	EIM_A16	General purpose IO
27	NANDF_RB0	3.3V	BI	NANDF_RB0	General purpose IO
28	EIM_DA8	3.3V	BI	EIM_DA8	General purpose IO
29	GND	-	-	-	Ground reference
30	GND	-	-	-	Ground reference
31	SD1_DAT1	1.8V	BI	SD1_DAT1	General purpose IO
32	SD1_CLK	1.8V	BI	SD1_CLK	General purpose IO
33	SD1_DAT2	1.8V	BI	SD1_DAT2	General purpose IO
34	SD1_DAT0	1.8V	BI	SD1_DAT0	General purpose IO
35	GND	-	-	-	Ground reference
36	SD1_CMD	1.8V	BI	SD1_CMD	General purpose IO
37	DISP0_CLK	3.3V	OUT	DIO_DISP_CLK	Clock signal of parallel video output
38	GND	-	-	-	Ground reference
39	DISP0_VSYNC	3.3V	OUT	DIO_PIN3	Vsync signal of parallel video output
40	DISP0_HSYNC	3.3V	OUT	DIO_PIN2	Hsync signal of parallel video output
41	DISP0_DAT1	3.3V	OUT	DISP0_DAT1	Data1 signal of parallel video output
42	DISP0_DRDY	3.3V	OUT	DIO_PIN15	Data Enable signal of parallel video output
43	DISP0_DAT4	3.3V	OUT	DISP0_DAT4	Data4 signal of parallel video output
44	DISP0_DAT16	3.3V	OUT	DISP0_DAT16	Data16 signal of parallel video output
45	DISP0_DAT3	3.3V	OUT	DISP0_DAT3	Data3 signal of parallel video output
46	DISP0_DAT15	3.3V	OUT	DISP0_DAT15	Data15 signal of parallel video output

Pos.	Name	Vdd	Dir.	iMX6 pin	Description
47	DISP0_CNTRST	3.3V	OUT	DIO_PIN4	Contrast signal of parallel video output
48	DISP0_DAT20	3.3V	OUT	DISP0_DAT20	Data20 signal of parallel video output
49	DISP0_DAT0	3.3V	OUT	DISP0_DAT0	Data0 signal of parallel video output
50	DISP0_DAT10	3.3V	OUT	DISP0_DAT10	Data10 signal of parallel video output
51	GND	-	-	-	Ground reference
52	GND	-	-	-	Ground reference
53	DISP0_DAT5	3.3V	OUT	DISP0_DAT5	Data5 signal of parallel video output
54	DISP0_DAT2	3.3V	OUT	DISP0_DAT2	Data2 signal of parallel video output
55	DISP0_DAT7	3.3V	OUT	DISP0_DAT7	Data7 signal of parallel video output
56	DISP0_DAT8	3.3V	OUT	DISP0_DAT8	Data8 signal of parallel video output
57	DISP0_DAT9	3.3V	OUT	DISP0_DAT9	Data9 signal of parallel video output
58	DISP0_DAT6	3.3V	OUT	DISP0_DAT6	Data6 signal of parallel video output
59	DISP0_DAT12	3.3V	OUT	DISP0_DAT12	Data12 signal of parallel video output
60	DISP0_DAT13	3.3V	OUT	DISP0_DAT13	Data13 signal of parallel video output
61	GND	-	-	-	Ground reference
62	GND	-	-	-	Ground reference
63	DISP0_DAT14	3.3V	OUT	DISP0_DAT14	Data14 signal of parallel video output
64	DISP0_DAT11	3.3V	OUT	DISP0_DAT11	Data11 signal of parallel video output
65	DISP0_DAT17	3.3V	OUT	DISP0_DAT17	Data17 signal of parallel video output
66	DISP0_DAT21	3.3V	OUT	DISP0_DAT21	Data21 signal of parallel video output
67	DISP0_DAT18	3.3V	OUT	DISP0_DAT18	Data18 signal of parallel video output
68	DISP0_DAT19	3.3V	OUT	DISP0_DAT19	Data19 signal of parallel video output
69	DISP0_DAT22	3.3V	OUT	DISP0_DAT22	Data22 signal of parallel video output
70	DISP0_DAT23	3.3V	OUT	DISP0_DAT23	Data23 signal of parallel video output

Table 22: RC2core – J6 connector pinout

4.1.4. Peripherals and available interfaces

4.1.4.1. Power supply and control signals

Table 23 summarizes the power supply and control signals of the core logic, all available on the connector J2.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
VDD_SYS_4V2	J2	1,2,3,4,6	VDD_SYS	IN	-
P3V3_LICELL	J2	5	LICELL	IN	-
VDD_3V3	J2	14	3.3V	OUT	-
PWRON	J2	7	3.0V	IN	-
CPU-ONOFF	J2	8	3.0V	IN	ONOFF
POR_B	J2	13	3.0V	BI	POR_B

Table 23: RC2core – power supply and control signals

VDD_SYS_4V2 is the main power supply of all core logic.
It delivers all the current absorbed by the core and must be connected to a voltage regulator, with dynamic compatible with "VDD_SYS" (ref. Table 19), capable of providing approximately 10W. On the control board, is better to "strengthen" the corresponding pins with a low ESR capacitor greater than 100µF.
Through the connector W3 is possible to power the core logic without using the main connector J2. The pinout of this auxiliary connector is summarized in Table 24.

Signal	Pos.
VDD_SYS_4V2	1
GND	2

Table 24: RC2core – auxiliary power supply on W3 connector

P3V3_LICELL is the power supply for the stand-by management.

It can be connected to a battery with dynamic compatible with "LICELL" (ref. Table 19) or to a source of energy always present and with similar dynamics. If the stand-by state is not required, this signal can be left floating.

VDD_3V3 is the 3.3V power supply used for most of the devices of the core.
It is made available on the connector only for reference and/or to inform the carrier board that the processor is "on". It is not recommended to use this signal to supply other components.

PWRON is the signal that allow the “brutal” restart of the core logic.
The signal has a pull-up and is active low; can be connected to a switch or a device that closes it to ground.
If PWRON is asserted, the system resets and restarts with complete re-boot.

CPU-ONOFF is the signal that allows the power management of the processor.
The signal has a pull-up and is active low; can be connected to a switch or a device that closes it to ground.
Since it is referred to the stand-by voltage (VSNVS), the signal allows the "intelligent" management of the supply core logic. In particular:

- if the processor is on:
  - if CPU-ONOFF is asserted for less than 1” ⇨ processor goes into stand-by
  - if CPU-ONOFF is asserted for more than 5” ⇨ processor turns off (shutdown)
- if the processor is off:
  - if CPU-ONOFF is asserted for less than 1” ⇨ the processor starts the system, with complete boot
- if the processor is in stand-by state:
  - if CPU-ONOFF is asserted for less than 1” ⇨ the processor restart the system, without boot

POR_B is the signal that allows the processor reset.
The signal has a pull-up and is active low; in order to execute the reset, it can be connected to a switch or a device that closes it to ground; at the same time, it can be monitored from the carrier board, reading it in high impedance.

4.1.4.2. Asynchronous serial channels

Table 25 summarizes the asynchronous serial channels provided by the core logic.
In total, 5 serial ports are available, 2 lines have 2 wire and the other 3 have 4 wires. The flow control signals of the 4-wire serial ports are of course optional. If any signal of the table is not used, it can be set as general purpose IO. All serial ports have a maximum transmission speed of 4Mbps.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
UART1_TX	J2	21	1.8V	OUT	CSI0_DAT10
UART1_RX	J2	22	1.8V	IN	CSI0_DAT11
UART2_TX	J2	30	3.3V	OUT	EIM_D26
UART2_RX	J2	32	3.3V	IN	EIM_D27
UART3_TX	J2	27	3.3V	OUT	EIM_D24
UART3_RX	J2	29	3.3V	IN	EIM_D25
UART3_RTS	J2	31	3.3V	OUT	EIM_D31
UART3_CTS	J2	25	3.3V	IN	EIM_D23
UART4_TX	J2	24	1.8V	OUT	CSI0_DAT12
UART4_RX	J2	23	1.8V	IN	CSI0_DAT13
UART4_RTS	J2	26	1.8V	OUT	CSI0_DAT16
UART4_CTS	J2	28	1.8V	IN	CSI0_DAT17
UART5_TX	J6	5	1.8V	OUT	CSI0_DAT14
UART5_RX	J6	8	1.8V	IN	CSI0_DAT15
UART5_RTS	J6	10	1.8V	OUT	CSI0_DAT18
UART5_CTS	J6	7	1.8V	IN	CSI0_DAT19

Table 25: RC2core - asynchronous serial channels

The UART1 dynamics is 1.8V and the UART1_RX signal has a pull-up.
Since this serial is uses as OS console, it would be appropriate to use it always just for this purpose.
The UART1 is also available on connector J7, in order to be able to connect a console to the core logic without using the main connector J2. The J7 connector pinout is resumed on Table 26.

Signal	Pos.	Vdd	Dir.
ENABLE	1	3.3V	IN
TX-DEBUG	2	3.3V	IN
RX-DEBUG	3	3.3V	OUT
GND	4	-	-

Table 26: RC2core – auxiliary connector for console

Between the connector J7 and UART1 port, a level shifter is provided; it adapts all UART1 signals to 3.3V. The signal TX-DEBUG is headed to UART1_RX; signal RX-DEBUG is headed to UART1_TX. If the ENABLE signal is connected to 3.3V then level shifter is enabled, else the translator is forced into high impedance.

The UART2 dynamics is 3.3V and its 2 signals have no pull-up/down.

The UART3 dynamics is 3.3V and its 4 signals have no pull-up/down.

The UART4 dynamics is 1.8V and its 4 signals have no pull-up/down.

The UART5 dynamics is 1.8V and its 4 signals have no pull-up/down.

4.1.4.3. I²C channels

Table 27 summarizes the I²C channels provided by the core logic.
All I²C channels have a maximum transmission rate of 400kbps.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
I2C1_SDA	2	50	1.8V	BI	CSI0_DAT8
I2C1_SCL	2	52	1.8V	OUT	CSI0_DAT9
I2C2_SDA	1	9	3.3V	BI	KEY-ROW3
I2C2_SCL	1	11	3.3V	OUT	KEY_COL3
I2C3_SDA	1	12	3.3V	BI	GPIO_6
I2C3_SCL	1	10	3.3V	OUT	GPIO_3

Table 27: RC2core – I²C channels

The I²C1 dynamics is 1.8V and its 2 signals have pull-up.

The I²C2 dynamics is 3.3V and its 2 signals have pull-up.

The I²C3 dynamics is 3.3V and its 2 signals have pull-up.

4.1.4.4. CAN channels

Table 28 summarizes the CAN channels provided by the core logic.
All CAN channels have a maximum transmission rate of 1Mbps.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
CAN1_TX	1	15	3.3V	OUT	GPIO_7
CAN1_RX	1	17	3.3V	IN	GPIO_8
CAN2_TX	1	16	3.3V	OUT	KEY_COL4
CAN2_RX	1	18	3.3V	IN	KEY_ROW4

Table 28: RC2core – CAN channels

The CAN1 dynamics is 3.3V and its 2 signals have no pull-up/down.

The CAN2 dynamics is 3.3V and its 2 signals have no pull-up/down.

4.1.4.5. SPI channels

Table 29 summarizes the SPI channels provided by the core logic.
The first channel (SPI1) has only 1 chip-select; the second channel (SPI2) has 2 chip-selects. All SPI channels have a maximum transmission rate of 50Mbps.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
SPI1_MISO	1	33	3.3V	IN	KEY_COL1
SPI1_MOSI	1	35	3.3V	OUT	KEY_ROW0
SPI1_SCLK	1	34	3.3V	OUT	KEY_COL0
SPI1_SS0	1	36	3.3V	OUT	KEY_ROW1
SPI2_MISO	1	39	3.3V	IN	EIM_OE
SPI2_MOSI	1	38	3.3V	OUT	EIM_CS1
SPI2_SCLK	1	37	3.3V	OUT	EIM_CS0
SPI2_SS0	1	40	3.3V	OUT	EIM_RW
SPI2_SS1	1	41	3.3V	OUT	EIM_LBA

Table 29: RC2core – SPI channels

The SPI1 dynamics is 3.3V; SPI1_SS0 has pull-up, the others have no pull-up/down.

The SPI2 dynamics is 3.3V; SPI2_SS0 and SPI2_SS1 have pull-up, the others have no pull-up/down.

4.1.4.6. USB channels

Table 30 summarizes the USB channels provided by the core logic.
The first channel is a HSB host 2.0; the second channel is a USB OTG 2.0.
Both USB channels have a maximum transmission rate of 480Mbps.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
USB_HOST_DN	1	44	5.0V	BI	USB_HOST_DN
USB_HOST_DP	1	46	5.0V	BI	USB_HOST_DP
USB_H1_OC#	1	55	3.3V	IN	EIM_D30
USB_H1_PWR	1	56	1.8V	OUT	ENET_TXD1
VDD_USB_H	1	50	-	IN	USB_H1_VBUS
USB_OTG_DN	1	45	5.0V	BI	USB_OTG_DN
USB_OTG_DP	1	47	5.0V	BI	USB_OTG_DP
USB_OTG_ID	1	52	1.8V	IN	ENET_RX_ER
USB_OTG_OC#	1	53	3.3V	IN	EIM_D21
USB_OTG_PWR	1	54	3.3V	OUT	EIM_D22
USB_OTG_OK	1	57	1.8V	IN	ENET_RXD0
VDD_USB_O	1	51	-	IN	USB_OTG_VBUS

Table 30: RC2core – USB channels

USB_HOST_DN and USB_HOST_DP are the USB host data.
USB_H1_OC# dynamics is 3.3V; it is the over-current flag, is active low and has a pull-up.
USB_H1_PWR dynamics is 1.8V; it is the enable signal for the USB host power supply, is active high and has a pull-down. It is used to turn on an external voltage regulator able to providing VDD_USB_H.
VDD_USB_H dynamics is 5V; it is the USB transceiver power supply (internal to the processor).

USB_OTG_DN and USB_OTG_DP are the USB OTG data.
USB_OTG_ID dynamics is 1.8V; it is the IDentification signal.
USB_OTG_OC# dynamics is 3.3V; it is the over-current flag, is active low and has a pull-up.
USB_OTG_PWR dynamics is 3.3V; it is the enable signal for the USB OTG power supply, is active high and has a pull-down. It is used to turn on an external voltage regulator able to providing VDD_USB_O.
USB_OTG_OK dynamics is 1.8V; it allows to the processor to know if the supply VDD_USB_O is correct; it is active low ahd has a pull-up.
VDD_USB_O dynamics is 5V; it is the USB OTG transceiver power supply (internal to the processor).
Caution: the USB channels deliver high-frequency signals.

4.1.4.7. PCIe channel

Table 31 summarizes the PCIe channel provided by the core logic.
The PCIe channel have a maximum transmission rate of 2.5Gbps.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
PCIE_TXM	1	69	1.35V	OUT	PCIE_TXM
PCIE_TXP	1	67	1.35V	OUT	PCIE_TXP
PCIE_RXM	1	61	1.35V	IN	PCIE_RXM
PCIE_RXP	1	63	1.35V	IN	PCIE_RXP
CLK1_N	1	70	1.35V	OUT	CLK1_N
CLK1_P	1	68	1.35V	OUT	CLK1_P
PCIE_RST_B	1	64	3.3V	OUT	GPIO_17
PCIE_PWR_EN	1	60	3.3V	OUT	EIM_D19
PCIE_WAKE_B	1	62	3.3V	IN	CSI0_DATA_EN

Table 31: RC2core – PCIe channels

PCIE_TXM and PCIE_TXP are the Tx differential pair.
PCIE_RXM and PCIE_RXP are the Rx differential pair.
CLK1_N and CLK1_P are the Clk differential pair.
PCIE_RST_B dynamics is 3.3V; it allows to reset any device connected to PCIe channel; it is active low e has no pull-up/down.
PCIE_PWR_EN dynamics is 3.3V; it allows to control the power supply of any device connected to PCIe channel; it is active high e has no pull-up/down.
PCIE_WAKE_B dynamics is 3.3V; it is the wake-up signal from PCIe channel; the signal is optional because the wake-up is typically required with an appropriate message on the channel PCIe.
Caution: the PCIe channel deliver high-frequency signals.

4.1.4.8. SATA channel

Table 32 summarizes the SATA channel provided by the core logic.
The SATA channel have a maximum transmission rate of 3Gbps.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
SATA_TXM	1	101	1.35V	OUT	SATA_TXM
SATA_TXP	1	103	1.35V	OUT	SATA_TXP
SATA_RXM	1	102	1.35V	IN	SATA_RXM
SATA_RXP	1	104	1.35V	IN	SATA_RXP

Table 32: RC2core – SATA channel

SATA _TXM and SATA _TXP are the Tx differential pair.
SATA _RXM and SATA _RXP are the Rx differential pair.
Caution: the SATA channel deliver high-frequency signals.

4.1.4.9. Ethernet channel

Table 33 summarizes the Ethernet channel provided by the core logic.
All the signals are provided by a PHY compatible with the formats 10/100/1000Mbit. The carrier board must provide the connection with a transformer or a switch.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
GBE_MDI0-	1	114	3.3V	BI	-
GBE_MDI0+	1	116	3.3V	BI	-
GBE_MDI1-	1	108	3.3V	BI	-
GBE_MDI1+	1	110	3.3V	BI	-
GBE_MDI2-	1	113	3.3V	BI	-
GBE_MDI2+	1	115	3.3V	BI	-
GBE_MDI3-	1	107	3.3V	BI	-
GBE_MDI3+	1	109	3.3V	BI	-
GBE_LED1	1	119	3.3V	BI	-
GBE_LED2	1	120	3.3V	BI	-

Table 33: RC2core – Ethernet channel

GBE_MDI0- and GBE_MDI0+ are the 1st pair. For a 10/100Mbit connection, this is the TX pair.
GBE_MDI1- and GBE_MDI1+ are the 2nd pair. For a 10/100Mbit connection, this is the RX pair
GBE_MDI2- and GBE_MDI2+ are the 3rd pair.
GBE_MDI3- and GBE_MDI3+ are the 4th pair.
GBE_LED1 and GBE_LED2 are the led-activity signals.
Caution: the Ethernet channel deliver high-frequency signals.

4.1.4.10. Secure Digital channels

Table 34 summarizes the SD-card channels provided by the core logic.
They are 2 complete SD-card channels able to connect card in 1, 4, 8-bit mode.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
SD2_DAT0	1	89	3.3V	BI	SD2_DAT0
SD2_DAT1	1	96	3.3V	BI	SD2_DAT1
SD2_DAT2	1	88	3.3V	BI	SD2_DAT2
SD2_DAT3	1	87	3.3V	BI	SD2_DAT3
SD2_DAT4	1	91	3.3V	BI	NANDF_D4
SD2_DAT5	1	93	3.3V	BI	NANDF_D5
SD2_DAT6	1	97	3.3V	BI	NANDF_D6
SD2_DAT7	1	90	3.3V	BI	NANDF_D7
SD2_CLK	1	94	3.3V	OUT	SD2_CLK
SD2_CMD	1	98	3.3V	OUT	SD2_CMD
SD2_CD_B	1	92	3.3V	IN	NANDF_D2
SD2_WP	1	95	3.3V	IN	NANDF_D3
SD3_DAT0	1	74	3.3V	BI	SD3_DAT0
SD3_DAT1	1	73	3.3V	BI	SD3_DAT1
SD3_DAT2	1	78	3.3V	BI	SD3_DAT2
SD3_DAT3	1	80	3.3V	BI	SD3_DAT3
SD3_DAT4	1	77	3.3V	BI	SD3_DAT4
SD3_DAT5	1	79	3.3V	BI	SD3_DAT5
SD3_DAT6	1	75	3.3V	BI	SD3_DAT6
SD3_DAT7	1	83	3.3V	BI	SD3_DAT7
SD3_CLK	1	76	3.3V	OUT	SD3_CLK
SD3_CMD	1	81	3.3V	OUT	SD3_CMD
SD3_CD_B	1	84	3.3V	IN	NANDF_D0
SD3_WP	1	82	3.3V	IN	NANDF_D1

Table 34: RC2core – SD-card channel

The SD2 dynamics is 3.3V and all signals have no pull-up/down.

The SD3 dynamics is 3.3V and all signals have no pull-up/down.

The “CardDetect” signals are active low; the “WriteProtect” signals are active high.

4.1.4.11. HDMI channel

Table 35 summarizes the HDMI channel provided by the core logic.
This video output supports resolutions up to 1920x1200 and a pixel-rate up to 266MHz.
The carrier board must provide a level-shifter for the EDID signals and the ESD protections.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
HDMI_D0M	2	57	1.35V	OUT	HDMI_D0M
HDMI_D0P	2	55	1.35V	OUT	HDMI_D0P
HDMI_D1M	2	63	1.35V	OUT	HDMI_D1M
HDMI_D1P	2	61	1.35V	OUT	HDMI_D1P
HDMI_D2M	2	64	1.35V	OUT	HDMI_D2M
HDMI_D2P	2	62	1.35V	OUT	HDMI_D2P
HDMI_CLKM	2	68	1.35V	OUT	HDMI_CLKM

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
HDMI_CLKP	2	70	1.35V	OUT	HDMI_CLKP
HDMI_DDC_SDA	2	69	3.3V	IN	KEY-ROW3
HDMI_DDC_SCL	2	67	3.3V	OUT	KEY_COL3
HDMI_HPD	2	58	1.35V	OUT	HDMI_HPD
HDMI_CEC_IN	2	56	3.3V	IN	KEY_ROW2
VDD_5V_PMIC	2	51	5.0V	OUT	-

Table 35: RC2core – HDMI channel

HDMI_D0M and HDMI_D0P are the 1st pair.
HDMI_D1M and HDMI_D1P are the 2nd pair.
HDMI_D2M and HDMI_D2P are the 3rd pair.
HDMI_CLKM and HDMI_CLKP are the Clk pair.
HDMI_HPD is the HDP (*Hot Plug Detect*) signal.
HDMI_CEC_IN is the CEC (*Consumer Electronics Control*) signal.
HDMI_DDC_SDA and HDMI_DDC_SCL dynamics is 3.3V; they are the dedicated I^2C channel (EDID).
VDD_5V_PMIC is the 5V voltage required to supply the level translator for EDID signals.
Caution: the HDMI channel deliver high-frequency signals.

4.1.4.12. LVDS channels

Table 36 summarizes the LVDS channels provided by the core logic.
This video output supports resolutions up to 1920x1200 and a pixel-rate up to 170MHz.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
LVDS0_TX0_N	2	15	2.5V	OUT	LVDS0_TX0_N
LVDS0_TX0_P	2	17	2.5V	OUT	LVDS0_TX0_P
LVDS0_TX1_N	2	27	2.5V	OUT	LVDS0_TX1_N
LVDS0_TX1_P	2	29	2.5V	OUT	LVDS0_TX1_P
LVDS0_TX2_N	2	28	2.5V	OUT	LVDS0_TX2_N
LVDS0_TX2_P	2	30	2.5V	OUT	LVDS0_TX2_P
LVDS0_TX3_N	2	22	2.5V	OUT	LVDS0_TX3_N
LVDS0_TX3_P	2	24	2.5V	OUT	LVDS0_TX3_P
LVDS0_CLK_N	2	21	2.5V	OUT	LVDS0_CLK_N
LVDS0_CLK_P	2	23	2.5V	OUT	LVDS0_CLK_P
LVDS1_TX0_N	2	3	2.5V	OUT	LVDS1_TX0_N
LVDS1_TX0_P	2	5	2.5V	OUT	LVDS1_TX0_P
LVDS1_TX1_N	2	11	2.5V	OUT	LVDS1_TX1_N
LVDS1_TX1_P	2	9	2.5V	OUT	LVDS1_TX1_P
LVDS1_TX2_N	2	18	2.5V	OUT	LVDS1_TX2_N
LVDS1_TX2_P	2	16	2.5V	OUT	LVDS1_TX2_P
LVDS1_TX3_N	2	6	2.5V	OUT	LVDS1_TX3_N
LVDS1_TX3_P	2	4	2.5V	OUT	LVDS1_TX3_P
LVDS1_CLK_N	2	10	2.5V	OUT	LVDS1_CLK_N
LVDS1_CLK_P	2	12	2.5V	OUT	LVDS1_CLK_P

Table 36: RC2core – LVDS channel

LVDS0_TX0_N and LVDS0_TX0_P are the 1st pair on 1st channel.
LVDS0_TX1_N and LVDS0_TX1_P are the 2nd pair on 1st channel.
LVDS0_TX2_N and LVDS0_TX2_P are the 3rd pair on 1st channel.
LVDS0_TX3_N and LVDS0_TX3_P are the 4th pair on 1st channel.
Lvds0_Clk_N and Lvds0_Clk_P are the Clk pair on 1st channel.

LVDS1_TX0_N and LVDS1_TX0_P are the 1st pair on 2nd channel.
LVDS1_TX1_N and LVDS1_TX1_P are the 2nd pair on 2nd channel.
LVDS1_TX2_N and LVDS1_TX2_P are the 3rd pair on 2nd channel.
LVDS1_TX3_N and LVDS1_TX3_P are the 4th pair on 2nd channel.

Lvds1_Clk_N and Lvds1_Clk_P are the Clk pair on 2nd channel.

The LVDS dynamics is 2.5V.
Caution: the LVDS channel deliver high-frequency signals.

4.1.4.13. Audio channels

Table 37 summarizes the digital audio channels provided by the core logic.
This audio output supports two AC97 stereo channels up to 1.4Mbps.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
AUD3_TXC	2	45	1.8V	OUT	CSI0_DAT4
AUD3_TXFS	2	47	1.8V	OUT	CSI0_DAT6
AUD3_TXD	2	46	1.8V	OUT	CSI0_DAT5
AUD3_RXD	2	44	1.8V	IN	CSI0_DAT7
GPIO_0_CLKO	2	40	3.3V	OUT	GPIO_0
MICROPHONE_DET	2	39	3.3V	IN	GPIO_9
HEADPHONE_DET	2	48	3.3V	IN	SD3_RST
KEY_VOL_UP	2	43	3.3V	BI	GPIO_4
KEY_VOL_DN	2	41	3.3V	BI	GPIO_5
CODEC_PWR_EN	2	42	3.3V	OUT	KEY_COL2

Table 37: RC2core – LVDS channel

AUD3_TXC dynamics is 1.8V and it is the bit clock.
AUD3_TXFS dynamics is 1.8V and it is the left/right clock.
AUD3_TXD dynamics is 1.8V and it is the digital output stream (from processor to codec).
AUD3_RXD dynamics is 1.8V and it is the digital input stream (from codec to processor).
GPIO_0_CLKO dynamics is 3.3V and it is the master clock for the external codec.
MICROPHONE_DET dynamics is 3.3V and it is the microphone detection signal, is active low and has no pull-up/down.
HEADPHONE_DET dynamics is 3.3V and it is the headphone detection signal, is active low and has no pull-up/down.
KEY_VOL_UP dynamics is 3.3V and it is the volume increase control; is active low and has no pull-up/down.
KEY_VOL_DN dynamics is 3.3V and it is the volume decrease control. È attivo basso e non ha nessun pull-up.
CODEC_PWR_EN dynamics is 3.3V and it is the codec enable, is active high e has no pull-up/down.

4.1.4.14. Parallel RGB channel

Table 38 summarizes the parallel RGB channel provided by the core logic.
This video output manages a 24 bit bus (8 bit per pixel) and support resolutions up to 1920x1200 and a pixel-rate up to 100MHz.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
DISP0_CLK	3	37	3.3V	OUT	DIO_DISP_CLK
DISP0_HSYNC	3	40	3.3V	OUT	DIO_PIN2
DISP0_VSYNC	3	39	3.3V	OUT	DIO_PIN3
DISP0_DRDY	3	42	3.3V	OUT	DIO_PIN15
DISP0_CNTRST	3	47	3.3V	OUT	DIO_PIN4
DISP0_DAT0	3	49	3.3V	OUT	DISP0_DAT0
DISP0_DAT1	3	41	3.3V	OUT	DISP0_DAT1
DISP0_DAT2	3	54	3.3V	OUT	DISP0_DAT2
DISP0_DAT3	3	45	3.3V	OUT	DISP0_DAT3
DISP0_DAT4	3	43	3.3V	OUT	DISP0_DAT4
DISP0_DAT5	3	53	3.3V	OUT	DISP0_DAT5
DISP0_DAT6	3	58	3.3V	OUT	DISP0_DAT6
DISP0_DAT7	3	55	3.3V	OUT	DISP0_DAT7
DISP0_DAT8	3	56	3.3V	OUT	DISP0_DAT8

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
DISP0_DAT9	3	57	3.3V	OUT	DISP0_DAT9
DISP0_DAT10	3	50	3.3V	OUT	DISP0_DAT10
DISP0_DAT11	3	64	3.3V	OUT	DISP0_DAT11
DISP0_DAT12	3	59	3.3V	OUT	DISP0_DAT12
DISP0_DAT13	3	60	3.3V	OUT	DISP0_DAT13
DISP0_DAT14	3	63	3.3V	OUT	DISP0_DAT14
DISP0_DAT15	3	46	3.3V	OUT	DISP0_DAT15
DISP0_DAT16	3	44	3.3V	OUT	DISP0_DAT16
DISP0_DAT17	3	65	3.3V	OUT	DISP0_DAT17
DISP0_DAT18	3	67	3.3V	OUT	DISP0_DAT18
DISP0_DAT19	3	68	3.3V	OUT	DISP0_DAT19
DISP0_DAT20	3	48	3.3V	OUT	DISP0_DAT20
DISP0_DAT21	3	66	3.3V	OUT	DISP0_DAT21
DISP0_DAT22	3	69	3.3V	OUT	DISP0_DAT22
DISP0_DAT23	3	70	3.3V	OUT	DISP0_DAT23

Table 38: RC2core – parallel RGB channel

DISP0_CLK dynamics is 3.3V and it is the pixel clock.
DISP0_HSYNC dynamics is 3.3V and it is the horizontal sync pulses.
DISP0_VSYNC dynamics is 3.3V and it is the vertical sync pulses.
DISP0_DRDY dynamics is 3.3V and it is the pixel enable.
DISP0_CNTRST dynamics is 3.3V and it is the contrast signal.

4.1.4.15. GPIOs

Table 38 summarizes the GPIOs provided by the core logic.

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
NANDF_CS3	J5	33	3.3V	BI	NANDF_CS3
NANDF_CS2	J5	34	3.3V	BI	NANDF_CS2
NANDF_CLE	J5	35	3.3V	BI	NANDF_CLE
NANDF_ALE	J5	36	3.3V	BI	NANDF_ALE
GPIO_16	J6	1	3.3V	BI	GPIO_16
GPIO_19	J6	2	3.3V	BI	GPIO_19
GPIO_2	J6	4	3.3V	BI	GPIO_2
ENET_TXD0	J6	11	1.8V	BI	ENET_TXD0
EIM_BCLK	J6	13	3.3V	BI	EIM_BCLK
EIM_D16	J6	14	3.3V	BI	EIM_D16
EIM_D28	J6	15	3.3V	BI	EIM_D28
EIM_A20	J6	16	3.3V	BI	EIM_A20
NANDF_WP_B	J6	17	3.3V	BI	NANDF_WP_B
EIM_A23	J6	18	3.3V	BI	EIM_A23
NANDF_CS0	J6	19	3.3V	BI	NANDF_CS0
EIM_A17	J6	20	3.3V	BI	EIM_A17
EIM_WAIT	J6	21	3.3V	BI	EIM_WAIT
EIM_A19	J6	22	3.3V	BI	EIM_A19
EIM_A18	J6	23	3.3V	BI	EIM_A18
EIM_A21	J6	24	3.3V	BI	EIM_A21
NANDF_CS1	J6	25	3.3V	BI	NANDF_CS1
EIM_A16	J6	26	3.3V	BI	EIM_A16
NANDF_RB0	J6	27	3.3V	BI	NANDF_RB0
EIM_DA8	J6	28	3.3V	BI	EIM_DA8
SD1_DAT1	J6	31	1.8V	BI	SD1_DAT1
SD1_CLK	J6	32	1.8V	BI	SD1_CLK
SD1_DAT2	J6	33	1.8V	BI	SD1_DAT2
SD1_DAT0	J6	34	1.8V	BI	SD1_DAT0

Signal	Conn.	Pos.	Vdd	Dir.	iMX6 pin
SD1_CMD	J6	36	1.8V	BI	SD1_CMD

Table 39: RC2core – GPIO

Caution: some signals have 1.8V dynamics, all other 3.3V, therefore on carrier board a level-shifter may be needed.
The direction of all the GPIO is "bi-directional", with means that the direction is not fixed, as all other signals, but is programmable via SW.

4.2. Carrier module

This chapter defines the characteristics of a device, hereinafter referred as "carrier module", intended to provide the support base and all the connectivity for the core logic to the external world.

4.2.1. Printed circuit board

Figure 4 shows the location of the elements on the circuit board of the core logic.

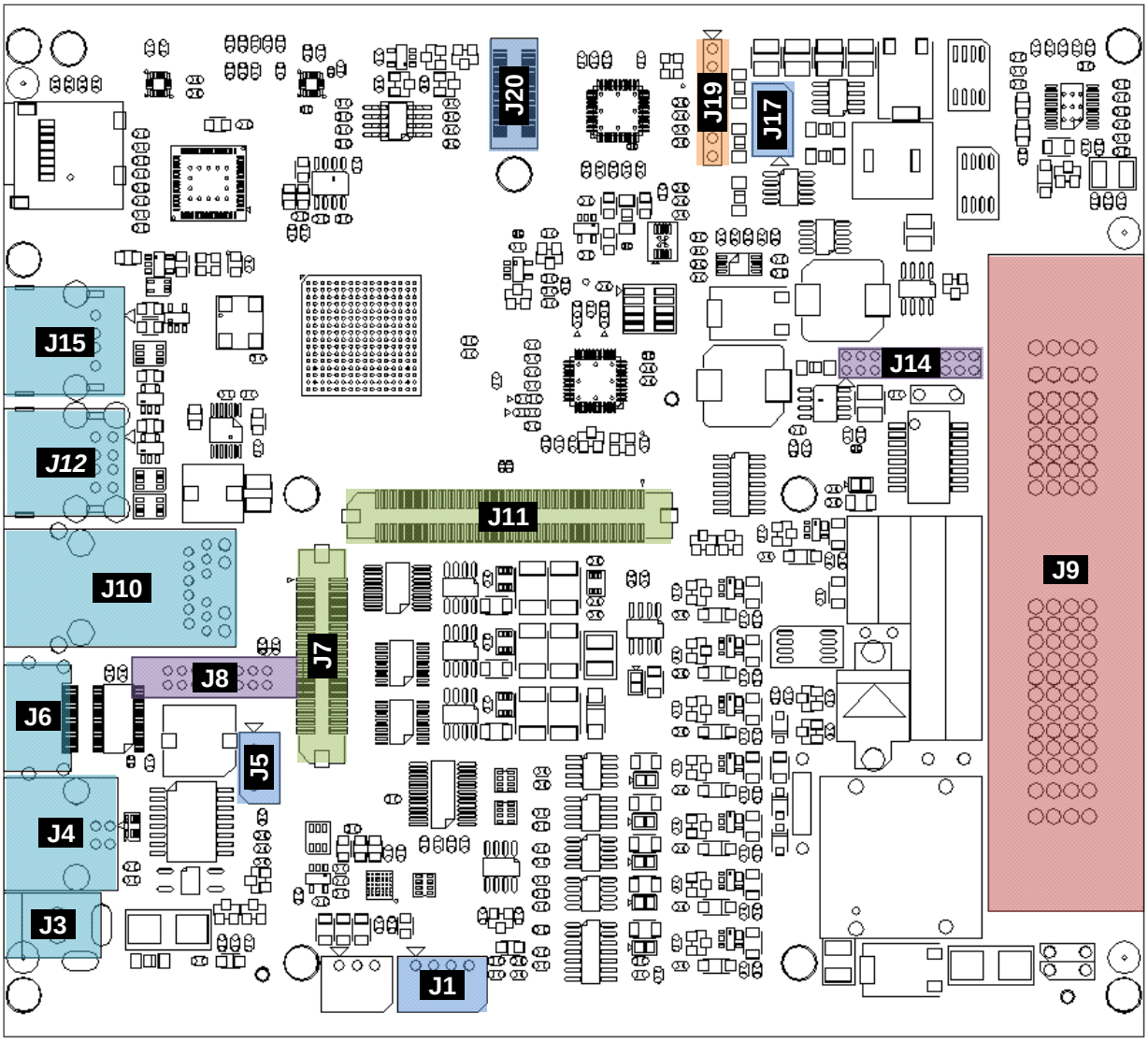


Figure 5: RC2carrier – component placement

- J9 is the automotive connector vehicle-side;
- J7 and J11 are the connectors for the core logic;
- in the left side, are visible:
  - J3 is the jack connector per the auxiliary power supply,
  - J4 is the connector for the USB device,
  - J6 is the HDMI connector,
  - J10 is the Ethernet connector,
  - J12 and J15 are the connectors for USB host
- J20 is the connector for the communication module;
- J19 is the connector for the diagnosis module;
- J8 e J14 are the connectors for the expansion module;
- J1 can be connected to the debug connector on logic core (J7, ref. Table 26); this allow to translate the logic level signal into RS232 levels; the converted signals are available in connector J5
- J17 is the connector per the internal backup battery

The PCB is almost square and measures 161x146mm.

In the carrier board the LVDS, RGB-parallel, SATA, SPI and some GPIO are completely unused; the serial lines, USB, PCIe, HDMI, Ethernet and SD interfaces are instead needed by the devices installed on carrier and communication modules; this allows to use only 2 of the 3 high density connectors on the bottom face of the core logic; therefore, the carrier module only uses the connectors J7 and J11 (associated with J2 and J5 on the core logic).
For the pinout of connector J7, refer to 4.1.3.2; for the pinout of connector J11, refer to 4.1.3.1.

4.2.2. Vehicle-side connector – J9

For all details, refer to 3.1.1.

4.2.3. User-side connector – J3, J4, J6, J10, J12 and J15

For all details, refer to 3.2.

4.2.4. Connector for communication module – J20

The connector for the communication module provides the power supply and all peripherals necessary for communication with devices on the module itself.

Below are listed the devices present on communication module:
- GPS module with dead-reckoning (Ublox NEO6V); it requires 1 channel USB 2.0;
- UMTS and CDMA module (Cinterion PXS8); it requires 1 channel USB 2.0;
- BT module (Bluegiga BT111); it requires 1 channel USB 2.0;
- WiFi b/g/n module (Bluegiga WF111); it requires 1 channel SDIO;
- some generic signals for future uses; this for guarantee the use of another communication module that integrates on board different devices from those listed above.

Table 40 lists the pinout of the connector J20.

Signal	Pin	Vdd	Dir.	Description
VCC	1	5.0V	Out	5V power supply
VCC	2	5.0V	Out	5V power supply
	3			n.c.
N6_USB_EN	4	5.0V	Out	Power supply enable of USB channel for GPS
N6_USB_DP	5	5.0V	Bi	Data+ signal of USB channel for GPS
N6_USB_D-	6	5.0V	Bi	Data- signal of USB channel for GPS
N6_VCC_EN	7	3.3V	Out	Power supply enable of GPS
N6_TX	8	3.3V	In	TX signal for GPS
N6_RX	9	3.3V	Out	RX signal for GPS
BT_USB_EN	10	5.0V	Out	Power supply enable of USB channel for BT
BT_USB_D-	11	5.0V	Bi	Data- signal of USB channel for BT

Signal	Pin	Vdd	Dir.	Description
BT_USB_D+	12	5.0V	Bi	Data+ signal of USB channel for BT
PLDC_EXP9	13	3.3V	Bi	General purpose IO for future use
PLDC_EXP8	14	3.3V	Bi	General purpose IO for future use
PLDC_EXP7	15	3.3V	Bi	General purpose IO for future use
PLDC_EXP6	16	3.3V	Bi	General purpose IO for future use
PLDC_EXP5	17	3.3V	Bi	General purpose IO for future use
VCC3	18	3.3V	Out	3.3V power supply
SD2_DAT0	19	3.3V	Bi	Data0 signal of 2nd SD channel for WiFi
SD2_DAT1	20	3.3V	Bi	Data1 signal of 2nd SD channel for WiFi
SD2_DAT2	21	3.3V	Bi	Data2 signal of 2nd SD channel for WiFi
SD2_DAT3	22	3.3V	Bi	Data3 signal of 2nd SD channel for WiFi
SD2_CLK	23	3.3V	Bi	Clk signal of 2nd SD channel for WiFi
SD2_CMD	24	3.3V	Bi	Cmd signal of 2nd SD channel for WiFi
WF_ON	25	3.3V	Out	Power supply enable of WiFi
PLDC_EXP1	26	3.3V	Bi	General purpose IO for future use
PLDC_EXP2	27	3.3V	Bi	General purpose IO for future use
PLDC_EXP3	28	3.3V	Bi	General purpose IO for future use
PLDC_EXP4	29	3.3V	Bi	General purpose IO for future use
VCC3_KL	30	3.3V	Out	Stand-by power supply
GSM_PWR_ON	31	3.3V	Out	Power supply enable of modem
	32			n.c.
SYNC	33	3.3V	In	Sync signal from modem
PXS8_USB_D-	34	5.0V	Bi	Data- signal of USB channel for modem
PXS8_USB_D+	35	5.0V	Bi	Data+ signal of USB channel for modem
WU_GSM	36	3.3V	In	WakeUp signal from modem
PXS8_USB _EN	37	5.0V	Out	Power supply enable of USB channel for modem
GSM_-ON/OFF	38	3.3V	Out	On/Off signal of modem
	39			n.c.
GSM_RST	40	3.3V	Out	Reset signal of modem
VDD_SYS_3V8	41	3.8V	Out	Power supply for modem
VDD_SYS_3V8	42	3.8V	Out	Power supply for modem
VDD_SYS_3V8	43	3.8V	Out	Power supply for modem
VDD_SYS_3V8	44	3.8V	Out	Power supply for modem
	45			n.c.
GND	46	-	-	Ground reference
GND	47	-	-	Ground reference
GND	48	-	-	Ground reference
GND	49	-	-	Ground reference
GND	50	-	-	Ground reference

Table 40: RC2carrier – connector pinout of communication module

All enable signal listed on Table 40 are active high.

4.2.5. Connector for diagnostic module – J19

The connector for the diagnostic module provides the power for the LED matrix and display needed to provide diagnostic system.
In order to reduce the dimensions of this connector, the philosophy adopted is to realize the diagnosis with a small processor mounted on the module; this processor communicates with the FPGA, through the connector, and manages the matrix LEDs and display; in this way, all diagnostic messages are encoded and communicated via serial line.

Table 41 lists the pinout of the connector J19.

Signal	Pin	Vdd	Dir.	Description
VCC	1	5.0V	Out	5V power supply
RX_DIAG	2	3.3V	In	RX signal from diagnosis module
TX_DIAG	3	3.3V	Out	TX signal to diagnosis module
VCC3	4	3.3V	Out	3.3V power supply
USER_LAN_ACT	5	3.3V	Out	activity LED for Ethernet user side
SYNC	6	3.3V	Out	modem sync
GND	7	-	-	Ground reference

Table 41: RC2carrier – connector pinout of diagnosis module

The matrix of LEDs present on the diagnosis module is used to highlight the behavior of the various elements present in the system, in particular can be highlighted:

- CAN and K lines activity;
- vehicle-side Ethernet activity;
- BT, WiFi and modem activity;
- GPS fix;
- the power supply status of and its possible failures.

In the full version, the alphanumeric display allows to add additional details as already indicated by the matrix LEDs.

4.2.6. Connectors for expansion module – J8 and J14

The pins on the vehicle-side connector (J9) currently free are available on connector J14 and some free signals of the FPGA are present on the connector J8. This allows to realize a possible expansion module to add specific functionalities to the system.

Table 42 lists the pinout of the connector J14.

Signal	Pin	Signal	Pin
VPWRPROT	1	GND	2
EXP_10	3	EXP_9	4
EXP_12	5	EXP_11	6
EXP_13	7	EXP_14	8
EXP_2	9	EXP_1	10
EXP_5	11	EXP_6	12
EXP_3	13	EXP_18	14
EXP_4	15	EXP_17	16
EXP_7	17	EXP_16	18
EXP_15	19	EXP_8	20

Table 42: RC2carrier – connector pinout of expansion module

All the signal EXPxy are also present in the right section of the vehicle-side connector, as shown in Table 2.

Caution: on pin 1 the protected power supply from external battery is available.

4.2.7. Connectors for debug – J1 and J5

Connector J1 can be connected to the debug connector on logic core (J7, ref. Table 26); this allow to translate the logic level signal into RS232 levels; the converted signals are available in connector J5.

The J1 connector pinout is resumed on Table 43.

Signal	Pin	Vdd	Dir.	Description
ENABLE	1	3.3V	Out	Enable the buffer on Tx-Rx signal in the core logic
RX-DEBUG	2	3.3V	Out	RX signal of debug console
TX-DEBUG	3	3.3V	In	TX signal of debug console
GND	4	-	-	Reference ground

Table 43: RC2carrier – auxiliary input connector for console

The J5 connector pinout is resumed on Table 44.

Signal	Pin	Vdd	Dir.	Description
TX-DEBUG-232	1	±5V	Out	RS232 TX signal of debug console
RX-DEBUG-232	2	±5V	In	RS232 RX signal of debug console
GND	3	-	-	Reference ground

Table 44: RC2carrier – auxiliary output connector for console

4.2.8. Connectors for backup battery – J17

The internal backup battery must be connected to connector J17; in this way, the circuit for power management is supplied with a buffered and always available voltage; moreover, the charge circuit is also connected to this connector, in order to guarantee the optimal charge-state of the backup battery.

The J17 connector pinout is resumed on Table 45.

Signal	Pin	Vdd	Dir.	Description
GND	1	-	-	Reference ground
VBATT	2	LICELL	Bi	Backup battery positive pole
NTC	3	LICELL	In	Temperature sensing signal

Table 45: RC2carrier – auxiliary output connector for console

Note: the backup battery voltage is also connected to the logic core on pin 5 (P3V3_LICELL) of connector J2; in this way, the keep-alive circuit on the processor is supplied with and always available voltage.

4.3. Communication module

This chapter defines the characteristics of a device, hereinafter referred as "communication module", intended to provide the connectivity for the core logic to the external world.
All signals between the core and communication module pass through the carrier board.

Below are listed the devices present on communication module:

- GPS module with dead-reckoning (Ublox NEO6V); it requires 1 channel USB 2.0
- UMTS and CDMA module (Cinterion PXS8); it requires 1 channel USB 2.0
- BT module (Bluegiga BT111); it requires 1 channel USB 2.0
- WiFi b/g/n module (Bluegiga WF111); it requires 1 channel SDIO

4.3.1. Printed circuit board

Figure 6 shows the location of the elements on the circuit board of the communication module.

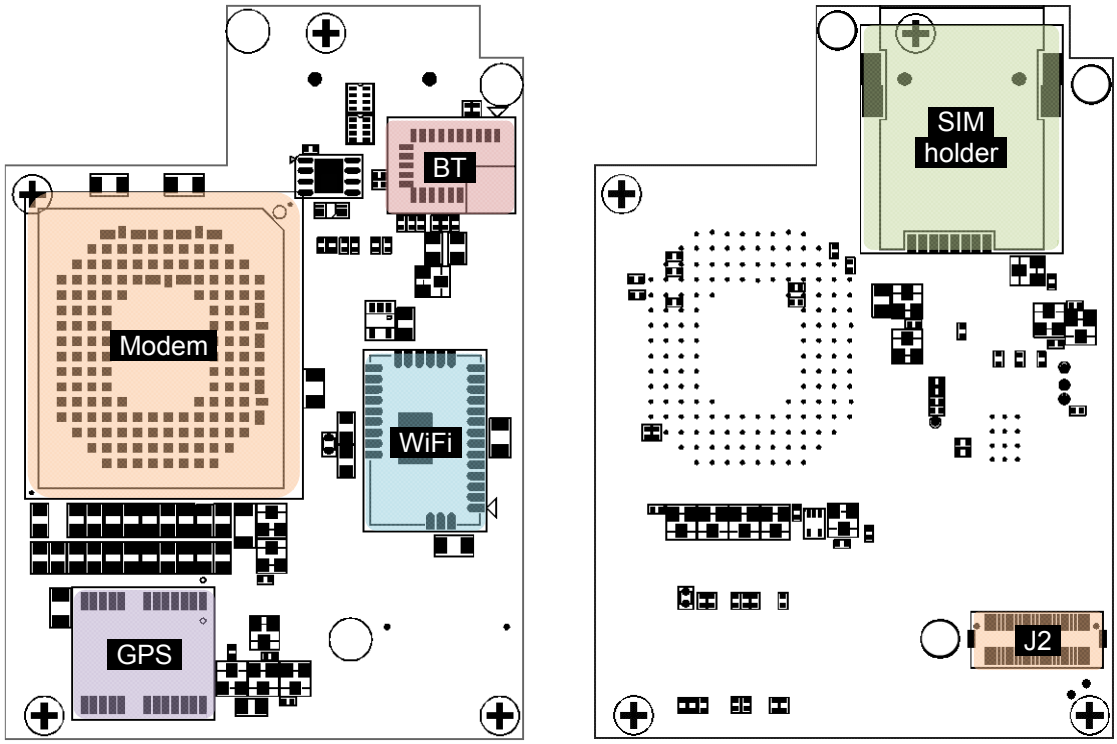


Figure 6: RC2comm – component placement

The PCB is rectangular (shaped) and measures 61x87mm.
The left image is the upper side of the core logic, the right is the bottom side.

4.3.2. Connector for carrier board connection – J2

This connector matched the J20 connector on carrier board (rif. Table 42).

Table 46 lists the pinout of the connector J2.

Signal	Pin	Vdd	Dir.	Description
VCC	1	5.0V	Out	5V power supply
VCC	2	5.0V	Out	5V power supply
	3			n.c.
N6_USB_EN	4	5.0V	Out	Power supply enable of USB channel for GPS
N6_USB_DP	5	5.0V	Bi	Data+ signal of USB channel for GPS
N6_USB_D-	6	5.0V	Bi	Data- signal of USB channel for GPS
N6_VCC_EN	7	3.3V	Out	Power supply enable of GPS
N6_TX	8	3.3V	In	TX signal for GPS
N6_RX	9	3.3V	Out	RX signal for GPS
BT_USB_EN	10	5.0V	Out	Power supply enable of USB channel for BT
BT_USB_D-	11	5.0V	Bi	Data- signal of USB channel for BT
BT_USB_D+	12	5.0V	Bi	Data+ signal of USB channel for BT
	13			n.c.
	14			n.c.
	15			n.c.
	16			n.c.
	17			n.c.
VCC3	18	3.3V	Out	3.3V power supply
SD2_DAT0	19	3.3V	Bi	Data0 signal of 2nd SD channel for WiFi
SD2_DAT1	20	3.3V	Bi	Data1 signal of 2nd SD channel for WiFi
SD2_DAT2	21	3.3V	Bi	Data2 signal of 2nd SD channel for WiFi

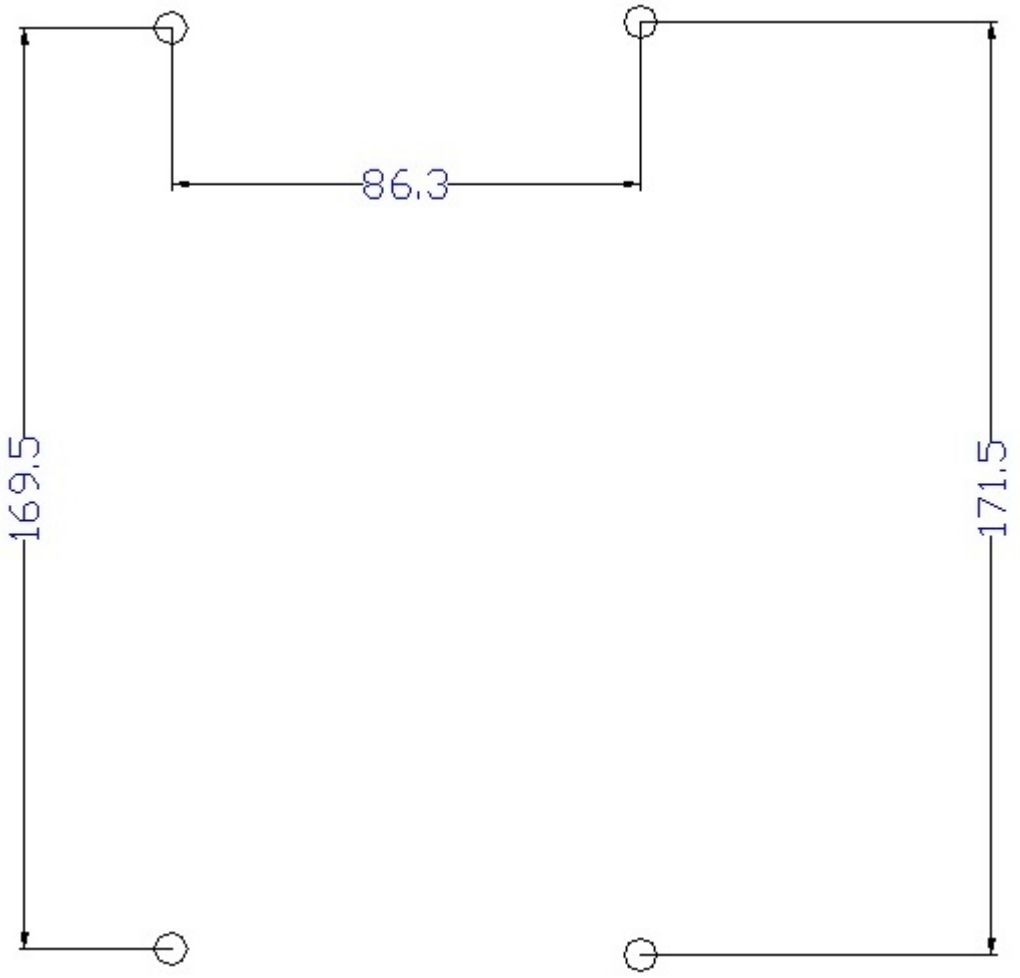
Signal	Pin	Vdd	Dir.	Description
SD2_DAT3	22	3.3V	Bi	Data3 signal of 2nd SD channel for WiFi
SD2_CLK	23	3.3V	Bi	Clk signal of 2nd SD channel for WiFi
SD2_CMD	24	3.3V	Bi	Cmd signal of 2nd SD channel for WiFi
WF_ON	25	3.3V	Out	Power supply enable of WiFi
	26			n.c.
	27			n.c.
	28			n.c.
	29			n.c.
VCC3_KL	30	3.3V	Out	Stand-by power supply
GSM_PWR_ON	31	3.3V	Out	Power supply enable of modem
	32			n.c.
SYNC	33	3.3V	In	Sync signal from modem
PXS8_USB_D-	34	5.0V	Bi	Data- signal of USB channel for modem
PXS8_USB_D+	35	5.0V	Bi	Data+ signal of USB channel for modem
WU_GSM	36	3.3V	In	WakeUp signal from modem
PXS8_USB _EN	37	5.0V	Out	Power supply enable of USB channel for modem
GSM_-ON/OFF	38	3.3V	Out	On/Off signal of modem
	39			n.c.
GSM_RST	40	3.3V	Out	Reset signal of modem
VDD_SYS_3V8	41	3.8V	Out	Power supply for modem
VDD_SYS_3V8	42	3.8V	Out	Power supply for modem
VDD_SYS_3V8	43	3.8V	Out	Power supply for modem
VDD_SYS_3V8	44	3.8V	Out	Power supply for modem
	45			n.c.
GND	46	-	-	Ground reference
GND	47	-	-	Ground reference
GND	48	-	-	Ground reference
GND	49	-	-	Ground reference
GND	50	-	-	Ground reference

Table 46: RC2comm – connector pinout of communication module

5. Mechanical

5.1. Top view

Hole fixing quotes.



6. Installation

6.1. General warnings

This manual is an integral and essential to the product. Carefully read the instructions contained herein as they provide important information regarding the safe use and maintenance.
This equipment is to be used only for the purposes it was designed to. Any other use is considered improper and therefore dangerous. The manufacturer can not be held responsible for any damage caused by improper, incorrect or unreasonable.
DMD is only responsible for the device in its original setting.
Any changes to the structure or operating cycle of the device must be performed or authorized by the technical department of the DMD.
DMD is not responsible for the consequences resulting from the use of non original aftermarket parts.
DMD reserves the right to make any technical changes to this manual and the device without prior notice. If you discover any typographical or other, the corrections will be included in new versions of the manual.
DMD is only responsible of the information contained in the original version of the Italian manual.

The box is composed of a plastic box with aluminum inserts designed to facilitate better heat dissipation and to be easily anchored in the designated location.
For installations above 60° C ambient temperature consider to protect device metallic parts from accidental contact.

6.2. Antenna mounting

Pay close attention to the minimum distance between the antennas and the driver: must be more than 50 cm

6.3. Connections

The unit is supplied with a battery connected internally to the system. Consequently, even if the wiring is disconnected (or however with VBATT and BGND not connected), a small portion of the system may be "turned on"; the internal PC, all devices are "off".
Where possible, keep the connecting cables away from sources and radio antennas.