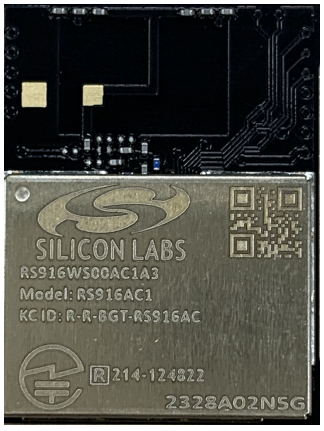
RS916AC0 and RS916AC1 Connectivity Module Data Sheet

Silicon Labs' RS916AC0 and RS916AC1 single band radio modules provide a comprehensive multi-protocol wireless connectivity solution including 802.11 b/g/n (2.4 GHz), 802.11j, and dual-mode Bluetooth 5. The modules offer high throughput, extended range with power-optimized performance. The modules come with modular radio type approvals for various countries, including USA (FCC), Canada (IC/ISED) and MIC (Japan), and are in compliance with the relevant EN standards (including EN 300 328 v2.2.2) for the conformity with the directives and regulations in the EU and UK.

Applications

- **Smart Home**
  - Smart Locks, Motion/Entrance Sensors, Water Leak sensors, Smart plugs/switches, LED lights, Door-bell cameras, Washers/Dryers, Refrigerators, Thermostats, Consumer Security cameras, Voice Assistants, etc.
- **Other Consumer Applications**
  - Toys, Anti-theft tags, Smart dispensers, Weighing scales, Blood pressure monitors, Blood sugar monitors, Portable cameras, etc.
- **Other Applications (Medical, Industrial, Retail, Agricultural, Smart City, etc.)**
  - Healthcare Tags, Medical patches/pills, Infusion pumps, Sensors/actuators in Manufacturing, Electronic Shelf labels, Agricultural sensors, Product tracking tags, Smart Meters, Parking sensors, Street LED lighting, Automotive After-market, Security Cameras, etc.



KEY FEATURES

- **Wi-Fi**
  - Compliant to single-spatial stream IEEE 802.11 b/g/n with single band support
  - Support for 20 MHz channel bandwidth
  - Transmit power up to +16 dBm with integrated PA
  - Receive sensitivity as low as -94.5 dBm
  - Data Rates: 802.11b: Up to 11 Mbps; 802.11g: Up to 54 Mbps; 802.11n: MCS0 to MCS7
  - Operating Frequency Range: 2412 MHz to 2462 MHz (default - US/Canada) or 2472 MHz (other countries, as required)
- **Bluetooth**
  - Transmit power up to +14 dBm with integrated PA
  - Receive sensitivity:- LE: -93 dBm, LR 125 Kbps: -104 dBm
  - Compliant to dual-mode Bluetooth 5
  - <8 mA transmit current in Bluetooth 5 mode, 2 Mbps data rate
  - Data rates: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps, 3 Mbps
  - Operating Frequency Range: 2.402 GHz - 2.480 GHz
  - Bluetooth 2.1 + EDR, Bluetooth Low Energy 4.0 / 4.1 / 4.2 / 5.0
  - Bluetooth Low Energy 1 Mbps, 2 Mbps and Long Range modes
  - Bluetooth Low Energy Secure connections
  - Bluetooth Low Energy supports central role and peripheral role concurrently
  - Bluetooth auto rate and auto TX power adaptation
  - Scatternet* with two secondary roles while still being visible
- **RF**
  - Integrated baseband processor with calibration memory, RF transceiver, high-power amplifier, balun and T/R switch

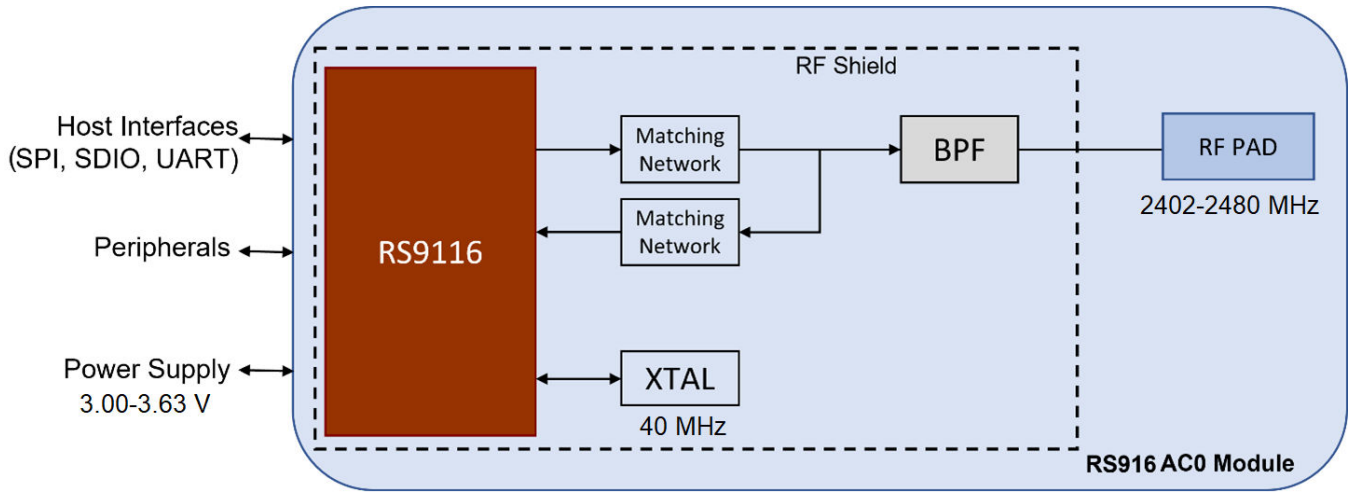
KEY FEATURES

- **Power Consumption[3]**
  - Wi-Fi Standby Associated mode current: 61 uA @ 1 second beacon listen interval
  - Wi-Fi 1 Mbps Listen current: 14 mA
  - Wi-Fi LP Rx current: 19 mA
  - Deep sleep current <1 uA, Standby current (RAM retention) < 10 uA
- **Operating Conditions**
  - Operating supply range: 3.0 V to 3.63 V
  - Operating temperature: -40 ºC to +85 ºC
- **Size**
  - Small Form Factor: 21.10 x 16 x 2.32 mm
- **Evaluation Kits**
  - RS916AC0-EXP8037A
  - RS916AC1-EXP8037B
- **Software Operating Modes[1]**
  - Embedded mode (WiSeConnect™): Wi-Fi stack, TCP/IP stack, IP modules, Bluetooth stack and some profiles reside in the modules; some of the Bluetooth profiles reside in the host processor
  - Hosted mode (n-Link™): Wi-Fi stack, Bluetooth stack and profiles and all network stacks reside on the host processor
- **Embedded Mode (WiSeConnect™)**
  - Available host interface: SDIO, UART and SPI
  - Support for Embedded Client mode, Access Point mode (Up to 4 clients), Concurrent Client and Access Point mode, and Enterprise Security
  - Supports advanced security features: WPA2/WPA3 - Personal and WPA/WPA2 - Enterprise
  - Integrated TCP/IP stack, HTTP/HTTPS, SSL/TLS, MQTT
  - Bluetooth built-in stack support for L2CAP, RFCOMM, SDP, SPP, GAP
  - Bluetooth profile support for GAP, SDP, SPP, GATT, L2CAP, RFCOMM
  - Wireless firmware update and provisioning
  - Support for concurrent Wi-Fi, dual-mode Bluetooth 5
- **Hosted Mode (n-Link™)**
  - Available host interface: SDIO 2.0
  - Application data throughput up to 50 Mbps (Hosted Mode) in 802.11n with 20MHz bandwidth.
  - Host drivers for Linux
  - Support for Client mode, Access point mode (Up to 16 clients), Concurrent Client and Access Point mode, Enterprise Security
  - Support for concurrent Wi-Fi, dual-mode Bluetooth 5
- **Security**
  - Accelerators: AES128/256 in Embedded Mode
  - WPA/WPA2/WPA3-Personal, WPA/WPA2 Enterprise for Client
- **Wireless Qualifications and Regulatory Certifications**
  - Wi-Fi Alliance, Bluetooth SIG
  - FCC (USA), IC/ISED (Canada), CE (EU), UKCA (UK), MIC (Japan), KC (South Korea), NCC (Taiwan)[2], SRRC (China)[2]

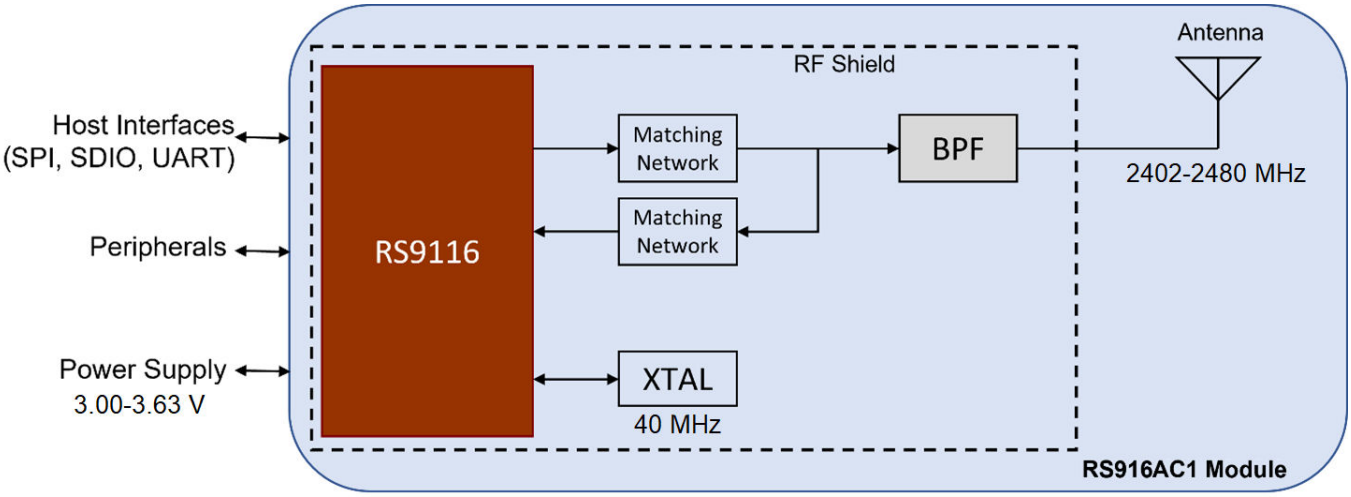
Note:

1. For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.
2. As of the time of release of this Rev 0.6, the modules are still undergoing regulatory certification testing and/or are in the final steps of obtaining the certification(s).
3. All power and performance numbers are under ideal conditions.

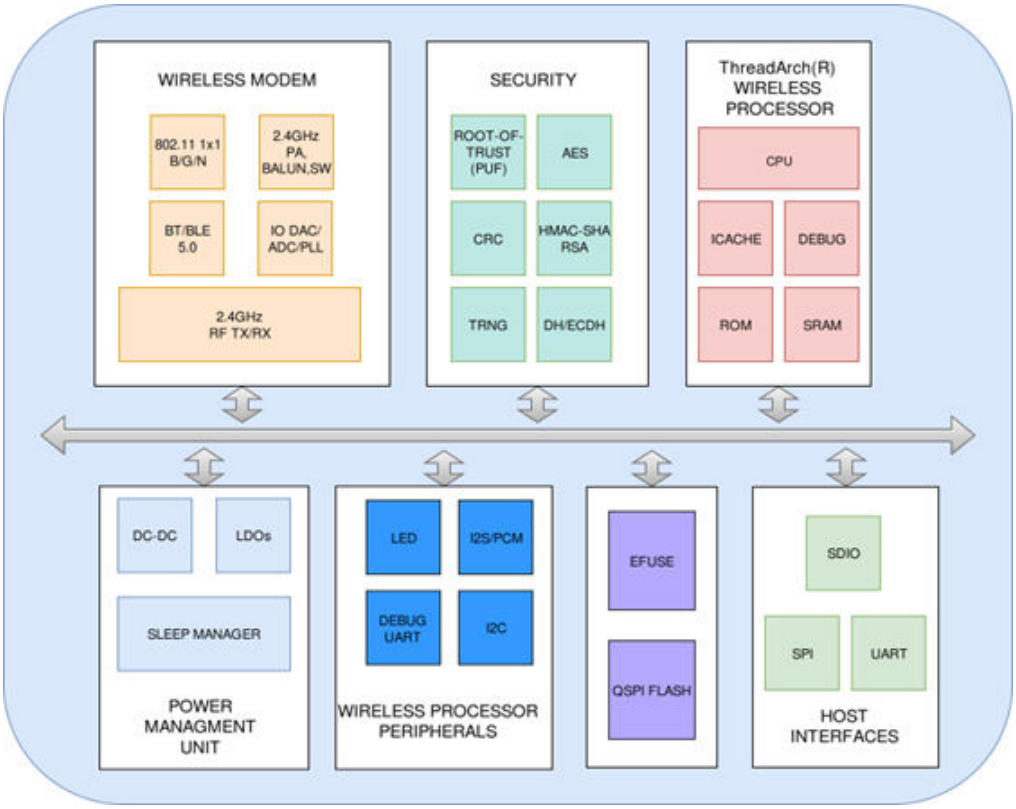
Block Diagrams



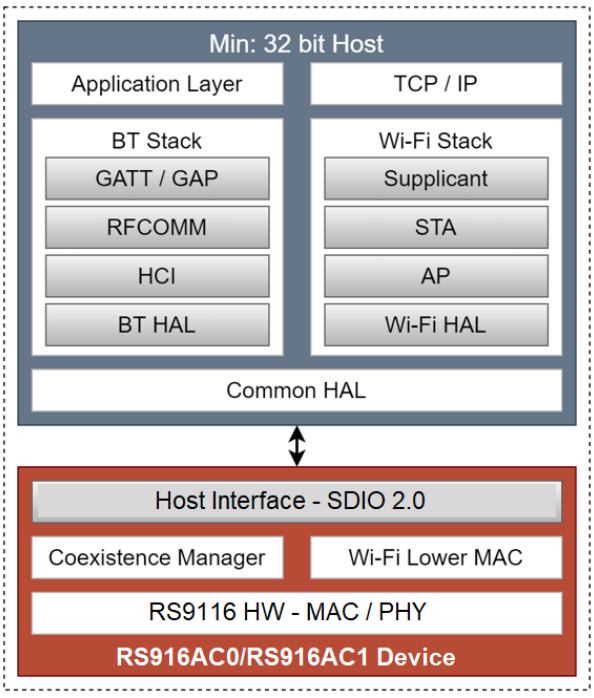
RS916AC0 Module Block Diagram



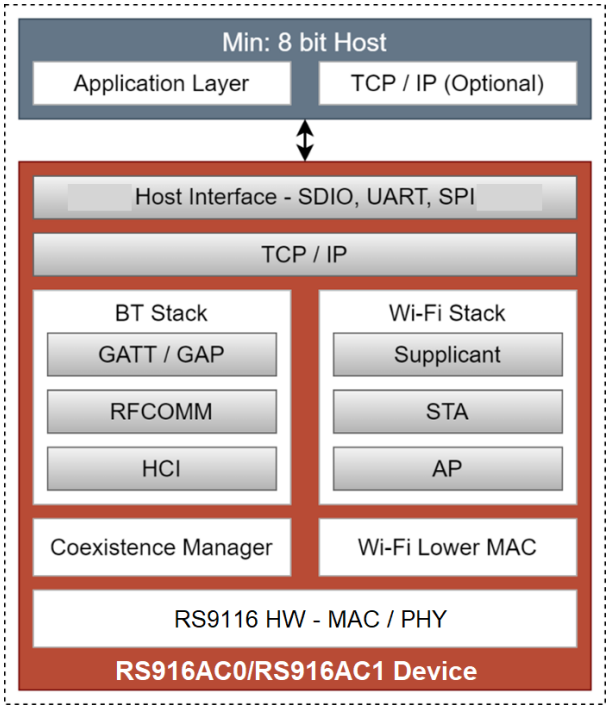
RS916AC1 Module Block Diagram



RS916 Connectivity Hardware Block Diagram



Hosted Software Architecture



Embedded Software Architecture

Note:

1. Customers can connect multiple hosts, but only one host interface can be active after power-on.

Table of Contents

1. RS916AC0 and RS916AC1 Module Pinout and Pin Description

1.1 Pin Diagram

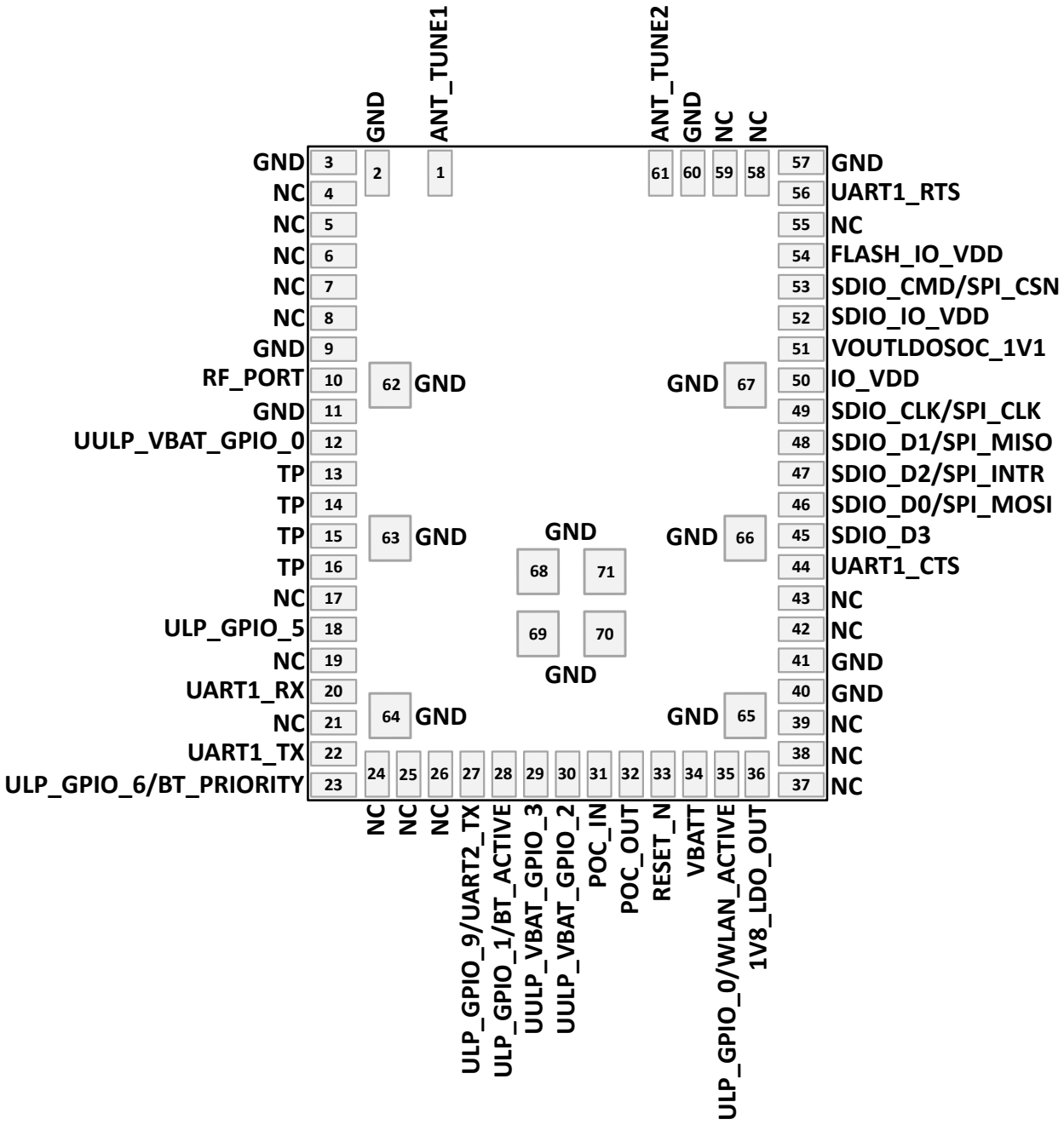


Figure 1.1. RS916AC0 and RS916AC1 Pin Diagram

1.2 Pin Description

1.2.1 RF and Control Interfaces

Table 1.1. RF and Control Interfaces

Pin Name	Pin #	I/O Supply Domain	Direction	Initial State (Power Up, Active Reset)	Description
RF_PORT[1]	10	NA	Inout	NA	Connect to Antenna with a 50 Ω impedance as per the Reference Schematics
RESET_N	33	VBATT	Input	NA	Active-low asynchronous reset signal
POC_IN	31	IO_VDD	Input	NA	Power On Control Input. This is an input to the chip. It should be made high only after supplies are valid to ensure the module is in safe state until valid power supply is available.
POC_OUT	32	IO_VDD	Output	NA	Power On Control Output. This is internally generated. Initially, it is low. But it becomes high when the supplies (VBATT) are valid.
ANT_TUNE1[2]	1	NA	Input	NA	External fine-tuning option for Antenna; connect same tuning circuit on both ANT_TUNE1 and ANT_TUNE2 pins
ANT_TUNE2[2]	61	NA	Input	NA	External fine-tuning option for Antenna; connect same tuning circuit on both ANT_TUNE1 and ANT_TUNE2 pins

Note:

1. Pin RF_PORT is available in RS916AC0 module only
2. Pins ANT_TUNE1 and ANT_TUNE2 are available in RS916AC1 module only.

1.2.2 Power and Ground and No Connect Pins

Table 1.2. Power and Ground Pins

Pin Name	Type	Pin #	Direction	Description
VBATT	Power	34	Input	Power supply for the on-chip Buck, RF circuit.
VOUTLDOSOC_1V1	Power	51	Output	Output of SoC LDO. Not intended to power external circuitry. This pin is internally decoupled and should be left unconnected.
1V8_LDO_OUT	Power	36	Output	Output of 1.8V LDO
FLASH_IO_VDD	Power	54	Input	I/O Supply for internal QSPI Flash signals; connect to 1V8_LDO_OUT as per the Reference Schematics
SDIO_IO_VDD	Power	52	Input	I/O Supply for SDIO I/Os; refer to the GPIOs section for details on which GPIOs have this as the I/O supply
IO_VDD	Power	50	Input	I/O Supply for GPIOs, ULP_GPIOs, UULP_GPIOs Refer to the GPIOs section for details on which GPIOs have this as the I/O supply
GND	Ground	2, 3, 9, 11, 40, 41, 57, 60, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71	GND	Common ground pins
TP	Test Point	13,14,15,16	TP	Test Point
NC	No Connect	4, 5, 6, 7, 8, 17, 18, 19, 21, 24, 25, 26, 37, 38, 39, 42, 43, 55, 58, 59	NC	Do Not Connect

1.2.3 Host and Peripheral Interfaces

Table 1.3. Host and Peripheral Interfaces

Pin Name	Pin #	I/O Supply Domain	Direction	Initial State (Power Up, Active Reset)	Description[1, 2, 3, 4, 5]		
UART1_RX	20	IO_VDD	Input	HighZ	**HOST**	**DEFAULT**	**SLEEP**
					UART	UART1_RX - UART Host interface serial input	HighZ
					Non-UART	HighZ	HighZ
					The UART interface is only supported in WiSeConnect™		
UART1_TX	22	IO_VDD	Output	HighZ	**HOST**	**DEFAULT**	**SLEEP**
					UART	UART1_TX - UART Host interface serial output	HighZ
					Non-UART	HighZ	HighZ
					The UART interface is only supported in WiSeConnect™		
UART1_RTS	56	IO_VDD	Output	HighZ	**Default**: HighZ **Sleep**: HighZ This pin can be configured by software to be the following: • UART1_RTS - UART interface Request to Send, if UART Host Interface flow control is enabled The UART interface is only supported in WiSeConnect™		
UART1_CTS	44	IO_VDD	Input	HighZ	**Default**: HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following: • UART1_CTS - UART interface Clear to Send, if UART Host Interface flow control is enabled • UART1_TRANSPARENT_MODE - UART Host interface Transparent Mode, Indication that module has entered TRANSPERENT_MODE • TSF_SYNC - Transmit Synchronization Function signal to indicate to the Host when a packet is transmitted; the signal is toggled once at the end of every transmitted packet The UART interface is only supported in WiSeConnect™		

Pin Name	Pin #	I/O Supply Domain	Direction	Initial State (Power Up, Active Reset)	Description[1, 2, 3, 4, 5]		
SDIO_CLK/ SPI_CLK	49	SDIO_IO_VDD	Input	HighZ	**HOST**	**DEFAULT**	**SLEEP**
					SDIO	SDIO_CLK - SDIO interface clock	HighZ
					SPI	SPI_CLK - SPI Secondary interface clock	HighZ
					Non-SDIO, SPI	HighZ	HighZ
					The SPI interface is only supported in WiSeConnect™		
SDIO_CMD/ SPI_CSN	53	SDIO_IO_VDD	Inout	HighZ	**HOST**	**DEFAULT**	**SLEEP**
					SDIO	SDIO_CMD - SDIO interface CMD signal	HighZ
					SPI	SPI_CSN - Active-low Chip Select signal of SPI Secondary interface	HighZ
					Non-SDIO, SPI	HighZ	HighZ
					The SPI interface is only supported in WiSeConnect™		
SDIO_D0/ SPI_MOSI	46	SDIO_IO_VDD	Inout	HighZ	**HOST**	**DEFAULT**	**SLEEP**
					SDIO	SDIO_D0 - SDIO interface Data0 signal	HighZ
					SPI	SPI_MOSI - SPI Secondary interface Main-Out-Secondary-In signal	HighZ
					Non-SDIO, SPI	HighZ	HighZ
					The SPI interface is only supported in WiSeConnect™		
SDIO_D1/ SPI_MISO	48	SDIO_IO_VDD	Inout	HighZ	**HOST**	**DEFAULT**	**SLEEP**
					SDIO	SDIO_D1 - SDIO interface Data1 signal	HighZ
					SPI	SPI_MISO - SPI Secondary interface Main-In-Secondary-Out signal	HighZ
					Non-SDIO, SPI	HighZ	HighZ
					The SPI interface is only supported in WiSeConnect™		

Pin Name	Pin #	I/O Supply Domain	Direction	Initial State (Power Up, Active Reset)	Description[1, 2, 3, 4, 5]		
SDIO_D2/ SPI_INTR	47	SDIO_IO_VDD	Inout	HighZ	**HOST**	**DEFAULT**	**SLEEP**
					SDIO	SDIO_D2 - SDIO interface Data2 signal	HighZ
					SPI	SPI_INTR - SPI Secondary interface Interrupt Signal to the host	HighZ
					Non-SDIO, SPI	HighZ	HighZ
					The SPI interface is only supported in WiSeConnect™		
SDIO_D3	45	SDIO_IO_VDD	Inout	Pullup	**HOST**	**DEFAULT**	**SLEEP**
					SDIO	SDIO_D3 - SDIO interface Data3 signal	HighZ
					Non-SDIO, SPI	HighZ	HighZ
					The SPI interface is only supported in WiSeConnect™		
ULP_GPIO_0/ WLAN_ACTIVE	35	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ This pin can be configured by software to be the following: • WLAN_ACTIVE*: Active-High signal to indicate to an external Bluetooth IC that WLAN transmission is active. Part of the 3-wire coexistence interface.[6] *This pin is intended to act as WLAN_ACTIVE for wireless coexistence.		
ULP_GPIO_1/ BT_ACTIVE	28	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ This pin can be configured by software to be the following: • BT_ACTIVE*: Active-High signal from an external Bluetooth IC that it is transmitting. Part of the 3-wire coexistence interface.[6] *This pin is intended to act as BT_ACTIVE for wireless coexistence.		

Pin Name	Pin #	I/O Supply Domain	Direction	Initial State (Power Up, Active Reset)	Description[1, 2, 3, 4, 5]
ULP_GPIO_5	18	IO_VDD	Inout	HighZ	**Default**: LP_WAKEUP_IN This is LP Powersave Wakeup indication to Device **Sleep**: HighZ This pin can be configured by software to be any of the following: • LP_WAKEUP_IN : This is LP Powersave Wake-up indication to Device from HOST. • HOST_WAKEUP_INDICATION : This is used as indication from Host to device that host is ready to take the packet and Device can transfer the packet to host. This is supported only in UART host mode. The UART interface is supported only in WiSeConnect™.
ULP_GPIO_6/ BT_PRIORITY	23	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following: • BT_PRIORITY*: Active-High signal from an external Bluetooth IC that indicates that the Bluetooth transmission are a higher priority. Part of the 3-wire coexistence interface.[6] • WAKEUP_FROM_Dev** - Used as a wakeup indication to host from device. *This pin is intended to act as BT_PRIORITY for wireless coexistence. **For Wake-on-Wireless (WAKEUP_FROM_DEV functionality), it is recommended to use an external weak pull-down resistor on this pin, and Software has to be configured suitably.
ULP_GPIO_9/ UART2_TX	27	IO_VDD	Output	HighZ	**Default**: UART2_TX- Debug UART Interface serial output **Sleep**: HighZ This pin can be configured by software to be the following: • UART2_TX : Debug UART interface serial output
UULP_VBAT_GPIO_0	12	IO_VDD	Output	High	**Default**: EXT_PG_EN **Sleep**: SLEEP_IND_FROM_DEV / EXT_PG_EN This pin can be configured by software to be any of the following: • SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode. • EXT_PG_EN: Active-high enable signal to an external power gate which can be used to control the power supplies other than Always-ON VBATT Power Supplies in ULP Sleep mode.

Pin Name	Pin #	I/O Supply Domain	Direction	Initial State (Power Up, Active Reset)	Description[1, 2, 3, 4, 5]
UULP_VBAT_GPIO_2/ HOST_BYP_ULP_WAKEUP	30	IO_VDD	Input	HighZ	**Default**: HOST_BYP **Sleep**: ULP_WAKEUP This signal has two functionalities – one during the bootloading process and one after the bootloading. During bootloading, this signal is an active-high input to indicate that the bootloader should bypass any inputs from the Host processor and continue to load the default firmware from Flash. After bootloading, this signal is an active-high input to indicate that the module should wakeup from its Ultra Low Power (ULP) sleep mode. The bootloader bypass functionality is supported only in WiSeConnect™.
UULP_VBAT_GPIO_3	29	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: XTAL_32KHZ_IN / SLEEP_IND_FROM_DEV This pin can be configured by software to be any of the following: • XTAL_32KHZ_IN: This pin can be used to feed external clock from a host processor or from external crystal oscillator • SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode.

Note:

1. "**Default**" state refers to the state of the device after initial boot loading and firmware loading is complete.
2. "**Sleep**" state refers to the state of the device after entering Sleep state which is indicated by Active-Low "SLEEP_IND_FROM_DEV" signal.
3. Please refer to "**RS9116N Open-Source Driver Technical Reference Manual**" for software programming information in hosted mode.
4. There are some functionalities, such as SLEEP_IND_FROM_DEV, that are available on multiple pins. However, these pins have other multiplexed functionalities. Any pin can be used based on the required functionality. Customer must note the default states before using appropriate pin.
5. In the application, wherever the module is connected to external host, during power-off state, the host should ensure that all the pins (analog or digital) connected to the module are not driven, or the pins must be grounded.
6. Please contact Silicon Labs to learn about availability of this feature.

1.3 Absolute Maximum Ratings

Functional operation above maximum ratings are not guaranteed and may damage the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 1.4. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{store}	**Storage temperature**	**-40**	**+105**	**°C**
$T_{j(max)}$	Maximum junction temperature	-	+125	°C
VBATT	3.3V power supply for the on-chip Buck, RF circuit	-0.5	3.63	V
IO_VDD	I/O supply for GPIOs, ULP_GPIOs, UULP_GPIOs	-0.5	3.63	V
SDIO_IO_VDD	I/O supplies for SDIO I/Os	-0.5	3.63	V
FLASH_IO_VDD	I/O supply for QSPI flash signals	-0.5	3.63	V
I_{max}	Maximum Current consumption in TX mode	-	400	mA
P_{max}	RF Power Level Input to the chip	-	10	dBm
I_{Pmax}	Peak current rating for power supply	-	500	mA

1.4 Recommended Operating Conditions

Table 1.5. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
$T_{ambient}$	**Ambient temperature**	**-40**	**25**	**85**	**°C**
VBATT	3.3V power supply for the on-chip Buck, RF circuit	3.0	3.3	3.63	V
IO_VDD	I/O supply for GPIOs, ULP_GPIOs, UULP_GPIOs	1.75/3.0	1.85/3.3	1.98/3.63	V
SDIO_IO_VDD	I/O supply for SDIO I/Os	1.75/3.0	1.85/3.3	1.98/3.63	V
FLASH_IO_VDD	I/O supply for QSPI flash signals	1.75	1.85	1.98	V

Note:

The module is equipped with RF XTAL and RF components rated up to +105 °C and with power supply decoupling capacitors rated up to +85 °C. The module will have +15 °C self-heating when transmitting continuously at full power. The self-heating depends on the nature of the application, in particular on the amount of data being transmitted, and on the layout and mechanical design of the host product. It is important to follow the layout guidelines for best thermal performance. The self-heating should be considered and taken into account in the end product design.

For the full compliance with the radio regulatory requirements in the countries the module is certified for, the above limits concerning the host supply range are actually mandatory to follow, together with the strict adherence to all the rest of the design guidelines.

1.5 DC Characteristics

1.5.1 Reset Pin

Table 1.6. Reset Pin

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High level input voltage @3.3V	0.8 * VDD	-	-	V
	High level input voltage @1.8V	1.17	-	-	V
V_{IL}	Low level input voltage @3.3V	-	-	0.3 * VDD	V
	Low level input voltage @1.8V	-	-	0.63	V
V_{hys}	Hysteresis voltage	0.05 * VDD	-	-	V

Note:

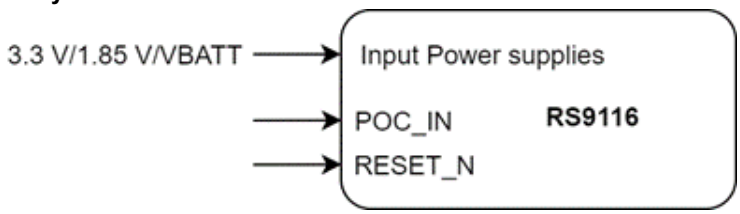
All numbers are at typical operating conditions unless otherwise stated.

1.5.2 Power Sequence

The POC_IN and RESET_N signals should be controlled from external sources such as R/C circuits, and/or other MCU's GPIOs. However, POC_OUT can be connected to POC_IN, if the supply voltage is 3.3V. Below waveforms show power sequence (Up & Down) requirements under various application needs. Note that below waveforms are not to scale.

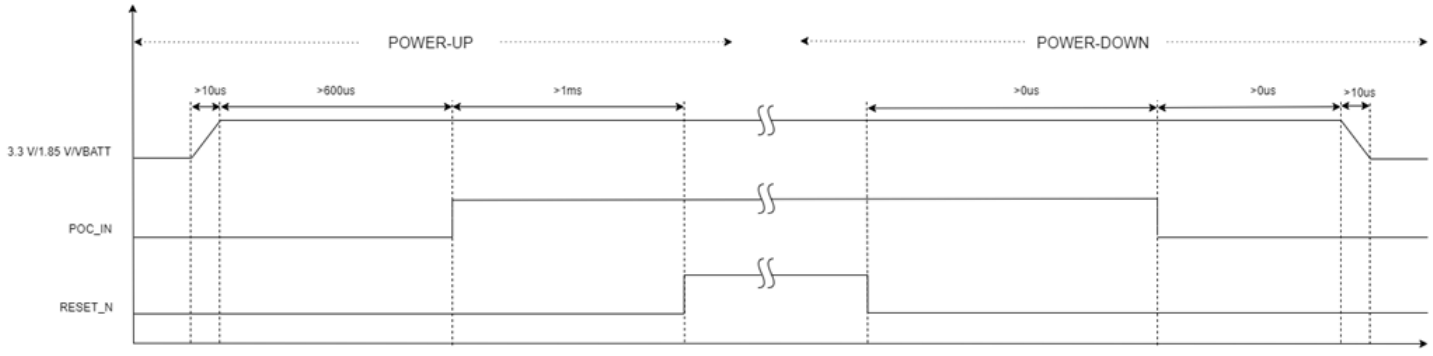
1.5.2.1 Power-Up and Down Sequence with External POC_IN

The diagram below shows connections of various power supply voltages, POC_IN and RESET_N. These connections can be used when **POC_IN is controlled externally**.



Note:

The diagram above is a typical connection diagram. Check the Reference Schematics for connections of other power supplies.



Note:

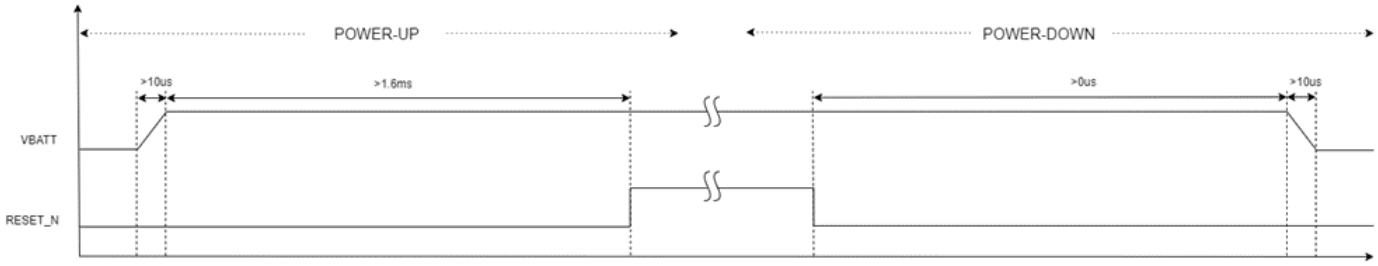
3.3 V/1.85 V/VBATT supply shown above must be connected to the power supply pins of IC/Module. For example, SDIO_IO_VDD, IO_VDD, VBATT, etc.

1.5.2.2 Power-Up and Down Sequence with POC_IN Loopback

The diagram below shows connections of various power supply voltages, POC_IN and RESET_N. The typical applications of this connection can be when **POC_IN is looped back from POC_OUT**. If this connection is used, the module cannot be reset a second time or beyond after power-up.

Note:

1. The diagram shown above is a typical connection diagram. Check the Reference Schematics for connections of other power supplies.
2. POC_OUT can be connected to POC_IN if the input supply voltage (IO_VDD) is 3.3 V only. Otherwise, POC_IN has to be driven externally.
3. This connection is not recommended if the design requires a second reset or beyond after power-up. In that case, please follow the connection diagram in the previous section.



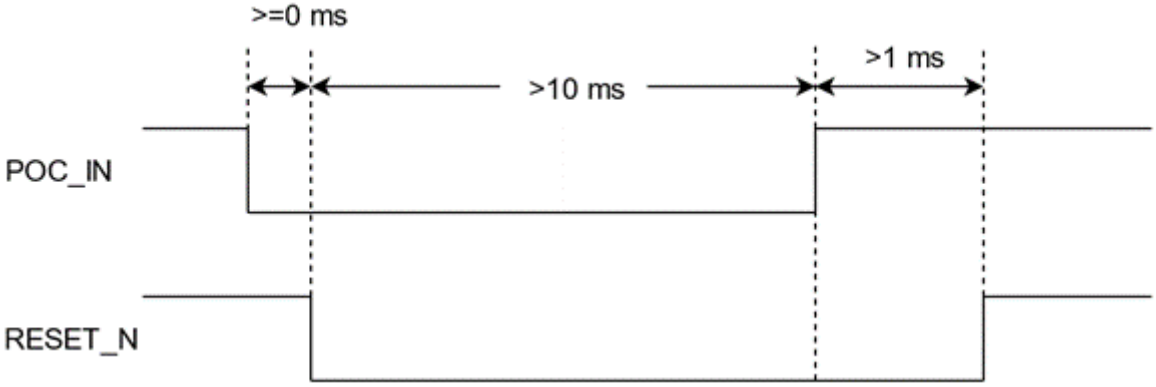
Note:

The VBATT supply as shown above must be connected to the power supply pins of the module. For example, VBATT, SDIO_IO_VDD, IO_VDD etc.

1.5.3 Hardware Resetting Sequence After Power On

During the power-up of the RS916AC0 and RS916AC1 module, a power-up sequence must be followed as per the requirements mentioned in the above section. In some applications, there is a need to reset the RS916AC0 and RS916AC1 module for a second time or beyond after power-up. Follow the below timing diagram in such cases. Because the POC_IN and RESET_N are applied externally, the present state of the device will be lost.

If POC_IN cannot be applied externally or POC_OUT is looped back to POC_IN, then a second reset (or beyond) cannot be applied.



1.5.4 Digital Input Output Signals

Table 1.7. Digital I/O Signals

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High level input voltage @3.3V	2.0	-	-	V
	High level input voltage @1.8V	1.17	-	-	V
V_{IL}	Low level input voltage @3.3V	-	-	0.8	V
	Low level input voltage @1.8V	-	-	0.63	V
V_{hys}	Hysteresis voltage	0.1 VDD	-	-	V
V_{OL}	Low level output voltage	-	-	0.4	V
V_{OH}	High level output voltage	VDD-0.4	-	-	V
I_{OL}	Low level output current (programmable)	-	4.0	-	mA
I_{OH}	High level output current (programmable)	-	4.0	-	mA

Note:

All numbers are at typical operating conditions unless otherwise stated.

1.5.5 Pin Capacitances

Table 1.8. Pin Capacitances

Symbol	Parameter	Min	Typ	Max	Unit
C_{io}	Input/output capacitance, digital pins only	-	-	2.0	pF

1.6 AC Characteristics

1.6.1 Clock Specifications

RS9116 chipsets require two primary clocks:

- Low frequency 32 kHz clock for sleep manager and RTC
  - Internal 32 kHz RC clock is used for applications with low timing accuracy requirements
  - 32 kHz crystal clock is used for applications with high timing accuracy requirements
- High frequency 40 MHz clock for the ThreadArch® processor, baseband subsystem and the radio
  - 40 MHz clock is integrated inside the module, and no external clock needs to be provided

The chipsets have integrated internal oscillators including crystal oscillators to generate the required clocks. Integrated crystal oscillators enable the use of low-cost passive crystal components. Additionally, in a system where an external clock source is already present, the clock can be reused. The following are the recommended options for the clocks for different functionalities:

Functionality	Default Clock Option	Other Clock Option	Comments
Wi-Fi or Wi-Fi + BLE Connectivity	Internal 32 kHz RC oscillator calibrated to <200ppm	32 kHz XTAL oscillator input on UULPGPIO.	32 kHz XTAL Oscillator clock is optional. No significant power consumption impact on connected power numbers (<10uA).

There is no impact on sleep/deep-sleep power consumption with/without 32 kHz XTAL oscillator clock.

32 kHz XTAL Sources:

Option 1: From Host MCU/MPU LVCMOS rail to rail clock input on UULPGPIO
Option 2: External Xtal oscillator providing LVCMOS rail to rail clock input on UULPGPIO (Nano-drive clock should not be supplied).

1.6.1.1 32-kHz Clock

The 32 kHz clock selection can be done through software. RC oscillator clock is not suited for high timing accuracy applications and can increase system current consumption in duty-cycled power modes.

1.6.1.1.1 RC Oscillator

Table 1.9. 32 kHz RC Oscillator

Parameter	Parameter Description	Min	Typ	Max	Unit
F_{osc}	Oscillator Frequency		32.0		kHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage		1.2		%
Jitter	RMS value of Edge jitter (TIE)		91		ns
Peak Period Jitter	Peak value of Cycle Jitter with 6σ variation		789		ns

1.6.1.1.2 32 kHz External Oscillator

An external 32 kHz low-frequency clock can be fed through the XTAL_32KHZ_IN functionality.

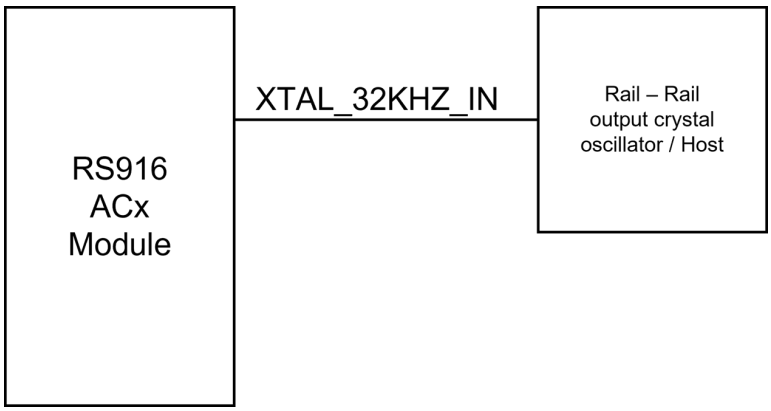


Figure 1.2. External 32 kHz Oscillator - Rail to Rail

Table 1.10. 32 kHz External Oscillator Specifications

Parameter	Parameter Description	Min	Typ	Max	Unit
F_{osc}	Oscillator Frequency		32.768		kHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage	-100		100	ppm
Duty cycle	Input duty cycle	30	50	70	%
V_{AC}	Input AC peak-peak voltage swing at input pin.	-0.3	-	VBATT +/- 10%	Vpp

1.6.2 SDIO 2.0 Secondary

1.6.2.1 Full Speed Mode

Table 1.11. AC Characteristics - SDIO 2.0 Secondary Full Speed Mode

Parameter	Parameter Description	Min	Typ	Max	Unit
T_{sdio}	SDIO_CLK	-	-	25	MHz
T_s	SDIO_DATA/SDIO_CMD, input setup time	4	-	-	ns
T_h	SDIO_DATA/SDIO_CMD, input hold time	1	-	-	ns
T_{od}	SDIO_DATA/SDIO_CMD, clock to output delay	-	-	13	ns
C_L	Output Load	5	-	10	pF

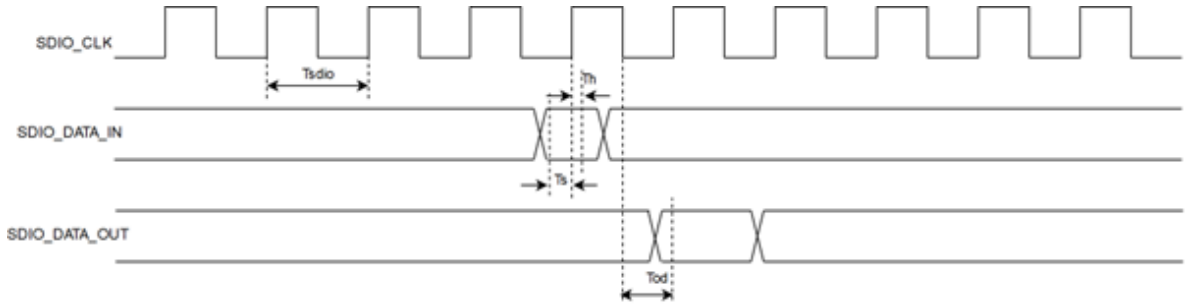


Figure 1.3. Interface Timing Diagram for SDIO 2.0 Secondary Full Speed Mode

1.6.2.2 High Speed Mode

Table 1.12. AC Characteristics - SDIO 2.0 Secondary High Speed Mode

Parameter	Parameter Description	Min	Typ	Max	Unit
T_{sdio}	SDIO_CLK	25	-	50	MHz
T_s	SDIO_DATA/SDIO_CMD, input setup time	4	-	-	ns
T_h	SDIO_DATA/SDIO_CMD, input hold time	1	-	-	ns
T_{od}	SDIO_DATA/SDIO_CMD, clock to output delay	2.5	-	13	ns
C_L	Output Load	5	-	10	pF

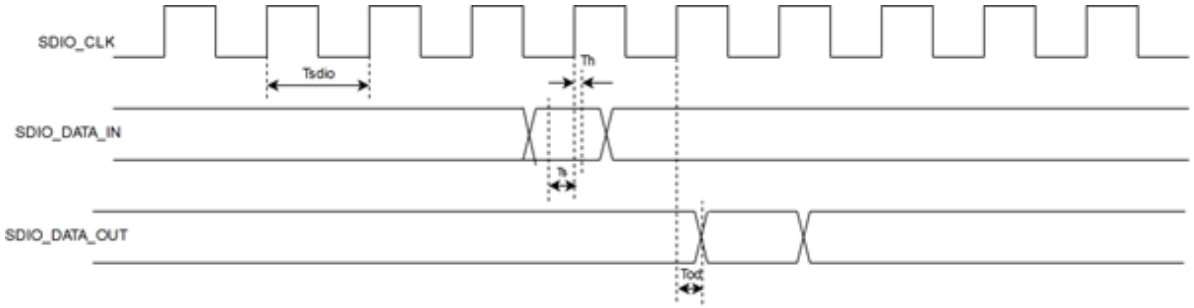


Figure 1.4. Interface Timing Diagram for SDIO 2.0 Secondary High Speed Mode

1.6.3 SPI Secondary

1.6.3.1 Low Speed Mode

Table 1.13. AC Characteristics - SPI Secondary Low Speed Mode

Parameter	Parameter Description	Min	Typ	Max	Unit
T_{spi}	SPI_CLK	0	-	25	MHz
T_{cs}	SPI_CS to output delay	-	-	7.5	ns
T_{cst}	SPI CS to input setup time	4.5	-	-	-
T_s	SPI_MOSI, input setup time	1.33	-	-	ns
T_h	SPI_MOSI, input hold time	1.2	-	-	ns
T_{od}	SPI_MISO, clock to output delay	-	-	8.75	ns
C_L	Output Load	5	-	10	pF

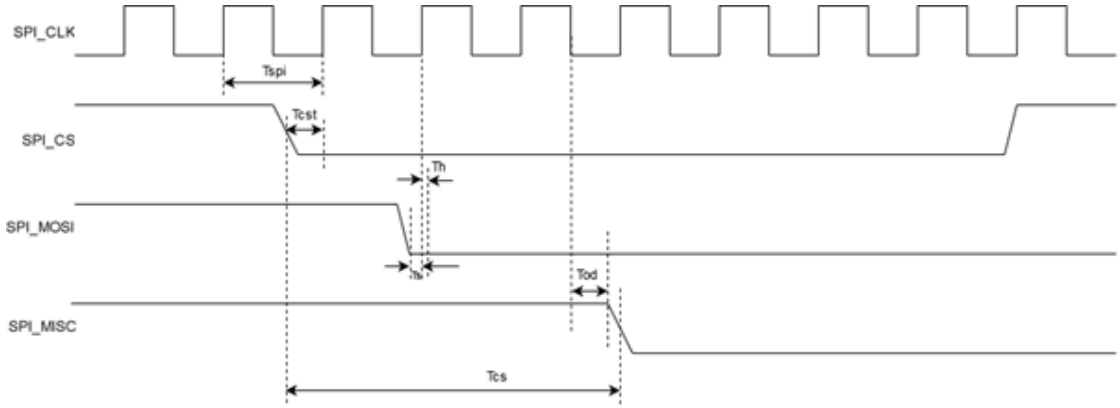


Figure 1.5. Interface Timing Diagram for SDIO 2.0 Secondary Low Speed Mode

1.6.3.2 High Speed Mode

Table 1.14. AC Characteristics - SPI Secondary High Speed Mode

Parameter	Parameter Description	Min	Typ	Max	Unit
T_{spi}	SPI_CLK	25	-	80	MHz
T_{cs}	SPI_CS to output delay	-	-	7.5	ns
T_{cst}	SPI CS to input setup time	4.5	-	-	-
T_s	SPI_MOSI, input setup time	1.33	-	-	ns
T_h	SPI_MOSI, input hold time	1.2	-	-	ns
T_{od}	SPI_MISO, clock to output delay	2.5	-	8.75	ns
C_L	Output Load	5	-	10	pF

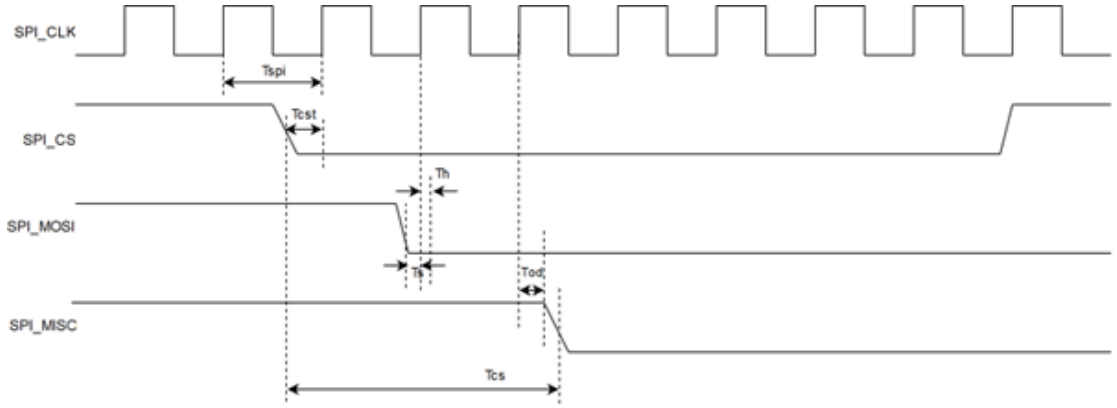


Figure 1.6. Interface Timing Diagram for SDIO 2.0 Secondary High Speed Mode

1.6.3.3 Ultra High Speed Mode

Table 1.15. AC Characteristics - SPI Secondary Ultra High Speed Mode

Parameter	Parameter Description	Min	Typ	Max	Unit
T_{spi}	SPI_CLK	-	-	100	MHz
T_s	SPI_MOSI, input setup time	1.33	-	-	ns
T_h	SPI_MOSI, input hold time	1.2	-	-	ns
T_{od}	SPI_MISO, clock to output delay	1.5	-	8.75	ns
C_L	Output Load	5	-	10	pF

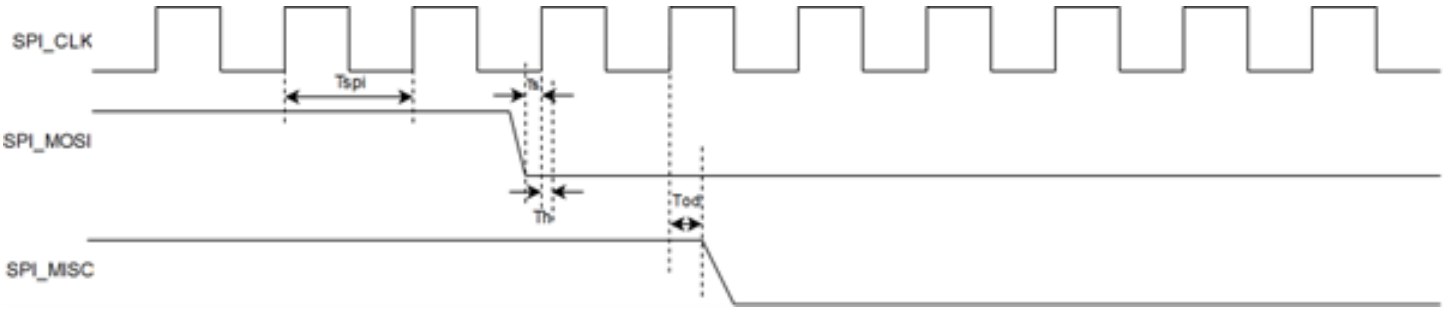


Figure 1.7. Interface Timing Diagram for SDIO 2.0 Secondary Ultra High Speed Mode

1.6.4 UART

Table 1.16. AC Characteristics - UART

Parameter	Parameter Description	Min	Typ	Max	Unit
T_{uart}	CLK	0	-	20	MHz
T_{od}	Output delay	0	-	10	ns
T_s	Input setup time	0	-	5	ns
C_L	Output load	5	-	25	pF

1.6.5 GPIO Pins

Table 1.17. AC Characteristics - GPIO Pins

Parameter	Parameter Description	Conditions	Min	Typ	Max	Unit
T_{rf}	Rise time	Pin configured as output; SLEW = 1(fast mode)	1.0	-	2.5	ns
T_{ff}	Fall time	Pin configured as output; SLEW = 1(fast mode)	0.9	-	2.5	ns
T_{rs}	Rise time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	4.3	ns
T_{fs}	Fall time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	4.0	ns
T_r	Rise time	Pin configured as input	0.3	-	1.3	ns
T_f	Fall time	Pin configured as input	0.2	-	1.2	ns

1.7 RF Characteristics

All specifications are subject to change. Contact Silicon Labs for final numbers.

Note:

In the sub-sections below,

- All numbers are measured at typical operating conditions unless otherwise stated.
- **PLEASE NOTE THAT THE FOLLOWING NUMBERS ARE PRELIMINARY AND ARE NOT THE FINAL VALUES. EXTENSIVE CHARACTERIZATION FOR THE MODULES ARE UNDERWAY. THERE WILL BE SLIGHT VARIATIONS IN THE FINAL VALUES.**

1.7.1 WLAN 2.4 GHz Transmitter Characteristics

1.7.1.1 Transmitter Characteristics with 3.3V Supply

- TA = 25°C, VBATT = 3.3V. Remaining supplies are at typical operating conditions.
- The transmit power numbers are based on average performance across all channels.

Table 1.18. WLAN 2.4 GHz Transmitter Characteristics (3.3V)

Parameter	Condition	Notes	Min	Typ	Max	Unit
Transmit Power for 20MHz Bandwidth, compliant with IEEE mask and EVM	DSSS - 1 Mbps	EVM< -9 dB	-	16	-	dBm
	DSSS - 2 Mbps	EVM< -9 dB	-	16	-	dBm
	CCK- 5.5 Mbps	EVM< -9 dB	-	16	-	dBm
	CCK - 11 Mbps	EVM< -9 dB	-	16	-	dBm
	OFDM - 6 Mbps	EVM< -5 dB	-	16	-	dBm
	OFDM - 9 Mbps	EVM< -8 dB	-	16	-	dBm
	OFDM - 12 Mbps	EVM< -10 dB	-	16	-	dBm
	OFDM - 18 Mbps	EVM< -13 dB	-	16	-	dBm
	OFDM - 24 Mbps	EVM< -16 dB	-	16	-	dBm
	OFDM - 36 Mbps	EVM< -19 dB	-	16	-	dBm
	OFDM - 48 Mbps	EVM< -22 dB	-	15.5	-	dBm
	OFDM - 54 Mbps	EVM< -25 dB (see note section)	-	15	-	dBm
	MCS0 Mixed Mode	EVM< -5 dB	-	16	-	dBm
	MCS1 Mixed Mode	EVM< -10 dB	-	16	-	dBm
	MCS2 Mixed Mode	EVM< -13 dB	-	16	-	dBm
	MCS3 Mixed Mode	EVM< -16 dB	-	16	-	dBm
	MCS4 Mixed Mode	EVM< -19 dB	-	16	-	dBm
	MCS5 Mixed Mode	EVM< -22 dB	-	15.5	-	dBm
	MCS6 Mixed Mode	EVM< -25 dB (see note section)	-	15	-	dBm
	MCS7 Mixed Mode	(see note section)	-	11.5	-	dBm

Parameter	Condition	Notes	Min	Typ	Max	Unit
Transmitter Emissions (6 Mbps @ Maximum Power)	776-794 MHz	CDMA2000	-	-151	-	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	-	-143	-	dBm/Hz
	1450–1495 MHz	DAB	-	-149	-	dBm/Hz
	1570–1580 MHz	GPS	-	-147	-	dBm/Hz
	1592–1610 MHz	GLONASS	-	-133	-	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	-	-145	-	dBm/Hz
	1805–1880 MHz	GSM 1800	-	-141	-	dBm/Hz
	1850–1910 MHz	GSM 1900	-	-140	-	dBm/Hz
	1910–1930 MHz	TDSCDMA,LTE	-	-137	-	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne,WCDMA	-	-132	-	dBm/Hz
	2010–2075 MHz	TDSCDMA	-	-125	-	dBm/Hz
	2110–2170 MHz	WCDMA	-	-123	-	dBm/Hz
	2305–2370 MHz	LTE Band 40	-	-104	-	dBm/Hz
	2370–2400 MHz	LTE Band 40	-	-103	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-110	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-109	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-115	-	dBm/Hz
	5000–5900 MHz	WLAN 5G	-	-136	-	dBm/Hz
Harmonic and Spurious Emissions (1 Mbps @ Maximum Power)	3.2 GHz	VCO	-	-35	-	dBm/MHz
	4.8-5.0 GHz	2nd Harmonic	-	-46	-	dBm/MHz
	7.2-7.5 GHz	3rd Harmonic	-	-60	-	dBm/MHz

Note:

1. There is a variation of up to 2 dB in power across channels.
2. To meet FCC emission limits, the TX power of band edge channels (1 and 11) are being reduced up to 6 dB in higher data rates.
3. Across the temperature range of -40 °C to +85 °C, no perceivable degradation in output power at -40 °C and by up to 4 dB at +85 °C for WLAN 11b.
4. Across the temperature range of -40 °C to +85 °C, the output power may degrade by up to 1.5 dB at -40 °C and by up to 3 dB at +85 °C for WLAN 11g/n.
5. There may be a reduction in EVM of up to 1 dB in 54 Mbps data rate, and 2 dB in MCS6 data rate.
6. EVM for MCS7 data rate may not meet IEEE spec of -27 dB.
7. IEEE spectral mask limits may be crossed in lower data rates in some channels, and if required power may be backed off by 1-2 dB.

1.7.2 WLAN 2.4 GHz Receiver Characteristics on High-Performance (HP) Mode

TA = 25°C. Parameters are measured at antenna port on channel 1(2412 MHz)

- All WLAN receiver sensitivity numbers and adjacent channel numbers are at < 10% PER limit. Packet sizes are 1024 bytes for 802.11 b/g data rates and 4096 bytes for 802.11 n data rates.
- For WLAN ACI cases, the desired signal power is 3 dB above standard defined sensitivity level.

Table 1.19. WLAN 2.4 GHz Receiver Characteristics on HP Mode

Parameter	Condition/Notes	Min	Typ	Max	Unit
Sensitivity for 20MHz Bandwidth(1)	1 Mbps DSSS	-	-94.5	-	dBm
	2 Mbps DSSS	-	-89.6	-	dBm
	5.5 Mbps CCK	-	-88	-	dBm
	11 Mbps CCK	-	-85.5	-	dBm
	6 Mbps OFDM	-	-90	-	dBm
	9 Mbps OFDM	-	-88.7	-	dBm
	12 Mbps OFDM	-	-88.4	-	dBm
	18 Mbps OFDM	-	-86.2	-	dBm
	24 Mbps OFDM	-	-83.4	-	dBm
	36 Mbps OFDM	-	-79.7	-	dBm
	48 Mbps OFDM	-	-75.6	-	dBm
	54 Mbps OFDM	-	-73.8	-	dBm
	MCS0 Mixed Mode	-	-88.7	-	dBm
	MCS1 Mixed Mode	-	-86.5	-	dBm
	MCS2 Mixed Mode	-	-84.2	-	dBm
	MCS3 Mixed Mode	-	-81.5	-	dBm
	MCS4 Mixed Mode	-	-77.7	-	dBm
	MCS5 Mixed Mode	-	-73.5	-	dBm
	MCS6 Mixed Mode	-	-71.5	-	dBm
	MCS7 Mixed Mode	-	-69.5	-	dBm
Maximum Input Level for PER below 10%	802.11 b	-	5	-	dBm
	802.11g	-	-9	-	dBm
	802.11n	-	-11	-	dBm
RSSI Accuracy Range		-3	-	3	dB

Parameter	Condition/Notes	Min	Typ	Max	Unit
Blocking level for 3 dB RX Sensitivity Degradation(Data rate 6Mbps OFDM, Desired signal at -79dBm)	776–794 MHz	-	-3	-	dBm
	824–849 MHz	-	-3	-	dBm
	880–915 MHz	-	-3	-	dBm
	1710–1785 MHz	-	-17	-	dBm
	1850–1910 MHz	-	-18	-	dBm
	1920–1980 MHz	-	-18	-	dBm
	2300–2400 MHz	-	-58	-	dBm
	2570–2620 MHz	-	-21	-	dBm
	2545–2575 MHz	-	-20	-	dBm
Return Loss		-10	-	-	dB
Adjacent Channel Interference	1 Mbps DSSS	-	36	-	dB
	11 Mbps DSSS	-	37	-	dB
	6 Mbps OFDM	-	38	-	dB
	54 Mbps OFDM	-	22	-	dB
	MCS0 Mixed Mode	-	38	-	dB
	MCS7 Mixed Mode	-	20	-	dB
Alternate Adjacent Channel Interference	1 Mbps DSSS	-	44	-	dB
	11 Mbps DSSS	-	35	-	dB
	6 Mbps OFDM	-	46	-	dB
	54 Mbps OFDM	-	30	-	dB
	MCS0 Mixed Mode	-	46	-	dB
	MCS7 Mixed Mode	-	28	-	dB

Note:

1. Receiver sensitivity may be degraded by up to 6.5 dB for channels 5,6,7,8,13 & 14 due to the desensitization of the receiver by harmonics of the system clock (40 MHz).
2. Across the operating temperature range of -40 °C to +85 °C, the output power may improve by up to 1 dB at -40 °C and degrade by up to 1.5 dB at +85 °C.

1.7.3 WLAN 2.4 GHz Receiver Characteristics on Low-Power (LP) Mode

TA = 25°C. Parameters are measured at antenna port on channel 1(2412 MHz)

Table 1.20. WLAN 2.4 GHz Receiver Characteristics on LP Mode

Parameter	Condition/Notes	Min	Typ	Max	Unit
Sensitivity for 20MHz Band-width(1)	1 Mbps DSSS	-	-92.8	-	dBm
	2 Mbps DSSS	-	-87.4	-	dBm
	5.5 Mbps CCK	-	-85.7	-	dBm
	11 Mbps CCK	-	-82.7	-	dBm
	6 Mbps OFDM	-	-87.7	-	dBm
	9 Mbps OFDM	-	-86.8	-	dBm
	12 Mbps OFDM	-	-86.6	-	dBm
	18 Mbps OFDM	-	-83.9	-	dBm
	24 Mbps OFDM	-	-80.9	-	dBm
	36 Mbps OFDM	-	-76.1	-	dBm
	MCS0 Mixed Mode	-	-87.2	-	dBm
	MCS1 Mixed Mode	-	-84.7	-	dBm
	MCS2 Mixed Mode	-	-82	-	dBm
	MCS3 Mixed Mode	-	-79	-	dBm
	MCS4 Mixed Mode	-	-74.1	-	dBm
Maximum Input Level for PER below 10%	802.11 b	-	-12	-	dBm
	802.11g	-	-15	-	dBm
	802.11n	-	-15	-	dBm
RSSI Accuracy Range		-3	-	3	dB
Blocking level for 3 dB RX Sensitivity Degradation(Data rate 6Mbps OFDM, Desired signal at -79dBm)	776–794 MHz	-	-3.5	-	dBm
	824–849 MHz	-	-3.5	-	dBm
	880–915 MHz	-	-3.5	-	dBm
	1710–1785 MHz	-	-19	-	dBm
	1850–1910 MHz	-	-18	-	dBm
	1920–1980 MHz	-	-23	-	dBm
	2300–2400 MHz	-	-60	-	dBm
	2570–2620 MHz	-	-22	-	dBm
	2545–2575 MHz	-	-21	-	dBm
Return Loss		-10	-	-	dB

Parameter	Condition/Notes	Min	Typ	Max	Unit
Adjacent Channel Interference	1 Mbps DSSS	-	40	-	dB
	11 Mbps DSSS	-	36	-	dB
	6 Mbps OFDM	-	42	-	dB
	36 Mbps OFDM	-	30	-	dB
	MCS0 Mixed Mode	-	40	-	dB
	MCS4 Mixed Mode	-	30	-	dB
Alternate Adjacent Channel Interference	1 Mbps DSSS	-	50	-	dB
	11 Mbps DSSS	-	38	-	dB
	6 Mbps OFDM	-	48	-	dB
	36 Mbps OFDM	-	38	-	dB
	MCS0 Mixed Mode	-	48	-	dB
	MCS4 Mixed Mode	-	36	-	dB

Note:

1. Receiver sensitivity may be degraded by up to 6.5 dB for channels 5,6,7,8,13 & 14 due to the desensitization of the receiver by harmonics of the system clock (40 MHz).
2. Across the operating temperature range of -40 °C to +85 °C, the output power may improve by up to 1 dB at -40 °C and degrade by up to 1.5 dB at +85 °C.

1.7.4 Bluetooth Transmitter Characteristics on High-Performance (HP) Mode

1.7.4.1 Transmitter Characteristics with 3.3 V Supply

TA = 25°C, VBATT = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are measured at antenna port.(1)
- For Bluetooth C/I cases, the desired signal power is 3 dB above standard defined sensitivity level.

Table 1.21. Bluetooth Transmitter Characteristics on HP Mode 3.3 V

Parameter	Condition	Notes	Min	Typ	Max	Unit
Transmit Power	BR		-	12	-	dBm
	EDR 2Mbps		-	8	-	dBm
	EDR 3Mbps		-	5	-	dBm
	LE 1Mbps		-	14	-	dBm
	LE 2Mbps		-	13	-	dBm
	LR 500 Kbps		-	11	-	dBm
	LR 125 Kbps		-	11	-	dBm
Power Control Step	BR, EDR		-	3	-	dB
Adjacent Channel Power | M-N| = 2	BR		-	-	-20	dBm
	EDR		-	-	-20	dBm
	LE		-	-	-20	dBm
	LR		-	-	-20	dBm
Adjacent Channel Power | M-N| > 2	BR		-	-	-40	dBm
	EDR		-	-	-40	dBm
	LE		-	-	-30	dBm
	LR		-	-	-30	dBm
BR Modulation Characteristics	DH1		-25	-	25	kHz
	DH3		-40	-	40	kHz
	DH5		-40	-	40	kHz
	Drift Rate		-20	-	20	kHz/50 us
	Δf1 Avg		140	-	175	kHz
	Δf2 Max		115	-		kHz
EDR Modulation Characteristics	RMS DEVM, EDR2		-	15	-	%
	RMS DEVM, EDR3		-	5.5	-	%
	99% DEVM, EDR2		-	23	-	%
	99% DEVM, EDR3		-	9.5	-	%
	peak DEVM,EDR2		-	28	-	%
	peak DEVM,EDR3		-	13.5	-	%

Parameter	Condition	Notes	Min	Typ	Max	Unit
BLE Modulation Characteristics	Δf1 Avg		225	-	275	kHz
	Δf2 Max		185	-	-	kHz
	Δf2 Avg/Δf1 Avg		0.8	-	-	-
Transmitter Emissions (BR @Maximum output power)	776-794 MHz	CDMA2000	-	-160	-	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	-	-160	-	dBm/Hz
	1450–1495 MHz	DAB	-	-160	-	dBm/Hz
	1570–1580 MHz	GPS	-	-160	-	dBm/Hz
	1592–1610 MHz	GLONASS	-	-160	-	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	-	-115	-	dBm/Hz
	1805–1880 MHz	GSM 1800	-	-148	-	dBm/Hz
	1850–1910 MHz	GSM 1900	-	-148	-	dBm/Hz
	1910–1930 MHz	TDSCDMA,LTE	-	-136	-	dBm/Hz
	1930–1990 MHz	GSM1900,CDMAOne,WCDMA	-	-148	-	dBm/Hz
	2010–2075 MHz	TDSCDMA	-	-148	-	dBm/Hz
	2110–2170 MHz	WCDMA	-	-116	-	dBm/Hz
	2305–2370 MHz	LTE Band 40	-	-142	-	dBm/Hz
	2370–2400 MHz	LTE Band 40	-	-134	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-128	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-139	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-139	-	dBm/Hz
	5000–5900 MHz	WLAN 5G	-	-148	-	dBm/Hz

Note:

1. There is a variation of up to 2dB in power across channels.
2. Noise-floor is -160 dBm/Hz with spurious tone power of -66 dBm at 1601.33 MHz when transmitted signal is at 2402 MHz.
3. Across the temperature range of -40 °C to +85 °C, the output power may degrade by up to 2 dB at -40 °C and by up to 1.5 dB at +85 °C.

1.7.5 Bluetooth Transmitter Characteristics on Low-Power (LP) Mode

TA = 25°C. Parameters are measured at antenna port and applicable to VBATT=3.3V

- For Bluetooth C/I cases, the desired signal power is 3 dB above standard defined sensitivity level.

Table 1.22. Bluetooth Transmitter Characteristics on LP 0 dBm Mode

Parameter	Condition/Notes	Min	Typ	Max	Unit
Transmit Power	LE 1Mbps	-	-	-4.5	dBm
	LE 2Mbps	-	-	-4.5	dBm
	LR 500 Kbps	-	-	-4.5	dBm
	LR 125 kbps	-	-	-4.5	dBm
Adjacent Channel Power | M-N| = 2	LE	-	-	-20	dBm
	LR	-	-	-20	dBm
Adjacent Channel Power | M-N| > 2	LE	-	-	-30	dBm
	LR	-	-	-30	dBm
BR Modulation Characteristics	DH1	-25	-	25	kHz
	DH3	-40	-	40	kHz
	DH5	-40	-	40	kHz
	Drift Rate	-20	-	20	kHz
	Δf1 Avg	140	-	175	kHz
	Δf2 Max	115	-	-	kHz
BLE Modulation Characteristics	Δf1 Avg	225	-	275	kHz
	Δf2 Max	185	-	-	kHz
	Δf2 Avg/Δf1 Avg	0.8	-	-	-

Note:

1. There is a variation of up to 2dB in power across channels.
2. Noise-floor is -160 dBm/Hz with spurious tone power of -66 dBm at 1601.33 MHz when transmitted signal is at 2402 MHz.
3. Across the temperature range of -40 °C to +85 °C, the output power may degrade by up to 1 dB at -40 °C and by up to 1 dB at +85 °C.

1.7.6 Bluetooth Receiver Characteristics on High-Performance (HP) Mode

TA = 25°C. Parameters are measured at antenna port and applicable to VBATT=3.3V

Table 1.23. Bluetooth Receiver Characteristics on HP Mode

Parameter	Condition/Notes	Min	Typ	Max	Unit
Sensitivity,Dirty TX off[1],[2]	BR (1 Mbps), 339 bytes, DH5 Packet, BER= 0.1%	-	-90.6	-	dBm
	EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet, BER= 0.01%	-	-91.6	-	dBm
	EDR3 (3 Mbps), 1020 bytes, 3-DH5 Packet, BER= 0.01%	-	-84.4	-	dBm
	LE (1 Mbps), 37 bytes, PER=30.8%	-	-93.2	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-90.8	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-100.1	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-104	-	dBm
Maximum Input Level	BR, EDR2, EDR3,BER= 0.1%	-	-13	-	dBm
	LE 1Mbps, 2Mbps,PER=30.8%	-	10	-	dBm
	LR 500kps, 125kbps,PER=30.8%	-	10	-	dBm
C/I Performance	BR, co-channel, BER=0.1%	9	-	-	dB
	BR, adjacent +1/-1 MHz, BER=0.1%	-2	-	-	dB
	BR, adjacent +2/-2 MHz BER=0.1%	-19	-	-	dB
	BR, adjacent >=|±3| MHz BER=0.1%	-19	-	-	dB
	BR, Image channel BER=0.1%	-11	-	-	dB
	BR, adjacent to Image channel BER=0.1%	-22	-	-	dB
	EDR2, co-channel BER=0.1%	11	-	-	dB
	EDR2, adjacent +1/-1 MHz BER=0.1%	-2	-	-	dB
	EDR2, adjacent +2/-2 MHz BER=0.1%	-17	-	-	dB
	EDR2, adjacent >=|±3| MHz BER=0.1%	-17	-	-	dB
	EDR2, Image channel BER=0.1%	-9	-	-	dB
	EDR2, adjacent to Image channel BER=0.1%	-22	-	-	dB
	EDR3, co-channel BER=0.1%	19	-	-	dB
	EDR3, adjacent +1/- MHz BER=0.1%	3	-	-	dB
	EDR3, adjacent +2/-2 MHz BER=0.1%	-12	-	-	dB
	EDR3, adjacent >=|±3| MHz BER=0.1%	-12	-	-	dB
	EDR3, Image channel BER=0.1%	-2	-	-	dB
	EDR3, adjacent to Image channel BER=0.1%	-15	-	-	dB
	LE 1Mbps, co-channel PER=30.8%	-	11	-	dB

Parameter	Condition/Notes	Min	Typ	Max	Unit
C/I Performance	LE 1Mbps, adjacent +1 MHz PER=30.8%	-	4	-	dB
	LE 1Mbps, adjacent -1 MHz PER=30.8%	-	-5	-	dB
	LE 1Mbps, adjacent +2 MHz PER=30.8%	-	-21	-	dB
	LE 1Mbps, adjacent -2 MHz PER=30.8%	-	-28	-	dB
	LE 1Mbps, adjacent +3 MHz PER=30.8%	-	-21	-	dB
	LE 1Mbps, adjacent -3 MHz PER=30.8%	-	-31	-	dB
	LE 1Mbps, adjacent >= |±4| MHz PER=30.8%	-	-36	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-26	-	dB
	LE 1Mbps, +1MHz adjacent to Image channel PER=30.8%	-	-36	-	dB
	LE 1Mbps, -1MHz adjacent to Image channel PER=30.8%	-	-21	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	10	-	dB
	LE 2Mbps, adjacent +2 MHz PER=30.8%	-	-3	-	dB
	LE 2Mbps, adjacent -2 MHz PER=30.8%	-	-5	-	dB
	LE 2Mbps, adjacent +4 MHz PER=30.8%	-	-14	-	dB
	LE 2Mbps, adjacent -4 MHz PER=30.8%	-	-20	-	dB
	LE 1Mbps, adjacent >= |±6| MHz PER=30.8%	-	-34	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-14	-	dB
	LE 1Mbps, +2MHz adjacent to Image channel PER=30.8%	-	-26	-	dB
	LE 1Mbps, -2MHz adjacent to Image channel PER=30.8%	-	-3	-	dB

Note:

1. **BR, EDR**: Receiver sensitivity is degraded by up to 9 dB for channels 38,78 due to the desensitization of the receiver by harmonics of the system clock (40MHz).
2. **BLE, LR**: Receiver sensitivity is degraded by up to 11.5 dB for channels 19,29,30,39 due to the desensitization of the receiver by harmonics of the system clock (40MHz).
3. Across the operating temperature range of -40 °C to +85 °C, the output power may improve by up to 1.5 dB at -40 °C and degrade by up to 1.5 dB at +85 °C.

1.7.7 Bluetooth Receiver Characteristics on Low-Power (LP) Mode

TA = 25°C. Parameters are measured at antenna port and applicable to VBATT=3.3V

Table 1.24. Bluetooth Receiver Characteristics on LP Mode

Parameter	Condition/Notes	Min	Typ	Max	Unit
Sensitivity,Dirty TX off(1),(2)	BR (1 Mbps), 339 bytes, DH5 Packet BER= 0.1%	-	-87.2	-	dBm
	EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet, BER= 0.01%	-	-87.9	-	dBm
	LE (1 Mbps), 37 bytes, PER=30.8%	-	-91.3	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-89	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-98.1	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-102.1	-	dBm
Maximum Input Level	BR, EDR2 BER= 0.1%	-	-16	-	dBm
	LE 1Mbps, 2Mbps PER=30.8%	-	3	-	dBm
	LR 500kps, 125kbps PER=30.8%	-	10	-	dBm
BER Floor		-	1e-4	-	%

Parameter	Condition/Notes	Min	Typ	Max	Unit
C/I Performance	BR, co-channel BER= 0.1%	9	-	-	dB
	BR, adjacent +1/-1 MHz, BER=0.1%	-2	-	-	dB
	BR, adjacent +2/-2 MHz BER=0.1%	-19	-	-	dB
	BR, adjacent >=|±3| MHz BER=0.1%	-19	-	-	dB
	BR, Image channel BER=0.1%	-11	-	-	dB
	BR, adjacent to Image channel BER=0.1%	-22	-	-	dB
	EDR2, co-channel BER=0.1%	11	-	-	dB
	EDR2, adjacent +1/-1 MHz BER=0.1%	-2	-	-	dB
	EDR2, adjacent +2/-2 MHz BER=0.1%	-17	-	-	dB
	EDR2, adjacent >=|±3| MHz BER=0.1%	-17	-	-	dB
	EDR2, Image channel BER=0.1%	-9	-	-	dB
	EDR2, adjacent to Image channel BER=0.1%	-22	-	-	dB
	LE 1Mbps, co-channel PER=30.8%	-	11	-	dB
	LE 1Mbps, adjacent +1 MHz PER=30.8%	-	5	-	dB
	LE 1Mbps, adjacent -1 MHz PER=30.8%	-	-4	-	dB
	LE 1Mbps, adjacent +2 MHz PER=30.8%	-	-21	-	dB
	LE 1Mbps, adjacent -2 MHz PER=30.8%	-	-28	-	dB
	LE 1Mbps, adjacent +3 MHz PER=30.8%	-	-22	-	dB
	LE 1Mbps, adjacent -3 MHz PER=30.8%	-	-29	-	dB
	LE 1Mbps, adjacent >= |±4| MHz PER=30.8%	-	-36	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-29	-	dB
	LE 1Mbps, +1MHz adjacent to Image channel PER=30.8%	-	-35	-	dB
	LE 1Mbps, -1MHz adjacent to Image channel PER=30.8%	-	-22	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	9	-	dB
	LE 2Mbps, adjacent +2 MHz PER=30.8%	-	-4	-	dB
	LE 2Mbps, adjacent -2 MHz PER=30.8%	-	-4	-	dB
	LE 2Mbps, adjacent +4 MHz PER=30.8%	-	-13	-	dB
	LE 2Mbps, adjacent -4 MHz PER=30.8%	-	-20	-	dB
	LE 2Mbps, adjacent >= |±6| MHz PER=30.8%	-	-35	-	dB
	LE 2Mbps, Image channel PER=30.8%	-	-13	-	dB
	LE 2Mbps, 2MHz adjacent to Image channel PER=30.8%	-	-25	-	dB
	LE 2Mbps, -2MHz adjacent to Image channel PER=30.8%	-	-4	-	dB

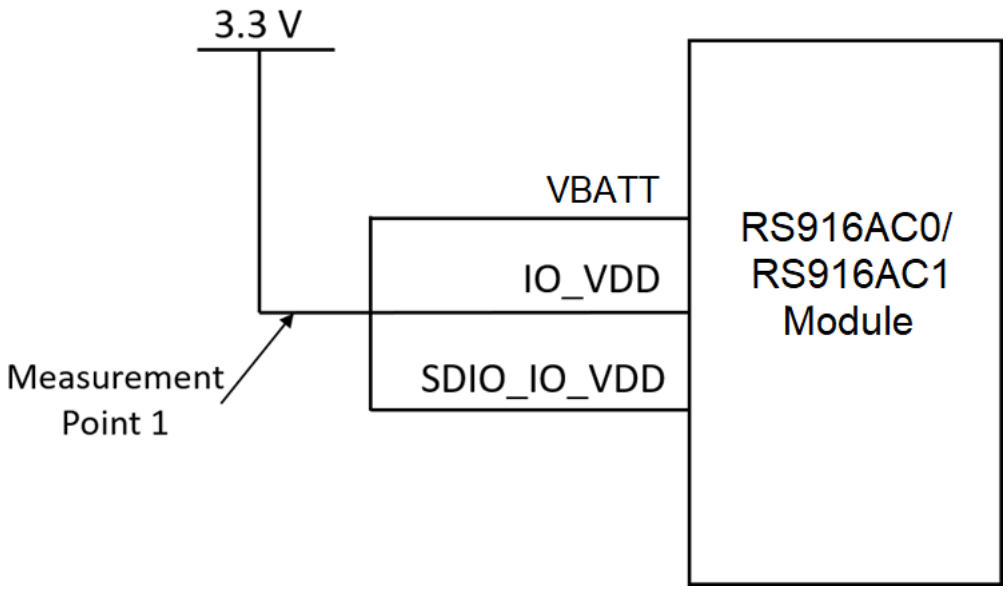
Note:

1. **BR, EDR**: Receiver sensitivity is degraded by up to 9 dB for channels 38,78 due to the desensitization of the receiver by harmonics of the system clock (40MHz).
2. **BLE, LR**: Receiver sensitivity is degraded by up to 11.5 dB for channels 19,29,30,39 due to the desensitization of the receiver by harmonics of the system clock (40MHz).
3. Across the operating temperature range of -40 °C to +85 °C, the output power may improve by up to 1.5 dB at -40 °C and degrade by up to 1.5 dB at +85 °C.

1.8 Typical Current Consumption

PLEASE NOTE THAT THE FOLLOWING NUMBERS ARE PRELIMINARY AND ARE NOT THE FINAL VALUES. EXTENSIVE CHARACTERIZATION FOR THE MODULES ARE UNDERWAY. THERE WILL BE SLIGHT VARIATIONS IN THE FINAL VALUES.

1.8.1 3.3. V



1.8.1.1 WLAN

Parameter	Description	Min	Unit
1 Mbps Listen	LP Mode	13.82	mA
1 Mbps RX Active	LP Mode	19.67	mA
6 Mbps RX Active	HP Mode	48.2	mA
72 Mbps RX Active	HP Mode	48.2	mA
11 Mbps TX Active	Tx Power = Maximum (16dBm)	270	mA
	Tx Power = 8dBm	130	mA
6 Mbps TX Active	Tx Power = Maximum (16dBm)	285	mA
	Tx Power = 8dBm	130	mA
54 Mbps TX Active	Tx Power = Maximum (15dBm)	200	mA
	Tx Power = 8dBm	130	mA
72 Mbps TX Active	Tx Power = Maximum (12dBm)	180	mA
	Tx Power = 8dBm	130	mA
Deep Sleep	GPIO Wake up	6.2	uA
Standby	State retained	13.1	uA
Standby Associated, DTIM = 1		293	uA
Standby Associated, DTIM = 3		119	uA
Standby Associated, DTIM = 10		61	uA

1.8.1.2 Bluetooth BR and EDR

Parameter	Description	Min	Unit
TX Active Current, 1 Mbps BR	LP Mode, Tx Power = -2 dBm HP Mode, Tx Power = Maximum (12 dBm)	9.9 130	mA mA
RX Active Current, 1 Mbps BR	LP Mode HP Mode	10.2 26.7	mA mA
TX Active Current, 2 Mbps EDR	HP Mode, Tx Power = Maximum (8 dBm)	130	mA
RX Active Current, 2 Mbps EDR	LP Mode HP Mode	10.2 26.7	mA mA
TX Active Current, 3 Mbps EDR	HP Mode, Tx Power = Maximum (5 dBm)	140	mA
RX Active Current, 3 Mbps EDR	HP Mode	26.7	mA
Deep Sleep	GPIO Wake up	0.9	uA
Standby	State RAM retained	13.1	uA
Inquiry Scan	Scan Interval = 1.28 s Scan Window = 128 ms	2.7	mA
Page Scan	Scan Interval = 1.28 s Scan Window = 128 ms	2.7	mA
Inquiry and Page Scan	Inquiry/Page Scan Interval = 1.28 s Scan Window = 128 ms	5.4	mA

1.8.1.3 Bluetooth LE

Parameter	Description	Min	Unit
TX Active Current	LP Mode, Tx Power = -2 dBm	8.9	mA
	LP Mode, Tx Power = 2 dBm	-	mA
	HP Mode, Tx Power = Maximum (14 dBm)	190	mA
RX Active Current	LP Mode	10.9	mA
	HP Mode	26.7	mA
Deep Sleep	GPIO Wakeup	0.9	uA
Standby	State retained	13.1	uA
Advertising, Unconnectable	Advertising on all 3 channels Advertising Interval = 1.28s Tx Power = 0 dBm, LP Mode	35	uA
Advertising, Connectable	Advertising on all 3 channels Advertising Interval = 1.28s Tx Power = 0 dBm, LP Mode	35	uA
Connected	Connection Interval = 1.28s No Data Tx Power = 0 dBm, LP Mode	35	uA
Connected	Connection Interval = 200ms No Data Tx Power = 0 dBm, LP Mode	106	uA
Scanning	Scan Interval = 1.28s Scan Window = 11.25ms LP Mode	54.5	uA

2. RS916AC0 and RS916AC1 Module Detailed Description

2.1 Overview

RS916AC0 and RS916AC1 modules are based on Silicon Labs' RS9116 ultra-low-power, single spatial stream, 802.11n + BT/BLE5.0 Convergence SoC. The RS916AC0 and RS916AC1 module provides low-cost CMOS integration of a multi-threaded MAC processor (ThreadArch®), baseband digital signal processing, analog front-end, crystal oscillator, calibration eFuse, 2.4GHz RF transceiver, integrated power amplifier, match, bandpass filters(BPF), and Quad-SPI Flash thus providing a fully-integrated solution for a range of hosted and embedded wireless applications. With Silicon Labs' embedded four-threaded processor and on-chip ROM and RAM, these chipsets enable integration into low-cost and zero host load applications. With an integrated PMU and support for a variety of digital peripherals, RS916AC0 and RS916AC1 modules enable very low-cost implementations for wireless hosted and embedded applications. It can be connected to a host processor through SDIO, SPI or UART interfaces. Wireless firmware upgrades and provisioning are supported.

2.2 Module Features

2.2.1 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n with single band support
- Support for 20 MHz channel bandwidth
- Transmit power up to +16 dBm with integrated PA
- Receive sensitivity as low as -94.5 dBm
- Data Rates: 802.11b: Up to 11 Mbps; 802.11g: Up to 54 Mbps; 802.11n: MCS0 to MCS7
- Operating Frequency Range: from 2412 MHz up to 2462 MHz (default, for US and Canada) or 2472 MHz (for other countries, as applicable)

2.2.1.1 MAC

- Conforms to IEEE 802.11b/g/n standards for MAC
- Dynamic selection of fragment threshold, data rate, and antenna depending on the channel statistics
- Hardware accelerators for WEP 64/128-bit and AES
- WPA, WPA2, and WMM support
- AMPDU and AMSDU aggregation for high performance
- Firmware downloaded from host based on application
- Hardware accelerators for DH (for WPS)

2.2.1.2 Baseband Processing

- Supports DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates (6, 9, 12, 18, 24, 36, 48, 54 Mbps, MCS0 to MCS7), and Short GI in Hosted mode
- Supports IEEE 802.11n single-stream modes with data rates up to 72.2 Mbps
- Supports long, short, and HT preamble modes
- High-performance multipath compensation in OFDM, DSSS, and CCK modes

2.2.2 Bluetooth

- Transmit power up to +14 dBm with integrated PA
- Receive sensitivity:- LE: -93 dBm, LR 125 Kbps: -104 dBm
- Compliant to dual-mode Bluetooth 5
- <8 mA transmit current in Bluetooth 5 mode, 2 Mbps data rate
- Data rates: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps, 3 Mbps
- Operating Frequency Range: 2.402 GHz - 2.480 GHz
- Bluetooth 2.1 + EDR, Bluetooth Low Energy 4.0 / 4.1 / 4.2 / 5.0
- Bluetooth Low Energy 1 Mbps, 2 Mbps and Long Range modes
- Bluetooth Low Energy Secure connections
- Bluetooth Low Energy supports central role and peripheral role concurrently
- Bluetooth auto rate and auto TX power adaptation
- Scatternet[1] with two Secondary roles while still being visible

Note:

1. For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

2.2.2.1 MAC

2.2.2.1.1 Link Manager

- Creation, modification & release of logical links
- Connection establishment between Link managers of two Bluetooth devices
- Link supervision is implemented in Link Manager
- Link power control is done depending on the inputs from Link Controller
- Enabling & disabling of encryption & decryption on logical links
- Services the data transport requests from L2CAP and provides required QOS
- Support for security using ECDH hardware accelerator

2.2.2.1.2 Link Controller

- Encodes and decodes header of BT packets
- Manages flow control, acknowledgment, retransmission requests, etc.
- Stores the last packet status for all logical transports
- Chooses between SCO & ACL buffers depending on the control information coming from BBP resource manager
- Indicates the success status of packet transmission to upper layers
- Indicates the link quality to the LMP layer

2.2.2.1.3 Host Controller

- Receives & decodes commands received from the Bluetooth Host
- Propagates the decoded commands to respective modules
- Responsible for transmitting and receiving packets from and to Host
- Formats the responses coming from other modules of Bluetooth Controller as events and sends them to the Host

2.2.2.1.4 Device Manager

- Controls Scan & Connection processes
- Controls all BT Device operations except data transport operations
- Storing link keys
- BT Controller state transition management
- Slot synchronization & management
- Access contract management
- Scheduler

2.2.2.2 Baseband Processing

- Supports GFSK (1 Mbps), EDR-DQPSK, EDR-D8PSK
- Supports BLE and Bluetooth long range
- Supports Data rates up to 3 Mbps

2.2.3 RF Transceiver

- Integrated 2.4 GHz transceiver with highly programmable operating modes
- Internal oscillator with 40 MHz crystal
- Built-in automatic boot up and periodic calibration enables ease of integration

2.2.4 Host Interfaces

- SDIO
  - Version 2.0-compatible
  - Supports SD-SPI, 1-bit, and 4-bit SDIO modes
  - Operation up to a maximum clock speed of 50 MHz
- SPI Interface
  - Operation up to a maximum clock speed of 100 MHz
- UART
  - Supports variable baud rates between 9600 and 3686400 bps
  - AT command interface for configuration and data transmission/reception

Note: Embedded Mode (WiSeConnect) supports SDIO, SPI and UART.

2.2.4.1 Auto Host Detection

The RS916AC0 and RS916AC1 modules detect the host interface automatically after connecting to respective host controllers like SDIO, SPI and UART. SDIO/SPI host interface is detected through the hardware packet exchanges. UART host interface is detected through the software based-on the received packets on the UART interface. This Host configuration is stored in always-on domain registers after detection (on power up) and reused this information at each wakeup.

2.2.5 Wireless Coexistence Manager

- Arbitration between Wi-Fi, Bluetooth, and Bluetooth Low Energy
- Application aware arbitration
- Adaptive frequency hopping (AFH) in Bluetooth is based on WLAN channel usage
- Pre inter thread interrupts generation for radio switching
- QoS assurance across different traffics

2.2.6 Software

The RS916AC0 and RS916AC1 software package supports 802.11 b/g/n Client, Access Point (Up to 16 clients), Concurrent Client and Access Point mode, Enterprise Security, dual-mode BT 5.0 functionality on a variety of host platforms and operating systems. The software package includes complete firmware, reference drivers, application profiles. The Wi-Fi driver has support for a simultaneous access point, and client mode. It has a wireless coexistence manager to arbitrate between protocols.

The RS916AC0 and RS916AC1 software package is available in the following flavors:

- **Embedded mode (WiSeConnect™):** Wi-Fi stack, TCP/IP stack, IP modules, Bluetooth stack and some profiles reside in the RS916AC0 and RS916AC1; some of the Bluetooth profiles reside in the host processor
- **Hosted mode (n-Link™):** Wi-Fi stack, Bluetooth stack and profiles and all network stacks reside on the host processor

Note: Please refer to the Software Manuals (TRM and PRM) in RS9116 Document Library for more details.

2.2.6.1 Embedded Mode (WiSeConnect™)

- Available host interface: SDIO, UART and SPI
- Support for Embedded Client mode, Access Point mode (Up to 4 clients), Concurrent Client and Access Point mode, and Enterprise Security
- Supports advanced security features: WPA/WPA2-Personal and Enterprise
- Integrated TCP/IP stack, HTTP/HTTPS, SSL/TLS, MQTT
- Bluetooth inbuilt stack support for L2CAP, RFCOMM, SDP, SPP, GAP
- Bluetooth profile support for GAP, SDP, SPP, GATT, L2CAP, RFCOMM
- Wireless firmware update and provisioning
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

Note: For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

2.2.6.2 Hosted Mode (n-Link™)

- Available host interfaces: SDIO 2.0
- Application data throughput up to 50 Mbps (Hosted Mode) in 802.11n with 20MHz bandwidth.
- Host drivers for Linux
- Support for Client mode, Access point mode (Up to 16 clients), Concurrent Client and Access Point mode, Enterprise Security
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

Note: For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

2.2.7 Security

The RS916AC0 and RS916AC1 modules support multiple levels of security capabilities available for the development of IoT devices.

- Accelerators: AES128/256 in Embedded Mode
- WPA/WPA2/WPA3-Personal, WPA/WPA2 Enterprise for Client

Note: For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

2.2.8 Power Management

The RS9116 chipsets have an internal power management subsystem, including DC-DC converters and linear regulators. This subsystem generates all the voltages required by the chipset to operate from a wide variety of input sources.

- LDO SOC - Linear regulator for digital blocks
  - Input - 1.4V from LC DC-DC or external regulated supply on pin VINLDOSOC. VINLDOSOC is an internal pin that is not terminated on the package, and it is not accessible.
  - Output - VOUTLDOSOC_1V1. It is not intended to power external circuitry.
- LDO FLASH - Linear regulator for internal and external Flash
  - Input - Wide input voltage range (1.85 to 3.6V) on pin VINLDO1P8. VINLDO1P8 is an internal pin that is not terminated on the package, and it is not accessible.
  - Output - 1.8V and 20mA maximum load on pin 1V8_LDO_OUT

2.2.8.1 Output Voltage Ranges

Table 2.1. Min and Max Specifications of Various Output Voltages

Pin Description	Supply Voltage (V)	
	Min	Max
VOUTLDOSOC_1V1	1.05	1.2
1V8_LDO_OUT	1.75	2.0
Note: The output voltages from the IC/module will be reflected as per specifications only after the firmware is loaded.		

2.2.9 Low Power Modes

The RS916AC0 and RS916AC1 Connectivity module supports Ultra-low power consumption with multiple power modes to reduce the system energy consumption.

- Dynamic Voltage and Frequency Scaling
- Low Power (LP) mode with only the host interface active
- Deep sleep (ULP) mode with only the sleep timer active – with and without RAM retention
- Wi-Fi standby associated mode with automatic periodic wake-up
- Automatic clock gating of the unused blocks or transit the system from Normal to LP or ULP modes

2.2.9.1 ULP Mode

In Ultra Low Power mode, the deep sleep manager has control over the other subsystems and processors and controls their active and sleep states. During deep sleep, the always-on logic domain operates on a lowered supply and a 32 kHz low-frequency clock to reduce power consumption. The ULP mode supports the following wake-up options:

- Timeout wakeup – Exit sleep state after programmed timeout value
- GPIO Based Wakeup: Exit sleep state when GPIO goes High/Low based on programmed polarity
- Analog Comparator Based wakeup – Exit sleep state on an event at the analog comparator
- RTC Timer wakeup – Exit Sleep state on timeout of RTC timer
- WatchDog Interrupt based wakeup - Exit Sleep state upon watchdog interrupt timeout

2.2.9.2 LP Mode

In Low Power mode, Network processor maintains system state and gate all internal high frequency clocks. But host interface is ready to accept any command from host controller.

The LP mode supports the following wake-up options:

- Host Request – Exit sleep state on a command from HOST controller. Whenever a command from the host is received, the processor serves the request with minimum latency and the clock is gated immediately after the completion of the operation to reduce power consumption.
- GPIO based wakeup - Wakeup can be initiated through a GPIO pin
- Timeout wakeup – Exit sleep state after the programmed timeout value

2.2.10 Memory

2.2.10.1 On-Chip Memory

The ThreadArch® processor has the following memory:

- On-chip SRAM for the wireless stack
- 512 Kbytes of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks, and security functions
- 16 Kbytes of Instruction cache enabling eXecute In Place (XIP) with quad SPI flash memory
- eFuse of 512 bytes (used to store primary boot configuration, security and calibration parameters)

3. RS916AC0 and RS916AC1 Module Reference Schematics, BOM, and Layout Guidelines

Note:

1. Customers should include provision for programming or updating the firmware at manufacturing.
2. If using UART, we recommend bringing out the SPI lines to test points, so designers could use the faster interface for programming the firmware as needed.
3. If using SPI as host interface, then firmware programming or update can be done through the host MCU, or if designer prefers to program standalone at manufacturing, then it is recommended to have test points on the SPI signals.
4. VBATT, SDIO_IO_VDD, IO_VDD must be powered using External/On-board Power.
5. FLASH_IO_VDD is powered by 1V8_LDO_OUT output.
6. If SDIO/SPI/UART interface is not used, then their respective IO domains must still be connected to the power supply.
7. Place all the Caps closer to the corresponding Module pins.

3.1 RS916AC0 Schematics

3.1.1 SDIO/SPI/UART

3.1.1.1 Schematics

The diagram below shows the typical schematic with SDIO/SPI/UART Host Interface and Internal Flash.

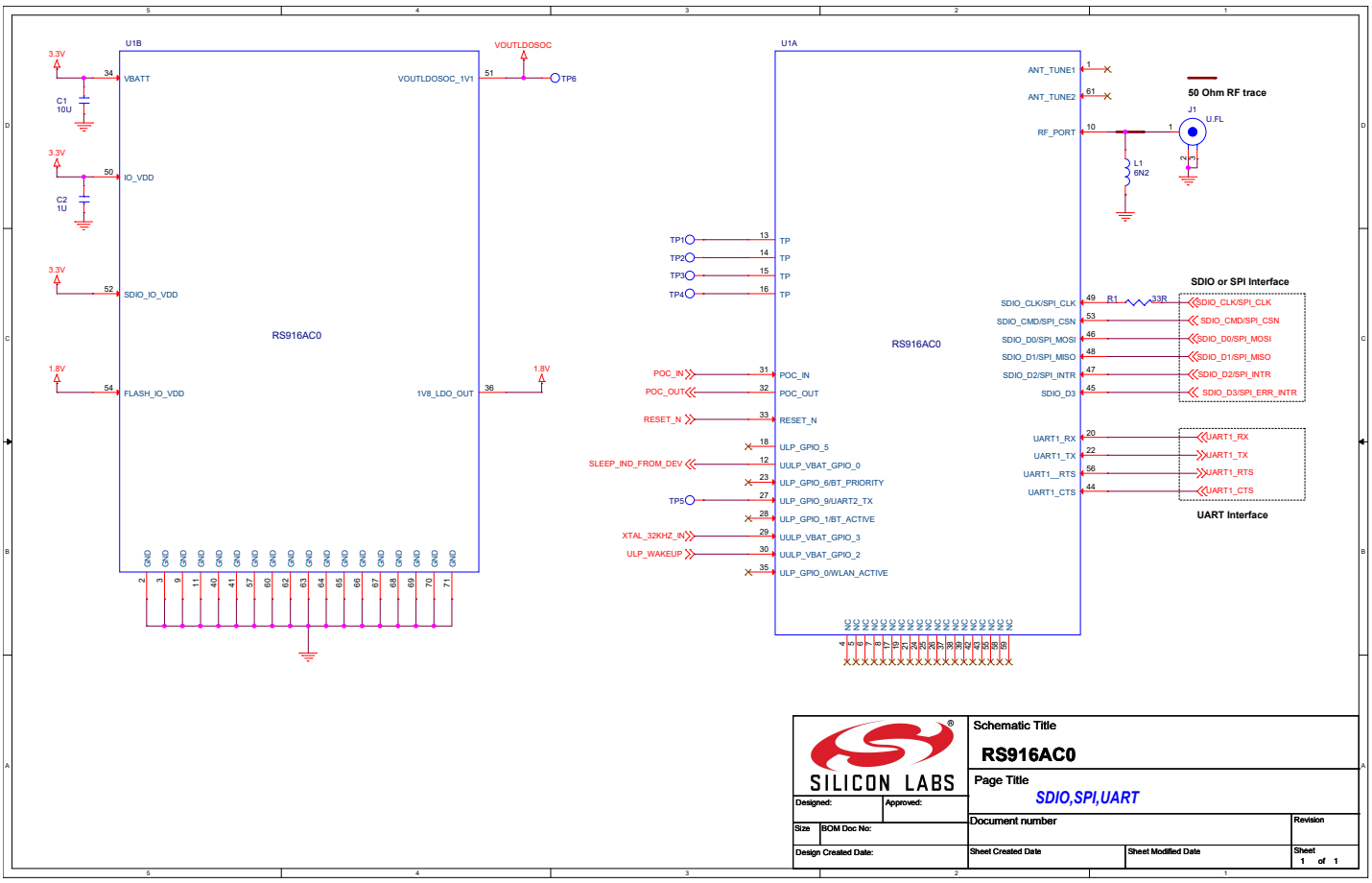


Figure 3.1. Schematics with SDIO/SPI/UART Host Interface

Note:

1. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Specifications section.
2. SDIO_IO_VDD can be driven by a different source irrespective of other sources to support different interfaces.
3. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification, version 2.0.
4. In SPI mode, ensure that the input signals, SPI_CS and SPI_CLK are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset. SPI_INTR is the interrupt signal driven by the Secondary device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required. The following action can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.
   - To use the signal in the Active-high or Active-low mode, ensure that, during the power up of the device, the Interrupt is disabled in the Host processor before deasserting the reset. After deasserting the reset, the Interrupt needs to be enabled only after the SPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.
   - The Host processor needs to be disable the interrupt before the ULP Sleep mode is entered and enable it after SPI interface is reinitialized upon wakeup from ULP Sleep.
5. In UART mode, ensure that the input signals, UART_RX and UART_CTS are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset.
6. Resistor “R1” should not be populated if UART is used as Host Interface.
7. Resistor "R1" should be placed close to the source of SDIO_CLK/SPI_CLK clock signal.
8. Table 1.5 holds the mandatory voltage range that the host system is meant to supply to the module, for the appropriate performance and also for the compliance with the radio regulatory rules. Failure to fulfill this design requirement would cause a deviation from the manufacturer's integration guidance, which would prevent among others the module's FCC/ISED IDs to be used, and would make the OEM liable.

3.1.1.2 Bill of Materials

Table 3.1. Bill of Materials with SDIO/SPI/UART Host Interface

S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
1	1	C1	10U	CAP CER 10UF 10V X7R 0805	0805	Murata	GRM21BR71A106KA73L
2	1	C2	1U	CAP CER 1UF 10V X7S 0402	0402	Murata	GCM155C71A105KE38
3	1	L1	6N2	6.2 nH Unshielded Thick Film Inductor 300 mA 600mOhm Max 0201	0201	Murata	LQP03TN6N2H02D
4	1	R1	33R	RES SMD 33 OHM 1% 1/16W 0402	0402	Yageo	RC0402FR-0733RL
5	1	J1		CONN U.FL RCPT STR 50 OHM SMD	SMD	Hirose	U.FL-R-SMT-1
6	1	U1		RS916AC0 and RS916AC1 module	LGA	Silicon Labs	RS916AC0

3.2 RS916AC1 Schematics

3.2.1 SDIO/SPI/UART

3.2.1.1 Schematics

The diagram below shows the typical schematic with SDIO/SPI/UART Host Interface and Internal Flash.

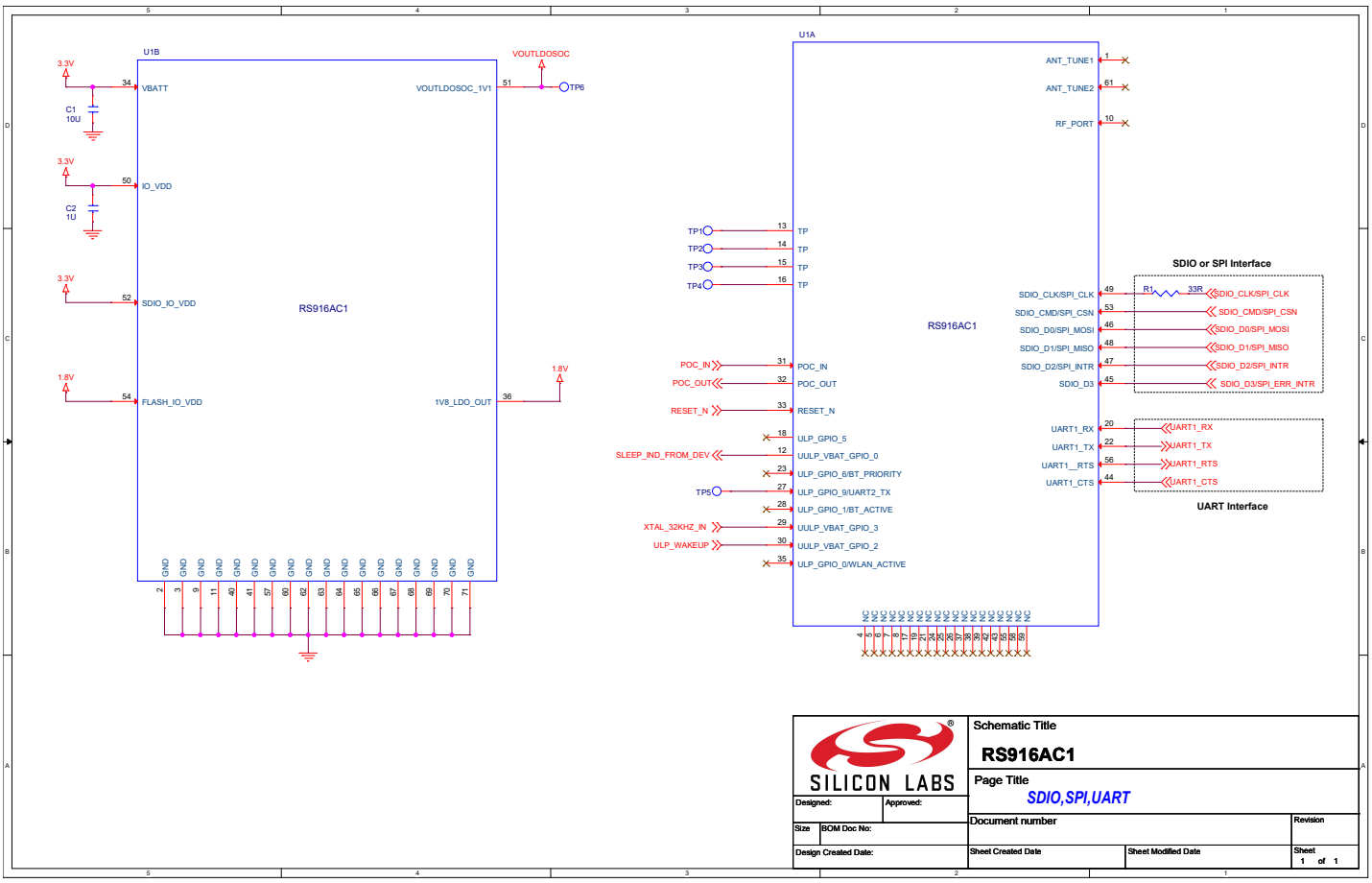


Figure 3.2. Schematics with SDIO/SPI/UART Host Interface

Note:

1. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Specifications section.
2. SDIO_IO_VDD can be driven by a different source irrespective of other sources to support different interfaces.
3. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification, version 2.0.
4. In SPI mode, ensure that the input signals, SPI_CS and SPI_CLK are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset. SPI_INTR is the interrupt signal driven by the Secondary device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required. The following action can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.
   - To use the signal in the Active-high or Active-low mode, ensure that, during the power up of the device, the Interrupt is disabled in the Host processor before deasserting the reset. After deasserting the reset, the Interrupt needs to be enabled only after the SPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.
   - The Host processor needs to be disable the interrupt before the ULP Sleep mode is entered and enable it after SPI interface is reinitialized upon wakeup from ULP Sleep.
5. In UART mode, ensure that the input signals, UART_RX and UART_CTS are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset.
6. Resistor “R1” should not be populated if UART is used as Host Interface.
7. Resistor "R1" should be placed close to the source of SDIO_CLK/SPI_CLK clock signal.
8. Table 1.5 holds the mandatory voltage range that the host system is meant to supply to the module, for the appropriate performance and also for the compliance with the radio regulatory rules. Failure to fulfill this design requirement would cause a deviation from the manufacturer's integration guidance, which would prevent among others the module's FCC/ISED IDs to be used, and would make the OEM liable.

3.2.1.2 Bill of Materials

Table 3.2. Bill of Materials with SDIO/SPI/UART Host Interface

S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
1	1	C1	10U	CAP CER 10UF 10V X7R 0805	0805	Murata	GRM21BR71A106KA73L
2	1	C2	1U	CAP CER 1UF 10V X7S 0402	0402	Murata	GCM155C71A105KE38
3	1	R1	33R	RES SMD 33 OHM 1% 1/16W 0402	0402	Yageo	RC0402FR-0733RL
4	1	U1		RS916AC0 and RS916AC1 module	LGA	Silicon Labs	RS916AC1

3.3 Layout Guidelines

1. The following Supply Pins needs to be STAR routed from the Supply Source
   - VBATT
   - IO_VDD
   - SDIO_IO_VDD
2. The RF_PORT Pin (No. 10) may be directly connected to an on-board chip antenna or terminated in an RF connector of any form factor for enabling the use of external antennas with the RS916AC0 variant. RF_PORT can be left floating when not used, like in the case of the RS916AC1 variant.
3. Antenna clearance area is not necessary if you are using an external antenna attached to the RF_PORT.
4. There need to be DC blocking capacitor (8.2pF) on RF_PORT if it is connected to an Antenna.
5. The RF trace on RF_PORT should have a characteristic impedance of 50 Ohms. Any standard 50 Ohms RF trace (Microstrip or Coplanar wave guide) may be used. The width of the 50 Ohms line depends on the PCB stack, e.g., the dielectric of the PCB, thickness of the copper, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.
6. To evaluate transmit and receive performance like Tx Power and EVM, Rx sensitivity and the like, an RF connector would be required. A suggestion is to place a ‘microwave coaxial connector with switch’ between RF_PORT and the antenna.
7. Each GND pin must have a separate GND via. Place the ground vias as close to the ground pads as possible.
8. All decoupling capacitors placement must be as much close as possible to the corresponding power pins, and the trace lengths as short as possible.
9. Ensure all power supply traces widths are sufficient enough to carry corresponding currents.
10. Add GND copper pour underneath the module in all layers, for better thermal dissipation.

3.3.1 Installation Guide for RS916AC0 Module

Figure 3.3 on page 55 below shows the recommended layout for RS916AC0 when using an u.fl connector for an external antenna. A 6.2nH shunt inductor is placed next to the module RF pad. The short RF trace from the RF pad of the module to the pad of the u.fl connector must be 50 ohm and exactly the same width as the RF pad of the module, i.e., 700 um. Figure 3.4 on page 55 and Figure 3.5 on page 56 show two examples on practical implementations of such a trace. The widths S is fixed to 700 um. The height h depends on the PCB stack-up, and the gap width W is adjusted until the impedance of the trace is exactly 50 ohm. Online calculators for coplanar waveguide with ground can be used to calculate the width W for any specific PCB stack-up. The integrator must use a unique connector, such as a “reverse polarity SMA” or “reverse thread SMA”, if detachable antenna is offered with the host chassis. This is especially required for the FCC and ISED approvals to remain valid, and any other kind of direct connector to the antenna might require a permissive change.

Ground vias underneath the module must be used extensively especially around the rectangular GND pins to enable heat transfer from the bottom of the module to the GND plane of the host board. Routing signal lines elsewhere underneath the module is acceptable.

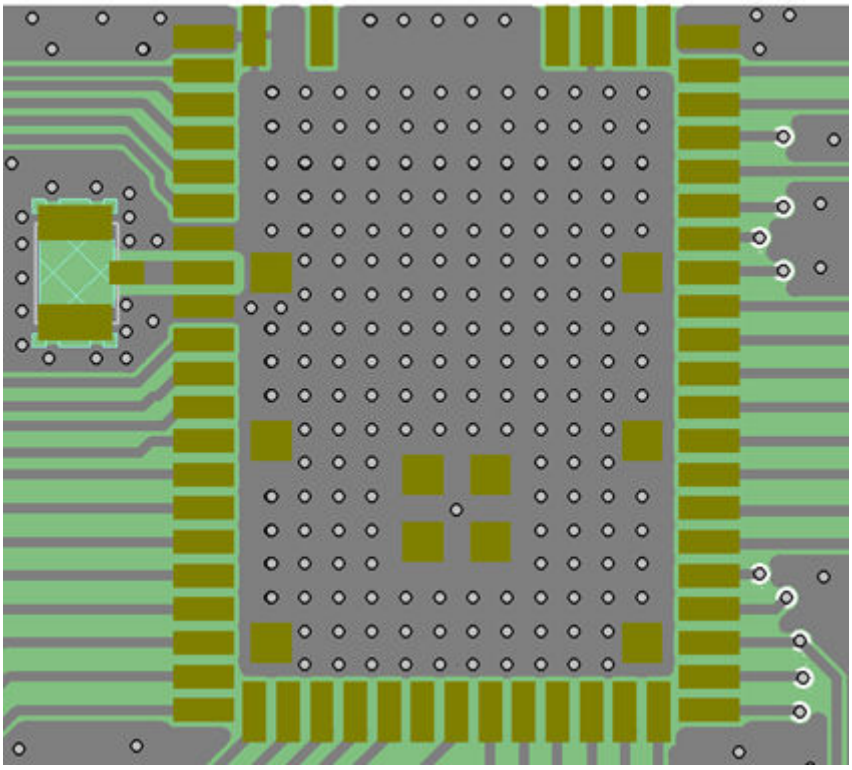


Figure 3.3. RS916AC0 Top Layer Application Layer with u.fl Connector

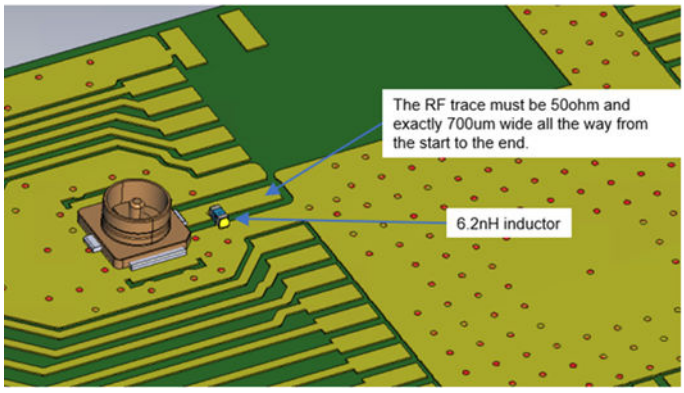


Figure 3.4. Layout for the RS916AC0 with an u.fl connector

The typical permittivity of PCB laminate is 4.6. If assuming permittivity of 4.6, in the example shown in Figure 3.5 on page 56 the dimensions would be:

S = 700 um

h = 420 um

W = 0.332 um

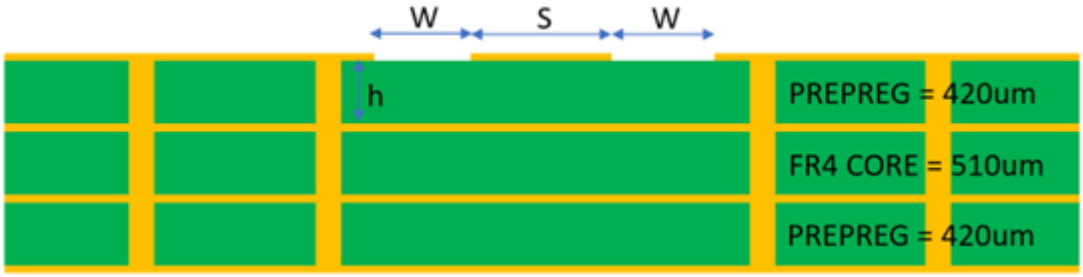


Figure 3.5. Example Implementation of a Co-planar Wave Guide with Ground and Thick Prepeg

Similarly, if assuming permittivity of 4.6, in the example shown in Figure 3.5 on page 56 the dimensions would be:

S = 700 um

h = 730 um

W = 132 um

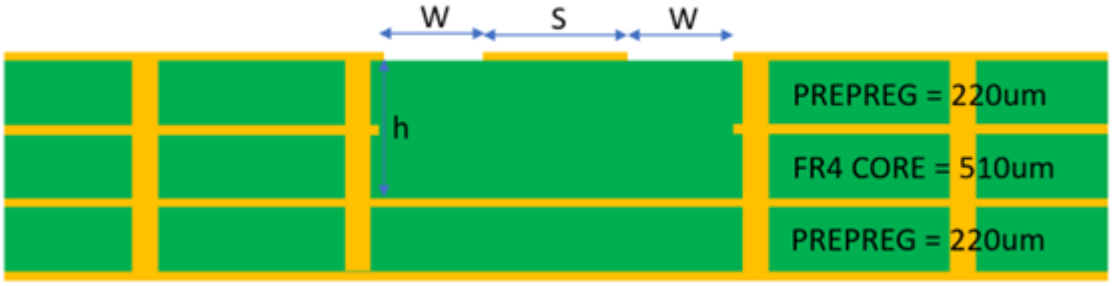
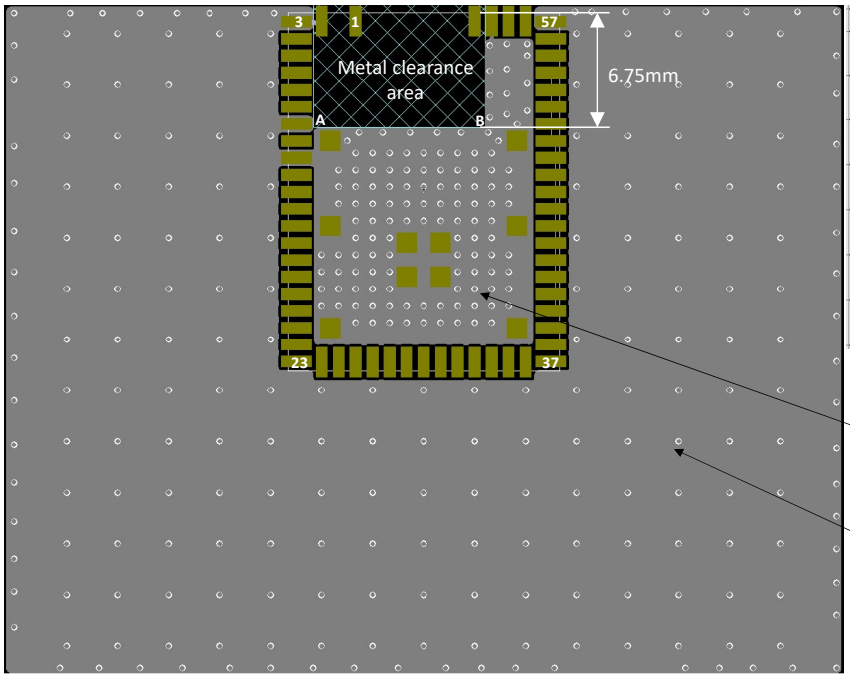


Figure 3.6. Example Implementation of a Co-planar Wave Guide with Ground and Thin Prepeg

3.3.2 Installation Guide for RS916AC1 Module



	X-cordinate (mm)	Y-cordinate (mm)
A (Corner of the metal clearance)	-6.5	3.8
B (Corner of the metal clearance)	3.6	3.8
1 (Center point of PAD1)	-4	10.05
3 (Center point of PAD3)	-7.5	10
23 (Center point of PAD23)	-7.5	-10
37 (Center point of PAD37)	7.5	-10
57 (Center point of PAD 57)	7.5	10

Figure 3.7. Application Layout of RS916AC1

For optimal performance of the RS916AC1:

- Place the module aligned to the edge of the application PCB, as illustrated in Figure 3.7 on page 57.
- Leave the antenna clearance area void of any traces, components, or copper on all layers of the application PCB.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Avoid plastic or any other dielectric material in direct contact with the antenna.

Figure 3.8 Figure on page 58 shows example layout scenarios which will lead to degraded performance and possible EMC issues with the module.

Ground vias underneath the module must be used extensively especially around the rectangular GND pins to enable heat transfer from the bottom of the module to the GND plane of the host board. Routing signal lines elsewhere underneath the module is acceptable.

Antennas are by nature affected by the surrounding PCB design and in particular the size and shape of the ground surrounding the antenna. The wide band antenna of RS916AC1 is designed to operate in various size/shape application boards and the antenna is not sensitive to dielectric material near the antenna. However, in certain extreme circumstances, such as extremely small board or narrow board, the antenna can be detuned enough to have an impact to the range, EVM characteristics and in-band emissions. In such cases it is possible to fine tune the antenna by using one or two external capacitors or inductors connected between the ANT_TUNE1 and GND and/or ANT_TUNE2 and GND. An example is shown in the Figure 3.9 Figure on page 58. Finding the correct value for these components requires empirical testing and measuring the antenna return loss.

The best antenna performance is achieved when the board width is 50mm and the antenna is placed at the center of the board edge. Having wider or narrower PCB will have up to 25% impact to the range. If the board is narrower than 35mm it is possible that external fine tuning becomes necessary to maintain the EVM performance.

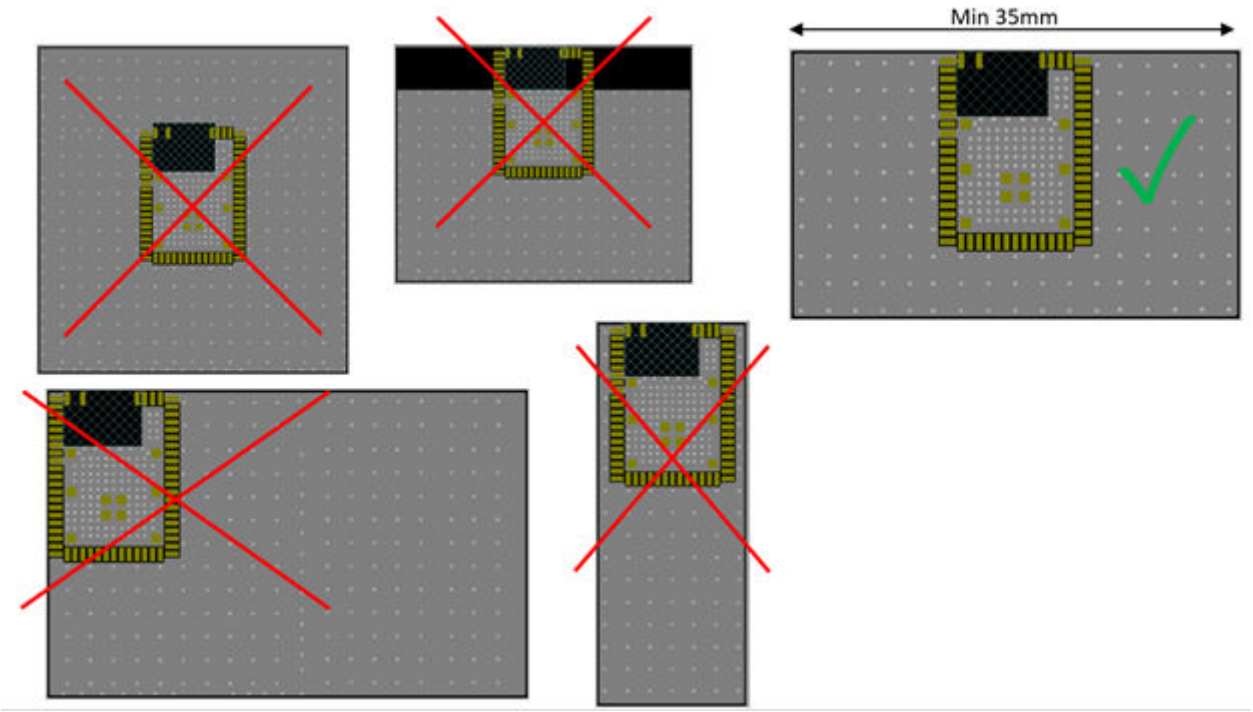


Figure 3.8. Layout Examples

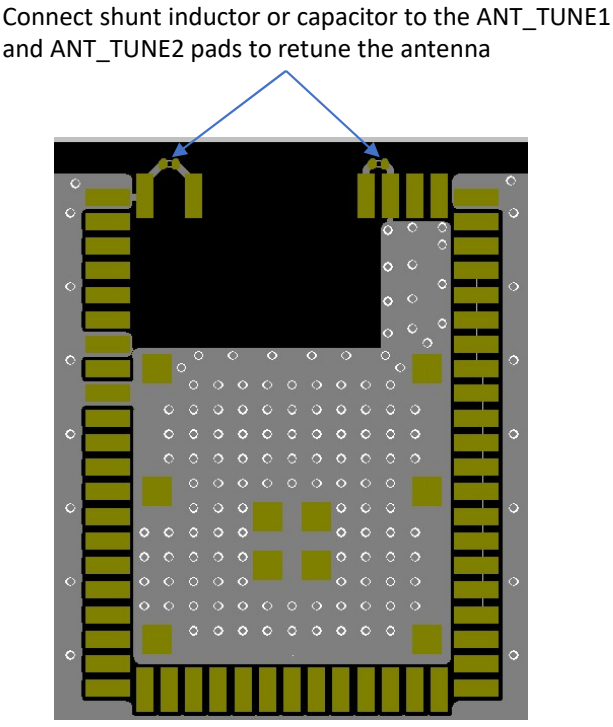


Figure 3.9. External Antenna Fine Tuning Option

3.4 RS916AC1 Antenna Radiation and Efficiency

Typical radiation patterns for the built-in antenna under optimal operating conditions are plotted in the figures that follow.

Table 3.3. Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1 dB	Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna. Refer to 3.3.2 Installation Guide for RS916AC1 Module for recommendations to archieve optimal antenna performance.
Peak gain	1.66 dBi	

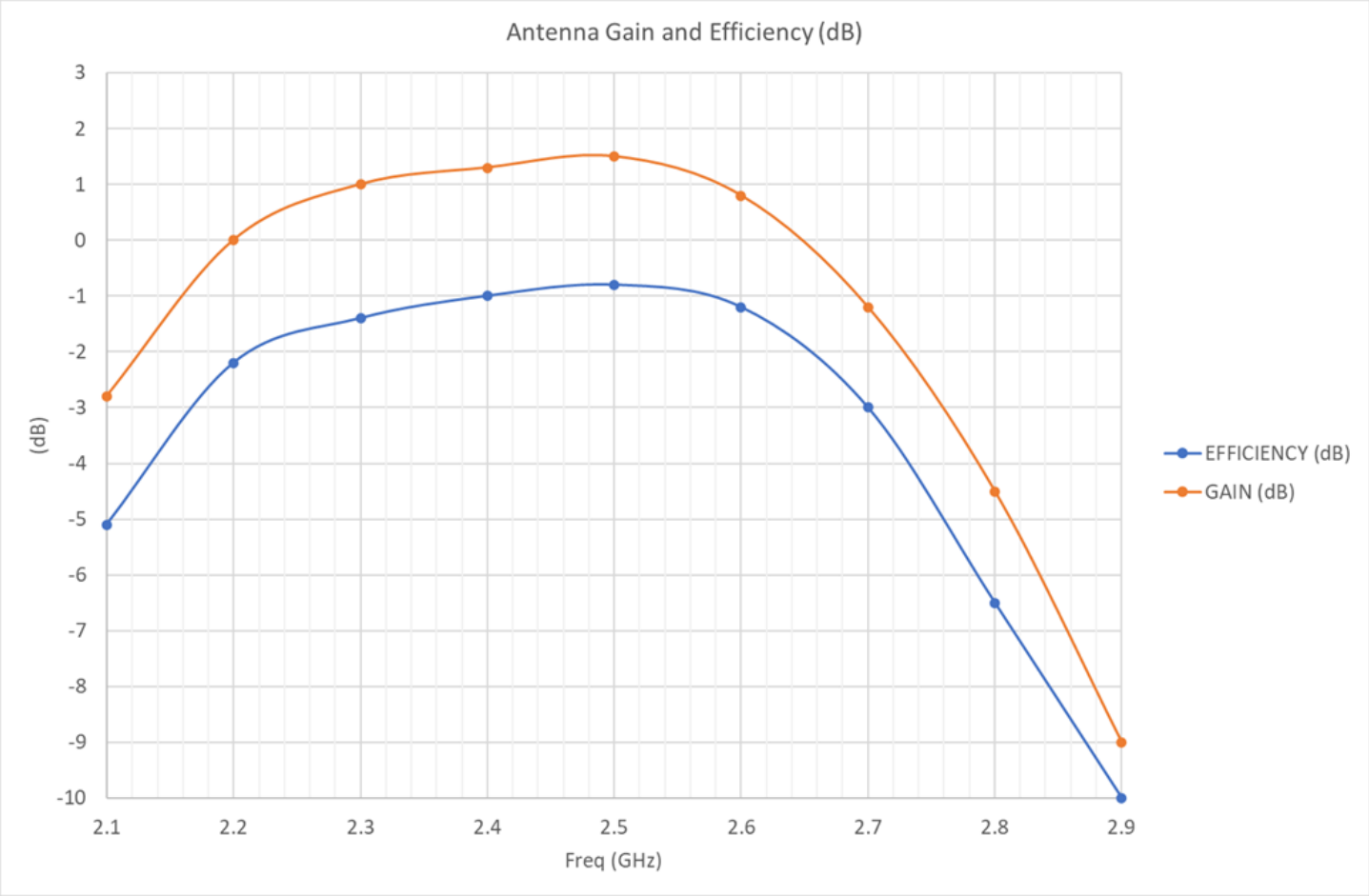


Figure 3.10. Efficiency and Gain of the Built-in Antenna

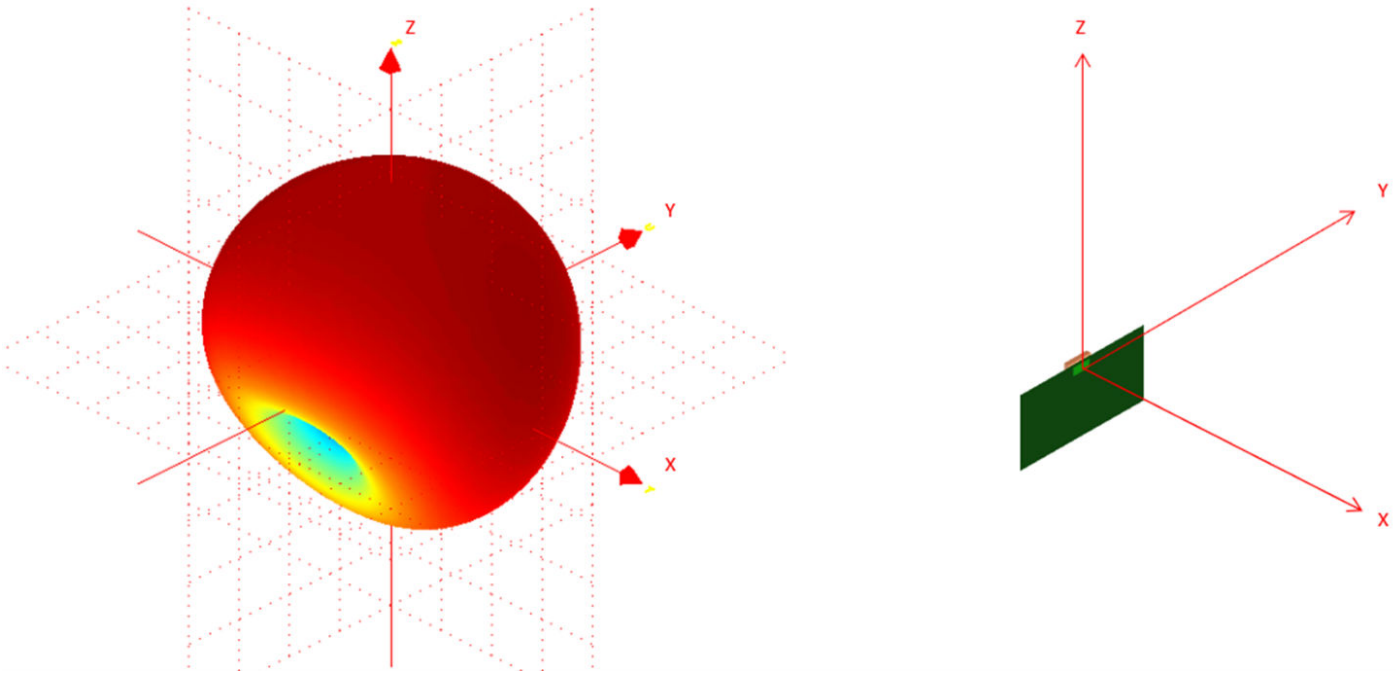


Figure 3.11. 3D Radiation Pattern of the Build-In Antenna

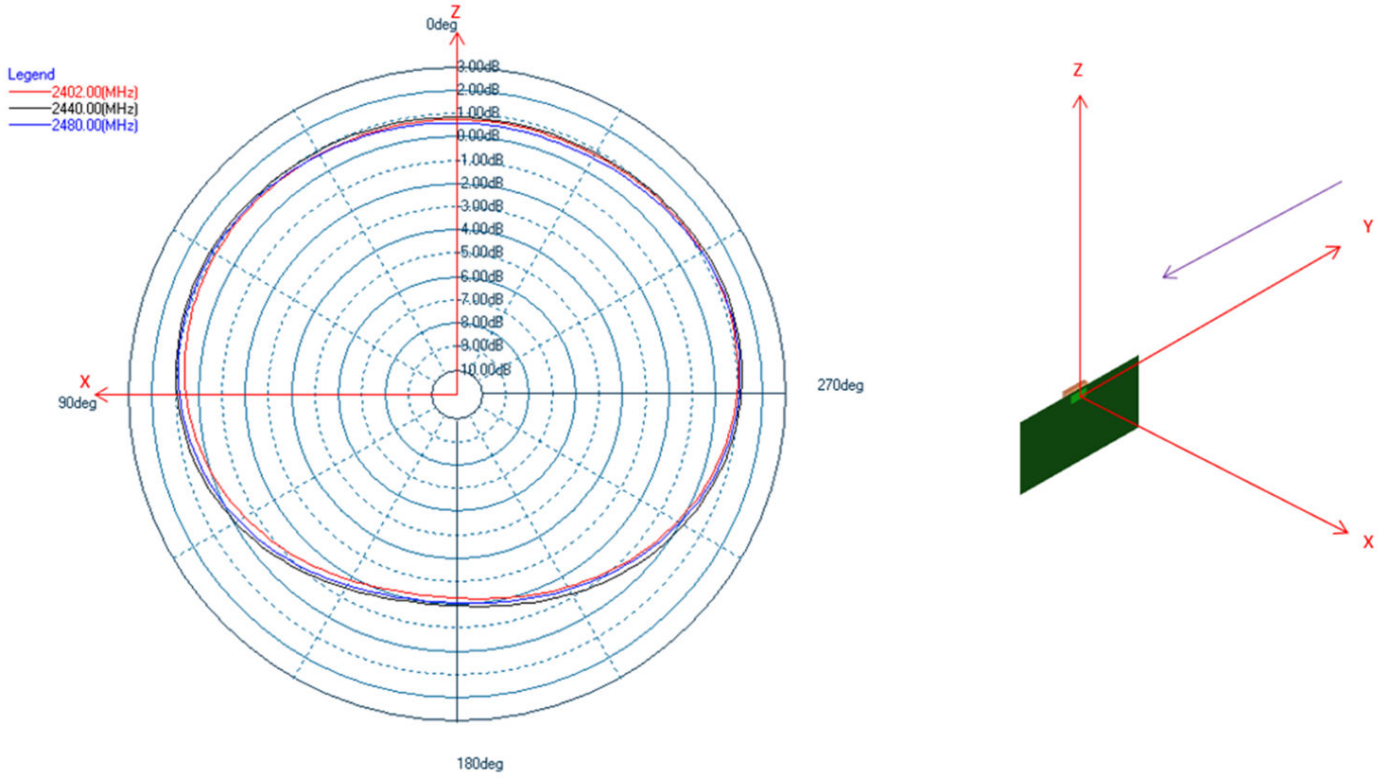


Figure 3.12. Typical 2D Antenna Radiation Patterns - Phi 0^{o} (Side View) Gain (dBi)

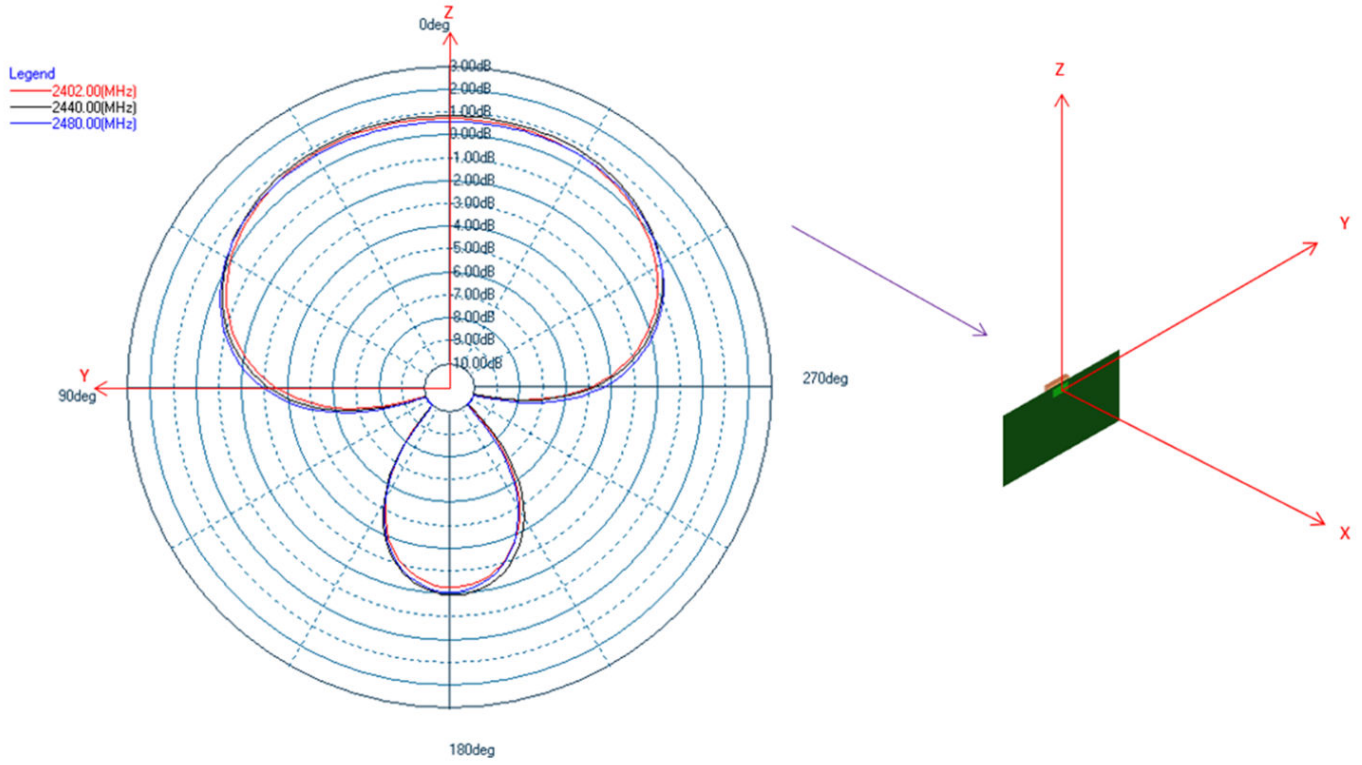


Figure 3.13. Typical 2D Antenna Radiation Patterns - Phi 90^{O} (Top View) Gain (dBi)

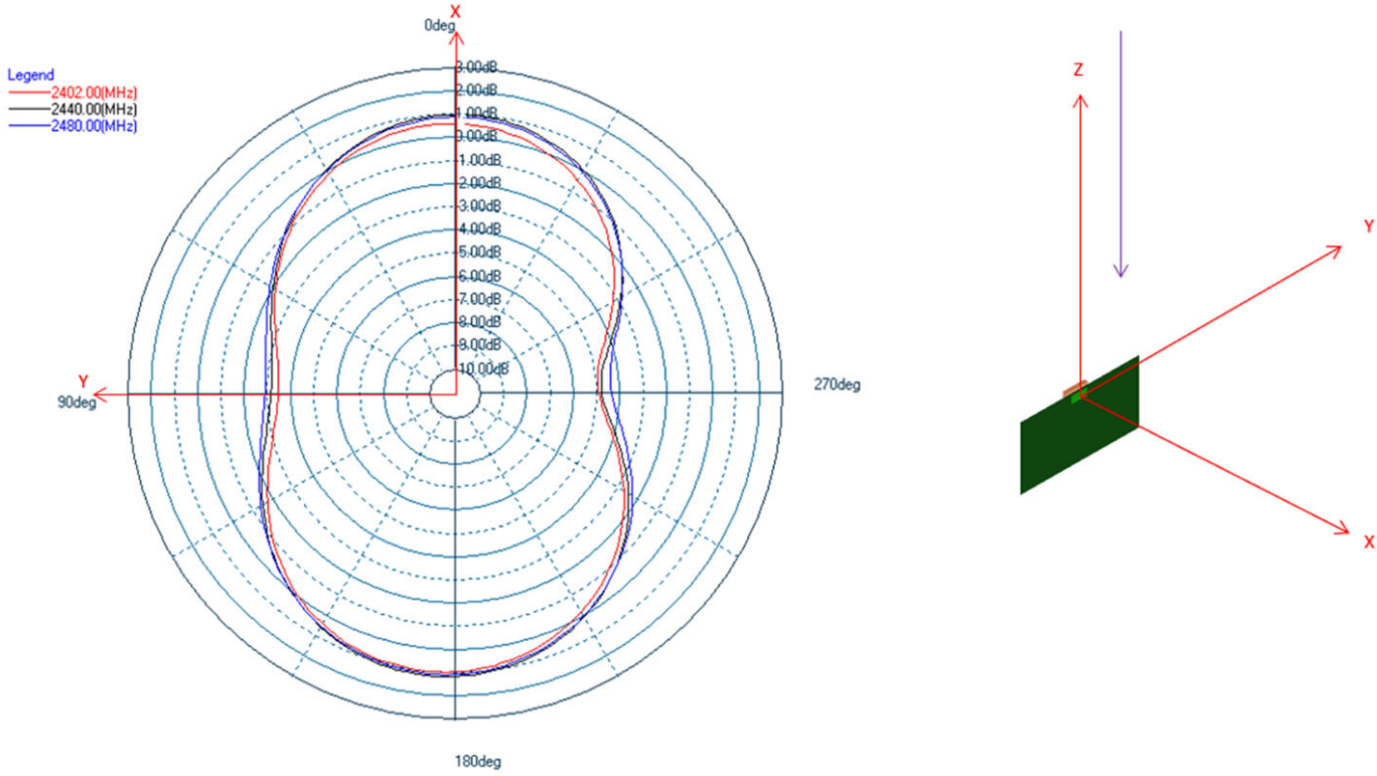


Figure 3.14. Typical 2D Antenna Radiation Patterns - Theta 90^{O} (Front View) Gain (dBi)

3.4.1 Proximity to Other Materials

Avoid placing plastic or any other dielectric material in close proximity to the antenna. Conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region, but this will also negatively impact antenna efficiency and reduce range.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

3.4.2 Proximity to Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

4. RS916AC0 and RS916AC1 Module Package Description

4.1 Dimensions

Table 4.1. Module Dimensions

Parameter	Value (LxWxH)	Units
Module Dimensions	21.10 x 16 x 2.32	mm
Tolerance	±0.2	mm

4.2 Package Outline

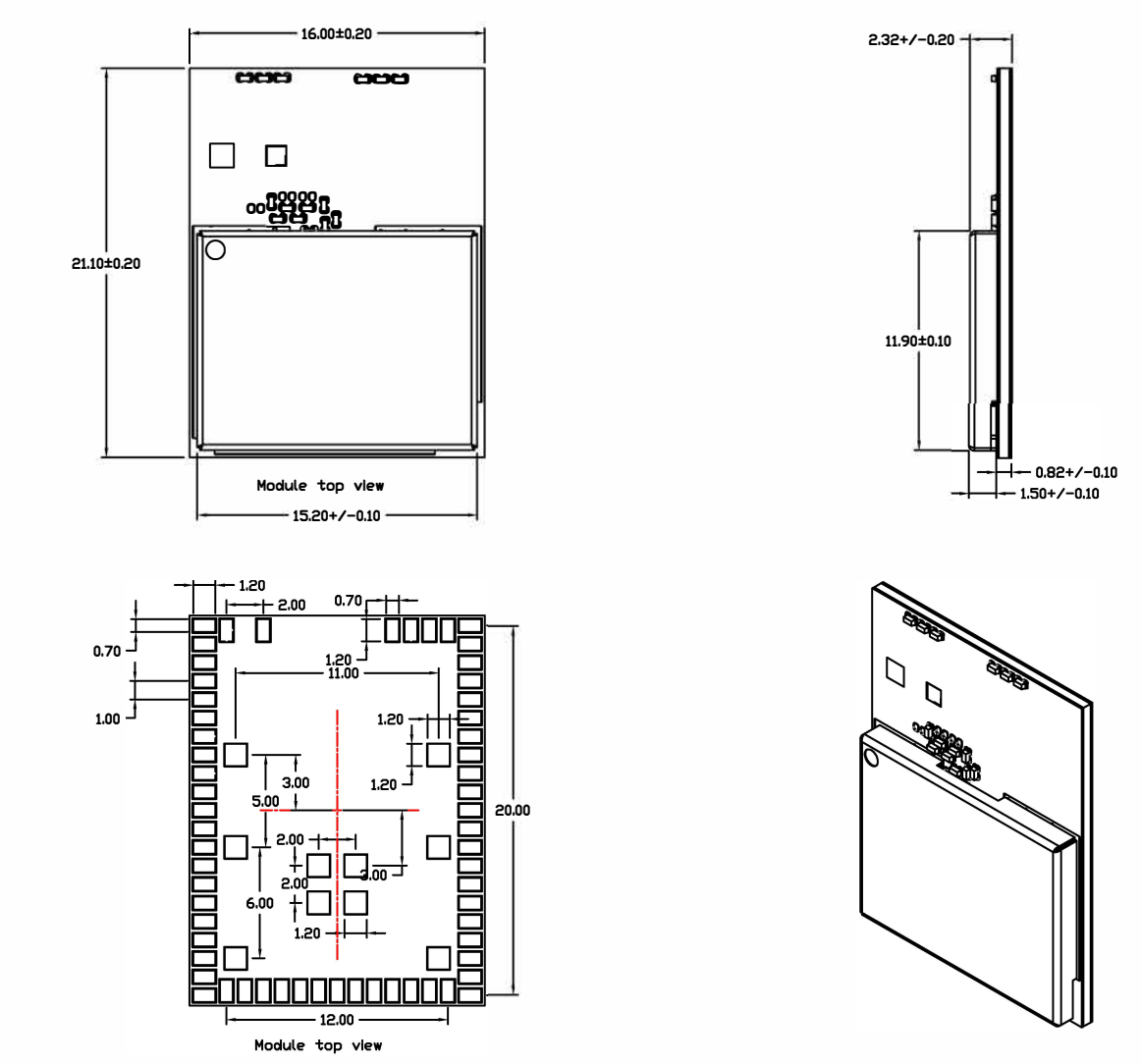


Figure 4.1. Package Outline

4.2.1 Pin Locations

Note: All coordinates in the table below are in millimeters, and in TOP VIEW.

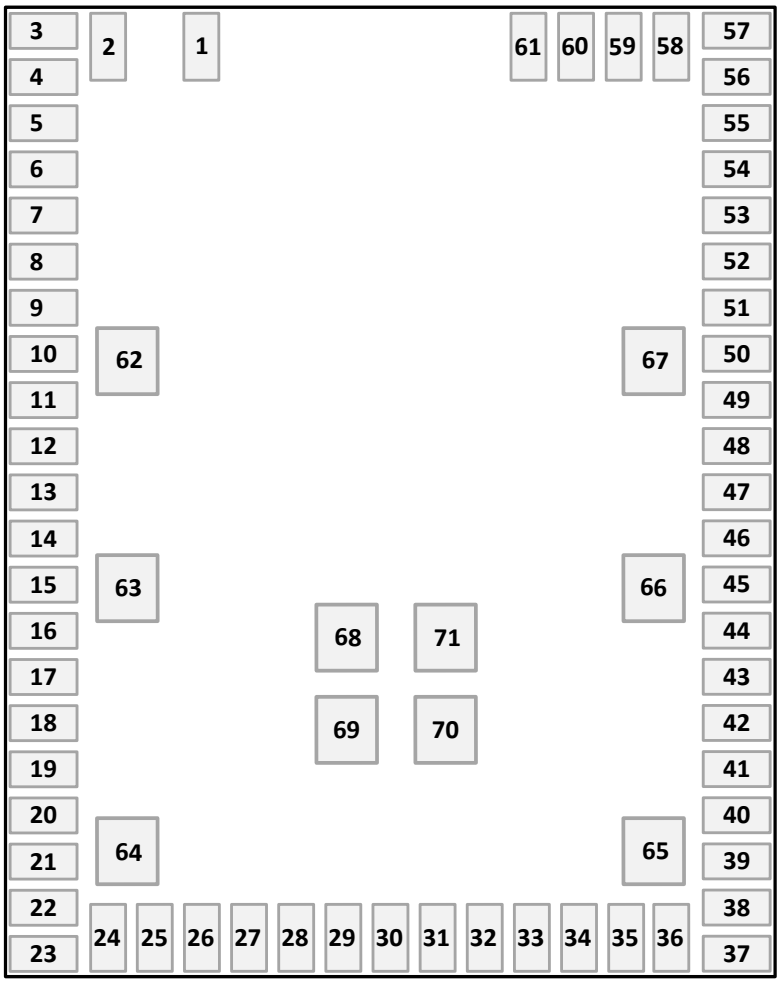


Figure 4.2. Pin Numbering

Table 4.2. Pin Locations

PAD X-Y Coordinates			
Pad #	**X**	**Y**	**Pad Size**
1	-4	9.75	(1.2 x 0.7) mm
2	-6	9.75	
3	-7.2	10	
23	-7.2	-10	
24	-6	-9.75	
36	6	-9.75	
37	7.2	-10	
57	7.2	-10	
58	6	9.75	
61	3	9.75	
62	-5.5	3	(1.2 x 1.2) mm
63	-5.5	-2	
64	-5.5	-8	
65	5.5	-8	
66	5.5	-2	
67	5.5	3	
68	-1	-3	
69	-1	-5	
70	1	-5	
71	1	-3	

4.3 PCB Landing Pattern

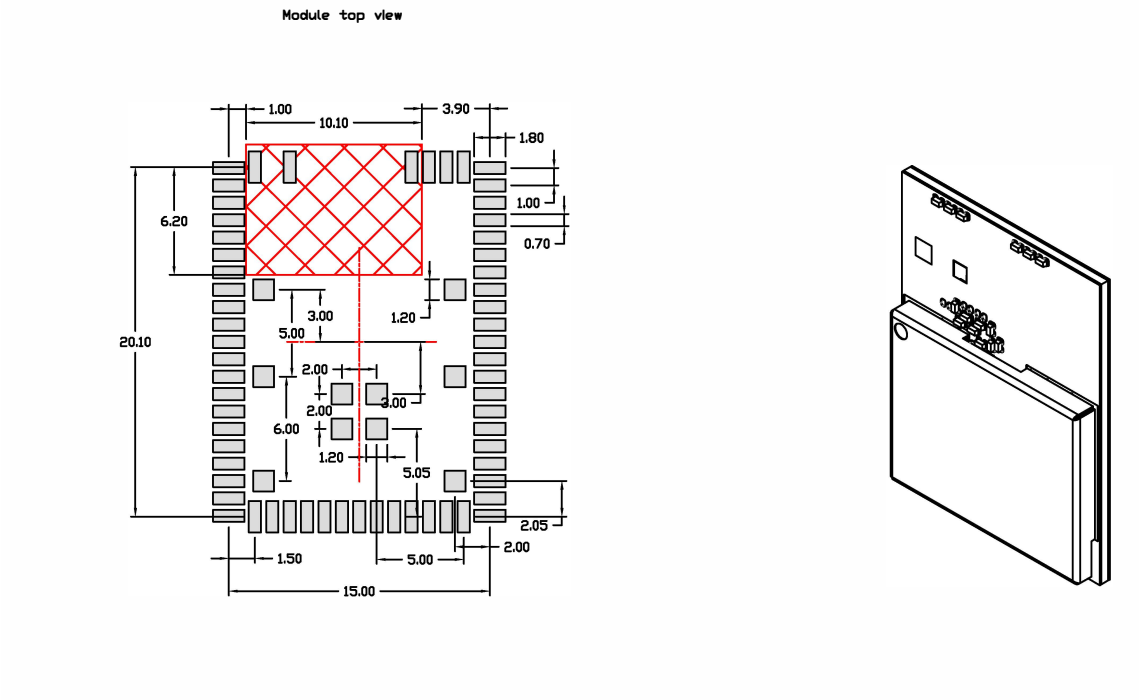


Figure 4.3. PCB Landing Pattern

Table 4.3. PCB Landing Pattern Pin Locations

PAD X-Y Coordinates			
Pad #	**X**	**Y**	**Pad Size**
1	-4	10.05	(1.8 x 0.7) mm
2	-6	10.05	
3	-7.5	10	
23	-7.5	-10	
24	-6	-10.05	
36	6	-10.05	
37	7.5	-10	
57	7.5	10	
58	6	10.05	
61	3	10.05	

PAD X-Y Coordinates			
Pad #	**X**	**Y**	**Pad Size**
62	-5.5	3	(1.2 x 1.2) mm
63	-5.5	-2	
64	-5.5	-8	
65	5.5	-8	
66	5.5	-2	
67	5.5	3	
68	-1	-3	
69	-1	-5	
70	1	-5	
71	1	-3	

4.4 Soldering Recommendations

It is recommended that final PCB assembly of the RS916AC0 and RS916AC1 follows the industry standard as identified by the Institute for Printed Circuits (IPC). This product is assembled in compliance with the J-STD-001 requirements and the guidelines of IPC-AJ-820. Surface mounting of this product by the end user is recommended to follow IPC-A-610 to meet or exceed class 2 requirements.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

Note: General SMT application notes are provided in the AN1223 document.

4.5 Tape and Reel

The RS916AC0 and RS916AC1 modules are delivered to the customer in cut tape (100 pcs) or reel (1000 pcs) packaging having the dimensions below. All dimensions are given in mm unless otherwise indicated.

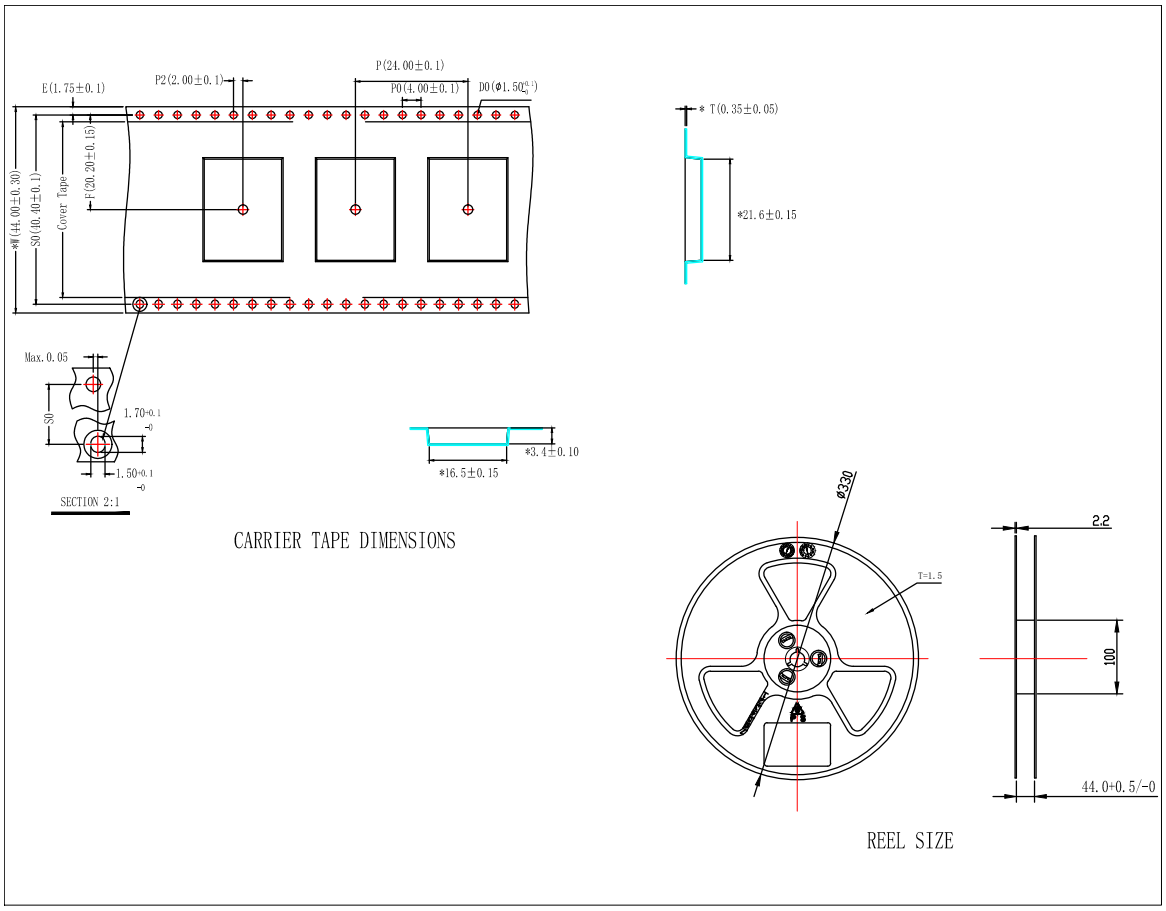


Figure 4.4. Carrier Tape Dimensions

4.6 Moisture Sensitivity Level

RS916AC0 and RS916AC1 modules are rated MSL3 (Moisture Sensitivity Level 3). Reels are delivered in packing which conforms to MSL3 requirements.

5. RS916AC0 and RS916AC1 Module Certification and Ordering Information

5.1 Certifications

This section details the certification status of the RS916AC0 and RS916AC1 Connectivity Modules with regards to regional regulatory radio approvals. Where applicable, the status with the qualifications against the specifications of the supported global industrial wireless standards is given too.

The address of the module manufacturer (technology owner) and certification applicant is:

SILICON LABS / SILICON LABORATORIES FINLAND OY
Alberga Business Park, Bertel Jungin aukio 3,
02600 Espoo, Finland

The RS916AC0 and RS916AC1 Connectivity Modules have a brand name of "SILICON LABS".

"SILICON LABS" (and "Silicon Labs") is a trademark globally owned by the Silicon Laboratories Inc. corporation, and all branches and subsidiaries, including the above applicant, holds the right to use it.

5.1.1 Qualified Antennas

The RS916AC1 and RS916AC0 Connectivity Modules have been tested and certified for the use with respectively the built-in integral antenna and a reference external antenna attached to the module's RF pin denoted as RF_PORT. The intended antenna impedance is 50 Ω.

Performance characteristics for the built-in antenna are presented in RS916AC1 Antenna Radiation and Efficiency. The details of the qualified external antenna are summarized in the table below.

Table 5.1. Qualified External Antennas for RS916AC0 Connectivity Modules

Brand and Model	Antenna Type	Maximum Gain	Impedance
Linx Technologies Inc., ANT-2.4-CW-CT-RPS	Connectorized Coaxial Dipole	+2.8 dBi	50 Ω

Any external antenna of the same general type and of equal or less peak directional gain compared to the one listed in the above table, and having similar in-band and out-of-band characteristics, can be used in the regulatory areas that have modular radio approvals, such as USA and Canada, as long as spot-check testing of the host is performed to verify that no performance changes compromising compliance have been introduced. In the particular FCC case, in order to comply with e-CFR Title 47, Part 15, Subpart C, Section 15.203, the module integrator using an external antenna must ensure it has a unique connector or it is nondetachable.

When using instead an external antenna of a different type (such as a chip antenna, a host PCB trace antenna, or a patch) or having non-similar in-band and out-of-band characteristics, but still with a gain less than or equal to the maximum gain listed in the table above, in principle it can be added to the existing modular grant/certificate by mean of a permissive change, for example with FCC and ISED. Typically, some radiated emission testing is demanded, but no modular or end-product re-certification is required. Please consult your certification house and/or a certification body and/or the module manufacturer for a confirmation of the correct procedures and for any authorization to perform permissive changes.

On the other hand, all products designed to be used with an external antenna having more gain than the maximum gain listed in the table above are very likely to require a full new end-product certification. Since the exact permissive change or registration or re-certification procedure is chosen on a case-by-case basis, please consult your certification house and/or a certification body for understanding the correct approach based on your unique design. You might also want or need to get in touch with Silicon Labs for any authorization letter that your certification body might ask for.

In countries applying the ETSI standards, where manufacturers issue a self-Declaration of Conformity before placing products in the market, like in the EU countries, the radiated emissions are always tested with the end-product and the external antenna type is not critical, but antennas with higher gain may violate some of the regulatory limits.

For Japan, the additional allowed external antennas are listed in the certificate and/or test report(s). Any other external antenna will have to be formally added to the list of approved antennas by the certificate holder: in this case, please reach out to the module manufacturer to discuss such addition, or consider certifying the end-product itself as an alternative.

5.1.2 CE and UKCA - EU and UK

The RS916AC0 and RS916AC1 Connectivity Modules have been tested against the relevant harmonized/designated standards and are in conformity with the essential requirements and other relevant requirements of the EU's Radio Equipment Directive (RED) (2014/53/EU) and of the UK's Radio Equipment Regulations (RER) (S.I. 2017/1206).

Please notice that every end-product integrating the RS916AC0 and RS916AC1 Connectivity Modules will need to perform the radio EMC tests on the whole assembly, according to the ETSI 301 489-x relevant standards.

Furthermore, it is ultimately the responsibility of the manufacturers to ensure the compliance of their end-products as a whole. The specific product assembly is likely to have an impact to RF radiated characteristics, when compared to the bare module. Hence, manufacturers should carefully consider RF radiated testing with the final product assembly, especially taking into account the gain of the external antenna if any, and the possible deviations in the PSD, EIRP and spurious emissions measurements, as defined in the ETSI EN 300 328 standard.

The modules are entitled to carry the CE and UKCA compliance marks, and the respective formal Declarations of Conformity (DoCs) are available at the product web page which is reachable starting from www.silabs.com.

Each OEM must also consider applying the compliance marks to a visible location on their end-products. In general, module customers assume full responsibility with regards to learning the guidelines and meeting the requirements for the compliance in each country where their end-products are marketed.

5.1.3 FCC - USA

This device complies with FCC's e-CFR Title 47, Part 15, Subpart C, Section 15.247 (and related relevant parts of the ANSI C63.10 standard) when operating with the built-in integral antenna or with an external antenna type as discussed in chapter 11.1.

Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user’s authority to operate the equipment.

FCC RF Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying the RF exposure compliance.

This transmitter meets the Mobile requirements at a distance of 20 cm and above from the human body, in accordance to the limit(s) exposed in the RF Exposure Analysis. This transmitter also meets the Portable requirements at distances equal or above those being reported in Minimum Separation Distances for SAR Evaluation Exemption.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM Responsibilities to Comply with FCC Regulations

This module has been tested for compliance to FCC Part 15.

OEM integrators are responsible for testing their end-product for any additional compliance requirements needed with this module installed (for example, digital device emissions, PC peripheral requirements, etc.)

Additionally, investigative measurements and spot-checking are strongly recommended to verify that the full system compliance is maintained when the module is integrated, even with a module having a full modular approval, in accordance with the "Host Product Testing Guidance" in FCC's KDB 996369 D04 Module Integration Guide V01.

- **General Considerations**

  This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement, which is typically applicable to the final host. The final host will still need to be assessed for compliance to this portion of the rule requirements, if applicable.

- **Manual Information to the End User**

  The OEM integrator has to be aware not to provide information to the end-user regarding how to install or remove this RF module, or how to change RF related parameters, in the user's manual of the final product which integrates this module.

  The end user manual shall include all required regulatory information/warnings as shown in this manual.

- **Host Manufacturer Responsibilities**

  Host manufacturers are ultimately responsible for the full compliance of their host system. The final product is supposed to be assessed against all the essential requirements of the FCC rules, such as FCC Part 15 Subpart B, before it can be placed on the US market. This includes re-assuring the compliance of the radio transmitter with the RF and EMF essential requirements of the FCC rules. The modular radio transmitter must not be incorporated into any other radio-equipped device or system without retesting for compliance as multi-radio and combined equipment.

  Except for minor (cosmetic) modifications, most changes to an FCC certified equipment require preliminary testing to determine whether any of such changes is a Class I or Class II permissive change. For more details about using the Single Modular Transmitter, refer to the following FCC documents:

  • KDB 996369 D01 Transmitter Module Equipment Authorization Guide

  • KDB 996369 D02 Frequently Asked Questions and Answers about Modules

  • KDB 178919 D01 Permissive Change Policy

  • KDB 178919 D02 Permissive Change Frequently-Asked Questions

Separation

- To meet the SAR exemption for portable conditions, the minimum separation distances indicated in Minimum Separation Distances for SAR Evaluation Exemption must be maintained between the human body and the radiator (antenna) at all times.
- This transmitter module is tested in a standalone RF Exposure condition, and in case of any co-located radio transmitter being allowed to transmit simultaneously, or in case of portable use at closer distances from the human body than those allowing the exceptions rules to be applied, a separate additional SAR evaluation, or a reduction in the max output power or in the duty-cycle, might be required for the host, ultimately leading to a Class II Permissive Change, or more rarely to a new grant.
- **Important Note:** In the event that the conditions for the exemption cannot be met, the final product will likely have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the FCC authorization to remain valid, and a permissive change will have to be applied. The SAR evaluation (and/or reconfiguration) is in the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body, following a *Change in ID* authorization by the module's original grant holder.

End Product Labeling

The RS916AC0 and RS916AC1 Connectivity Modules are labeled with their own FCC ID. In all those cases when the module's label is not visible, for example after the module becomes enclosed inside the end-product casing, or if the FCC ID is printed on the module's PCB silkscreen, then the outside of the device into which the module is installed must also have a label with a reference to the embedded module. In that case, the final product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQRS916AC"

or

"Contains FCC ID: QOQRS916AC"

Final note:

As long as all the conditions in this and all the above chapters are met, further RF testing of the transmitter will not be strictly required. However, still consider the good practice and the FCC strong recommendation to ensure the compliance of the host by spot-checking. Nevertheless, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements which might be mandatory with this module installed.

5.1.4 ISED - Canada

This radio transmitter (with IC: 5123A-RS916AC and PMN: *Bluetooth Low Energy, Bluetooth Classic BR/EDR, and 802.11b/g/n wireless radio module*) has been approved by *Innovation, Science and Economic Development Canada* (*ISED Canada*, formerly *Industry Canada*) to operate with the built-in integral antenna or with the external antenna type(s) listed in Qualified Antennas, having the maximum permissible gain indicated in the table. External antenna types not included in this list, or having a gain greater than the maximum gain listed, are strictly prohibited for use with this device.

This radio-equipped device complies with ISED's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference.
2. This device must accept any interference, including interference that may cause undesired operation of the device.

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

The module meets the requirements for Mobile use cases when the minimum separation distance from the human body is 20 cm or greater, in accordance to the limit(s) exposed in the RF Exposure Analysis.

For Portable use cases, RF exposure or SAR evaluation is not required when the separation distances from the human body are equal or above those reported in Minimum Separation Distances for SAR Evaluation Exemption .

If the separation distance from the human body is less than the values stated in Minimum Separation Distances for SAR Evaluation Exemption, then the OEM integrator is responsible for evaluating the SAR with the end-product, or for the re-configuration of the radio module in the host in terms of lowering the max RF TX power and/or the duty-cycle. A permissive change would be required too, under the responsibility of the host manufacturer, following a *Multiple Listing* authorization by the module's original certificate holder.

OEM Responsibilities to comply with IC Regulations

The RS916AC0 and RS916AC1 Connectivity Modules have been certified for integration into products only by OEM integrators, under the following conditions:

- The module must be installed in such a way that the intended minimum separation distances are maintained between the radiator (antenna) and all persons at all times. Minimum Separation Distances for SAR Evaluation Exemption indicates the distances in accordance to the use cases.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

Important Note: In the event that the above conditions cannot be met, the final product will have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the ISED authorization to remain valid; a permissive change will have to be applied too**.** The RF Exposure evaluation (SAR, or possibly a re-configuration) is in the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body, following a *Multiple Listing* authorization by the module's original certificate holder.

End Product Labeling

The RS916AC0 and RS916AC1 Connectivity Modules are labeled with their own IC ID. In all those cases when the module's label is not visible, for example after the module becomes enclosed inside the end-product casing, or if the IC ID is printed on the module's PCB silkscreen, then the outside of the device into which the module is installed must also have a label with a reference to the embedded module. In that case, the final product must be labeled in a visible area with the following:

“**Contains Transmitter Module IC: 5123A-RS916AC**”

or

“**Contains IC: 5123A-RS916AC**"

Final notes:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end-product.

As long as all the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.)

ISED (Français)

Le présent émetteur radio (IC: 5123A-RS916AC, PMN: *Bluetooth Low Energy, Bluetooth Classic BR/EDR, and 802.11b/g/n wireless radio module*) a été approuvé par *Innovation, Sciences et Développement Économique Canada* (*ISED Canada*, anciennement *Industrie Canada*) pour fonctionner avec l'antenne intégrée et le ou les types d'antenne énumérés à la section Qualified Antennas, avec le gain maximal admissible indiqué. Les types d'antenne non inclus dans cette liste, ayant un gainsupérieur au gain maximal indiqué, sont strictement interdits d'utilisation avec cet appareil.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage;
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Déclaration d'exposition RF

Les exceptions aux limites de l'évaluation SAR sont données dans le numéro 5 de la publication RSS-102.

Le module répond aux exigences pour les cas d'utilisation Mobile lorsque la distance minimale de séparation du corps humain est de 20 cm ou plus, conformément à la (aux) limite(s) exposée(s) dans l'analyse de l'exposition RF.

Pour les cas d'utilisation portables, l'évaluation de l'exposition RF ou l'évaluation SAR n'est pas requise lorsque les distances de séparation du corps humain sont égales ou supérieures à celles indiquées dans Minimum Separation Distances for SAR Evaluation Exemption.

Si la distance de séparation du corps humain est inférieure aux valeurs indiquées dans Minimum Separation Distances for SAR Evaluation Exemption, l'intégrateur OEM est responsable de l'évaluation du SAR avec le produit final, ou de la reconfiguration du module radio dans l'hôte en termes de réduction de la puissance RF TX maximale et/ou du rapport cyclique. Une modification permissive serait également nécessaire, sous la responsabilité du fabricant de l'hôte, suite à une autorisation de cotation multiple par le titulaire du certificat du module d'origine.

Responsabilités du fabricant de se conformer à la réglementation IC

Le module a été certifié pour l'intégration dans les produits uniquement par les intégrateurs OEM dans les conditions suivantes:

- Le module émetteur doit être installée de manière à maintenir une distance de séparation minimale, comme indiqué ci-dessus, entre le radiateur (antenne) et toutes les personnes à tout moment.
- Le module émetteur ne doit pas être localisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

Remarque Importante: au cas où ces conditions ne pourraient pas être remplies, le produit final devra être soumis à des tests supplémentaires pour évaluer l'exposition RF, ou passer par une reconfiguration de la puissance de sortie maximale et/ou du rapport cyclique, afin que l'autorisation ISED reste valable; une modification permissive devra également être appliqué. L'évaluation de l'exposition aux radiofréquences (SAR, ou éventuellement une reconfiguration) est sous la responsabilité du fabricant du produit final, ainsi que le changement permissif qui peut être effectué avec l'aide de l'organisme de certification des télécommunications du client, après autorisation de cotation multiple par le titulaire de la certification du module.

Étiquetage des produits finis

Les modules RS916AC0 and RS916AC1 sont étiquetés avec leur propre IC ID. Dans tous ces cas, si l'ID IC n'est pas visible après l'installation du module à l'intérieur d'un autre appareil, alors l'extérieur de l'appareil dans lequel le module est installé doit également afficher une étiquette faisant référence au module inclus. Dans ce cas, le produit final doit être étiqueté dans une zone visible avec les éléments suivants:

"**Contient le module transmetteur IC: 5123A-RS916AC**"

ou

"**Contient IC: 5123A-RS916AC**"

Remarques finales:

L'intégrateur OEM doit être conscient de ne pas fournir à l'utilisateur final d'informations sur la procédure d'installation ou de retrait de ce module RF ni sur la modification des paramètres liés à la RF dans le manuel d'utilisation du produit final.

Tant que toutes les conditions ci-dessus sont remplies, aucun test supplémentaire de l'émetteur ne sera nécessaire. Toutefois, l'intégrateur OEM reste responsable de l'essai de son produit final pour déterminer les exigences de conformité supplémentaires requises avec ce module installé (par exemple, émissions d'appareils numériques, exigences relatives aux périphériques PC, etc.)

5.1.5 MIC - Japan

The RS916AC0 and RS916AC1 Connectivity Modules are certified in Japan with following certification number:

- 214-124822

It is the end-product manufacturer's responsibility to ensure that a module is configured to meet the compliance limits, as documented in the formal certification test report(s) being available at www.silabs.com. Refer to the API reference manual(s) to learn for example how to configure (limit) the maximum RF TX power for the normal operations if need be, and refer as well to the power setting tables in the test report(s) in order to realize the maximum output power allowed for the regulatory compliance in Japan.

Manufacturers integrating a radio module into their host equipment are supposed to make the compliance mark and the certification number visible on the outside of their device. This combination of mark and number, and their relative placement, is depicted in the example Figure 5.1 below, and depending on the overall size it might also appear among the top shield markings of the radio module. The certification mark and certification number must be placed close to the text in the Japanese language which is provided below. This requirement in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

Certification text to be placed on the outside surface of the host equipment:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation of the text:

“This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”

The "Giteki" compliance mark, together with the actual module's certification number, as shown in the following example figures, must be affixed to an easily noticeable section of the specified radio-enabled host equipment. Note that such section may be required to contain additional information if the end-device embedding the module is also subject to a Telecom approval.

The manufacturer of the final product is also responsible to provide a Japanese language version of the User Manual and/or Installation Instructions as a companion document coming with the final product when placed on the market in Japan. Such a document will have to mention the integrated radio component and the related certification information.

Figure 5.1. Example of GITEKI Mark with placeholder for actual Certification Number

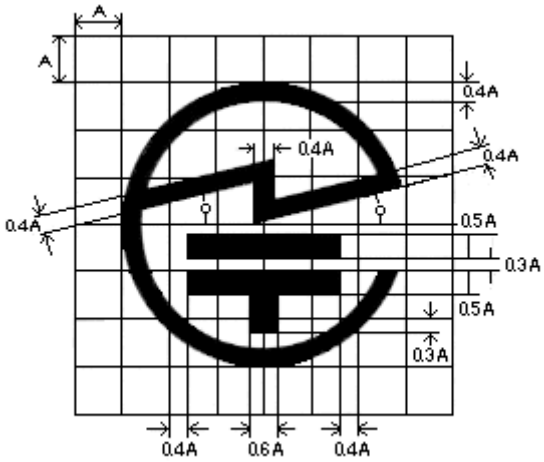


Figure 5.2. Detail of GITEKI Compliance Mark

5.1.6 KC - South Korea

The RS916AC0 and RS916AC1 Connectivity Modules have a RF registration for import and use in South Korea.

Registration number is KC ID: R-R-BGT-RS916AC

These modules are meant to be integrated into end-products, which then become exempted from doing the RF emission testing, as long as the recommended design guidance is followed, and as long as, where applicable, the approved external antennas are used and any additional transmit power backoff is implemented in accordance to the measurements and configurations seen in the formal test report(s).

EMC testing and any other relevant test applicable to the end-product as a whole, plus appropriate labeling of the end-product, might still be required for the full regulatory compliance in the country.

5.1.7 NCC - Taiwan

RS916AC0 and RS916AC1 modules are certified in Taiwan with NCC certification number TBD.

RS916ACx 模塊在台灣通過了 NCC 認證編號 TBD 的認證。

Manufacturers are required to mark their end-products with the following sentence: "This product contains a radio frequency module with certification number TBD."

系統製造商應在平台上放置如下聲明：“本產品包含認證號為 TBD 的射頻模塊。”

Note: The outer packaging of the final product must also be marked with the NCC conformity mark by the manufacturer.

注意：最終產品的外包裝也必須由製造商打上 NCC 合格標誌

Additionally, the final product will have to be listed in the NCC database of approved radio-equipped devices. Consequently, the end manufacturer is also supposed to contact the certification house that originally released the full modular approval and apply for the registration of their device under the above certification number (fees might apply.)

該平台還需要列入經批准的無線電設備的 NCC 數據庫；因此，平台製造商還應聯繫最初頒發全模塊化批准的認證機構，並根據上述認證編號申請註冊其設備（可能需要付費）。

NCC Statement
For low-power radio frequency equipment that has been certified, companies, firms, or users are not allowed to change the frequency, increase the power, or change the characteristics and functions of the original design without further NCC approval. The use of low-power radio frequency equipment shall not affect flight safety and interfere with legal communications. If interference is found, it shall be immediately stopped, and the equipment can be brought back into use only after it has been improved, so that interference is found no more. The aforementioned legal communication refers to radio communications operating in accordance with the provisions of the Telecommunications Management Act. Low-power radio frequency equipment must withstand interference from legitimate communications or radiating electrical equipment for industrial, scientific, and medical applications.
NCC 警語
取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。 低功率射頻器材之使用不得影響飛航安全及干擾合法通信。 經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。 前述合法通信，指依電信管理法規定作業之無線電通信。 低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

5.1.8 SRRC - China

The RS916AC1 module has a full modular radio type approval for re-use by the OEM integrators:

Certificate number: 2023-XXXX

CMIIT ID: 2023YYXXXX

The RS916AC0 module has a limited modular radio type approval for re-use by the OEM integrators:

Certificate number: 2023-ZZZZ

CMIIT ID: 2023YYZZZZ(M)

Note for modules with a full modular approval: every end-product integrating the module must be labeled with the following statement, or alternatively the statement will have to go to the end-product's user manual:

本设备包含一个无线电发射器模块，型号核准代码为：CMIIT ID：2023YYXXXX

(Translation: This equipment contains a radio transmitter module with model approval code: CMIIT ID: XXXXYYZZZZ)

中国–SRRC

RS916AC1 模塊具有完整的模塊化認證，可供 OEM 集成商重複使用：

认证编号：2023-XXXX
CMIIT ID: 2023YYXXXX

RS916AC0 模塊具有有限的模塊化認證，可供 OEM 集成商重複使用：

认证编号：2023-ZZZZ
CMIIT ID: 2023YYZZZZ

具有完全模塊化批准的模塊注意事項：以下聲明必須出現在嵌入模塊的最終產品的標籤和/或用戶手冊中：

本设备包含一个无线电发射器模块，型号核准代码为：CMIIT ID：2023YYXXXX

5.1.9 RF Exposure and Proximity to Human Body

When using the RS916AC0 and RS916AC1 Connectivity Modules in an application where the radio-equipped end-product is located close to the human body, the human RF Exposure must be taken into account. FCC, ISED, and CE/UKCA all have different standards and rules for evaluating the RF Exposure. In particular, each regulator has different requirements when it comes to the exemption from having to perform RF Exposure and SAR (Specific Absorption Rate) measurements, and the minimum separation distances between the module's antenna and the human body varies accordingly. The properties of the RS916AC0 and RS916AC1 Connectivity Modules allow the minimum separation distances detailed in the table below for the SAR evaluation exemption in the Portable use cases (less than 20 cm from the human body). These modules are approved for the Mobile use case (more than 20 cm) without any need for RF Exposure evaluation.

Table 5.2. Minimum Separation Distances for SAR Evaluation Exemption

Certification	RS916AC0 and RS916AC1
FCC	25 mm
ISED	30 mm
CE / UKCA	In general, the RF exposure should always be evaluated with the end-product when transmitting with EIRP power levels higher than 20 mW (13 dBm) while at a closer than 20cm distance from the human body. With the RS916AC0 and RS916AC1 modules, this is the case only with the 802.11b/g/n protocols at full power, in particular when the distance is 2.55 cm and below. In all other cases, modules comply with the requirements of the relevant standard(s).

The exemption minimum distances above, calculated for reference in the full output power use-case while taking into account the most restrictive among the supported wireless protocol and the most restrictive of the hardware variants, are based on the rules in force at the time of writing this datasheet. Even though changes happen rarely, always ensure to apply the rules in force at the time of placing a product in the market.

In the cases of FCC and ISED, it is allowed to use the module at its max RF TX power in end-products where the typical separation distance from the human body is smaller than mentioned above, but it requires evaluating the RF Exposure in the final assembly and applying for a *Class 2 Permissive Change* to the FCC and ISED approvals of the module. In order to proceed with the permissive changes, first the module manufacturer should be asked for an authorization to do an FCC's *Change in ID* and an ISED's *Multiple Listing*; then, the new Portable condition will be added to the new parallel grants owned by the end-product manufacturer, for extending the approvals to their unique host under their unique configuration and mode of use.

For those end-products where the embedded module is configured to implement only a single wireless protocol, the test report for the Portable use case could be consulted, where further calculations are made for the exemption distances with the single protocols separately, in each hardware variant if applicable. In those cases when the single wireless protocol in use would allow for the exemption at a shorter distance than the highest of the minimum distances, there would be no need the evaluate the RF Exposure at such a shorter distance and above, but a permissive change would be needed as a mean to notify the FCC/ISED of the reason why in the field the module is allowed to operate at a shorter distance than in the table above.

An example of another use case where the module could operate at a shorter distance than in the table above, without having to do the RF Exposure evaluation / SAR measurement, is when the power or the duty-cycle is reduced during normal operation. However, the new minimum distance for the exemption should be re-calculated, and still a permissive change would be needed to notify the regulators of the new conditions.

For the CE/UKCA compliance, RF Exposure must be considered and evaluated by the OEM in all cases when the end-product is transmitting at higher power level (or shorter distance from the human body) than indicated in the table above.

Note: Placing the module in touch or very close to the human body will have a negative impact on the efficiency of the antenna thus a reduced range is to be expected.

5.1.10 Bluetooth Qualification

The RS916AC0 and RS916AC1 modules have the following Qualified Design Listings (QDL) with corresponding Qualified Design Identification (QDID) based on the Bluetooth Core Specification 5.0:

1. **QDID 126032**
   - This Tested Component is for the Low Energy RF-PHY and the BR/EDR Radio interface.
2. **QDID 125795**
   - This Tested Component is for Host Controller Interface, BR/EDR Link Manager and Low Energy Link Layer.
3. **QDID 127696**
   - This Controller Subsystem combines the above QDID 126032 and QDID 125795. It encompasses the Low Energy RF-PHY and the BR/EDR Radio interface, the Low Energy Link Layer and the BR/EDR Link Manager, plus the Host Controller Interface, for easier integration when doing an End-Product Listing (EPL).

5.2 Module Marking Information

The figure and table below illustrate the marking on the Single band module and explains the marking on the module.

Figure 5.3. Module Marking Information

Marking		Description
Part	RS916WS00ACxxx/ RS916NS00ACxxx	Part number designation
Model	RS916AC0/RS916AC1	Model number designation
Firmware	RS916WS00AC0Ax/ RS916WS00AC1Ax	Software/Firmware supported – refer to the Part Ordering Section for more details.
QR Code	YYWWMMABCDE	YY – Last two digits of the assembly year WW – Two-digit workweek when the device was assembled MMABCDE – Silicon Labs unit code
Lot Code	YYWWTTTTTT	YY – Last two digits of the assembly year WW – Two-digit workweek when the device was assembled TTTTTT – Manufacturing trace code. The first letter is the device revision
Compliance Marks		Certification marks such as the CE and UKCA and GITEKI marks, and certification numbers like the FCC and IC IDs, etc. will be engraved on the hatched-out area or printed on the back side of the module, according to regulatory body requirements.

5.3 Ordering Information

Table 5.3. Part Ordering Options

Part Number	Wireless and Memory
Embedded Connectivity (WiSeConnect)	
RS916WS00AC0A3	SBW + BT 5 with internal flash
RS916WS00AC1A3	SBW + BT 5 with internal flash & integrated antenna
Hosted Connectivity (n-Link)	
RS916NS00AC0A3	SBW + BT 5 with internal flash
RS916NS00AC1A3	SBW + BT 5 with internal flash & integrated antenna

Note:

- SBW: Single Band Wi-Fi (2.4 GHz).
- Customer should include provision for programming or updating the firmware at manufacturing.
- Throughout this document, the modules are referred to by their model names of RS916AC0 and RS916AC1, respectively for the hardware variants with RF pad and with integral antenna.

6. RS916AC0 and RS916AC1 Module Documentation and Support

Silicon Labs offers a set of documents which provide further information required for evaluating, and developing products and applications using the *RS9116* IC on which the *RS916AC0 and RS916AC1* modules are based. These documents are available in RS9116 Document Library on the Silicon Labs website. The documents include information related to Software releases, Evaluation Kits, User Guides,Programming Reference Manuals, Application Notes, and others.

For further assistance, you can contact Silicon Labs Technical Support here.

6.1 Resource Location

RS9116 Document Library : https://docs.silabs.com/rs9116/

Technical Support : http://www.silabs.com/support/

7. Revision History

Revision 0.6

June, 2023

- Updated pin information and reference schematic
- Updated OPN table
- Updated EVK OPNs
- Updated certification chapters

Revision 0.5

February, 2023

- Updated features set and characterization numbers based on latest test values.

Revision 0.2

January, 2022

- Updated Reference Schematics for RS916AC0 and RS916AC1 modules.
- Updated Layout guidelines. Separate guidelines for RS916AC0 and RS916AC1 included.
- Included PCB Landing pattern for the RS916AC0 and RS916AC1 modules.

Revision 0.1

September, 2021

Preliminary version.

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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

www.silabs.com