BGM240S Bluetooth™ SiP Module Data Sheet

The BGM240S is a secure, high-performance wireless module optimized for the needs of battery and line-powered IoT devices running on Bluetooth networks.

Based on the Series 2 EFR32BG24 SoC, it enables Bluetooth® Low Energy connectivity, delivering exceptional RF performance and energy efficiency, industry-leading Secure Vault® technology, and future-proofing capabilities.

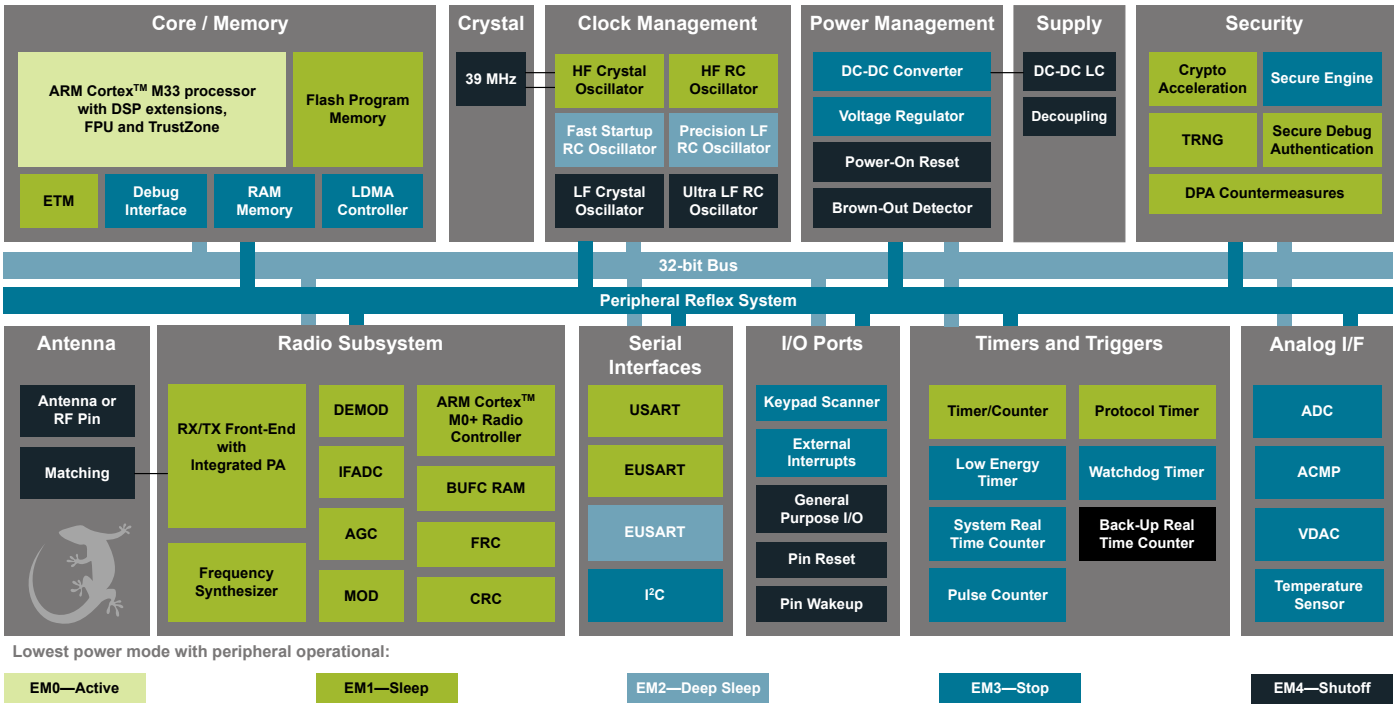
The BGM240S is a complete System in Package solution offered with robust and fully-upgradeable software stacks, global regulatory certifications, advanced development and debugging tools, and documentation that simplifies and minimizes the development cycle of your end-product, helping to accelerate its time-to-market.

The BGM240S is targeted for a broad range of applications, including:

- Smart Home Devices
- Lighting
- Gateways and Digital Assistants
- Building Automation and Security

KEY FEATURES

- Bluetooth Low Energy 5.3 and Bluetooth Mesh connectivity
- Built-in antenna or RF pin
- Up to 10 dBm TX output power
- -97 dBm BLE 1M RX sensitivity
- 32-bit ARM® Cortex®-M33 core running up to 78 MHz
- 1536/256 kB of Flash/RAM memory
- Vault High or Vault Mid security
- Rich set of analog and digital peripherals
- 32 GPIO pins
- -40 to 105 °C
- 7mm x 7mm x 1.18mm



1. Features

- **Supported Protocols**
  - Bluetooth Low Energy (BLE) 5.3
  - Bluetooth Mesh
  - Matter-ready Smart Home Connectivity
- **Wireless System-on-Chip**
  - 2.4 GHz radio
  - TX power up to +10 dBm
  - 32-bit ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - 1536 kB flash program memory
  - 256 kB RAM data memory
  - Embedded Trace Macrocell (ETM) for advanced debugging
- **Receiver Sensitivity**
  - -105.1 dBm (0.1% BER) at 125 kbps GFSK
  - -100.7 dBm (0.1% BER) at 500 kbps GFSK
  - -97.0 dBm (0.1% BER) at 1 Mbps GFSK
  - -94.3 dBm (0.1% BER) at 2 Mbps GFSK
- **Current Consumption**
  - 5.1 mA RX current at 1 Mbps GFSK
  - 4.6 mA TX current at 0 dBm
  - 23.4 mA TX current at 10 dBm
  - 33.4 µA/MHz in Active Mode (EM0) at 39.0 MHz
  - 1.3 µA EM2 DeepSleep current (16 kB RAM retention and RTC running from LFRCO)
- **Regulatory Certifications**[1]
  - CE (EU)
  - UKCA (UK)
  - FCC (USA)
  - ISED (Canada)
  - MIC (Japan)
  - KC (South Korea)
- **Operating Range**
  - 1.8 to 3.8 V
  - -40 to +105 °C
- **Dimensions**
  - 7 mm x 7 mm x 1.18 mm
- **Security**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration with DPA counter-measures for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, and ECDH
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug Interface lock/unlock
  - Secure Key Management with PUF
  - Anti-Tamper
  - Secure Attestation
- **MCU Peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - 2 × Analog Comparator (ACMP)
  - 2 × Digital to Analog Converter (VDAC)
  - Up to 26 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 16 Channel Peripheral Reflex System (PRS)
  - 3 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 2 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 2 x 32-bit Real Time Counter (SYSRTC/BURTC)
  - 24-bit Low Energy Timer for waveform generation (LETIMER)
  - 16-bit Pulse Counter with asynchronous operation (PCNT)
  - 2 × Watchdog Timer (WDOG)
  - 1 × Universal Synchronous/Asynchronous Receiver/Transmitter (USART), supporting UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S
  - 2 × Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART) supporting UART/SPI/DALI/IrDA
  - 2 × I^2C interface with SMBus support
  - Low-Frequency RC Oscillator with precision mode to replace 32 kHz sleep crystal (LFRCO)
  - Keypad scanner supporting up to 6x8 matrix (KEYSCAN)
  - Die temperature sensor with +/- 1.5 °C accuracy after single-point calibration

1. Available at product launch

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	TX Power	Freq Band	Antenna	Secure Vault	Flash/ RAM(kB)	GPIO	Temp Range	Pack-aging
BGM240SA22VNA2	Bluetooth 5.3	10 dBm	2.4 GHz	Built in or RF PIN	MID	1536/256	32	-40 to 105 °C	Tray
BGM240SA22VNA2R	Bluetooth 5.3	10 dBm	2.4 GHz	Built in or RF PIN	MID	1536/256	32	-40 to 105 °C	Reel
BGM240SB22VNA2	Bluetooth 5.3	10 dBm	2.4 GHz	Built in or RF PIN	HIGH	1536/256	32	-40 to 105 °C	Tray
BGM240SB22VNA2R	Bluetooth 5.3	10 dBm	2.4 GHz	Built in or RF PIN	HIGH	1536/256	32	-40 to 105 °C	Reel

Note:

1. BGM240S modules operate over the 2.4 GHz ISM band (BLE range: 2402 - 2480 MHz).
2. The maximum RF TX power allowed by different regional regulatory authorities may differ from the maximum output power a module can produce. End-product manufacturers must then verify that the module is configured to meet the regulatory limits for each region in accordance with the local rules and the formal certification test reports.
3. BGM240S modules are pre-programmed with UART BGAPI bootloader.
4. Throughout this document, the modules may be referred to by their product family/marketing name (e.g. BGM240S), by their model name (BGM240S22A), or by their full ordering codes as seen in the table above.
5. Radio board **xGM240-RB4318A** (+10 dBm) is available for BGM240S evaluation and development.
6. Devices are pre-programmed for xGM240-RB4318A (+10dBm), which uses the pin configuration in Section 5. Reference Diagrams.

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3. System Overview

3.1 Block Diagram

The BGM240S module is a highly-integrated, high-performance system in package with all the hardware components needed to enable 2.4 GHz wireless connectivity and support robust networking capabilities via multiple wireless protocols.

Built around the EFR32BG24 Wireless SoC, the BGM240S includes a built-in antenna, an RF matching network (optimized for transmit power efficiency), supply decoupling and filtering components, an LC tank for DC-DC conversion, a 39 MHz reference crystal, and an RF shield. Also, it supports the use of an external 32 kHz crystal as a low frequency reference signal via GPIO pins for use cases demanding maximum energy efficiency.

For designs where an external antenna solution may be beneficial, a module variant with a 50 Ω-matched RF pin instead of the built-in antenna is available.

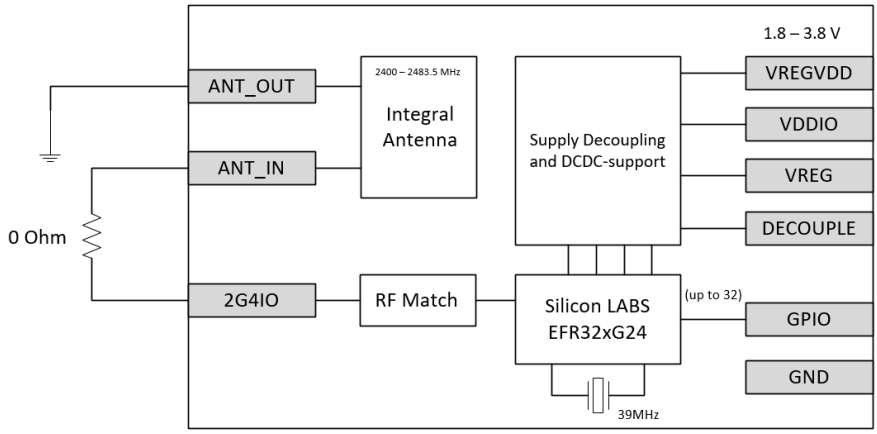


Figure 3.1. BGM240S Block Diagram - Integral Antenna

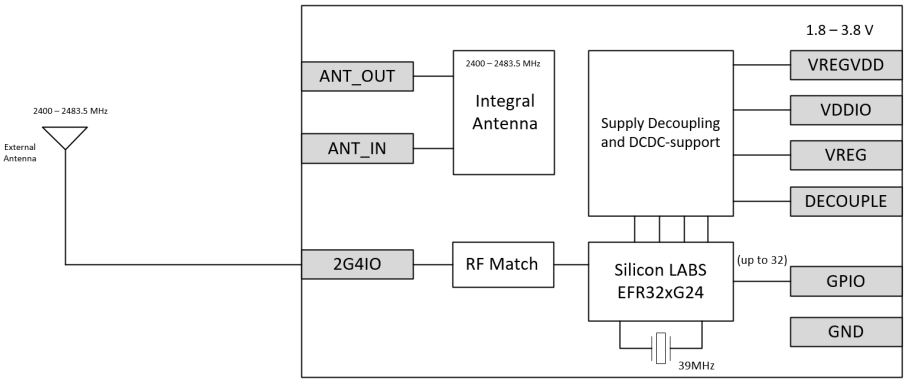


Figure 3.2. BGM240S Block Diagram - External Antenna

A simplified internal schematic for the BGM240S module is shown in Figure 3.3 BGM240S Module Schematic on page 7.

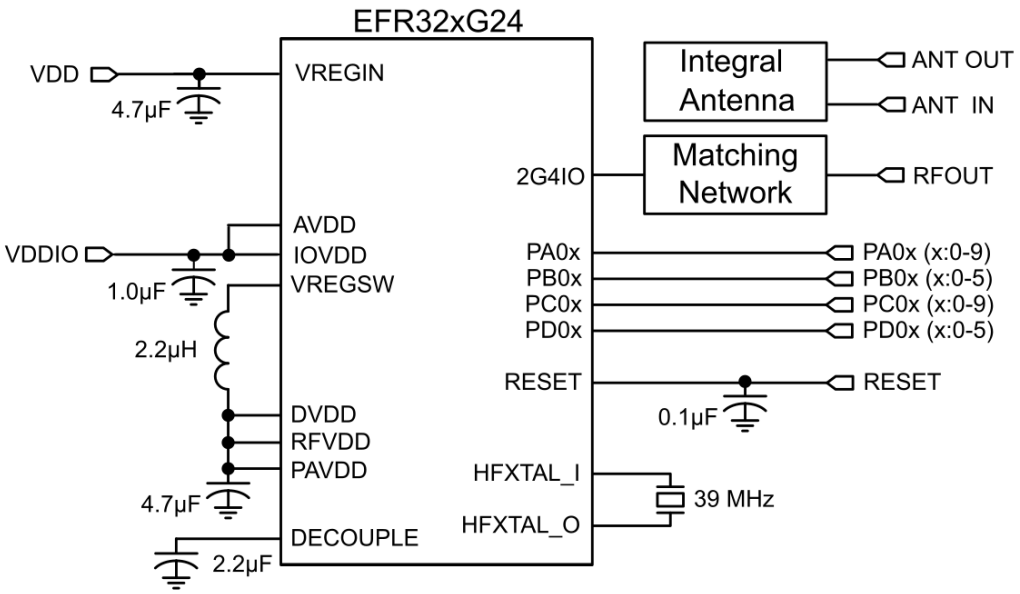


Figure 3.3. BGM240S Module Schematic

3.2 EFR32BG24 SoC

The EFR32BG24 SoC features a 32-bit ARM Cortex M33 core, a 2.4 GHz high-performance radio, 1536 kB of Flash memory, 256 kB of RAM, a dedicated core for security, a rich set of MCU peripherals, and various clock management and serial interfacing options. See the EFR32xG24 Reference Manual for details.

3.3 Antenna

BGM240S modules come with two antenna solution variants: a built-in integral ground loop type antenna realized by a PCB trace design, or a 50Ω-matched RF pin to support an external antenna. Typical performance characteristics for the built-in antenna are detailed in the table below. See Section 4.16 Typical Performance Curves and Section 11.1 Qualified Antennas for other relevant details.

Table 3.1. BGM240S antenna specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Antenna frequency range	F_{RANGE}		2400	—	2483.5	MHz
Antenna Gain	G_{MAX}	Maximum relative to isotropic	—	—	1.48	dBi
Antenna Efficiency	Efficiency		-2.5	—	-1.36	dB
Reference impedance	Z		—	50	—	Ω
Dielectric Constant Host Board	DI_{CONST}		—	4.3	—	
Trace Thickness	$T_{THICKNESS}$		—	47	—	um
VSWR	VSWR	Maximum	—	—	2:1	

Antenna efficiency, gain and radiation pattern are dependent on the application PCB layout and mechanical design. Antenna specification is based on the assumption that the host board design guidelines in Section 7. Design Guidelines are followed.

3.4 Power Supply

The BGM240S requires a primary supply (VDD) and IO supply (VDDIO) voltage to operate. All necessary decoupling, filtering and DC-DC-related components are included in the module.

3.5 General Purpose Input/Output (GPIO)

The BGM240S has up to 32 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in the Table 6.2 GPIO Alternate Functions Table on page 31

3.6 Security

BGM240S modules support one of two levels in the Security Portfolio offered by Silicon Labs: Secure Vault Mid or Secure Vault High.

Secure Vault is a collection of technologies that deliver state-of-the-art security and upgradability features to protect and future-proof IoT devices against costly threats, attacks, and tampering. A dedicated security CPU enables the Secure Vault functions and isolates cryptographic functions and data from the Cortex-M33 core. BGM240SA part numbers support Secure Mid Vault and BGM240SB part numbers support Secure Vault High.

Table 3.2. Secure Vault Features

Feature	Secure Vault Mid	Secure Vault High
True Random Number Generator (TRNG)	Yes	Yes
Secure Boot with Root of Trust and Secure Loader (RTSL)	Yes	Yes
Secure Debug with Lock/Unlock	Yes	Yes
DPA Countermeasures	Yes	Yes
Anti-Tamper		Yes
Secure Attestation		Yes
Secure Key Management		Yes

Symmetric Encryption	• AES 128 / 192 / 256 bit
	  • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC
		• AES 128 / 192 / 256 bit
		  • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC
		• ChaCha20

Public Key Encryption - ECDSA / ECDH / EdDSA	• p192 and p256	• p192, p256, p384 and p521 • Curve25519 (ECDH) • Ed25519 (EdDSA)
Key Derivation	• ECJ-PAKE p192 and p256	• ECJ-PAKE p192, p256, p384, and p521 • PBKDF2 • HKDF
Hashes	• SHA-1 • SHA-2/256	• SHA-1 • SHA-2 256, 384, and 512 • Poly1305

3.6.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates.

For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

3.6.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations, and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CCM (Counter with CBC-MAC)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192, P-256, P-384, and P-521 for ECDH (Elliptic Curve Diffie-Hellman) key derivation, and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for EdDSA (Edwards-curve Digital Signature Algorithm) sign and verify operations.

Secure Vault also supports ECJ-PAKE (Elliptic Curve variant of Password Authenticated Key Exchange by Juggling) and PBKDF2 (Password-Based Key Derivation Function 2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.6.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.6.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

In addition, Secure Vault High also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see AN1190: Series 2 Secure Debug.

3.6.5 DPA Countermeasures

The AES and ECC accelerators have Differential Power Analysis (DPA) countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.6.6 Secure Key Management with PUF

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a Physically Unclonable Function (PUF) to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

3.6.7 Anti-Tamper

Secure Vault High devices provide internal tamper protection which monitors parameters such as voltage, temperature, and electromagnetic pulses as well as detecting tamper of the security sub-system itself. Additionally, 8 external configurable tamper pins support external tamper sources, such as enclosure tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see AN1247: Anti-Tamper Protection Configuration and Use.

3.6.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see AN1268: Authenticating Silicon Labs Devices Using Device Certificates.

4. Electrical Specifications

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and VDD = VDDIO = 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

4.1 Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+105	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{VDDIO} + 0.3	V
DC voltage on RESETn pin[1]	V_{RESETn}		-0.3	—	3.8	V
Absolute voltage on RFOUT pin	V_{MAX2G4}		-0.3	—	V_{VDD} + 0.3	V
Total current into VDD pin	I_{VDDMAX}	Source	—	—	200	mA
Total current into GND pin	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. The RESETn pin has a pull-up device to the internal DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.

4.2 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A		-40	—	+105	°C
VDD operating supply voltage	V_{VDD}	DC-DC in regulation	2.2	3.0	3.8	V
		DC-DC in bypass	1.8	3.0	3.8	V
VDDIO operating supply voltage	V_{VDDIO}	AVDDBODEN=0, IOVDDxBODEN=0[1]	1.71	3.0	3.8	V
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	78	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
		VSCALE1, MODE = WS0	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	78	MHz
		VSCALE1	—	—	40	MHz
EM01 Group C clock frequency	$f_{EM01GRPCCLK}$	VSCALE2	—	—	78	MHz
		VSCALE1	—	—	40	MHz
Radio HCLK frequency	f_{RHCLK}	VSCALE2 or VSCALE1	—	39.0	—	MHz

Note:
1. The AVDD and IOVDD BOD enable bits are in the EMU_BOD3SENSE register. These BODs are disabled on reset.

4.3 MCU current consumption at 3.0 V

Unless otherwise indicated, typical conditions are: VDD = VDDIO = 3.0 V, DC-DC in regulation. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.3. MCU current consumption at 3.0 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2	—	33.3	—	µA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2	—	32.8	—	µA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	49.1	—	µA/MHz
		39 MHz crystal, CPU running Prime from flash	—	33.9	—	µA/MHz
		39 MHz crystal, CPU running while loop from flash	—	33.4	—	µA/MHz
		39 MHz crystal, CPU running CoreMark loop from flash	—	49.4	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	28.1	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2	—	22.6	—	µA/MHz
		39 MHz crystal	—	24.4	—	µA/MHz
		38 MHz HFRCO	—	19.0	—	µA/MHz
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	256 kB RAM and full Radio RAM retention, RTC running from LFXO[1]	—	3.1	—	µA
		256 kB RAM and full Radio RAM retention, RTC running from LFRCO[1]	—	3.1	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from LFXO[1]	—	1.3	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO[1]	—	1.3	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO in precision mode[1]	—	1.9	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	256 kB RAM and full Radio RAM retention, RTC running from ULFRCO[1]	—	2.9	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from ULFRCO[1]	—	1.1	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.31	—	µA
		BURTC with LFXO	—	0.64	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	467	—	µA

Note:
1. CPU cache retained, EM0/1 peripheral states retained

4.4 Radio Current Consumption with 3.0 V Supply

RF current consumption measured with MCU in EM1 and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VDD = VDDIO = 3.0 V, DC-DC in regulation. T_A = 25 °C.

Table 4.4. Radio Current Consumption with 3.0 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception, VSCALE1, EM1P	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	5.4	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	5.5	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	5.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	5.8	—	mA
Current consumption in receive mode, listening for packet, VSCALE1, EM1P	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	5.4	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	5.4	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	5.0	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	5.8	—	mA
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 10 dBm output power	—	23.4	—	mA

4.5 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: VDD = VDDIO = 3.0 V, DC-DC in regulation. RF center frequency 2.45 GHz. T_A = 25 °C.

Table 4.5. RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2402	—	2480	MHz
Maximum TX power	$POUT_{MAX}$	10 dBm	—	10.0	—	dBm
		0 dBm	—	-1.4	—	dBm
Minimum active TX power	$POUT_{MIN}$	10 dBm	—	-29.1	—	dBm
		0 dBm	—	-24.9	—	dBm
Output power step size	$POUT_{STEP}$	0 dBm	0.1	0.6	10	dB
		10 dBm, -5 dBm < Output power < 0 dBm	0.2	0.7	1.7	dB
		10 dBm, 0 dBm < Output power < 10 dBm	0.04	0.2	0.8	dB
Output power variation vs supply voltage variation, frequency = 2450 MHz	$POUT_{VAR\_V}$	10 dBm output power with VDD voltage swept from 1.8 V to 3.8 V	—	0.02	—	dB
		0 dBm output power with VDD voltage swept from 1.8 V to 3.8 V	—	0.06	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	$POUT_{VAR\_T}$	0 dBm, (-40 to +105 °C)	—	1.1	—	dB
Output power variation over the RF tuning frequency range	$POUT_{VAR\_F}$	10 dBm	—	0.6	—	dB
		0 dBm	—	0.07	—	dB

4.6 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: VDD = VDDIO = 3.0 V, DC-DC in regulation. RF center frequency 2.45 GHz. T_A = 25 °C.

Table 4.6. RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2402	—	2480	MHz

4.7 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: VDD = VDDIO = 3.0 V, DC-DC in regulation. RF center frequency 2.45 GHz. T_A = 25 °C.

Table 4.7. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-97	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-95.4	—	dBm
		With non-ideal signals[2 1]	—	-95.0	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	8.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 4 3 5]	—	-5.4	—	dB
		Interferer is reference signal at -1 MHz offset[1 4 3 5]	—	-5.3	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 4 3 5]	—	-40.9	—	dB
		Interferer is reference signal at -2 MHz offset[1 4 3 5]	—	-39.7	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 4 3 5]	—	-45.5	—	dB
		Interferer is reference signal at -3 MHz offset[1 4 3 5]	—	-45.7	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-23.3	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5]	—	-40.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5]	—	-5.4	—	dB
Intermodulation performance	IM	n = 3 (see note[6])	—	-17.3	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -67 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.8 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: VDD = VDDIO = 3.0 V, DC-DC in regulation. RF center frequency 2.45 GHz. T_A = 25 °C.

Table 4.8. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-94.3	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-92.7	—	dBm
		With non-ideal signals[2 1]	—	-92.5	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	8.6	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1 4 3 5]	—	-5.3	—	dB
		Interferer is reference signal at -2 MHz offset[1 4 3 5]	—	-5.8	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1 4 3 5]	—	-42.2	—	dB
		Interferer is reference signal at -4 MHz offset[1 4 3 5]	—	-44.2	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1 4 3 5]	—	-48.1	—	dB
		Interferer is reference signal at -6 MHz offset[1 4 3 5]	—	-50.2	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-22.8	—	dB
Selectivity to image frequency ± 2 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1 5]	—	-42.2	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1 5]	—	-5.3	—	dB
Intermodulation performance	IM	n = 3 (see note[6])	—	-18.3	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -64 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.9 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: VDD = VDDIO = 3.0 V, DC-DC in regulation. RF center frequency 2.45 GHz. T_A = 25 °C.

Table 4.9. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-100.7	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-99.4	—	dBm
		With non-ideal signals[2 1]	—	-98.4	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	2.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 4 3 5]	—	-7.1	—	dB
		Interferer is reference signal at -1 MHz offset[1 4 3 5]	—	-7.4	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 4 3 5]	—	-46.8	—	dB
		Interferer is reference signal at -2 MHz offset[1 4 3 5]	—	-49.7	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 4 3 5]	—	-49.4	—	dB
		Interferer is reference signal at -3 MHz offset[1 4 3 5]	—	-54.5	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-49	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5]	—	-49.4	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5]	—	-46.8	—	dB

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -72 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.

4.10 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: VDD = VDDIO = 3.0 V, DC-DC in regulation. RF center frequency 2.45 GHz. T_A = 25 °C.

Table 4.10. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-105.1	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-104.7	—	dBm
		With non-ideal signals[2 1]	—	-104.3	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	0.9	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 4 3 5]	—	-12.4	—	dB
		Interferer is reference signal at -1 MHz offset[1 4 3 5]	—	-12.8	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 4 3 5]	—	-52.6	—	dB
		Interferer is reference signal at -2 MHz offset[1 4 3 5]	—	-55.5	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 4 3 5]	—	-53.8	—	dB
		Interferer is reference signal at -3 MHz offset[1 4 3 5]	—	-60	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-53	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5]	—	-53.8	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5]	—	-52.6	—	dB

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -79 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.

4.11 High-Frequency Crystal

Table 4.11. High-Frequency Crystal

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXTAL}		—	39	—	MHz
Initial calibrated accuracy	ACC_{HFXTAL}		-5	—	+5	ppm
Temperature drift	$DRIFT_{HFXTAL}$	Across specified temperature range	-30	—	30	ppm

4.12 Low Frequency Crystal Oscillator

Table 4.12. Low Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kΩ
		GAIN = 1 to 3	—	—	100	kΩ
Supported range of crystal load capacitance [1]	C_{L_LFXO}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note[2])	10	—	12.5	pF
		GAIN = 3 (see note[2])	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kΩ, C_L = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	—	294	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 kΩ, C_L = 7 pF, GAIN[3] = 1, AGC[4] = 1	—	52	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE = 0	—	5.2	—	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	26.2	—	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.13 Precision Low Frequency RC Oscillator (LFRCO)

Table 4.13. Precision Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}	Normal mode	-3	—	3	%
		Precision mode[1], across operating temperature range[2]	-500	—	500	ppm
Startup time	$t_{STARTUP}$	Normal mode	—	204	—	µs
		Precision mode[1]	—	11.7	—	ms
Current consumption	I_{LFRCO}	Normal mode	—	189.9	—	nA
		Precision mode[1], T = stable at 25 °C [3]	—	649.8	—	nA

Note:

1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ± 40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.14 GPIO Pins

Table 4.14. GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, VDD = VDDIO = 3.0 V	—	2.5	—	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3 * VDDIO	V
		RESETn	—	—	0.3 * DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7 * VDDIO	—	—	V
		RESETn	0.7 * DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05 * VDDIO	—	—	V
		RESETn	0.05 * DVDD	—	—	V
Output high voltage	V_{OH}	Sourcing 20 mA, VDDIO = 3.0 V	0.8 * VDDIO	—	—	V
Output low voltage	V_{OL}	Sinking 20 mA, VDDIO = 3.0 V	—	—	0.2 * VDDIO	V
GPIO rise time	T_{GPIO_RISE}	VDDIO = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
GPIO fall time	T_{GPIO_FALL}	VDDIO = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to VDDIO: MODEn = DISABLE DOUT=1. Pull-down to GND: MODEn = WIREDORPULLDOWN DOUT = 0.	35	44	55	kΩ
		RESETn pin. Pull-up to DVDD	35	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns

Note:

1. GPIO input thresholds are proportional to the VDDIO pin. RESETn input thresholds are proportional to the internal DVDD supply, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.
2. GPIO pull-ups connect to VDDIO supply, pull-downs connect to GND. RESETn pull-up connects to internal DVDD supply, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.

4.15 Microcontroller Peripherals

The set of peripherals available in BGM240S modules includes:

- 12-bit 1 Msps ADC
- Analog Comparators
- 16-bit and 32-bit Timers/Counters
- 24-bit Low Energy Timer for waveform generation
- 32-bit Real Time Counter
- USART (UART/SPI/SmartCards/IrDA/I2S)
- I^2C peripheral interfaces
- 12 Channel Peripheral Reflex System

Details on their electrical performance can be found in the relevant portions of Section 4 of the EFR32BG24 SoC data sheet.

To learn which GPIO ports provide access to every peripheral, consult the 6.4 Digital Peripheral Connectivity and 6.3 Analog Peripheral Connectivity tables.

4.16 Typical Performance Curves

Typical BGM240S radiation patterns for the built-in antenna under optimal operating conditions are plotted in the figures that follow. Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna.

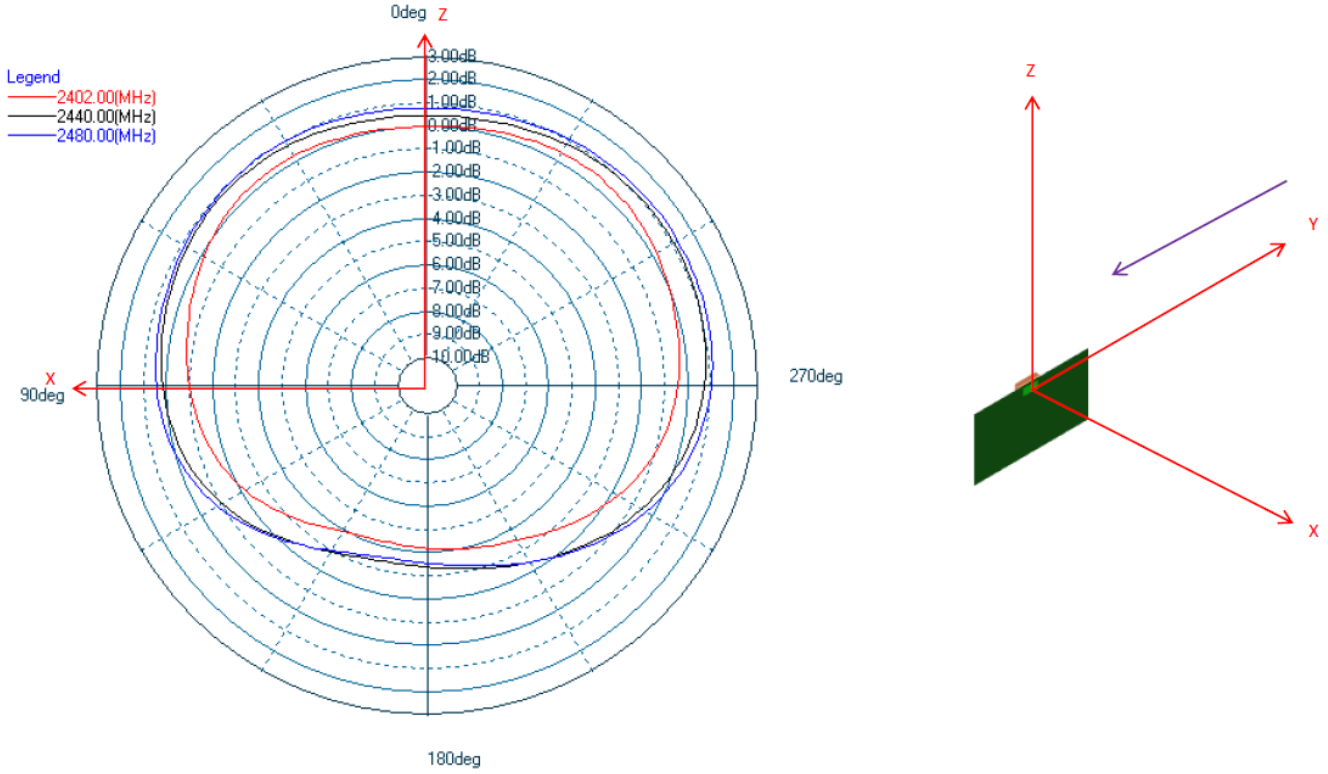


Figure 4.1. Typical 2D Antenna Radiation Patterns - Phi 0^{o} (Side View) Gain (dBi)

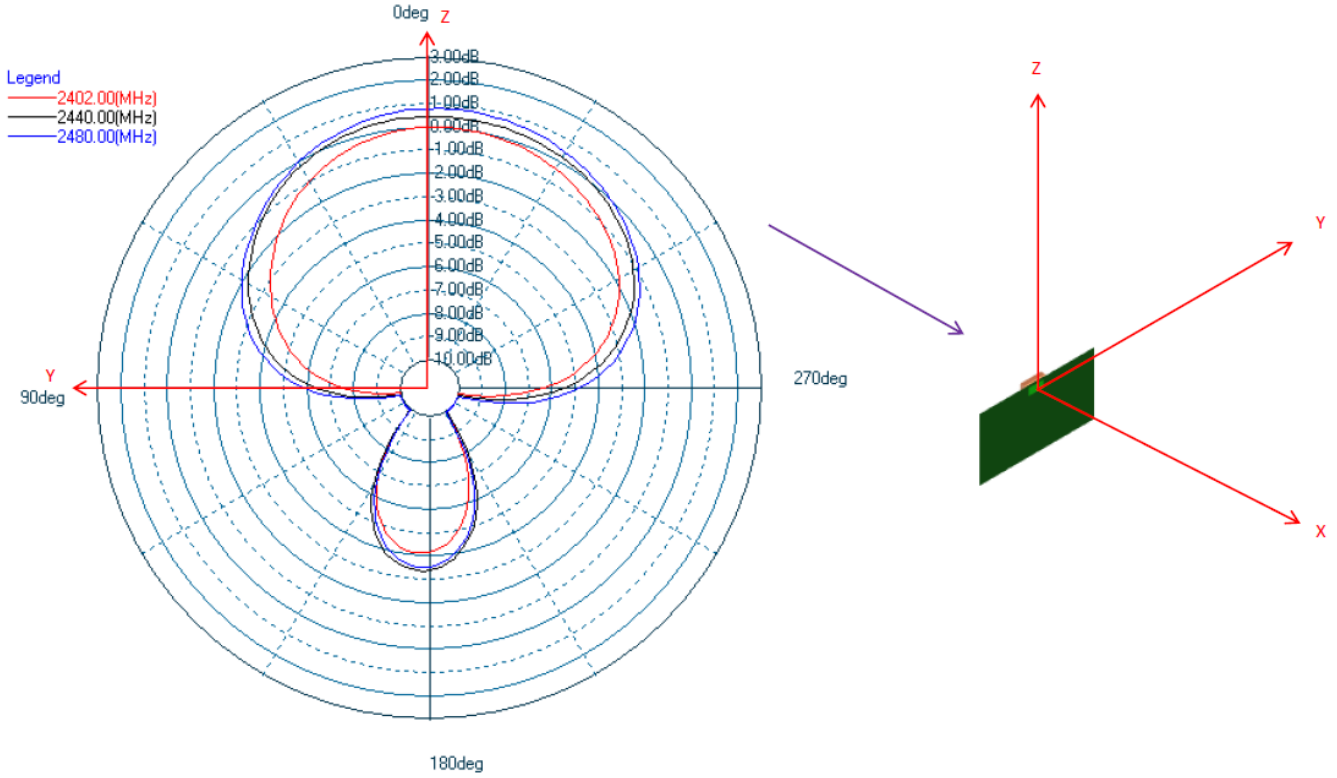


Figure 4.2. Typical 2D Antenna Radiation Patterns - Phi 90° (Top View) Gain (dBi)

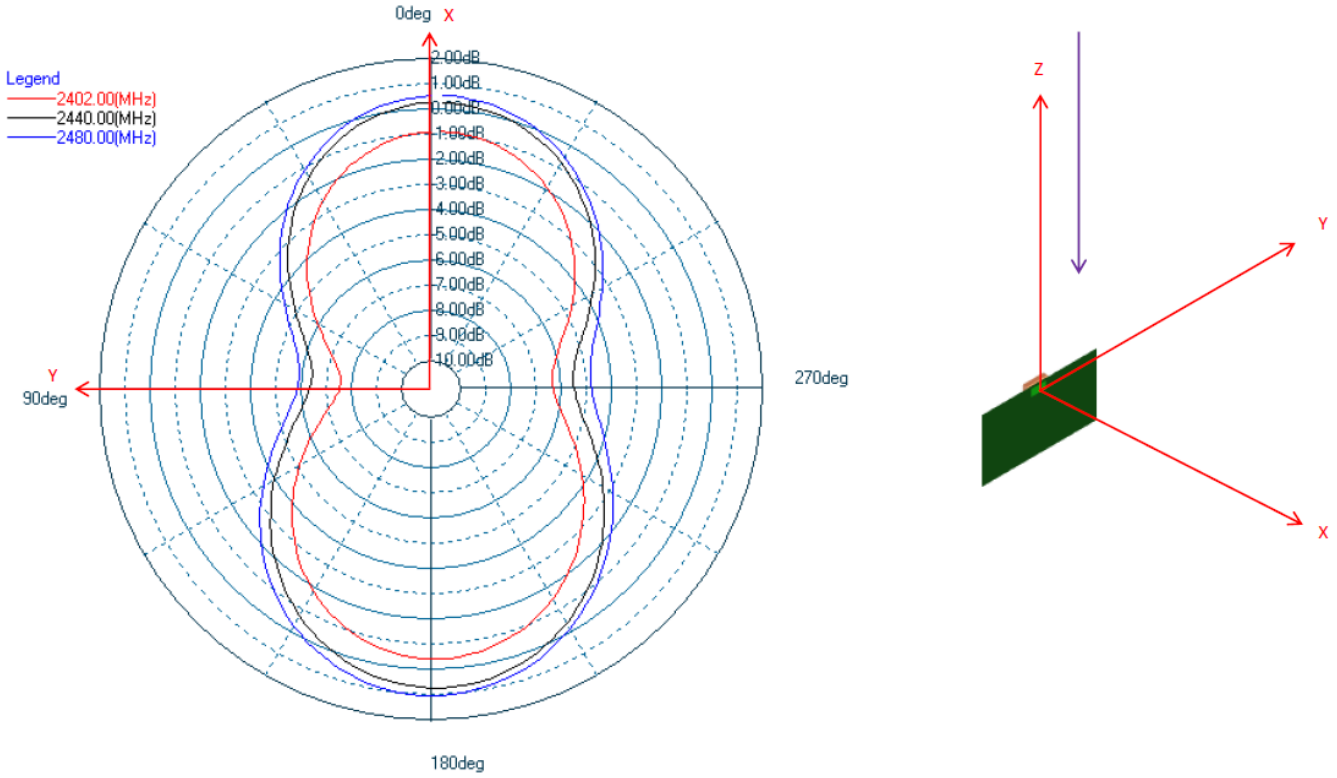


Figure 4.3. Typical 2D Antenna Radiation Patterns - Theta 90° (Front View) Gain (dBi)

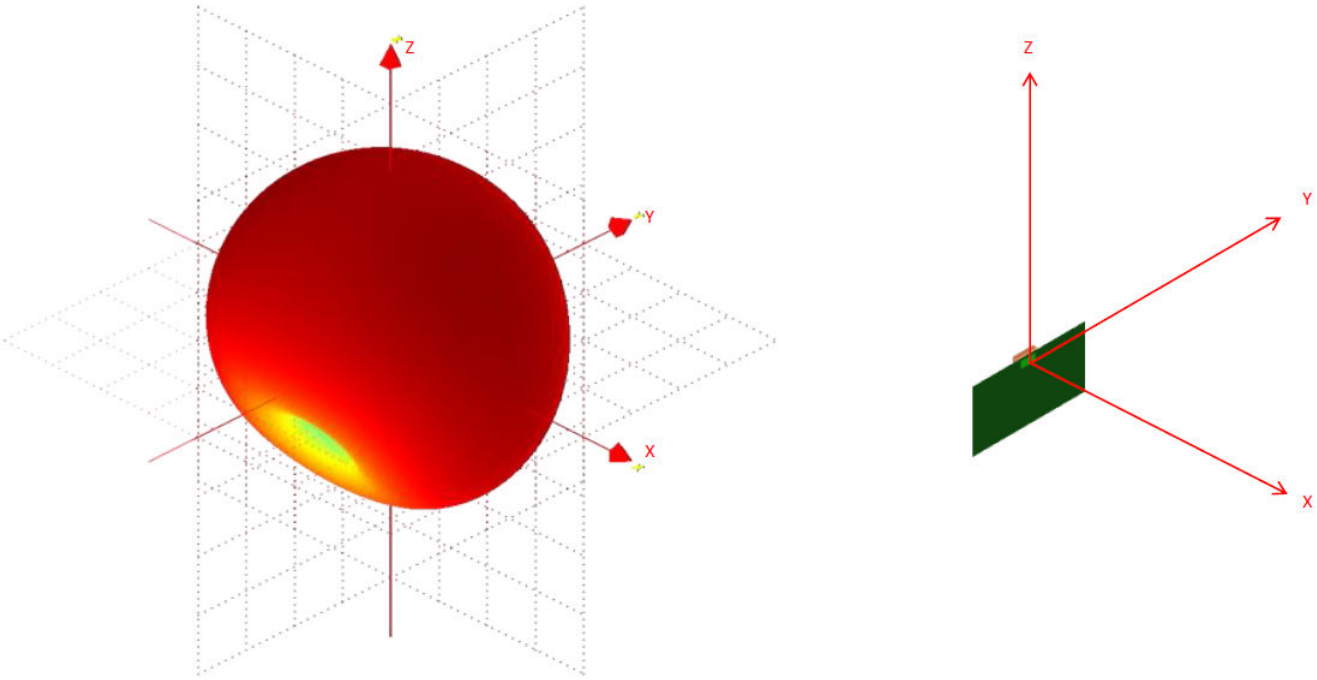


Figure 4.4. 3D Radiation Pattern at 2440MHz

5. Reference Diagrams

5.1 Network Co-Processor (NCP) Application with UART Host

The BGM240S can be controlled via the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug interface, and host interface connections are shown in the figure below. For more details, see *AN958: Debugging and Programming Interfaces for Custom Designs*.

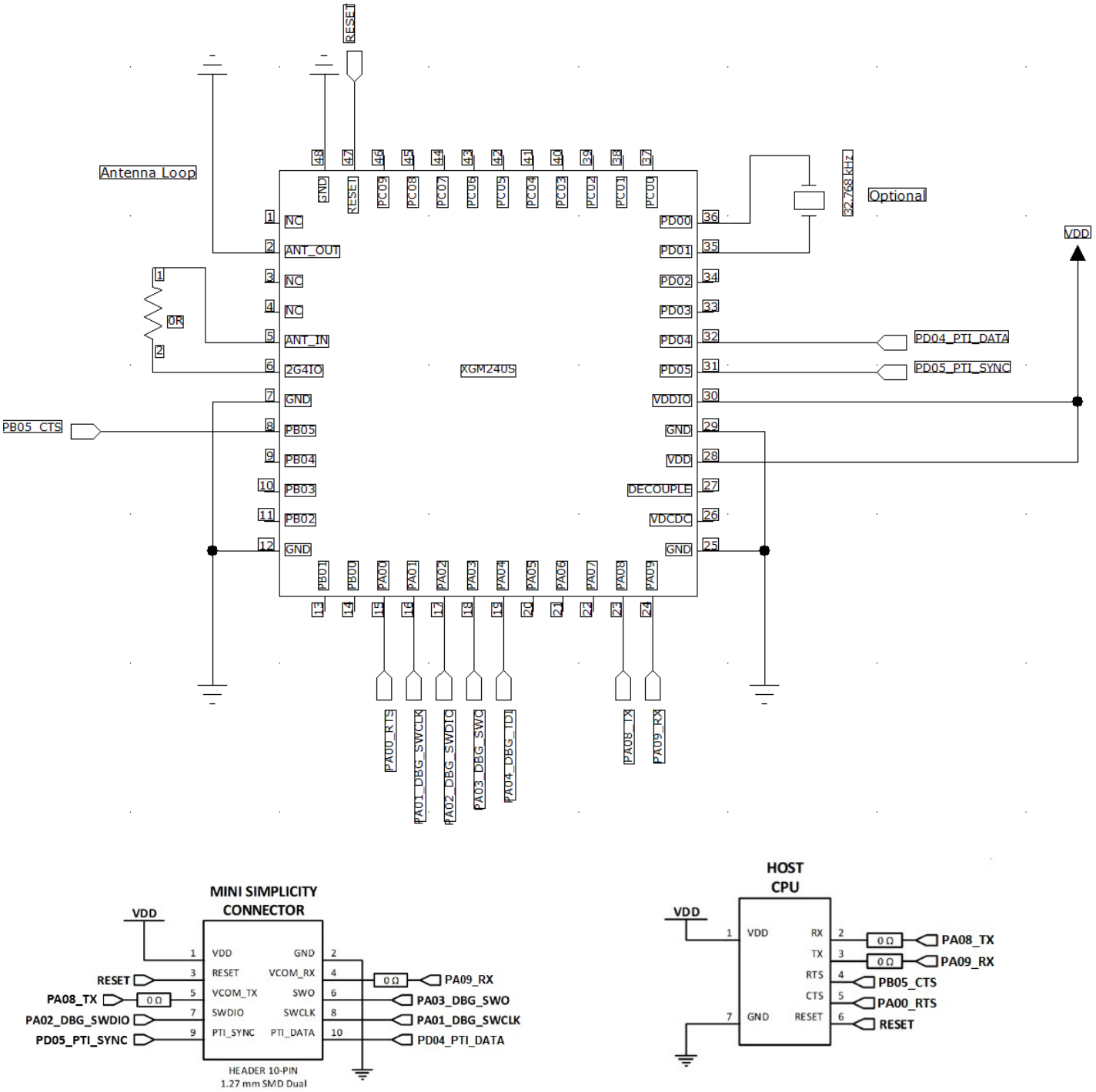


Figure 5.1. UART NCP Configuration

5.2 SoC Application

The BGM240S can be used in a stand-alone SoC configuration without an external host processor. Typical power supply and programming/debug interface connections are shown in the figure below. For more details, see *AN958: Debugging and Programming Interfaces for Custom Designs*.

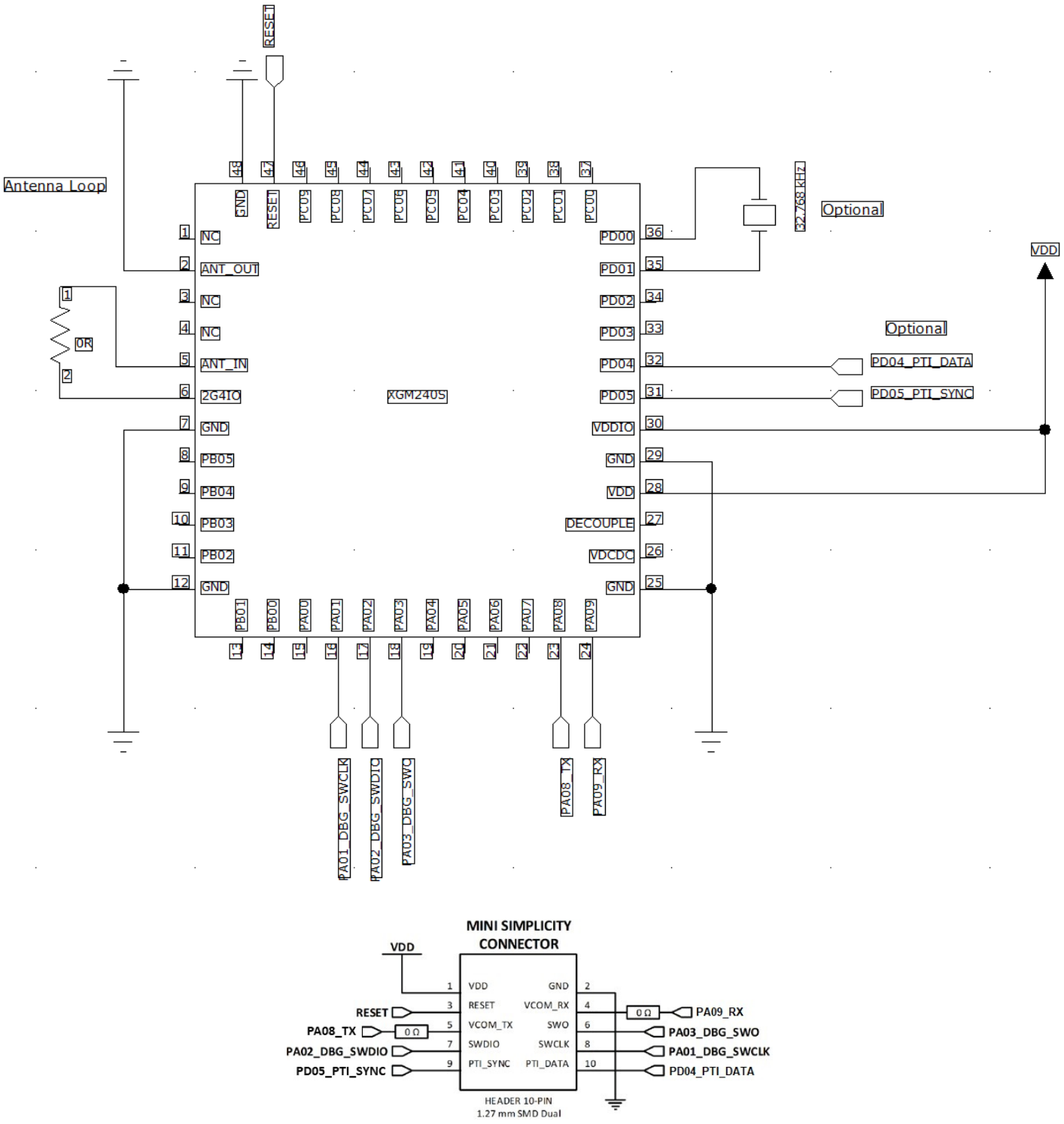


Figure 5.2. Stand-Alone SoC Configuration

6. Pin Definitions

6.1 Module Pinout

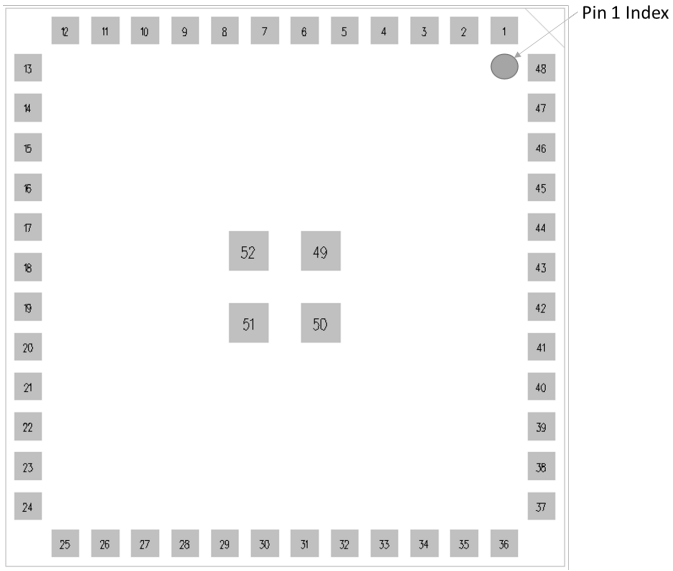


Figure 6.1. BGM240S Module Pinout (Top view)

The next table shows the BGM240S pinout and general descriptions for each pin. Refer to 6.2 Alternate Pin Functions, 6.3 Analog Peripheral Connectivity, and 6.4 Digital Peripheral Connectivity for details on functions and peripherals supported by each GPIO pin.

Table 6.1. BGM240S Module Pin Definitions

Pin Name	No.	Description	Pin Name	No.	Description
DNC	1	Do not connect	GND	52	GROUND
ANT OUT	2	Integral Ant Out	GND	51	GROUND
DNC	3	Do not connect	GND	50	GROUND
DNC	4	Do not connect	GND	49	GROUND
ANT IN	5	Integral Ant In	GND	48	GROUND
2G4IO	6	RF IN/OUT	RESETn[1]	47	RESET
GND	7	GROUND	PC09	46	GPIO
PB05	8	GPIO	PC08	45	GPIO
PB04	9	GPIO	PC07	44	GPIO
PB03	10	GPIO	PC06	43	GPIO
PB02	11	GPIO	PC05	42	GPIO
GND	12	GROUND	PC04	41	GPIO
PB01	13	GPIO	PC03	40	GPIO
PB00	14	GPIO	PC02	39	GPIO
PA00	15	GPIO	PC01	38	GPIO
PA01	16	GPIO	PC00	37	GPIO
PA02	17	GPIO	PD00	36	GPIO

Pin Name	No.	Description	Pin Name	No.	Description
PA03	18	GPIO	PD01	35	GPIO
PA04	19	GPIO	PD02	34	GPIO
PA05	20	GPIO	PD03	33	GPIO
PA06	21	GPIO	PD04	32	GPIO
PA07	22	GPIO	PD05	31	GPIO
PA08	23	GPIO	VDDIO	30	IO power supply
PA09	24	GPIO	GND	29	GROUND
GND	25	GROUND	VDD	28	Power supply
VDCDC	26	Test pin (internal test usage)	DECOUPLE	27	Test pin (internal test usage)

Note:

1. The RESETn pin is pulled up to an internal DVDD supply. An external pull-up is not recommended. To apply an external reset source to this pin, it is, required to only drive this pin low during, reset, and let the internal pull-up ensure that reset is released. The RESETn pin can be left unconnected if no external reset switch or source is used.

6.2 Alternate Pin Functions

Some GPIOs support alternate functions like debugging, wake-up from EM4, external low frequency crystal access, etc. The following table shows both which module pins have alternate capabilities and the functions they support. Refer to the SoCs reference manual for more details.

Table 6.2. GPIO Alternate Functions Table

GPIO	Alternate Functions		
PA00	IADC0.VREFP		
PA01	GPIO.SWCLK		
PA02	GPIO.SWDIO		
PA03	GPIO.SWV GPIO.TDO GPIO.TRACEDATA0		
PA04	GPIO.TDI GPIO.TRACECLK		
PA05	GPIO.TRACEDATA1 GPIO.EM4WU0		
PA06	GPIO.TRACEDATA2		
PA07	GPIO.TRACEDATA3		
PB00	VDAC0.VDAC_CH0_MAIN_OUTPUT		
PB01	GPIO.EM4WU3	VDAC0.VDAC_CH1_MAIN_OUTPUT	
PB02	VDAC1.VDAC_CH0_MAIN_OUTPUT		
PB03	GPIO.EM4WU4	VDAC1.VDAC_CH1_MAIN_OUTPUT	
PC00	GPIO.EM4WU6		
PC01	GPIO.EFP_TX_SDA		
PC02	GPIO.EFP_TX_SCL		
PC05	GPIO.EFP_INT GPIO.EM4WU7		
PC07	GPIO.EM4WU8	GPIO.THMSW_EN	GPIO.THMSW_HALFSWITCH
PD00	LFXO.LFXTAL_O		
PD01	LFXO.LFXTAL_I LFXO.LF_EXTCLK		
PD02	GPIO.EM4WU9		

6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used positive inputs are restricted to the EVEN pins and negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is available on all pins. See the SoC's Reference Manual for more details on the ABUS and analog peripherals.

Table 6.3. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACMP1	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC0	VDAC_CH0_ABUS_OUT-PUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	VDAC_CH1_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC1	VDAC_CH0_ABUS_OUT-PUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	VDAC_CH1_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIOs. The table below indicates which peripherals are available on each GPIO port.

Table 6.4. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
ACMP1.DIGOUT	Available	Available	Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUSART0.CS	Available	Available		
EUSART0.CTS	Available	Available		
EUSART0.RTS	Available	Available		
EUSART0.RX	Available	Available		
EUSART0.SCLK	Available	Available		
EUSART0.TX	Available	Available		
EUSART1.CS	Available	Available	Available	Available
EUSART1.CTS	Available	Available	Available	Available
EUSART1.RTS	Available	Available	Available	Available
EUSART1.RX	Available	Available	Available	Available
EUSART1.SCLK	Available	Available	Available	Available
EUSART1.TX	Available	Available	Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
HFXO0.BUFOUT_REQ_IN_ASYNC	Available	Available		
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
KEYSCAN.COL_OUT_0	Available	Available	Available	Available
KEYSCAN.COL_OUT_1	Available	Available	Available	Available
KEYSCAN.COL_OUT_2	Available	Available	Available	Available
KEYSCAN.COL_OUT_3	Available	Available	Available	Available
KEYSCAN.COL_OUT_4	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
KEYSCAN.COL_OUT_5	Available	Available	Available	Available
KEYSCAN.COL_OUT_6	Available	Available	Available	Available
KEYSCAN.COL_OUT_7	Available	Available	Available	Available
KEYSCAN.ROW_SENSE_0	Available	Available		
KEYSCAN.ROW_SENSE_1	Available	Available		
KEYSCAN.ROW_SENSE_2	Available	Available		
KEYSCAN.ROW_SENSE_3	Available	Available		
KEYSCAN.ROW_SENSE_4	Available	Available		
KEYSCAN.ROW_SENSE_5	Available	Available		
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PCNT0.S0IN	Available	Available		
PCNT0.S1IN	Available	Available		
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH12	Available	Available		
PRS.ASYNCH13	Available	Available		
PRS.ASYNCH14	Available	Available		
PRS.ASYNCH15	Available	Available		
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
RAC.LNAEN	Available	Available	Available	Available
RAC.PAEN	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available

7. Design Guidelines

7.1 Layout and Placement

For optimal performance of the BGM240S the following guidelines are recommended:

- Place the module 1.50 mm from the edge of the copper “keep-in” area at the middle of the long edge of the application PCB, as illustrated in Figure 7.1 on page 37.
- Copy the exact design from Figure 7.2 on page 38 with the values for coordinates A to L given in Table 7.1 Antenna Polygon Coordinates, Referenced to Center of BGM240S on page 38.
- Make a cutout in all lower layers aligned with the right edge and the bottom edge of the integral loop antenna as indicated by the red box in Figure 7.3 Antenna Clearance in Inner and Bottom Layers on page 39.
- Connect all ground pads directly to a solid ground plane in the top layer.
- Connect 2G4IO to ANT_IN through a 0-ohm resistor.
- The 0-ohm gives the ability to test conducted and to evaluate the antenna impedance in the design.
- Place ground vias as close to the ground pads of the BGM240S as possible.
- Place ground vias along the antenna loop right and bottom side.
- Place ground vias along the edges of the application board.
- Do not place plastic or any other dielectric material in contact with the antenna.
- A minimum clearance of 0.5 mm is advised.
- Solder mask, conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region.
- Proper module placement and electrical connection should be ensured by measuring radiated output power from antenna.
- Impedance of the antenna can be verified by measuring S11 at ANT_IN pin that is corresponding antenna specification.
- With an external antenna, use a 50Ω trace to connect RF signal to the antenna, as it is illustrated in Figure 7.4 Recommended Layout for BGM240S (External Antenna) on page 39

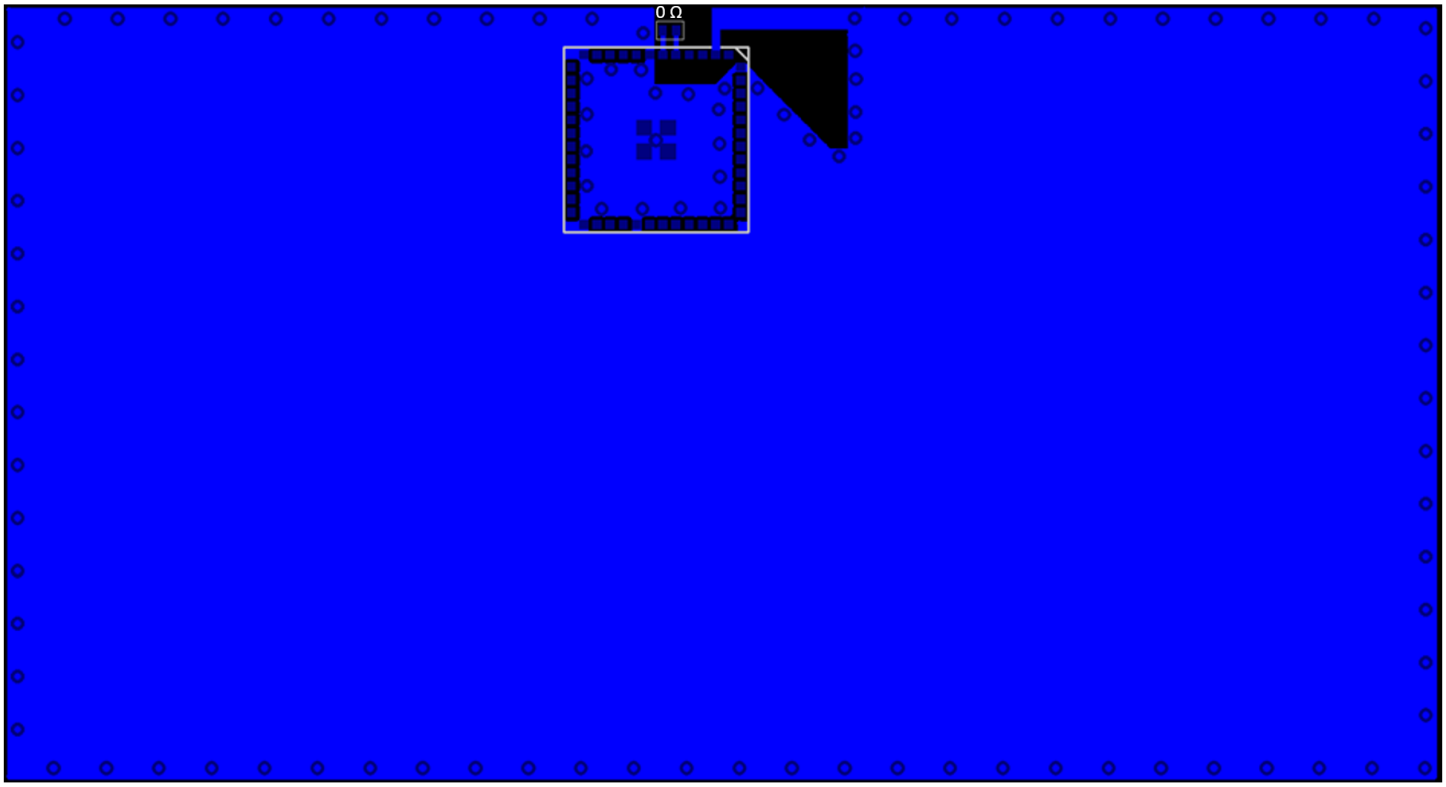


Figure 7.1. Recommended Layout for BGM240S (Integral Antenna)

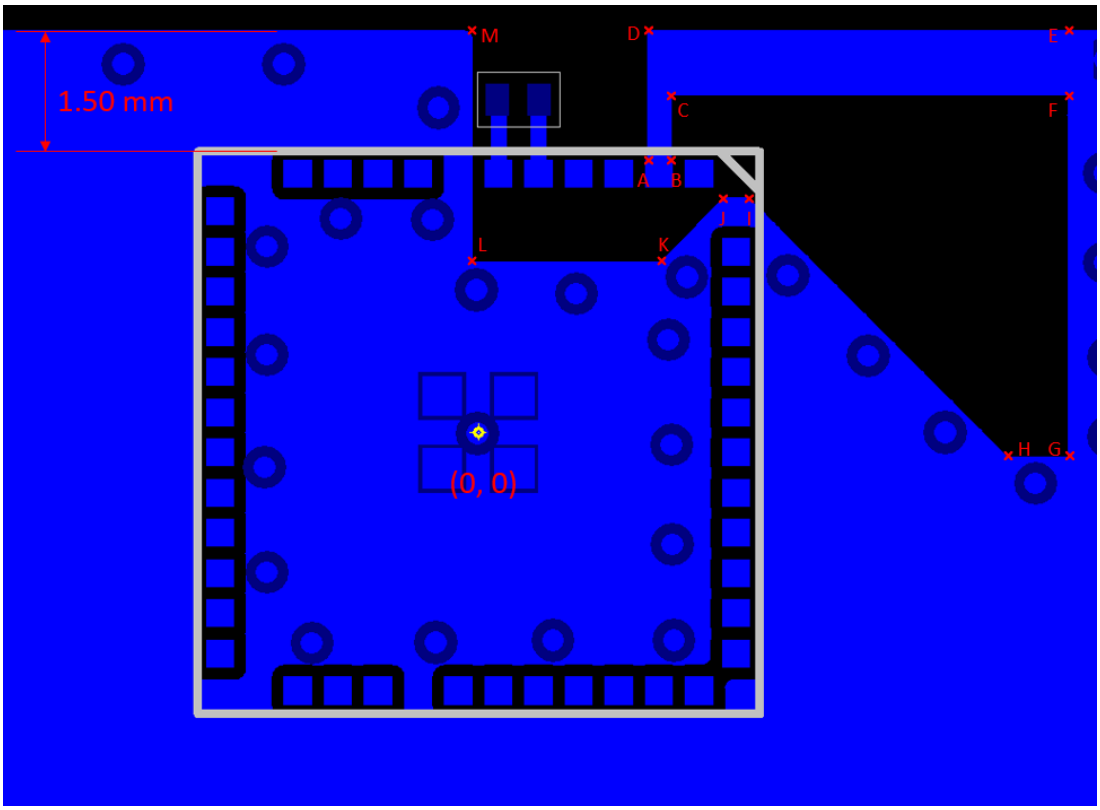


Figure 7.2. TOP Layer Antenna Layout With Coordinates

Table 7.1. Antenna Polygon Coordinates, Referenced to Center of BGM240S

Point	Coordinate
A	(2.10, 3.30)
B	(2.40, 3.30
C	(2.40, 4.20)
D	(2.10, 5.00)
E	(7.35, 5.00)
F	(7.35, 4.20)
G	(7.35, -0.03)
H	(6.59, -0.30)
I	(3.39, 2.90)
J	(3.05, 2.90)
K	(2.27, 2.13)
L	(-0.08, 2.13)
M	(-0.08, 5.00)

Tolerance for the coordinates is +/- 0.05 mm.

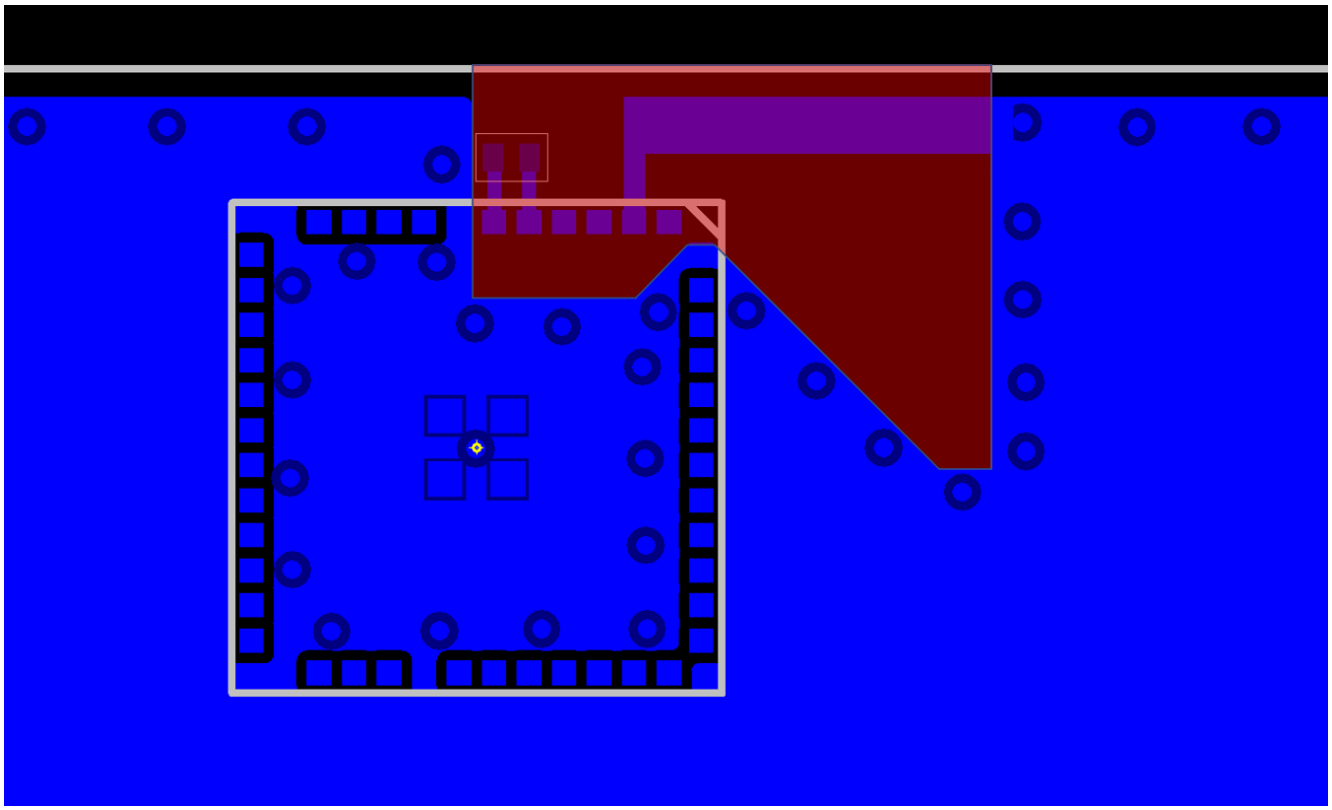


Figure 7.3. Antenna Clearance in Inner and Bottom Layers

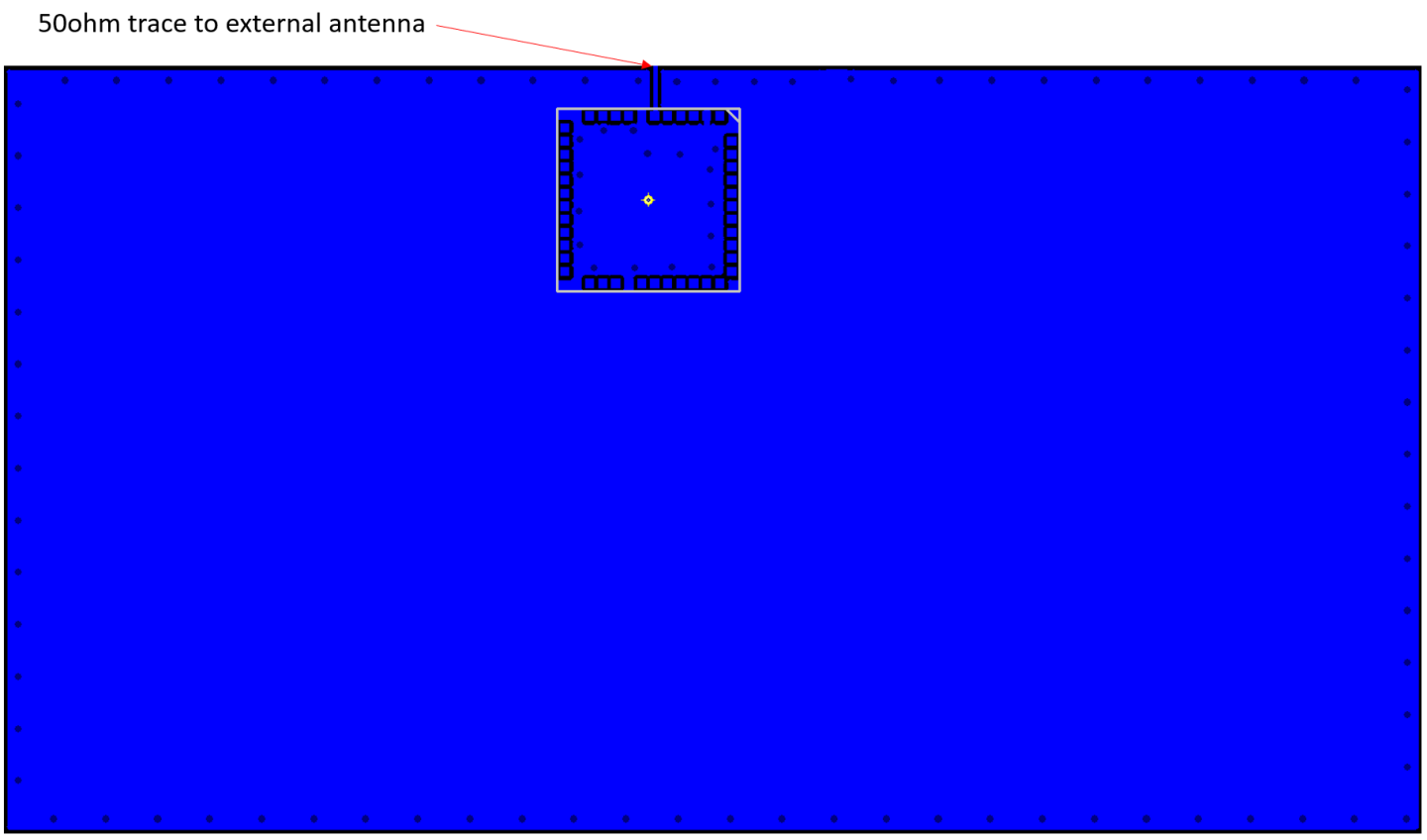


Figure 7.4. Recommended Layout for BGM240S (External Antenna)

7.2 Best Design Practices

The design of a good RF system relies on thoughtful placement and routing of the RF signals. The following guidelines are recommended:

- Place the BGM240S and antenna close to the center of the longest edge of the application board.
- Do not place any circuitry between the board edge and the antenna.
- Make sure to tie all GND planes in the application board together with as many vias as can be fitted.
- Generally ground planes are recommended in all areas of the application board except in the antenna keep-out area shown in Figure 7.3 Antenna Clearance in Inner and Bottom Layers on page 39.
- Open-ended stubs of copper in the outer layer ground planes must be removed if they are more than 5 mm long to avoid radiation of spurious emissions.
- The width of the GND plane to the sides of the BGM240S will impact the efficiency of the on-board integral loop antenna.
- To achieve optimal performance, a GND plane width of 55 mm is recommended as seen on Figure 7.5 Illustration of Recommended Board Width on page 40.
- See 4.16.1 Antenna Typical Characteristics for reference. Figure 7.6 Non-Recommended Layout Examples on page 41 illustrates layout scenarios that will lead to severely degraded RF performance for the application board.

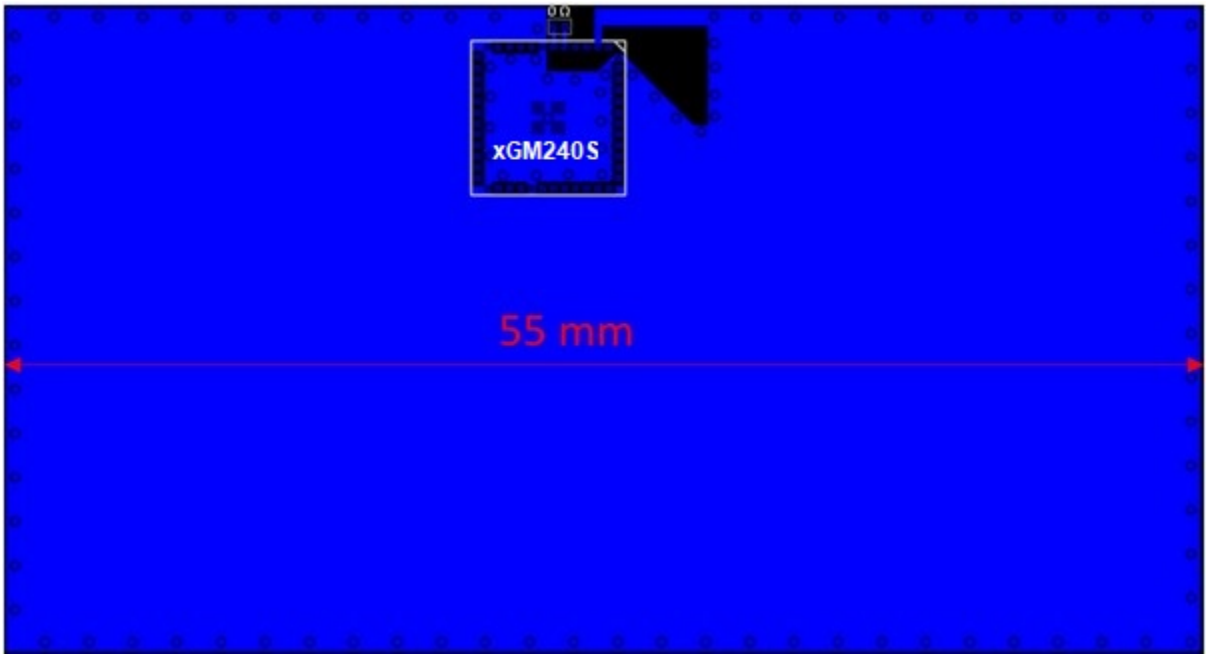


Figure 7.5. Illustration of Recommended Board Width

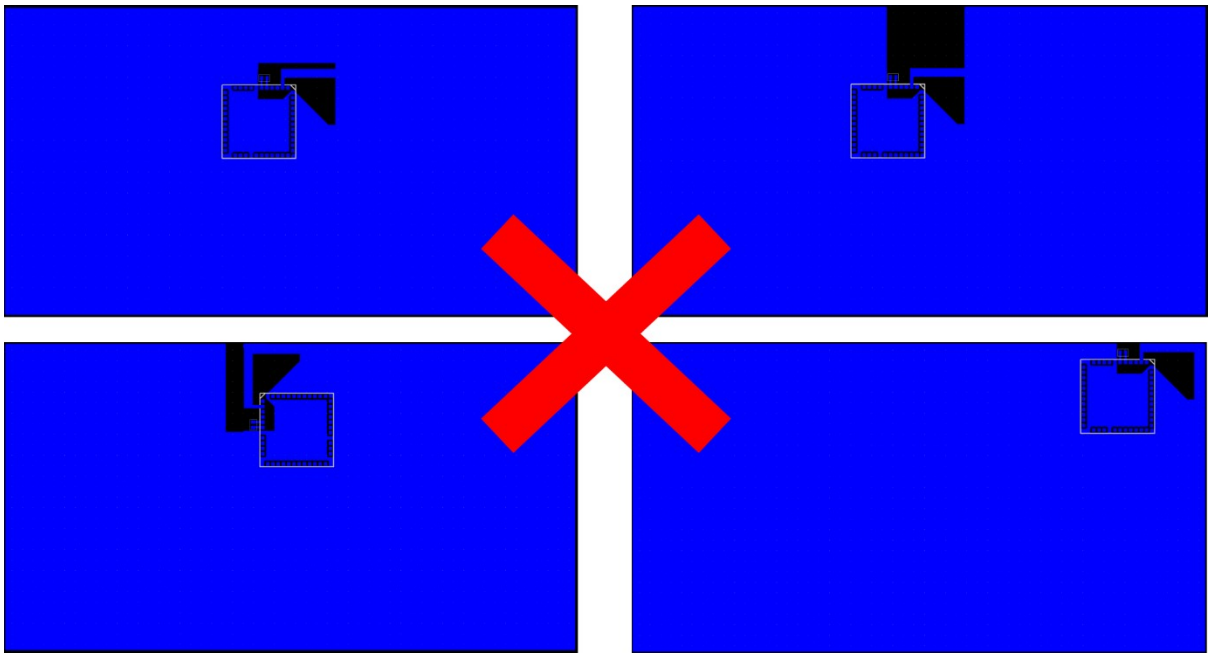


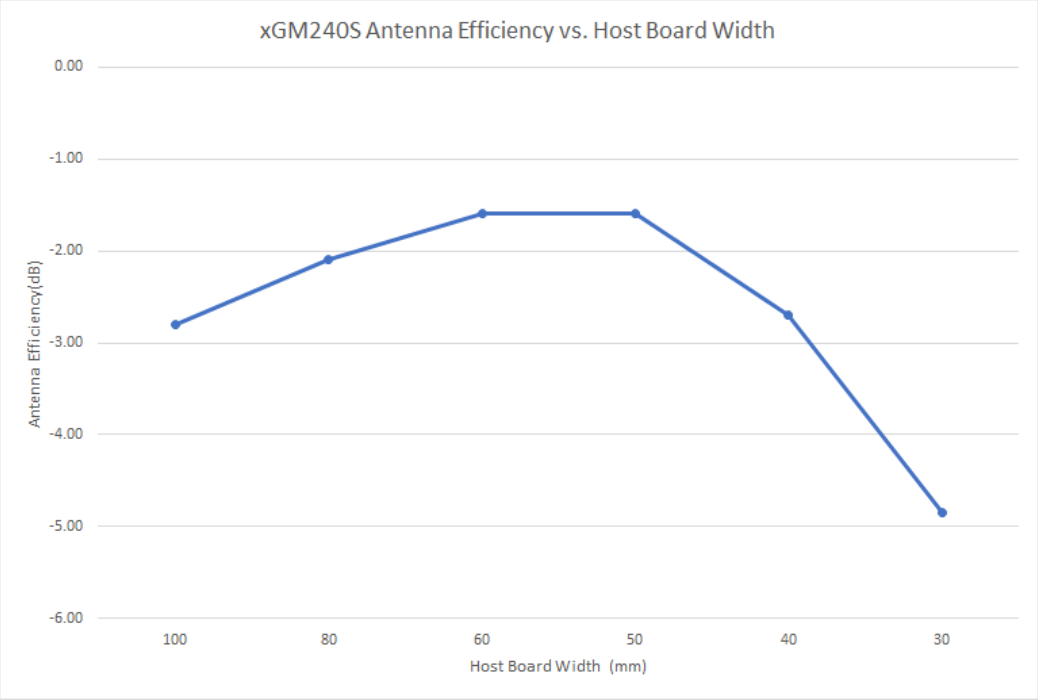
Figure 7.6. Non-Recommended Layout Examples

7.3 Radio Performance vs. Carrier Board Size

As with most applications, the carrier board size is determined by the overall form factor or size of the additional circuitry. The recommended carrier board width of 55 mm is thus not always possible in the end-application. If another form factor is required, the antenna performance of the integrated antenna will likely be compromised, but it may still be sufficiently good for providing the required link quality and range of the end-application. As can be seen in Figure 7.7 on page 42, the best performance is achieved for a carrier board size of 55 mm x 30, with relatively constant performance for larger boards and rapidly declining performance for smaller boards.

WARNING: Any antenna tuning, and/or change of the loop dimensions, is likely to invalidate a modular certification, unless it is done to compensate for the degradation caused by a host board deviating in size from the manufacturer's best-case reference. Separate guidance might be provided by the manufacturer to address this particular kind of degradation, in which case a Permissive Change to the modular approval might not even become necessary: however, since this is evaluated on a case-by-case basis, please consult your certification house on the best approach.

Figure 7.7. Efficiency of the Integrated Antenna as Function of the Carrier Board Size for BGM240S



7.4 Impact of Human Body and Other Materials in Close Proximity

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

Avoid placing plastic or any other dielectric material in close proximity to the antenna. Conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region, but this will also negatively impact antenna efficiency and reduce range.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

7.5 Reset

The BGM240S can be reset by pulling the RESET line low, by the internal watchdog timer, or by software command.

The reset state does not provide power saving functionality and it is not recommended as a means to conserve power.

7.6 Debug

See *AN958: Debugging and Programming Interfaces for Custom Designs*.

The BGM240S supports hardware debugging via 4-pin JTAG or 2-pin serial-wire debug (SWD) interfaces. It is recommended to expose the debug pins in your own hardware design for firmware update and debug purposes. The table below lists the required pins for JTAG and SWD debug interfacing, which are also presented in Section 6.2 Alternate Pin Functions.

If JTAG interfacing is enabled, the module must be power cycled to return to a SWD debug configuration if necessary.

Table 7.2. Debug Pins

Pin Name	JTAG Signal	SWD Signal	Comments
PA04	TDI	N/A	This pin is disabled after reset. Once enabled the pin has a built-in pull-up.
PA03	TDO	N/A	This pin is disabled after reset.
PA02	TMS	SWDIO	Pin is enabled after reset and has a built-in pull-up.
PA01	TCK	SWCLK	Pin is enabled after reset and has a built-in pull-down.

7.7 Packet Trace Interface (PTI)

The BGM240S integrates a true PHY-level packet trace interface (PTI) peripheral that can capture packets non-intrusively to monitor and log device and network traffic without burdening processing resources in the module's SoC. The PTI generates two output signals that can serve as a powerful debugging tool, especially in conjunction with other hardware and software development tools available from Silicon Labs. The PTI_DATA and PTI_FRAME signals can be accessed through any GPIO on ports C and D (see FRC.DOUT and FRC.DFRAME peripheral resources in Section 6. Pin Definitions.

8. Package Specifications

8.1 Package Outline

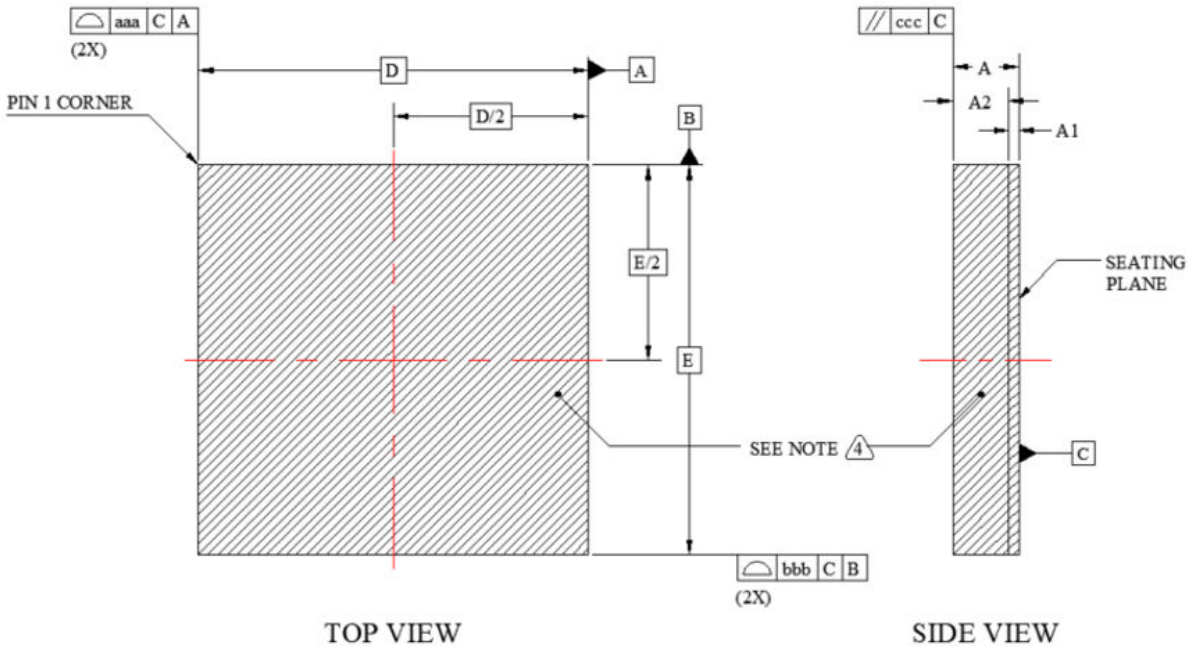


Figure 8.1. Top and Side Views

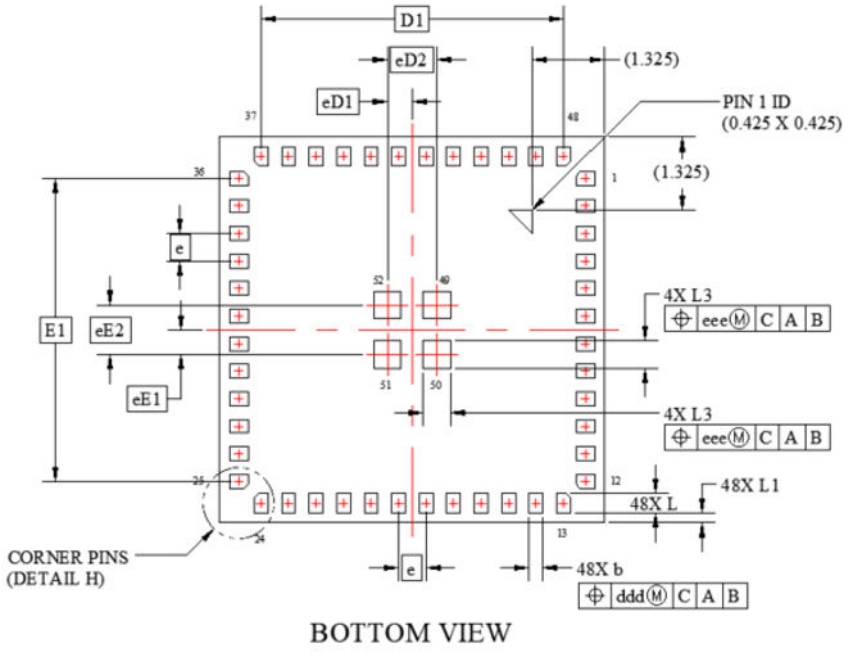


Figure 8.2. Bottom View

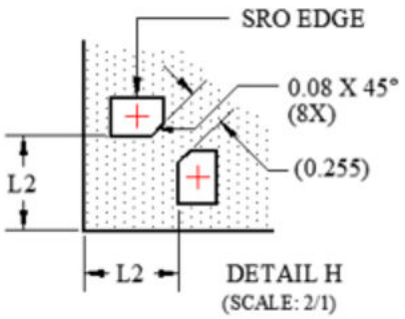


Figure 8.3. Bottom View about Package Corner

Table 8.1. QFN40 Package Dimensions

Dimension	Min	Typ	Max
A	1.080	1.180	1.280
A1	0.140	0.180	0.220
A2	0.950	1.000	1.050
b	0.200	0.250	0.300
D	7.000 BSC		
D1	5.5000 BSC		
e	0.500 BSC		
E	7.000 BSC		
E1	5.500 BSC		
L	0.300	0.350	0.400
L1	0.125	0.175	0.225
L2	0.575	0.625	0.675
L3	0.450	0.500	0.550
eD1	0.450 BSC		
eD2	0.900 BSC		
eE1	0.450 BSC		
eE2	0.900 BSC		
aaa	0.100		
bbb	0.100		
ccc	0.100		
ddd	0.100		
eee	0.100		

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. The dimensions in parenthesis are reference.
3. Hatching lines indicate package shielding area

4. Unless otherwise specified, Decimal tolerances are:
   - X.X = +/- 0.1
   - X.XX = +/- 0.05
   - X.XXX = +/- 0.03
5. Unless otherwise specified, Angular tolerances are:
   - +/- 0.1 (in Deg)

8.2 PCB Land Pattern

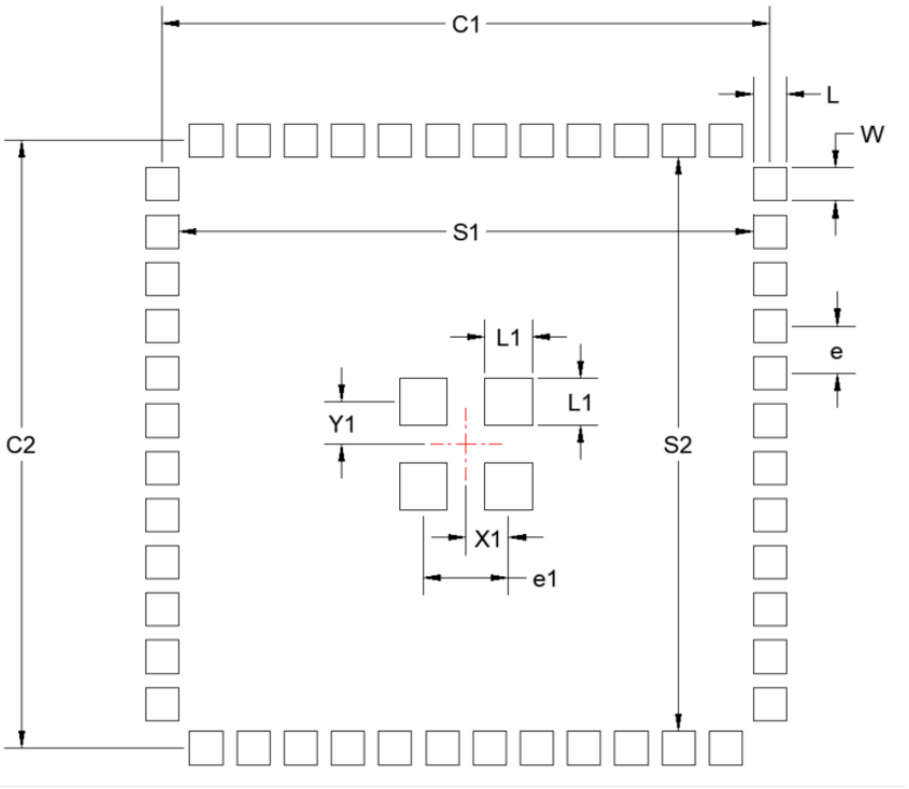


Figure 8.4. Recommended Land Pattern for Modules with a Built-in Antenna

Table 8.2. PCB Land Pattern Dimensions

Dimension	Typ
C1	6.43
C2	6.43
W	0.35
L	0.35
e	0.5
L1	0.50
X1	0.45
Y1	0.45
S1	6.08
S2	6.08
e1	0.90

Dimension	Typ

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
5. All pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60um minimum, all the way around the pad.
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
11. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

8.3 Package Marking

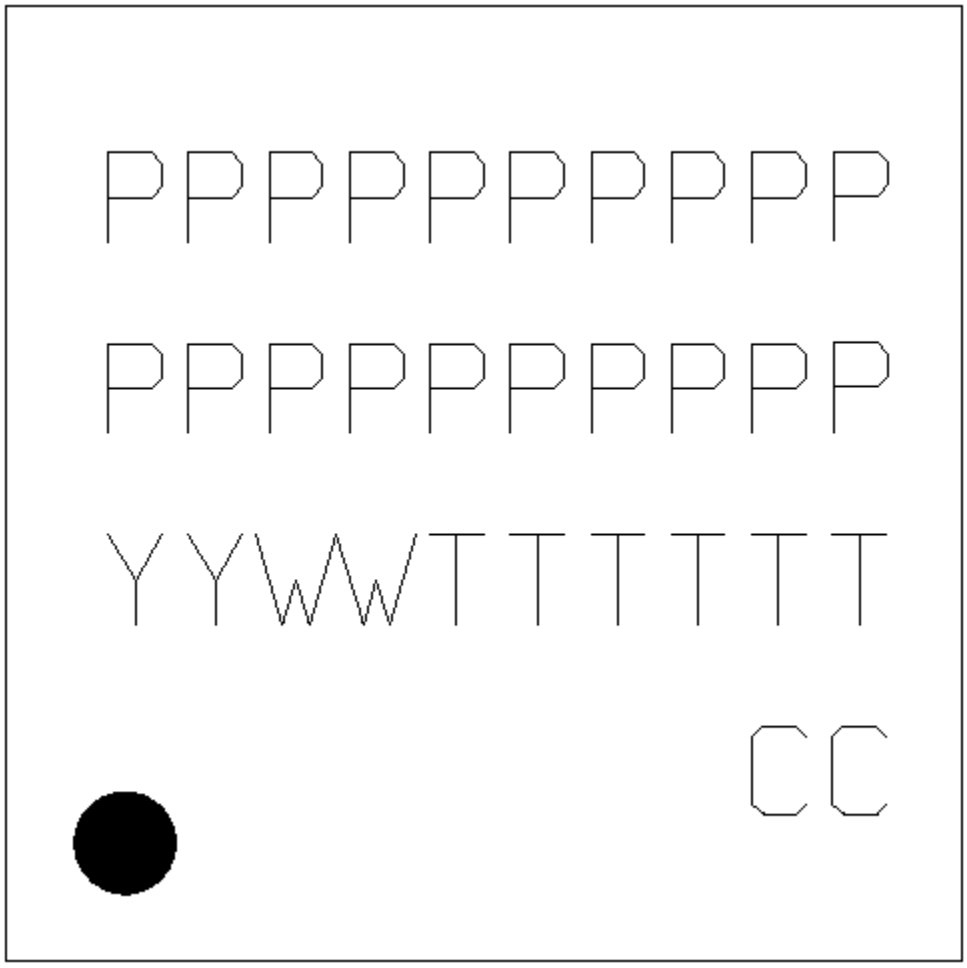


Figure 8.5. BGM240S Top Marking

Table 8.3. Top Marking Definition

OPN	Line 1 Marking	Line 2 Marking	Line 3 Marking	Line 4 Marking
BGM240SA22VNA2	BGM240S22A	SA22VNA2	See note 1	See note 2
BGM240SA22VNA2R	BGM240S22A	SA22VNA2	See note 1	See note 2
BGM240SB22VNA2	BGM240S22A	SB22VNA2	See note 1	See note 2
BGM240SB22VNA2R	BGM240S22A	SB22VNA2	See note 1	See note 2

Note:

1. YY = Year. WW = Work Week, TTTTTTT = Trace Code
2. Country of Origin ISO Code Abbreviation to be marked as specified in mark instructions of PO.

9. Soldering Recommendations

It is recommended that final PCB assembly of the BGM240S follows the industry standard as identified by the Institute for Printed Circuits (IPC). This product is assembled in compliance with the J-STD-001 requirements and the guidelines of IPC-AJ-820. Surface mounting of this product by the end user is recommended to follow IPC-A-610 to meet or exceed class 2 requirements.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

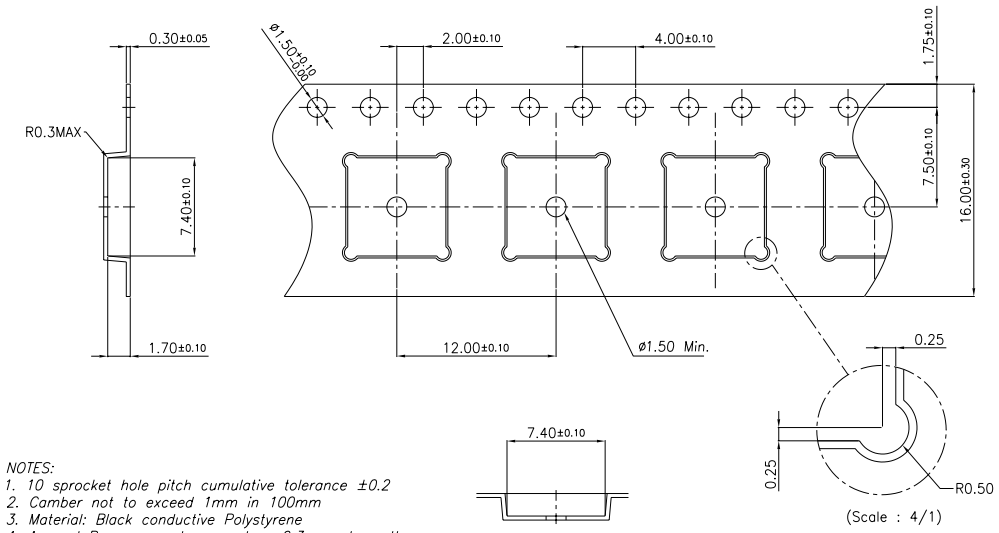
Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

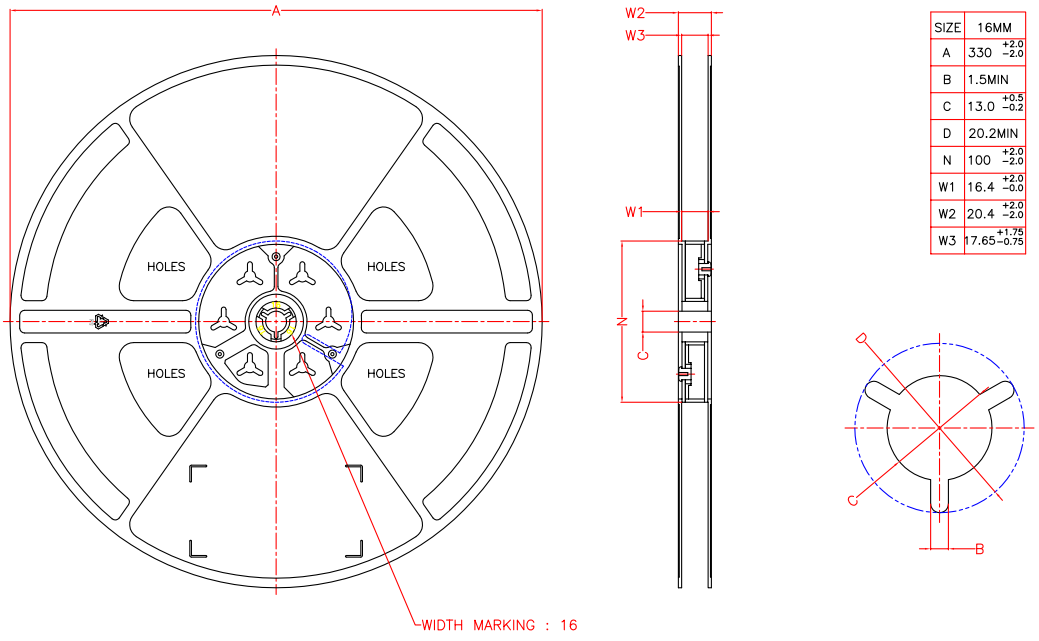
10. Tray and Reel

BGM240S modules are delivered to the customer in Tray or reel. Find the packaging dimensions below. All dimensions are given in mm unless otherwise indicated.



NOTES:
1. *10 sprocket hole pitch cumulative tolerance ±0.2*
2. *Camber not to exceed 1mm in 100mm*
3. *Material: Black conductive Polystyrene*
4. *Ao and Bo measured on a plane 0.3mm above the bottom of the pocket*
5. *Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.*
6. *Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.*
7. *Pocket center and pocket hole center must be same position.*

Figure 10.1. Carrier Tape Dimensions



SIZE	16MM
A	330 +2.0 −2.0
B	1.5MIN
C	13.0 +0.5 −0.2
D	20.2MIN
N	100 +2.0 −2.0
W1	16.4 +2.0 −0.0
W2	20.4 +2.0 −2.0
W3	17.65 +1.75 −0.75

Figure 10.2. Reel Dimensions

11. Certifications

This section details the regulatory certification status of the module in various regions.

The address for the module manufacturer and certification applicant is:

SILICON LABORATORIES FINLAND OY
Alberga Business Park, Bertel Jungin aukio 3,
02600 Espoo, Finland

11.1 Qualified Antennas

The BGM240S modules have been tested and certified both with the built-in integral antenna and with a reference external antenna attached to the module's RF pin denoted as RFOUT. The antenna impedance is 50 Ω.

Performance characteristics for the built-in antenna are presented in 3.3 Antenna and 4.16 Typical Performance Curves. The details of the qualified external antenna are summarized in the table below.

Table 11.1. Qualified External Antennas for BGM240S

Antenna Type	Maximum Gain	Impedance
Connectorized Coaxial Dipole	2.8 dBi	50 Ω

Any external antenna of the same general type and of equal or less directional gain compared to the one listed in the above table, and having similar in-band and out-of-band characteristics, can be used in the regulatory areas that have modular radio approvals, such as USA and Canada, as long as spot-check testing of the host is performed to verify that no performance changes compromising compliance have been introduced. In the particular FCC case, in order to comply with e-CFR Title 47, Part 15, Subpart C, Section 15.203, the module integrator using an external antenna must ensure it has a unique connector or it is nondetachable.

In countries applying the ETSI standards, where manufacturers issue a self-Declaration of Conformity before placing products in the market, like in the EU countries, the radiated emissions are always tested with the end-product and the antenna type is not critical, but antennas with higher gain may violate some of the regulatory limits.

When using instead an external antenna of a different type (such as a chip antenna, a PCB trace antenna, or a patch) or having non-similar in-band and out-of-band characteristics, but still with a gain less than or equal to the maximum gain listed in the table above, in principle it can be added to an existing modular grant/certificate by mean of a permissive change (for example with FCC and ISED), or by the administrative registration of such additional antenna (for example with MIC and KC). In many of these cases, some radiated emission testing is demanded, but no modular or end-product re-certification is required.

On the other hand, all products with external antennas having more gain than the maximum gain listed in the table above are very likely to require a full new end-product certification. Since the exact permissive change or registration or re-certification procedure is chosen on a case-by-case basis, please consult your certification house and/or a certification body for understanding the correct approach based on your unique design. You might also want or need to get in touch with Silicon Labs for any authorization letter that your certification body might ask for.

11.2 CE and UKCA - EU and UK

The BGM240S modules have been tested against the relevant harmonized/designated standards and are in conformity with the essential requirements and other relevant requirements of the EU's Radio Equipment Directive (RED) (2014/53/EU) and of the UK's Radio Equipment Regulations (RER) (S.I. 2017/1206).

Please notice that every end-product integrating a BGM240S module will need to perform the radio EMC tests on the whole assembly, according to the ETSI 301 489-x relevant standards.

Furthermore, it is ultimately the responsibility of the manufacturers to ensure the compliance of their end-products as a whole. The specific product assembly is likely to have an impact to RF radiated characteristics, when compared to the bare module. Hence, manufacturers should carefully consider RF radiated testing with the final product assembly, especially taking into account the gain of the external antenna if any, and the possible deviations in the PSD, EIRP and spurious emissions measurements, as defined in the ETSI EN 300 328 standard.

The modules are entitled to carry the CE and UKCA Marks, and a formal Declaration of Conformity (DoC) is available at the product web page which is reachable starting from https://www.silabs.com/.

11.3 FCC - USA

This device complies with FCC's e-CFR Title 47, Part 15, Subpart C, Section 15.247 (and related relevant parts of the ANSI C63.10 standard) when operating with the built-in integral antenna or with an external antenna type as discussed in Section 11.1 Qualified Antennas.

Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

FCC RF Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance.

This transmitter meets the Mobile requirements at a distance of 20 cm and above from the human body, in accordance to the limit(s) exposed in the RF Exposure Analysis. This transmitter also meets the Portable requirements at distances equal or above those reported in Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 59.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM Responsibilities to comply with FCC Regulations

This module has been tested for compliance to FCC Part 15.

OEM integrators are responsible for testing their end-product for any additional compliance requirements needed with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Additionally, investigative measurements and spot-checking are strongly recommended to verify that the full system compliance is maintained when the module is integrated, even with a module having a full modular approval, in accordance with the "Host Product Testing Guidance" in FCC's KDB 996369 D04 Module Integration Guide V01.

- **General Considerations**

  This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement, which is typically applicable to the final host. The final host will still need to be assessed for compliance to this portion of the rule requirements, if applicable.

- **Manual Information to the End User**

  The OEM integrator has to be aware not to provide information to the end-user regarding how to install or remove this RF module, or how to change RF related parameters, in the user's manual of the final product which integrates this module.

  The end user manual shall include all required regulatory information/warnings as shown in this manual.

- **Host Manufacturer Responsibilities**

  Host manufacturers are ultimately responsible for the full compliance of their host system. The final product is supposed to be assessed against all the essential requirements of the FCC rules, such as FCC Part 15 Subpart B, before it can be placed on the US market. This includes re-assuring the compliance of the radio transmitter with the RF and EMF essential requirements of the FCC rules. The modular radio transmitter must not be incorporated into any other radio-equipped device or system without retesting for compliance as multi-radio and combined equipment.

  Except for minor (cosmetic) modifications, most changes to an FCC certified equipment require preliminary testing to determine whether any of such changes is leading to a Class I or Class II Permissive Change. For more details about using the Single Modular Transmitter, refer to the following FCC documents:

  • KDB 996369 D01 Transmitter Module Equipment Authorization Guide

  • KDB 996369 D02 Frequently Asked Questions and Answers about Modules

  • KDB 178919 D01 Permissive Change Policy

  • KDB 178919 D02 Permissive Change Frequently-Asked Questions

Separation

- To meet the SAR exemption for portable conditions, the minimum separation distance indicated in Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 59 must be maintained between the human body and the radiator (antenna) at all times.
- This transmitter module is tested in a standalone RF Exposure condition, and in case of any co-located radio transmitter being allowed to transmit simultaneously, or in case of portable use at closer distances from the human body than those allowing the exceptions rules to be applied, a separate additional SAR evaluation, or a reduction in the max output power or in the duty-cycle, might be required for the host, ultimately leading to a Class II Permissive Change, or more rarely to a new grant.
- **Important Note:** In the event that the conditions for the exemption cannot be met, the final product will likely have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the FCC authorization to remain valid, and a permissive change will have to be applied. The SAR evaluation (and/or re-configuration) is under the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body, following a Change in ID authorization by the module's original grant holder.

End Product Labeling

BGM240S modules are not labeled with their own FCC ID due their very small size. Instead, the anti-static bags containing the modules' reels or trays come with a special label displaying the FCC ID. In all those cases when the module's FCC ID is not visible after the module is installed inside another device, then the outside of the device into which the module is installed must also have a label with a reference to the enclosed module. In that case, the final product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQ-GM240S"

or

"Contains FCC ID: QOQ-GM240S"

Final note: As long as all the conditions in this and all the above chapters are met, further RF testing of the transmitter will not be strictly required. However, still consider the good practice and the FCC strong recommendation to ensure the compliance of the host by spot-checking. Nevertheless, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements which might be mandatory with this module installed.

Class B Device Notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

11.4 ISED - Canada

This radio transmitter (IC: 5123A-GM240S) has been approved by *Innovation, Science and Economic Development Canada (ISED Canada, formerly Industry Canada*) to operate with the built-in integral antenna and with the antenna type(s) listed in Section 11.1 Qualified Antennas, with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain listed, are strictly prohibited for use with this device.

This radio-equipped device complies with ISED's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

The module meets the requirements for Mobile use cases when the minimum separation distance from the human body is 20 cm or greater, in accordance to the limit(s) exposed in the RF Exposure Analysis.

For Portable use cases, RF exposure or SAR evaluation is not required when the separation distances from the human body are equal or above those reported in Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 59.

If the separation distance from the human body is less than the values stated in Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 59, then the OEM integrator is responsible for evaluating the SAR with the end-product, or for the re-configuration of the radio module in the host in terms of lowering the max RF TX power and/or the duty-cycle. A permissive change would be required too, under the responsibility of the host manufacturer, following a Multiple Listing authorization by the original module's certificate holder.

OEM Responsibilities to comply with IC Regulations

The BGM240S modules have been certified for integration into products only by OEM integrators under the following conditions:

- The antenna must be installed so as to maintain the intended minimum separation distance between the radiator (antenna) and all persons at all times. Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 59 indicates the distances in accordance to the use cases.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

Important Note: In the event that the above conditions cannot be met, the final product will have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the ISED authorization to remain valid. A permissive change will have to be applied too**.** The RF Exposure evaluation (SAR, or possibly a re-configuration) is under the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body, following a Multiple Listing authorization by the module's original grant holder.

End Product Labeling

The BGM240S modules are not labeled with their own IC ID due their very small size. Instead, the anti-static bags containing the modules' reels or trays come with a special label displaying the IC ID. In all those cases when the module's IC ID is not visible after the module is installed inside another device, then the outside of the device into which the module is installed must also have a label with a reference to the enclosed module. In that case, the final product must be labeled in a visible area with the following:

“**Contains Transmitter Module IC: 5123A-GM240S** ”

or

“**Contains IC: 5123A-GM240S”**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end-product.

As long as all the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

CAN ICES-003 (B)

This Class B digital apparatus complies with Canadian ICES-003.

ISED (Français)

Le présent émetteur radio (IC: 5123A-GM240S) a été approuvé par Innovation, Sciences et Développement Économique Canada (ISED Canada, anciennement Industrie Canada) pour fonctionner avec l'antenne intégrée et le ou les types d'antenne énumérés à la section 11.1 Qualified Antennas, avec le gain maximal admissible indiqué. Les types d'antenne non inclus dans cette liste, ayant un gain supérieur au gain maximal indiqué, sont strictement interdits d'utilisation avec cet appareil. .

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage;
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptibled'en compromettre le fonctionnement.

Déclaration d'exposition RF

L'exception tirée des limites courantes d'évaluation SAR est donnée dans le document RSS-102 Issue 5.

Le module répond aux exigences pour les cas d'utilisation Mobile lorsque la distance minimale de séparation du corps humain est de 20 cm ou plus, conformément à la (aux) limite(s) exposée(s) dans l'analyse de l'exposition RF.

Pour les cas d'utilisation Portables, l'évaluation de l'Exposition RF ou l'évaluation SAR n'est pas requise lorsque les distances de séparation du corps humain sont égales ou supérieures à celles indiquées dans le tableau 11.2 à la page 57.

Si la distance de séparation du corps humain est inférieure aux valeurs indiquées dans le tableau 11.2 à la page 57, l'intégrateur OEM est responsable de l'évaluation du SAR avec le produit final, ou de la reconfiguration du module radio dans l'hôte en termes de réduction de la puissance RF TX maximale et/ou du rapport cyclique. Une modification permissive serait également nécessaire, sous la responsabilité du fabricant de l'hôte, suite à une autorisation de cotation multiple par le titulaire du certificat du module d'origine.

Responsabilités du fabricant de se conformer à la réglementation IC

Le module a été certifié pour l'intégration dans les produits uniquement par les intégrateurs OEM dans les conditions suivantes:

- L'antenne doit être installée de manière à maintenir une distance de séparation minimale entre le radiateur (antenne) et toutes les personnes à tout moment. Le tableau 11.2 à la page 57 indique les distances en fonction des cas d'utilisation.
- Le module émetteur ne doit pas être localisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

Remarque Importante: au cas où ces conditions ne pourraient pas être remplies, le produit final devra être soumis à des tests supplémentaires pour évaluer l'exposition RF, ou passer par une reconfiguration de la puissance de sortie maximale et/ou du rapport cyclique, afin que l'autorisation ISED reste valable; une modification permissive devra également être appliqué. L'évaluation de l'exposition aux radiofréquences (SAR, ou éventuellement une reconfiguration) est sous la responsabilité du fabricant du produit final, ainsi que le changement permissif qui peut être effectué avec l'aide de l'organisme de certification des télécommunications du client, après autorisation de cotation multiple par le titulaire de la certification du module.

Étiquetage des produits finis

Les modules BGM240S ne sont pas étiquetés avec leur propre IC ID en raison de leur taille. Au lieu de cela, l'étiquette d'emballage contient l'ID IC. Dans tous ces cas, si l'ID IC n'est pas visible après l'installation du module à l'intérieur d'un autre appareil, alors l'extérieur de l'appareil dans lequel le module est installé doit également afficher une étiquette faisant référence au module inclus. Dans ce cas, le produit final doit être étiqueté dans une zone visible avec les éléments suivants:

"**Contient le module transmetteur IC: 5123A-GM240S** "

ou

"**Contient IC: 5123A-GM240S"**

L'intégrateur OEM doit être conscient de ne pas fournir à l'utilisateur final d'informations sur la procédure d'installation ou de retrait de ce module RF ni sur la modification des paramètres liés à la RF dans le manuel d'utilisation du produit final.

Tant que toutes les conditions ci-dessus sont remplies, aucun test supplémentaire de l'émetteur ne sera nécessaire. Toutefois, l'intégrateur OEM reste responsable de l'essai de son produit final pour déterminer les exigences de conformité supplémentaires requises avec ce module installé (par exemple, émissions d'appareils numériques, exigences relatives aux périphériques PC, etc.)

CAN ICES-003 (B)

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

11.5 MIC - Japan

The BGM240S modules are certified in Japan with following certification numbers:

020-220206

It is the end-product manufacturer's responsibility to ensure that a module is configured to meet the compliance limits, as documented in the formal certification test report(s) being available at www.silabs.com. Refer to the API reference manual(s) to learn for example how to configure (limit) the maximum RF TX power for the normal operations, and refer as well to the power setting tables in the test report(s) in order to realize the maximum output power allowed for the regulatory compliance in Japan.

Manufacturers integrating a radio module into their host equipment are supposed to make the certification mark and the certification number visible on the outside of the host equipment. This combination of mark and number, and their relative placement, is depicted in Figure 11.1, and depending on the overall size it might also appear among the top shield markings of the radio module. The certification mark and certification number must be placed close to the text in the Japanese language which is provided below. This requirement in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

Certification Text to be Placed on the Outside Surface of the Host Equipment:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation of the text:

“This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”

The "Giteki" Mark shown in the following figures must be affixed to an easily noticeable section of the specified radio-enabled host equipment. Note that such section may be required to contain additional information if the end-device embedding the module is also subject to a Telecom approval.

The manufacturer of the final product is also responsible to provide a Japanese language version of the User Manual and/or Installation Instructions as a companion document coming with the final product when placed on the market in Japan. Such a document will have to mention the integrated radio component and the related certification information.

Figure 11.1. GITEKI Mark and ID

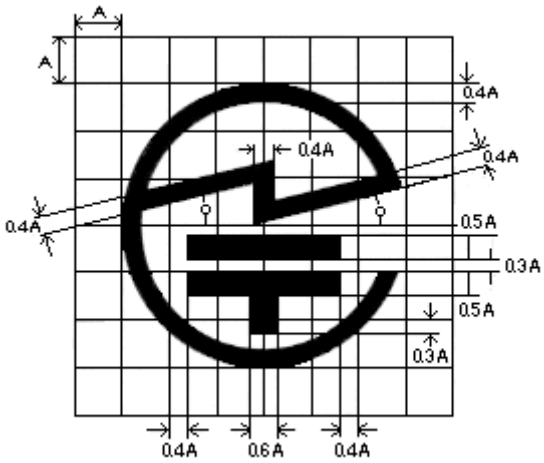


Figure 11.2. Detail of GITEKI Mark

11.6 KC - South Korea

The BGM240S modules have a RF registration for import and use in South Korea.

Registration number is R-R-BGT-GM240S.

These modules are meant to be integrated into end-products, which then become exempted from doing the RF emission testing, as long as the recommended design guidance is followed, and as long as, where applicable, the approved external antennas are used and any additional transmit power backoff is implemented in accordance to the measurements and configurations seen in the formal test report(s).

EMC testing and any other relevant test applicable to the end-product as a whole, plus appropriate labeling of the end-product, might still be required for the full regulatory compliance in the country.

11.7 RF Exposure and Proximity to Human Body

When using the BGM240S modules in an application where the radio-equipped end-product is located close to the human body, the human RF Exposure must be taken into account. FCC, ISED, and CE all have different standards and rules for evaluating the RF Exposure. In particular, each regulator has different requirements when it comes to the exemption from having to perform RF Exposure and SAR (Specific Absorption Rate) measurements, and the minimum separation distances between the module's antenna and the human body varies accordingly. The properties of the BGM240S modules allow for the minimum separation distances detailed in Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 59 for the SAR evaluation exemption in portable use cases (less than 20 cm from human body). The module is approved for the Mobile use case (more than 20 cm) without any need for RF Exposure evaluation.

Table 11.2. Minimum Separation Distances for SAR Evaluation Exemption

Certification	BGM240S22A, Bluetooth
FCC	Integral Antenna: 11 mm External Reference Dipole Antenna: 12 mm
ISED	Integral Antenna: 16 mm External Reference Dipole Antenna: 18 mm
CE	The RF exposure should always be evaluated with the end-product when transmitting with power levels higher than 20 mW (13 dBm).

The exemption distances above, calculated for reference in the full output power use case, are based on the rules in force at the time of writing this datasheet. Even though changing rarely, always ensure to apply the rules in force at the time of placing a product in the market.

In the cases of FCC and ISED, it is allowed to use the module at its max RF TX power in end-products where the typical separation distance from the human body is smaller than mentioned above, but it requires evaluating the RF Exposure in the final assembly and applying for a Class 2 Permissive Change to the FCC and ISED approvals of the module. In order to proceed with the permissive change, module manufacturer should be asked for an authorization to proceed first with a Change in ID and/or Multiple Listing, so that the new portable condition will be added to the new parallel grant owned by the end-product manufacturer.

For CE, RF Exposure must be evaluated using the end-product in all cases when transmitting at more than the power level indicated in the table.

Note: Placing the module in touch or very close to the human body will have a negative impact on the efficiency of the antenna thus a reduced range is to be expected.

11.8 Bluetooth Qualification

The BGM240S modules are launched with a pre-qualified Bluetooth Low Energy RF-PHY Tested Component based on Core Specification 5.3 having Declaration ID of D059594 and QDID of 184327.

The RF-PHY Tested Component should be imported and combined together with the latest Wireless Gecko Link Layer and Host prequalified Components by Silicon Labs, when in the process of qualifying an end-product which embeds the BGM240S via the SIG's Launch Studio. Please find out more in chapter 2.2 of the quick start guides QSG139 and GSG169.

Notice that the validity set by the SIG for Tested Components is currently of 3 years: during the product lifetime, Silicon Labs will reassess or re-qualify the RF-PHY Component as it expires, whenever applicable. In case of a re-qualification, a Tested Component will come with a new DID and a new QDID, and the latter will be then referred to in new end-product listings. Newer DIDs and QDIDs can be discovered by using the search engine in the SIG's Launch Studio, or by asking Silicon Labs via the technical support platform.

12. Revision History

Revision 0.51

October, 2022

- Updated top marking

Revision 0.5

September, 2022

- Initial Draft

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

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