# SiWG917 Wireless Module Data Sheet

Silicon Labs SiWG917 module is our lowest power Wi-Fi 6 plus Bluetooth LE 5.4 module, ideal for ultra-low power IoT wireless devices using Wi-Fi®, Bluetooth, Matter, and IP networking for secure cloud connectivity. It is optimal for developing battery operated devices that need long battery life. SiWG917 module includes an ultra-low power Wi-Fi 6 plus Bluetooth Low Energy (LE) 5.4 wireless CPU subsystem, and an integrated microcontroller (MCU) application subsystem, security, peripherals and power management subsystem all in a single 16 x 21.1 x 2.3 mm package. The wireless subsystem consists of a multi-threaded processor running up to 160 MHz, baseband digital signal processing, analog front end, 2.4 GHz RF transceiver and integrated power amplifier. The ARM® Cortex®-M4 is dedicated for peripheral and application-related processing, while the multi-threaded processor runs the wireless and networking stacks on independent threads, thus providing a fully integrated solution that is ready for a wide range of embedded wireless IoT applications. The modules come with modular radio type approvals for various countries, including USA (FCC), Canada (IC/ISED) and Japan (MIC), and are in compliance with the relevant EN standards (including EN 300 328 v2.2.2) for the conformity with the directives and regulations in the EU and UK.

SiWG917 applications include:

- Smart Home
- Security Cameras
- HVAC
- Smart Sensors
- Smart Appliances
- Health and Fitness
- Pet Trackers

- Smart Cities
- Smart Meters
- Industrial Wearables
- Smart Buildings
- Asset Tracking
- Smart hospitals
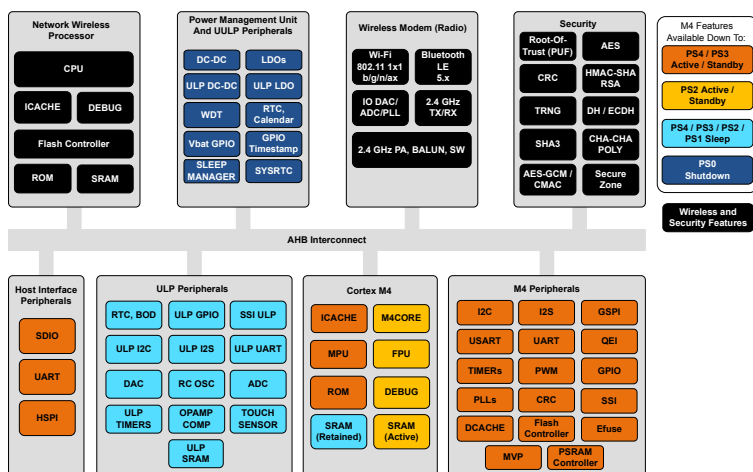
KEY FEATURES

- Wi-Fi 6 Single Band 2.4 GHz 20 MHz 1x1 stream IEEE 802.11 b/g/n/ax
- Bluetooth LE 5.4
- Single chip Matter Over Wi-Fi Solution
- ARM® Cortex® M4 Processor with FPU subsystem up to 180 MHz with rich set of Digital and Analog Peripherals.
- Wi-Fi 6 Benefits: TWT for improved efficiency and longer battery life, MU-MIMO/OFDMA for Higher Throughput, network capacity and low latency
- Best in Class Device and Wireless Security
- WLAN Tx power up to +16.5 dBm with integrated PA
- Bluetooth LE Tx power up to +16.5 dBm with integrated PA
- WLAN Rx sensitivity as low as -94.5 dBm
- Wi-Fi Standby Associated mode current: 55 µA @ 1-second listen interval
- Embedded Flash option up to 8 MB/ optional external Flash up to 16 MB
- Embedded PSRAM option up to 8 MB/ optional external PSRAM option up to 16 MB
- Ultra-low power sensor hub peripherals
- Embedded Wi-Fi, Bluetooth LE, Matter, and networking stacks supporting wireless coexistence
- Three software-configurable MCU application memory options for sharing the RAM between the wireless, system, and application (192/256/320 kB)
- Operating temperature: -40 ºC to +85 ºC
- Operating supply range: 3.0 V to 3.63 V
- Suppy voltage for GPIOs: 1.71 V - 3.63 V

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This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

1. Feature List

- **Microcontroller**
  - ARM® Cortex® M4 core with up to 180 MHz, 225 DMIPS performance
  - Integrated FPU (Floating Point Unit), MPU (Memory Protection Unit), and NVIC (Nested Vectored Interrupt Controller).
  - SWD (Serial Wire Debug) and JTAG (Joint Test Action Group) debug options
  - Internal and external oscillators with Phase Locked Loops (PLLs)
  - IAP (In-Flash Application Programming), ISP (In-System Programming), and OTA (Over-the-Air) Wireless Firmware Upgrade
  - Power-On Reset (POR), Brown-Out and Black-out Detect (BOD) with separate thresholds
  - M4 has 2 dedicated QSPI (Quad Serial Peripheral Interface) controllers for PSRAM (Pseudo Static Random Access Memory) and Flash.
- **Hardware Accelerator**
  - Delivers faster Machine Learning (ML) inference with lower power consumption than a non-accelerated MCU
  - Accelerates Real and Complex Matrix and Vector operations, providing manifold computing efficiency
- **Memory**
  - Embedded SRAM (Static Random Access Memory) up to 672 kB total for Application and Wireless Processor
  - On-chip SRAM of 192 K/256 K/320 Kbytes for M4 Application Processor based on the memory configuration
  - Support for Flash up to 8 MB (in-package), or Optional External Flash up to 16 MB.
  - Support for PSRAM option up to 8 MB (in-package), Optional External PSRAM up to 16 MB
- **Digital Peripherals**
  - Secure Digital Input Output (SDIO) 2.0 secondary
  - 1x Universal Synchronous/Asynchronous Receiver Transmitter (USART)
  - 2x Universal Asynchronous Receiver Transmitter (UART)
  - 4x Serial Peripheral Interface (SPI)
  - 3x Inter-Integrated Circuit (I2C)
  - 2x Inter-IC Sound Bus (I2S)
  - Serial Input Output (SIO)
  - Pulse Width Modulation (PWM)
  - Quadrature Encoder Interface (QEI)
  - Timers: 4x 16/32-bit, 1x 24-bit, Watchdog Timer (WDT), Real Time Counter (RTC)
  - Up to 43 General Purpose Input Outputs (GPIOs) with GPIO multiplexer
- **Analog Peripherals**
  - 12-bit 16-ch, 5 Mbps Analog to Digital Converter (ADC)
  - 10-bit Digital to Analog Converter (DAC)
  - 3x Op-amps

- **Security**
  - Secure Boot
  - Secure firmware upgrade through boot-loader, Secure OTA.
  - Secure Key storage and HW device identity with PUF
  - Secure Zone
  - Secure XIP (Execution in place) from flash/ PSRAM
  - Secure Attestation
  - Hardware Accelerators: Advanced Encryption Standard (AES) 128/256/192, Secure Hash Algorithm (SHA) 256/384/512, Hash Message Authentication Code (HMAC), Random Number Generator (RNG), Cyclic Redundancy Check (CRC), SHA3, AES-Galois Counter Mode (GCM)/ Cipher based Message Authentication Code (CMAC), Cha-Cha-poly, True Random Number Generator (TRNG)
  - Software Accelerators: RSA, ECC
  - Programmable Secure Hardware Write protect for Flash sectors
  - Anti Rollback
  - Debug Lock
- **Wi-Fi**
  - Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
  - Support for 20 MHz channel bandwidth for 802.11n and 802.11ax.
  - Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi + BLE
  - Wi-Fi 6 Features: Individual Target wake-up time (iTWT), Broadcast TWT (bTWT), Intra PPDU power save, SU extended range (ER), DCM (Dual Carrier Modulation), DL MU-MIMO, DL/UL OFDMA, MBSSID, BFRP, Spatial Re-use, BSS Coloring, and NDP feedback up to 4 antennas
  - Transmit power up to +16.5 dBm with integrated PA
  - Receive sensitivity as low as -94.5 dBm
  - Data Rates: 802.11b: 1, 2, 5.5, 11; 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
  - Operating Frequency Range [MHz]: 2412-2462 (North America, default), 2412-2472 (Europe, and other countries where applicable), 2412-2484 (Japan)
  - PTA Coexistence with Zigbee/Thread/Bluetooth
- **Bluetooth**
  - Transmit power up to +16.5 dBm with integrated PA
  - Receive sensitivity — LE: -93 dBm, LR 125 Kbps: -105 dBm
  - Operating Frequency Range — 2.402 GHz - 2.480 GHz
  - Supports Bluetooth® Low Energy (LE): High Speed (1Mbps and 2Mbps) and Long Range (LE Coded PHYs, 125Kbps and 500Kbps; these are referred to as "LR" throughout this data sheet)
  - Advertising extensions
  - Data length extensions

Feature List (cont.)

- **Analog Peripherals (cont.)**
  - 2x Comparators
  - InfraRed (IR) detector and Temperature Sensor
  - 8 capacitive touch sensor inputs
- **Embedded Bluetooth Stack**
  - Support GAP profile
  - Support GATT profile
  - Support SMP
  - Support LE L2CAP
- **WiSeConnect SDK Features**
  - Simplified and Unified DX for Wi-Fi API and Platform APIs
  - Simplifies application development and presents clean and standardized APIs
  - UC (Universal Configurator) enables componentization, simplifying configuration of peripherals and examples
  - BSD and ARM IoT-compliant socket API
  - Available through Simplicity Studio and Github
- **Intelligent Power Management**
  - Power optimizations leveraging multiple power domains and partitioned sub systems
  - Many system-, component-, and circuit-level innovations and optimizations
  - Different Power Modes and Power States
  - Dynamic Voltage & Frequency Scaling (DVFS)
  - Dynamic Gear Shifting (switches from one power state to another based on processing requirements)
  - Deep sleep mode with only timer active – with and without RAM retention
- **Ultra Low Power Sensor Hub System**
  - Extends battery life and recharging interval for IoT Sensors
  - SensorHub with an easy-to-use configuration wizard, decouples software from peripheral and sensor drivers
- **MCU Sub-System Power Consumption**
  - Active current as low as 32 µA/MHz @ 20 MHz in low-power mode
  - Active current as low as 50 µA/MHz @ 180 Mhz in high performance mode
  - Deep sleep mode current: ~2.5 µA
  - Dynamic voltage & frequency scaling
  - Deep sleep mode with only timer active – with and without RAM retention
- **Wireless Sub-System Power Consumption**
  - Wi-Fi 4 standby associated mode current: 55 µA @ 1-second beacon listen interval
  - Wi-Fi 1 Mbps Listen current: 13 mA
  - Wi-Fi LP mode Rx current: 18 mA
  - Deep sleep current ~ 2.5 µA, standby current (352 K RAM retention) ~ 10 µA
- **Operating Range**
  - 3.0 V to 3.63 V
  - -40 °C to +85 °C

- **Ultra Low Power (ULP) Peripherals**
  - RTC
  - BOD
  - ULP I2C
  - ULP I2S
  - ULP UART
  - ULP GPIO
  - ULP Timers
- **RF & Modem Features**
  - Integrated baseband processor with calibration memory
  - Integrated RF transceiver, high-power amplifier, balun and T/R switch
- **Embedded Wi-Fi Stack**
  - Support for Embedded Wi-Fi STA mode, Wi-Fi access point mode, and concurrent (AP+STA) mode
  - Supports advanced Wi-Fi security features: WPA personal, WPA2 personal, WPA3 personal, WPA/WPA2 enterprise in STA mode
  - Networking: Integrated IPv4/IPv6 stack, TCP, UDP, ICMP, ICMPv6, ARP, DHCP Client/Server, DHCPv6 Client, DNS Client, SSL3.0/TLS1.3 Client, SNTP, SNI
  - Applications: HTTP/s Client, HTTP/s Server, MQTT/s Client, AWS Client, Azure Client
  - Sockets: BSD sockets, IoT sockets
  - Over-the-Air (OTA) wireless firmware update
  - Provisioning using Wi-Fi AP or BLE
- **Software and Regulatory Certifications**
  - Wi-Fi Alliance: Wi-Fi 4, Wi-Fi 6
  - Matter Certification
  - Bluetooth SIG Qualification
  - Regulatory pre-certifications: [FCC (USA), IC/ISED (Canada), CE (EU), UKCA (UK), MIC (Japan), KC (South Korea), NCC (Taiwan), SRRC (China), ACMA (Australia), RSM (New Zealand)][3]
- **Advanced Software Features**
  - Amazon FreeRTOS, Zephyr
  - Amazon AWS Cloud Connectivity, Microsoft Azure Cloud Connectivity
  - SensorHub
  - SoC communication to external host via Co-Processor Communication (CPC) - Supported host interfaces are SDIO/UART
  - Dual-Host: Support both embedded TCP-IP and TCP-IP bypass simultaneously
- **Development Environment**
  - Simplicity Studio™ IDE and Debugger Integration
  - Advanced energy measurement for ultra-low power
  - Sample examples for Wireless, MCU peripherals, Matter, Cloud Connectivity.
  - Manufacturing Tools Framework support through Simplicity Commander. This enables provision of MBR programming, security key management, and calibration support for crystal and gain offsets.

- **Supported Protocols**
  - Bluetooth Low Energy (BLE) 5.4
  - Wifi 6 (802.11 b/g/n/ax)

- **Dimensions**
  - 16 x 21.1 x 2.3 mm

Note:

1. For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.
2. All power and performance numbers are under ideal conditions.
3. For information about software roadmap features and additional certification information, contact Silicon Labs for availability and timeline.
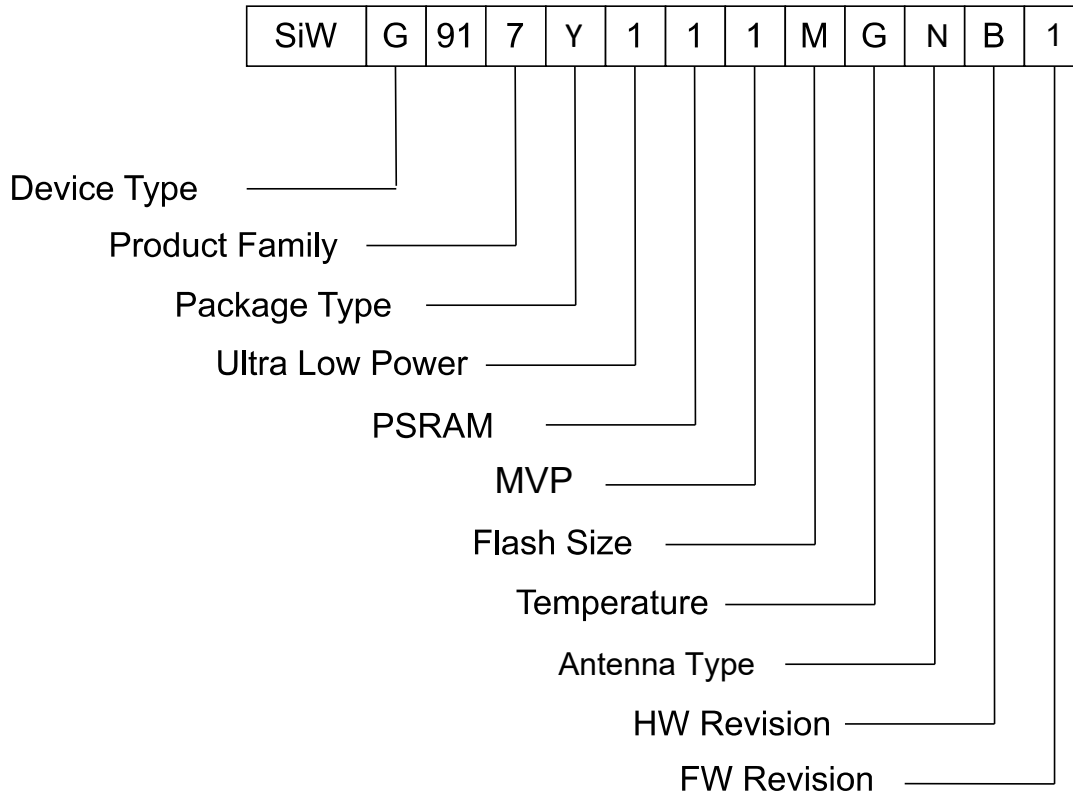
2. Ordering Information

| SiW | G | 91 | 7 | Y | 1 | 1 | 1 | M | G | N | B | 1 |

Device Type
Product Family
Package Type
Ultra Low Power
PSRAM
MVP
Flash Size
Temperature
Antenna Type
HW Revision
FW Revision

Figure 2.1. Ordering Guide

Table 2.1. Orderable Part Number (OPN) Decoder

Field	Options
Device Type	**T**: RCP (Transceiver) **N**: NCP **G**: SoC
Product Family	**7**: Ultra-low power
Package Type	**Y**: PCB Modules
Ultra Low Power	**1**: ULP Features enabled
PSRAM	**0**: No PSRAM Support **1**: External PSRAM **2**: 2 MB In-package PSRAM **4**: 8 MB In-package PSRAM
MVP	**0**: MVP features disabled **1**: MVP Features enabled

Field	Options
Flash Size	**X**: No Flash **L**: 4 MB Flash **M**: 8 MB Flash
Temperature	**G**: -40ºC to 85ºC **N**: -40ºC to 105ºC
Antenna Type	**N**: No Antenna **A**: Built-in Antenna
HW Revision	DIE revision was used: (A, B, C...)
FW Revision	Before launch numeric characters are used. After launch alphabetic characters are used

Table 2.2. Part Ordering Options

Module OPN	Protocol Stack	Freq Band	Antenna	MVP	Flash/ RAM (kB)	GPIO	Temp Range	Pack- aging
SiWG917Y111XGNBA	BLE 5.4 Wifi 6	2.4GHz	No Antenna	Yes	No internal flash	43	-40 to 85 °C	Tape and Reel
SiWG917Y110LGNBA	BLE 5.4 Wifi 6	2.4GHz	No Antenna	No	4MB flash	43	-40 to 85 °C	Tape and Reel
SiWG917Y111MGNBA	BLE 5.4 Wifi 6	2.4GHz	No Antenna	Yes	8MB flash	43	-40 to 85 °C	Tape and Reel
SiWG917Y121MGNBA	BLE 5.4 Wifi 6	2.4GHz	No Antenna	Yes	8MB flash, 2MB PSRAM	43	-40 to 85 °C	Tape and Reel
SiWG917Y111XGABA	BLE 5.4 Wifi 6	2.4GHz	Built in Antenna	Yes	No internal flash	43	-40 to 85 °C	Tape and Reel
SiWG917Y110LGABA	BLE 5.4 Wifi 6	2.4GHz	Built in Antenna	No	4MB flash	43	-40 to 85 °C	Tape and Reel
SiWG917Y111MGABA	BLE 5.4 Wifi 6	2.4GHz	Built in Antenna	Yes	8MB flash	43	-40 to 85 °C	Tape and Reel
SiWG917Y121MGABA	BLE 5.4 Wifi 6	2.4GHz	Built in Antenna	Yes	8MB flash, 2MB PSRAM	43	-40 to 85 °C	Tape and Reel

Note: Throughout this document, the modules are referred to by their ordering codes above, or by their model names of SiW917Y1GN and SiW917Y1GA, respectively for the hardware variants with no antenna and with integral antenna, or by their marketing/friendly name of SiWG917.

Table of Contents

3. Applications

Smart Home

Smart Locks, Motion/Entrance Sensors, Water Leak sensors, Smart plugs/switches, Light Emitting Diode (LED) lights, Door-bell cameras, Washers/Dryers, Refrigerators, Thermostats, Consumer Security cameras, Voice Assistants, etc.

Other Consumer Applications

Toys, Anti-theft tags, Smart dispensers, Weighing scales, Fitness Monitors, Smart Glasses, Blood pressure monitors, Blood sugar monitors, Portable cameras, etc.

Other Applications (Medical, Industrial, Retail, Agricultural, Smart City, etc.)

Healthcare Tags, Industrial Wearables, Infusion pumps, Sensors/actuators in Manufacturing, Electronic Shelf labels, Agricultural sensors, Product tracking tags, Smart Meters, Parking sensors, Street LED lighting, Automotive After-market, Security Cameras, etc.

4. Block Diagrams
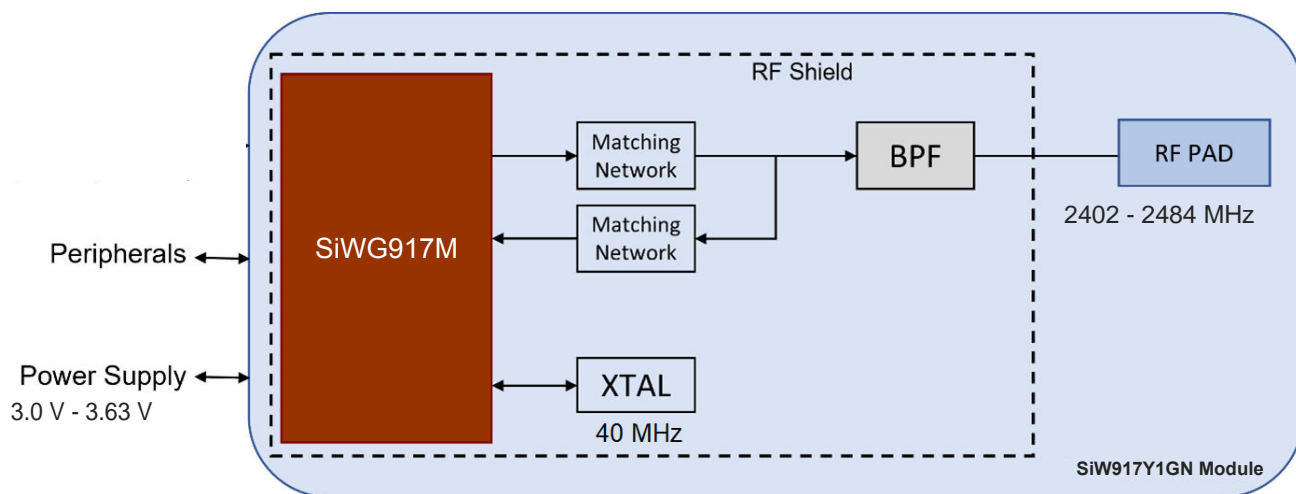
SiW917Y1GN (Without Antenna) Module Block Diagram
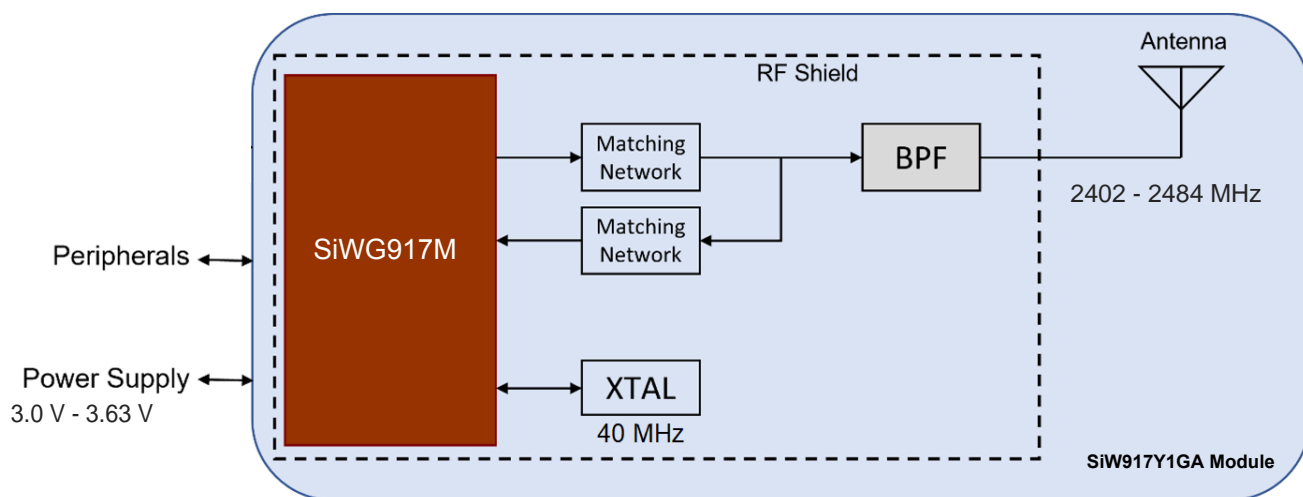
SiW917Y1GA (With Antenna) Module Block Diagram

External Processor MCU (optional)

Customer Application (optional)

External Interface – SDIO, SPI, UART

Customer Applications / Profile

Matter

Cloud Agents and Network Apps

Dual Host CCP Mode

Peripheral Drivers, Security

BLE Profiles	Networking Stack
BLE Stack	Wi-Fi Stack

BLE Controller	Wi-Fi MAC HAL	Co-Existence Managers

HW – MAC/PHY (2.4 GHz Wi-Fi + Bluetooth LE)
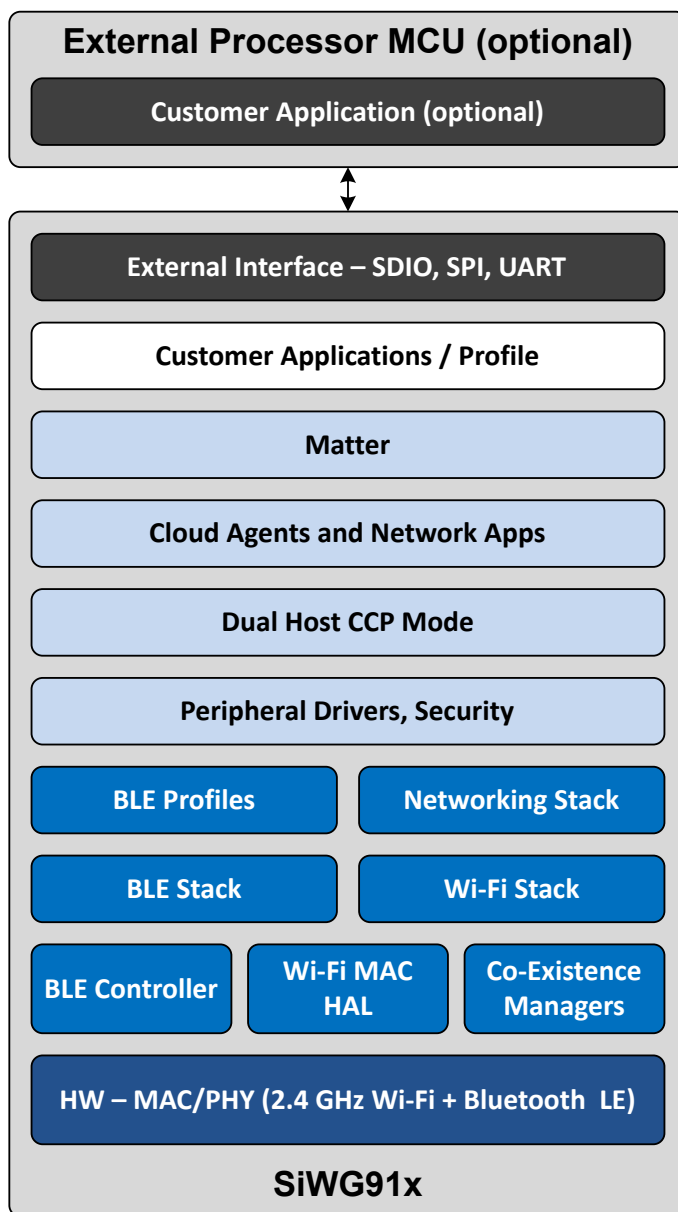
SiWG91x

SiWG917 SoC Software Architecture

5. System Overview

5.1 Introduction

SiWG917 modules are based on Silicon Labs' SiWG917M ultra-low-power, single spatial stream, 802.11 b/g/n/ax+ BLE 5.4 Convergence SoC. The SiWG917 module provides low-cost CMOS integration of a multi-threaded MAC processor, baseband digital signal processing, analog front-end, crystal oscillator, calibration eFuse, 2.4GHz RF transceiver, integrated power amplifier, matching network, bandpass filter (BPF), and Quad-SPI Flash thus providing a fully-integrated solution for a range of hosted and embedded wireless applications. With Silicon Labs' embedded four-threaded processor and on-chip ROM and RAM, these chipsets enable integration into low-cost and zero host load applications. With an integrated PMU and support for a variety of digital peripherals, SiWG917 modules enable very low-cost implementations for wireless hosted and embedded applications. It can be connected to a host processor through SDIO, SPI or UART interfaces. Wireless firmware upgrades and provisioning are supported.

5.2 ARM Cortex M4

The ARM Cortex-M4 is the main application processor in the SiWG917M embedded SoC. It is a high-performance 32-bit processor designed by ARM for the microcontroller market. It is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The M4 processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and Single Instruction Multiple Data (SIMD) multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division. The Cortex M4 microcontroller integrated into the SiWG917M embedded SoC supports the following features:

- MPU (Memory Protection Unit) with 8 memory regions, FPU (Floating Point Unit), and NVIC (Nested Vectored Interrupt Controller) with 64 levels of interrupt priority
- Debug port with both JTAG as well as Serial Wire Debug (SWD) interface; comprehensive debug functionality including data matching for a watch-point generation
- To provide optimal power vs performance tradeoff, unique gear-shifting is available for the Cortex-M4 that enables optimal power consumption based on the required performance. The available power-states are Power State 4 (PS4 at 1.15 V): max 180 MHz, Power State 3 (PS3 at 1.05 V): max 90 MHz, Power State 2 (PS2 at 0.75 V): max 20 MHz. More details are provided in Section 5.3.3 Power States .
- Architectural clock gates are included to minimize dynamic power dissipation.
- The multi-threaded processor and Cortex-M4 communicate through thread to thread interrupting and memory.
- On-chip M4 SRAM of 192 K/256 K/320 Kbytes based on the SiWG917M chip configuration
- 8 Kbytes is present in the ultra-low-power (ULP) peripheral subsystem. This memory is present on the S-bus of the Cortex-M4 and is primarily used by the ULP MCU peripherals like ULP I2S, etc.
- 64 Kbytes of ROM which hold the Cortex-M4 peripheral drivers
- 16 Kbytes of instruction cache enabling eXecute In Place (XIP) with external quad/octal SPI Single Data Rate (SDR) flashes
- Based on the SiWG917M package configuration, up to 8MBytes of in-package Quad Serial Peripheral Interface (QSPI) flash is available for the Cortex-M4. This flash can be shared with TA in common flash mode.
- eFuse of 32 bytes (available for customer applications)
- 225 Dhrystone million instructions per second (DMIPS) performance

The Cortex-M4 core includes the following core peripherals:

Nested Vectored Interrupt Controller

The NVIC is an embedded interrupt controller that supports low latency interrupt processing.

Memory Protection Unit

The memory protection unit (MPU) improves system reliability by defining the memory attributes for different memory regions. It provides up to eight different regions and an optional predefined background region. It provides fine-grain memory control, enabling applications to utilize multiple privilege levels, separating and protecting code, data, and stack on a task-by-task basis. Such requirements are becoming critical in many embedded applications such as automotive.

The memory map and the programming of the MPU split the memory map into regions. Each region has a defined memory type, and some regions have additional memory attributes. The memory type and attributes determine the behavior of accesses to the region.

The memory types are:

• **Normal:** The M4 processor can re-order transactions for efficiency, or perform speculative reads.
• **Device:** The M4 processor preserves transaction order relative to other transactions to device or strongly-ordered memory.
• **Strongly-ordered:** The M4 processor preserves transaction order relative to all other transactions. The different ordering requirements for device and strongly-ordered memory mean that the memory system can buffer a write to device memory, but must not buffer a write to strongly-ordered memory.

The additional memory attributes include:

• **Shareable:** For a shareable memory region, the memory system provides data synchronization between bus primaries in a system with multiple bus primaries, for example, a M4 processor with a Direct Memory Access (DMA) controller. Strongly-ordered memory is always shareable. If multiple bus primaries can access a non-shareable memory region, the software must ensure data coherency between the bus primaries.
• **Execute Never (XN):** Means the M4 processor prevents instruction accesses. A fault exception is generated only on execution of an instruction executed from an XN region.

Floating-Point Unit

The Floating-point unit (FPU) provides IEEE754-compliant operations on single-precision, 32-bit, floating-point values. It supports addition, subtraction, multiplication, division and square root.

5.2.1 Memory Architecture

There are on chip Read Only Memory (ROM), Random Access Memory (RAM) and off chip FLASH connectivity. Sizes of ROM/RAM/ FLASH will vary depending on the chip configuration.

Highlights:
- Unified memory architecture - software can partition the memory between code and data usage
- Multiport - RAMs support multi port access - allowing simultaneous access from different primaries (I, D, DMAs) to non overlapping regions without any cycle penalty
- ROM/RAMs are tightly coupled to the M4 processor I/D buses to reduce the latency and power
- Supports memory protection - generates trap if unintended primary accesses the memory

The Cortex-M4 processor has following memory:
- On-chip M4 SRAM of 192K/256K/320Kbytes based on the chip configuration
- 8Kbytes is present in the Ultra-low-power(ULP) peripheral subsystem. This memory is present on the S-bus of the Cortex-M4 and is primarily used by the ULP MCU peripherals like ULP I2S, ADC, DAC etc.
- 64Kbytes of ROM which holds the M4 peripheral drivers and bootloader.
- 16Kbytes of Instruction cache (I cache) enabling eXecute In Place (XIP) with external quad/octal SPI SDR flashes.
- Based on the package configuration up to 8MBytes of "in-package" Quad SPI flash is available for the M4. This flash can be shared with the multi-threaded processor in common flash mode
- eFuse of 32 bytes (available for customer applications)
- 16Kbytes of Data cache (D cache) enabling data fetching with PSRAM and Instruction cache (I cache) to execute code from PSRAM
- Flash Memory:
  - Based on the package configuration (OPN) up to 8 MB of "in-package" Quad SPI flash is available.
  - In addition, IC can support external flash option
    - IC has the support for 2-flash configuration
      - Common flash: Flash is common for both Cortex M4 and multi-threaded processor
      - Dual Flash: Separate flash can be used for Cortex M4 and multi-threaded processor

5.3 Power Architecture

The Power Control Hardware implements the control sequences for transitioning between different power states (Active/Standby/Sleep/ Shutdown) and the power control for different group of peripherals. In addition, wakeup from any of the Standby/Sleep/Shutdown states based on hardware events or peripheral interrupts is supported. The Standby and Shutdown states can be reached from Active mode only through a Wait for Interrupt (WFI) instruction. Wakeup from Standby/Sleep/Shutdown states is through a hardware event or inter- rupt (Peripheral or External).

5.3.1 Highlights

- High performance and ultra-low-power MCU peripheral subsystems and buses.
- Multiple voltage domains with independent voltage scaling of each domain.
- Fine grained power-gating including peripherals, buses and pads, thereby reducing power consumption when the peripheral/buses/ pads are inactive.
- Multiple active states using "gear-shifting" approach based on processing requirements, thereby reducing power consumption for low-power applications.
- Flexible switching between different active states with controls from software.
- Hardware based wakeup from Standby/Sleep/Shutdown states.
- All the peripherals are clock gated by default, thereby reducing the power consumption in inactive state.
- Wakeup times are configurable by software before going into sleep.

5.3.2 Power Domains

All the applications, high-speed interfaces, and peripherals are segregated into multiple power domains to achieve lower current consumption when they are inactive. At reset, all the domains are powered ON.

The table below describes the different group of peripherals for which power is controlled through software.

Table 5.1. List of Power Domains

S.No	Section	Domain Name	Functionality of the Power Domain
1	APPLICATIONS	DEBUG_FPU	Debug Functionality for Cortex-M4, Floating Point Unit for Cortex-M4
		ROM	ROM Core/Interface
		SRAM	SRAM Banks
2	HIGH SPEED INTERFACE	QSPI_ICACHE	Quad/Octal 1 SPI SDR Flash Interface and ICache for the Cortex-M4 Processor, QSPI2 PSRAM interface, DCACHE
3	HP-PERIPHERALS	PERI_EFUSE	SPI/Synchronous Serial Interface (SSI) Primary, I2C, USART, Micro-DMA Controller, UART, SPI/SSI Secondary, Generic-SPI Primary, Config Timer, Random-Number Generator, CRC Accelerator, SIO, I2C, I2S Primary/Secondary, QEI, MCPWM and EFUSE for configuration information , MVP
		DMA	General Purpose DMA Controller
		SDIO-SPI	SDIO 2.0 Secondary, SPI Secondary.
4	HIGH SPEED FLASH MEMORY	FLASH-LDO	Low DropOut (LDO)-FL 1.8 for Flash Memory
5	HIGH-FREQ-PLL	PLL-REGISTERS	PLL Programming Registers for High frequency clocks.
6	ULP-PERIPHERALS	DMA	Micro-DMA Controller
		IR	IR Receiver
		ADC-DAC	ADC and DAC Controller
		I2C	I2C Primary/Secondary
		SSI	SPI/SSI Primary
		UART	UART
		TOUCH	Capacitive Touch Sensor Controller
		TIMER	Timers

S.No	Section	Domain Name	Functionality of the Power Domain
7	UULP-PERIPHERALS	WDT	Watch Dog Timer
		TS	Temperature Sensor Controller
		PS	Process Sensor Controller
		RTC	Real-Time Clock, MCU System Real Time Clock (SYSRTC)
		STORAGE-DOMAIN1	Storage Flops - Set1. Contains 8 bytes
		STORAGE-DOMAIN2	Storage Flops - Set2. Contains 8 bytes
		STORAGE-DOMAIN3	Storage Flops - Set3. Contains 16 bytes
		SLEEP-FSM	Finite State Machine (FSM) for Sleep/Wakeup
		CLOCK-CALIB	Calibration block for Sleep Clock.
		BBFFS	Programming Registers which can be retained during sleep.
		DS-TIMER	DEEP SLEEP Timer.
		TIMESTAMP	Timestamping Controller.
		LP-FSM	Low-Power (LP) FSM
		RETEN	Retention Flops which can be retained during sleep.
8	Analog-PERIPHER-ALS	Aux-ADC	Auxiliary ADC
		Aux-DAC	Auxiliary DAC
		BOD	Brown-Out Detector

The SRAM is also segregated into multiple power domains to achieve lower current consumption per the memory requirement. The power for the SRAM domains in active states can be controlled in the following manners:

- **Shut-Down Mode/Deepsleep without Retention Mode:** SRAM domains as described in the table below can be powered down for unused SRAM sections. The RAM contents are not retained in this mode.
- **Deep-Sleep (Lower Power Consumption) Mode:** The RAM contents are retained in this mode. The SRAM is not accessible in this state. This is configurable on a bank granularity.

The table below describes the segregation of power domains for SRAM (328 KB).

Table 5.2. Segregation of Power Domains for SRAM (328 KB)

S.No	Section	Domain Name	Functionality of the Power Domain
1	LP-SRAM	LP-SRAM-1	4 KB of SRAM (1x Banks)
		LP-SRAM-2	4 KB of SRAM (1x Banks)
		LP-SRAM-3	4 KB of SRAM (1x Banks)
		LP-SRAM-4	4 KB of SRAM (1x Banks)
		LP-SRAM-5	16 KB of SRAM (1x Banks)
		LP-SRAM-6	32 KB of SRAM (2x Banks)
		LP-SRAM-7	64 KB of SRAM (4x Banks)
		LP-SRAM-8	64 KB of SRAM (4x Banks)
		LP-SRAM-9	64KB of SRAM (4x Banks)
		LP-SRAM-10	64 KB of SRAM (4x Banks)

S.No	Section	Domain Name	Functionality of the Power Domain
2	ULP-SRAM	ULP-SRAM-1	2 KB of SRAM (1x Banks)
		ULP-SRAM-2	2 KB of SRAM (1x Banks)
		ULP-SRAM-3	2 KB of SRAM (1x Banks)
		ULP-SRAM-4	2 KB of SRAM (1x Banks)

5.3.3 Power States

The power states available in different power modes (PS0, PS1, PS2, PS3, PS4) are listed below

- Reset State
- Active States
  - Power State1 (PS1)
  - Power State2 (PS2)
  - Power State3 (PS3)
  - Power State4 (PS4)
- Standby States
  - PS2-STANDBY
  - PS3-STANDBY
  - PS4-STANDBY
- Sleep States
  - PS2-SLEEP
  - PS3-SLEEP
  - PS4-SLEEP
- Shutdown States
  - Power State0 (PS0)

After reset, the M4 processor starts in the PS4 state which is the highest activity state where the full functionality is available. The other active states (PS2/PS3) will have limited functionality or processing power.

A transition from active states (PS2/PS3/PS4) to any other state (Sleep/Standby) can only be triggered by software.

A transition from Standby/Sleep/Shutdown states can be triggered by an enabled interrupt as configured by software before entering these states.

A transition from Standby/Sleep to active state is possible from where these states are entered.

There are different wakeup sources available in each Standby/Sleep/Shutdown state.

The figure below shows the transitions between different power states.
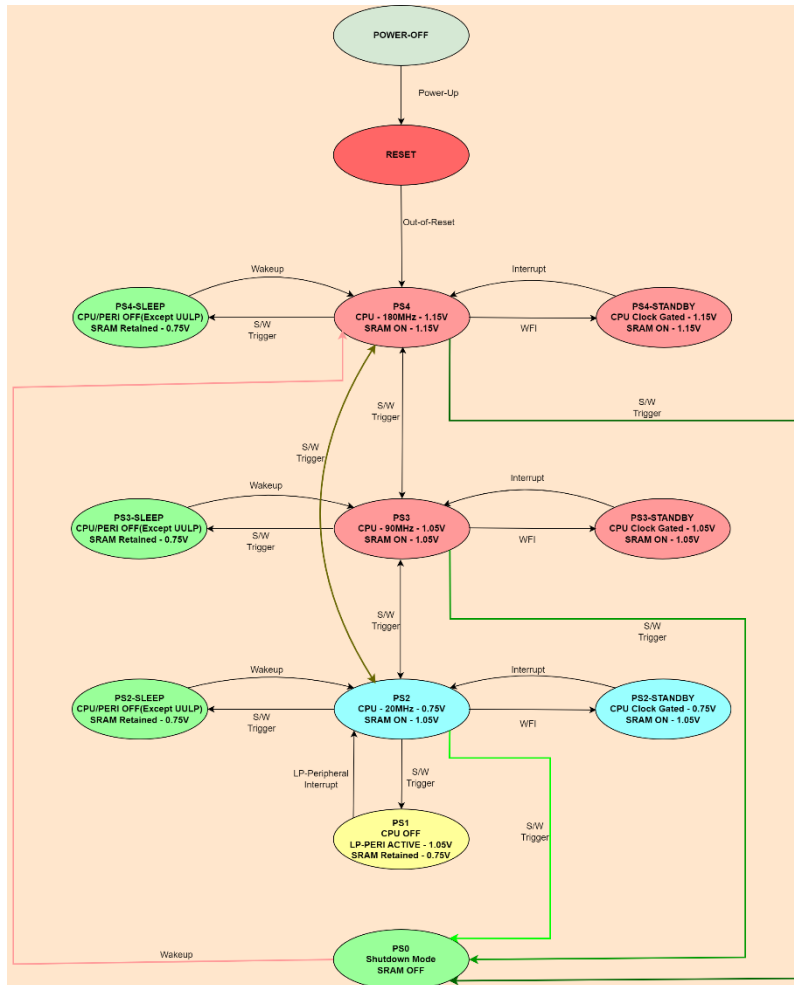
Figure 5.1. Power States

5.3.3.1 PS4

This is an active state where the complete functionality is available. The CPU, peripherals, and SRAM operate on the SoC LDO supply at voltage of 1.15V.

The functionalities available in this state are mentioned below:

- Maximum CPU operating frequency of 180 MHz. The CPU can operate on the HIGH-FREQ-PLL output clocks.
- APPLICATIONS - DEBUG, FPU, ICACHE, and ROM.
- HIGH SPEED INTERFACE - as listed in Table 5.1 List of Power Domains on page 17.
- HIGH-FREQ-PLL - as listed in Table 5.1 List of Power Domains on page 17.
- All the peripherals consisting of HP-PERIPHERALS, ULP-PERIPHERALS, Ultra Ultra Low Power (UULP-PERIPHERALS), and Analog-PERIPHERALS - as listed in Section 5.3.2 Power Domains.
- All the GPIOs: 30 (GPIO) + 10 (ULP-GPIO) + 3 (UULP Vbat GPIO)
- Complete SRAM of 328 Kbytes (Low Power (LP)-SRAM and ULP-SRAM).
- PS4 wakeup time is around 1.2 msec

5.3.3.2 PS3

This is an active state where the complete functionality is available, similar to PS4 state, but it operates at a lower voltage, thereby reducing current consumption. The CPU, peripherals, and SRAM operate on the SoC LDO supply with output voltage of 1.05 V. The Maximum CPU frequency is limited to 90 MHz in this state.

5.3.3.3 PS2

This is an active state where a limited set of functionality is available, and the device operates at a much lower voltage compared to PS3/PS4, thereby achieving lower current consumption. The CPU, peripherals, and SRAM can operate at different voltages and are configurable by software before entering this state.

The functionalities available in this state are mentioned below:
- CPU operating frequency depends on the voltage source selected for PS2 state. The CPU operates on the ULP-Peripheral AHB Interface clock.
  - If LDO 0.75 V is used, maximum frequency is 20 MHz.
  - If SC-DC 1.05V is used, maximum frequency is 32 MHz.
- APPLICATIONS - DEBUG, FPU, and ROM.
- Limited peripherals consisting of ULP-PERIPHERALS, UULP-PERIPHERALS and Analog-PERIPHERALS - as listed in Table 5.1 List of Power Domains on page 17.
- 13 GPIOs are available - 10 (ULP-GPIO) + 3 (UULP Vbat GPIO)
- Total SRAM of 328 KB (Low Power (LP)-SRAM and ULP-SRAM).
- PS2 wakeup time is around 200 μsec

5.3.3.4 PS1

This state can be entered from PS2 only through a software instruction. The CPU is power-gated, and a limited set of peripherals are active. The peripheral interrupts are used as wakeup sources or to trigger sleep once the peripheral functionality is complete. The peripherals and SRAM operate at the same voltage as the PS2 state. The peripherals need to be configured by the software for the defined functionality in the PS2 state before entering this state.

The functionalities available in this state are mentioned below:
- Limited peripherals consisting of ULP-PERIPHERALS, UULP-PERIPHERALS, and Analog-PERIPHERALS - as listed in Table 5.1 List of Power Domains on page 17.
- 13 GPIOs are available - 10 (ULP-GPIO) + 3 (UULP Vbat GPIO)
- SRAM of 320 KB (Low Power (LP)-SRAM) can be retained in this state.
- SRAM of 8 KB (ULP-SRAM) is active for peripheral functionality.

5.3.3.5 STANDBY

This includes multiple states: PS4-STANDBY, PS3-STANDBY, and PS2-STANDBY. These are standby states entered from PS4/PS3/PS2 states through a WFI instruction. CPU is clock gated in this state.

All the interrupts in the NVIC table will act as a wakeup source in the PS4-STANDBY and PS3-STANDBY states. Wakeup sources for the PS2-STANDBY state are defined in the wakeup sources section below. See Section 5.3.5 Wakeup Sources for details.

5.3.3.6 SLEEP

This includes multiple states: PS4-SLEEP, PS3-SLEEP, and PS2-SLEEP. These sleep states can be entered from the PS4, PS3, and PS2 states respectively through a software instruction.

The status of resources in this state are as follows:
- UULP-PERIPHERALS and Analog-PERIPHERALS are available and are configured before entering this state.
- 3 GPIOs are available - 3 (UULP Vbat GPIO)
- SRAM can be retained.

Wakeup sources for these states are defined in Section 5.3.5 Wakeup Sources. While transitioning from sleep to active state, all the configuration related to peripheral registers are set to default.

5.3.3.7 PS0

This is a shutdown state entered from PS4 state through a software instruction. The CPU is power-gated, and a much smaller set of peripherals are available.

The status of resources in this state are
- UULP-PERIPHERALS and Analog-PERIPHERALS are available and are configured before entering this state.
- 3 GPIOs are available - 3 (UULP Vbat GPIO)
- SRAM can not be retained.

5.3.4 Memory Retention in Sleep / Shutdown States

The table below indicates the SRAM banks and Backup Register Array which can be retained in each Sleep/Shutdown state.

Table 5.3. SRAM in Different States

S.No	Power State	LP-SRAM (320KB)	ULP-SRAM (8KB)	Backup Register Array (32 bytes)
1	PS4-SLEEP	Yes	Yes	Yes
2	PS3-SLEEP	Yes	Yes	Yes
3	PS2-SLEEP	Yes	Yes	Yes
4	PS1	Yes	Yes	Yes
5	PS0	No	No	Yes

5.3.5 Wakeup Sources

The table below indicates the wakeup sources available in Standby/Sleep/Shutdown states.

Table 5.4. List of Wakeup Sources in Different States

S.No	Wakeup Source	PS2-STANDBY	PS4-SLEEP/ PS4-STANDBY	PS3-SLEEP/ PS3-STANDBY	PS2-SLEEP	PS1	PS0
1	UULP Vbat GPIO	Yes	Yes	Yes	Yes	Yes	Yes
2	Watch-Dog Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
3	Analog Comparator	Yes	Yes	Yes	Yes	Yes	Yes
4	BOD	Yes	Yes	Yes	Yes	Yes	Yes
5	ULP-Peripheral SDC	Yes	No	No	No	Yes	No
6	Wireless Processor Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
7	Deep-Sleep Timer Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
8	Alarm Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
9	Second Based Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
10	Milli-Second Based Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
11	ULP-Peripheral GPIO Group Interrupt	Yes	No	No	No	Yes	No
12	ULP-Peripheral GPIO Pin Interrupt	Yes	No	No	No	Yes	No
13	ULP-Peripheral SPI/SSI Primary Interrupt	Yes	No	No	No	Yes	No
14	ULP-Peripheral IR Interrupt	Yes	No	No	No	Yes	No
15	ULP-Peripheral I2S Interrupt	Yes	No	No	No	Yes	No
16	ULP-Peripheral I2C Interrupt	Yes	No	No	No	Yes	No
17	ULP-Peripheral UART Interrupt	Yes	No	No	No	Yes	No
18	ULP-Peripheral ADC/DAC Interrupt	Yes	No	No	No	Yes	No
19	ULP-Peripheral DMA Interrupt	Yes	No	No	No	Yes	No

S.No	Wakeup Source	PS2-STANDBY	PS4-SLEEP/ PS4-STANDBY	PS3-SLEEP/ PS3-STANDBY	PS2-SLEEP	PS1	PS0
20	ULP-Peripheral GPIO Wakeup Interrupt	Yes	No	No	No	Yes	No
21	ULP-Peripheral Touch Sensor Interrupt	Yes	No	No	No	Yes	No
22	ULP-Peripheral Timer Interrupt	Yes	No	No	No	Yes	No

5.4 Digital and Analog Peripherals and Interfaces

In addition to the wireless interfaces, the SiWG917 provides a rich set of peripherals and interfaces - both digital and analog - thus enabling varied systems and applications. The following are the categories of the peripherals and interfaces, description of each category, and list of the peripherals in that category.

5.4.1 Digital Peripherals and Interfaces

5.4.1.1 I^2C

- Up to three I^2C primary/secondary controllers - two in MCU HP peripherals and one in the MCU ULP subsystem
- I^2C standard compliant bus interface with open-drain pins
- Configurable as Primary or Secondary
- Four speed modes: Standard Mode (100 kbps), Fast Mode (400 kbps), Fast Mode Plus (1Mbps), and High-Speed Mode (3.4 Mbps)
- 7 or 10-bit addressing
- 7 or 10-bit combined format transfers
- Support for Clock synchronization and Bus Clear
- Programmable SDA Hold time

The I^2C controllers also support additional features listed below to reduce the load on the M4 processor:
- Integrated transmit and receive buffers with support for DMA
- Bulk transmit mode in I^2C Secondary mode
- Interrupt based operation (polled mode also available)

5.4.1.2 UART/USART

- Up to two UART and one USART controllers
- 9-bit serial data support
- Multi-drop RS485 interface support
- 5, 6, 7, and 8-bit character encoding with even, odd, and no parity
- 1, 1.5 (only with 5 bit character encoding) and 2 stop bits
- Hardware Auto flow control (RTS/CTS)
- IrDA 1.0 SIR mode support (only for USART1) with up to 115.2 K baud data rate and programmable pulse duration and low-power reception capabilities

The UART controllers also support additional features which are listed below and which help in achieving better performance and reducing the burden on the M4 processor:
- Programmable fractional baud rate support
- Programmable baud rate supporting up to 5 Mbps
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Prioritized interrupt identification

The following features are supported by the USART controller in the MCU HP peripherals (USART1):
- Support for both synchronous and asynchronous modes.
- Supports full duplex and half duplex (single wire) mode of communication.
- 1-9 bit wide character support.
- Supports programmable baud rates up to 20 Mbps in synchronous mode
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events.

The UART controller in the MCU ULP subsystem (ULP_UART) supports the following additional power-save features:
- After the DMA is programmed in PS2 state for UART transfers, the MCU can switch to PS1 state (M4 processor is turned off) while the UART controller continues with the data transfer
- In PS1 state (ULP Peripheral mode) the UART controller completes the data transfer and, triggered by the peripheral interrupt, shifts to the PS2 active state.

5.4.1.3 I^2S / PCM

- Up to two I^2S controllers
- Each I^2S supports PCM mode of operation
- The I2S_2CH supports two stereo channels while the ULP_I2S and the NWP/Security subsystem I^2S support one stereo channel
- Programmable audio data resolutions of 12, 16, 20, 24, and 32 bits.
- Supported audio sampling rates are 8, 11.025, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, and 192 kHz
- Support for primary and secondary modes
- Full duplex communication due to the independence of transmitter and receiver

The PCM mode of operation supports the following additional features:
- Mono audio data is supported
- Supports two modes for data transmission with respect to the Frame Synchronization signal – the MS bit is transmitted in the same clock cycle that the Frame Synchronization signal is asserted or one clock cycle after the Frame Synchronization signal is asserted
- Programmable FIFO thresholds with maximum FIFO depth of 8 and support for DMA
- Supports generation of interrupts for different events

The I^2S in the MCU ULP subsystem supports the following additional power-save features:
- After the DMA is programmed in PS2 state for I^2S transfers, the MCU can switch to PS1 state (M4 processor is turned off) while the I^2S controller continues with the data transfer
- In PS1 state (ULP Peripheral mode) the I^2S controller completes the data transfer and, triggered by the Peripheral Interrupt, shifts to the PS2 active state.

5.4.1.4 Quadrature Encoder Interface (QEI)

- Tracks encoder wheel position
- Programmable for 1x, 2x, or 4x position counting. Increments/decrements depending on direction.
- Index counter for revolution counting
- Velocity capture using built-in timer
- Supports position counter reset for rollover/underflow or index pulse
- Position, index, and velocity compare registers with interrupts
- Supports logically swapping the A and B inputs
- Accepts decoded signal inputs (clock and direction) in timer mode

5.4.1.5 Motor Control PWM

- Part of the MCU HP peripheral subsystem
- Supports up to eight PWM outputs with four duty cycle generators
- Complementary and independent output modes are supported
- Dead time insertion in complementary mode
- Manual override option for PWM output pins. Output pin polarity is programmable.
- Supports generation of interrupt for different events
- Supports two hardware fault input pins
- Special event trigger for synchronizing analog-to-digital conversions

5.4.1.6 Synchronous Serial Interface (SSI) Primary

- Up to two Synchronous Serial Interface (SSI) primaries
- The SSI_MST provides an option to connect up to four secondaries and supports single, dual, and quad modes.
- The ULP_SSI_MST supports single-bit mode and can be connected to only one secondary
- Programmable receive sampling delay

In addition to the above features, the SSI primaries reduce the load on the M4 processor by supporting the features below:
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events
- Programmable division factor for generating SSI clock out

The ULP_SSI_MST supports the following additional power-save features:
- After the DMA is programmed in the PS2 state for SSI transfers, the MCU can switch to PS1 state (M4 processor is turned off) while the SSI primary continues with the data transfer.
- In PS1 state (ULP Peripheral mode), the SSI primary completes the data transfer and, triggered by the peripheral interrupt, shifts to the PS2 active state.

5.4.1.7 Synchronous Serial Interface (SSI) Secondary

- Support for SSI Primaries which comply with Motorola SPI, TI SSP and National Semiconductors Microwire protocols
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events

5.4.1.8 Serial Input Output (SIO)

- Can be used to implement serial interfaces like I^2C, UART, and SPI protocols
- Supports eight GPIO pins
- Supports eight SIOs
- Supports pattern matching
- Performs serial-to-parallel and parallel-to-serial conversion
- Provides DMA flow control signals
- Supports generation of interrupt for different events.
- Programmable clock division factors for generating SIO clock out

5.4.1.9 Configurable Timers

- Supports 4 configurable inputs and 8 outputs signals for 4 configurable timers.
- Supports one 32-bit configuration timer
- 32-bit timer can be configured to contain one 32-bit or two 16-bit timers. The timer accepts clocks or events as input tick.
- Wide range of features like starting the counter, stopping the counter, continuing the counter from the stopped value, halt, increment the counter and capturing the events
- Support for PWM signals as output with any cycle/pulse length and superimpose a waveform on the PWM signal. It can start the ADC at any time in sync with PWM signal
- Support for DMA flow control
- Generates interrupt for different events

5.4.1.10 CRC Accelerator

- Part of MCU HP peripheral subsystem
- Support for one 32 bit polynomials
- Support for one 32 bit stream-in data widths
- Supports DMA flow control

5.4.1.11 Enhanced GPIO (EGPIO)

- Two EGPIO controllers - one in MCU HP and MCU ULP subsystem
- Supports various alternate functions like set, clear, toggle on all the pins
- Option to program Mode for each GPIO pin independently
- Supports edge and level detection based interrupt generation

5.4.1.12 Generic SPI (GSPI) Primary

- Part of MCU HP peripheral subsystem
- Supports single bit SPI primary mode.
- Support for Mode-0 and Mode-3 (Motorola)
- Supports both Full speed and High speed modes
- SPI clock out is programmable to meet required baud rates
- Support for full duplex mode
- Connect up to four SPI peripheral devices
- Support byte swapping during read and write operation
- Support up to 32 KB of read data from a SPI device in a single read operation
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Generates interrupt for different events

5.4.1.13 Hardware Random Number Generator (HRNG)

- Part of MCU HP peripheral subsystem
- Supports 32-bit True Random Number Generator
- Supports 32-bit Pseudo Random Number Generator
- Option to selectively enable these random number generators

5.4.1.14 General Purpose DMA (GPDMA)

- Two primaries interface over AHB bus
- Supports 8 channels
- Linked-list based descriptors
- Has two AHB primaries for parallel data transfer. The Primary is selectable for descriptor fetch, per channel and per source and destination
- Dynamically configurable FIFO for 8 channels
- Programmable source and destination burst sizes
- Programmable beats per bursts
- Source and Destination address alignment
- Programmable Transfer Types: Memory to Memory, Memory to Peripheral and Peripheral to Memory
- Programmable priority encoded arbiter
- Supports generation of interrupt for different events
- Support for DMA squash
- Support for memory Zero Fill and One Fill

5.4.1.15 Micro DMA (µDMA)

- Supports 32 channels
- Each DMA channel has dedicated handshake signals and programmable priority level
- Supported transfer types: memory-to-memory, memory-to-peripheral, peripheral-to-memory
- Supports multiple DMA cycle types and transfer data widths
- Programmable number of transfers in a single DMA cycle
- Average throughput is four cycles per one word reading
- Each DMA channel can access a primary, and alternate, channel control data structure
- Supports generation of interrupt for different events
- Support half-word (16 bit) and word (32 bit) size transfers

5.4.1.16 eFuse Controller

- Provides 32 bytes eFuse as one-time programmable memory locations
- Supports eFuse programming and read operations
- Supports memory mapped and FSM based read operation

5.4.1.17 SPI Flash Controllers

A serial Flash device is a non-volatile memory that can be electrically erased and reprogrammed. It is used for storing executable code or data readily available for M4/TA processor. After power-up, the executable code is read by the M4/TA processor from the serial Flash and then executed. The code in the serial Flash is write-protected and cannot be altered.

Reasons for the widespread use of serial Flash devices include:

• Non-volatile memory
• Cost effective and space-saving solution thanks to a reduced number of pins
• Life cycle of about 20 years

Serial Flash memories are controlled by many kinds of serial interface protocols (SPI, SSP, SSI, SMI, etc.). SiWG917M chips support a SPI based flash. SPI Flash memory is a secondary device.

To access it, dedicated SPI Flash controller is present which is Primary.

SiWG917M has SPI Flash Controller which has 2/4/8 - wired interface for serial access of data from Flash. Dedicated SPI controllers are present for Flash. It can be used in either Single, Dual, Quad or Octa modes with support for SDR to read the processor's instructions and for data transfers to/from the Flash. The Controller supports inline decryption of encrypted instructions read from the Flash before they are passed on to the M4/TA processor's Instruction Cache. Instructions are read using the Direct Access mode while data transfers use the Indirect Access mode in case of Flash. The SPI Controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with Flash ICs. The Direct Access mode is used to read instructions and data directly from Flash. It supports inline decryption using an AES engine for the instructions or data transfer with Flash. The Indirect Access mode is used to read and write data/instructions from Flash. The two modes - Direct Access and Indirect Access - can be used to access the same Flash or two different Flashes (using CSN0 and CSN1) at a time by enabling hardware controlled mode. The SPI Controllers have independent AHB secondaries for these modes of access.

The SiWG917M can use a single Common SPI flash for executing instructions by both TA and M4 processors. Each processor has dedicated SPI Flash controller(QSPI). Dynamic arbitration has taken place between two controllers without any processor intervention for executing instructions from common flash. Arbitration multiplexes the two SPI interfaces into a single SPI interface connected to the flash. The flash memory is partitioned into two parts dedicated to each processor respectively.

There are two flash configurations available.

Flash Configurations

1. Common Flash
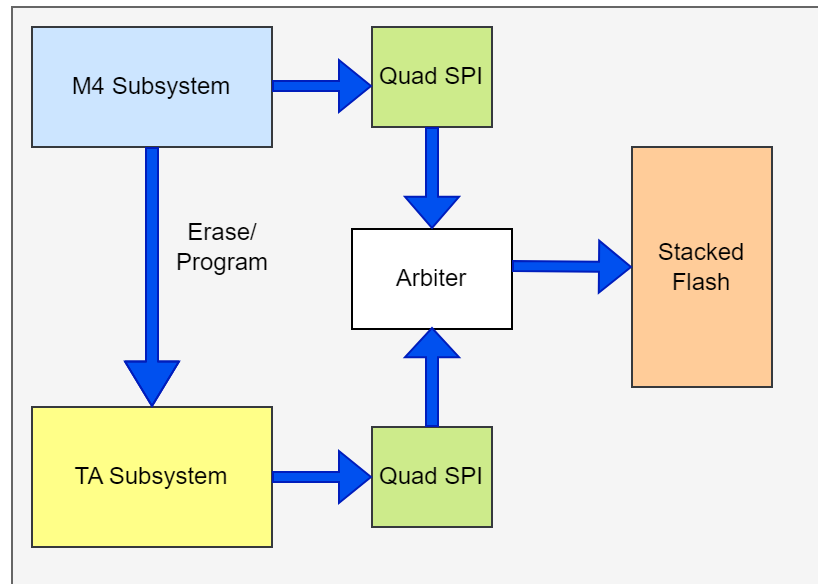
In this case, Flash is shared between both TA and M4 processors. Flash Initialization, configuration, program and erase can be done only by TA processor. M4 processor can do only instruction fetching in direct access mode. Flash memory is divided into two regions, one each for the processor. M4 can only read M4 assigned memory region. TA has no restriction and it can access complete Flash memory.

2. Dual Independent Flashes
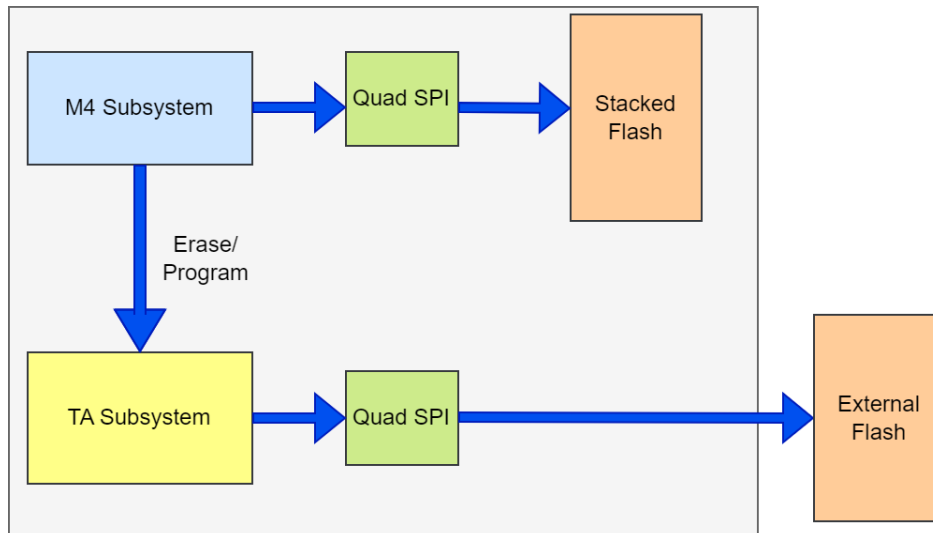
Each processor has its own dedicated Flash memory. In this configuration, M4 can access complete Flash memory. M4 can do Flash Initialization, configuration, program and erase.

The features of SPI Flash Primary controller is given below.

- Supports Single/Dual/Quad/Octal (S/D/Q/O) modes for reading M4/TA processor instructions and data transfers to/from Flash.
- Support for SPI Mode-0 and Mode-3
- Support for SDR mode Flash
- Supports both 8 and 16-bit Flash commands.
- Support both 24 and 32-bit addressing modes
- Supports inline decryption (AES) in XTS/CTR mode with 128-bit and 256-bit key sizes while reading encrypted instructions from the Flash
- Supports up to two Flashes connected to CSN0 and CSN1

- Direct Access Mode:
  - Instructions are read from Flash using the Direct Access mode which does not need any processor involvement after the initial configuration of the Controller. The read command used for this mode is programmable depending on the Flash used.
  - Direct Access mode supports Wrap / Incremental / Single read operations.
  - Supports prefetch option - enabling this option makes the SPI Controller prefetch the next instruction before the request is posted on the internal AHB bus. If the address for the next instruction is different from the prefetch address, the instruction is scrapped.
  - Supports continuous fetch option to reduce instruction fetch delay from Flash - this option makes the SPI controller to post the Command and Address only once on the bus to read contiguous instructions by controlling only the CSN.
  - Supports programmable CSN high time.
- Indirect Access Mode:
  - Configuration of Flash and reading/writing data from/to the Flash uses the Indirect Access mode which requires the M4/TA processor to program the SPI Flash controller for each access.
  - Supports reading of up to 32KB bytes of data from Flash in a single read operation.
  - In addition to 24 and 32-bit addressing, the SPI Controller supports 9, 10 and 16-bit addressing in this mode.
- Common flash mode - Flash can be accessed by both MCU and mutli-threaded processor simultaneously
- Clock Configuration
  - Support for selection of source clock between AHB bus clock and PLL clock.
  - Support for even division factors up to 64 to generate the SPI clock from the source clock.
- Transmission of Extra-byte after the address phase is supported. The contents of this byte are programmable. There is also an option to only transmit the first nibble of the extra byte and maintain a Hi-z on the bus for the next nibble.
- Each phase of a Read operation (Command, Address, Dummy Byte, Extra Byte, Read Data) can be in any of the S/D/Q/O modes depending on the Flash requirements.
- The number of dummy bytes is programmable and can be programmed as per the instruction and the mode of operation.
- Supports DMA flow control and programmable FIFO thresholds
- Supports interrupt generation based on different events
- Supports dual Flash mode - reading of data from two flashes simultaneously
- Supports Flash Write Protect

The SPI Controller in the MCU has been designed with programmable options for most of the single and multi-bit operations so that it can interface with the Flash ICs from multiple vendors. The list of supported Flashes and vendors is given below:

5.4.1.18 SPI PSRAM Controllers

For applications that require additional RAM, an additional external RAM can be added in the form of pseudo static RAM (PSRAM). The PSRAM is an additional RAM of size that is selected e.g. 2/4/8/16MB.

PSRAM memory is a QSPI secondary device. M4 microcontroller communicates with the PSRAM through dedicated Quad SPI Primary controller.

The SiWG917M has SPI PSRAM Controller which has 2/4/8 - wired interface for serial access of data from PSRAM. Dedicated SPI controllers are present for PSRAM. It can be used in either Single, Dual or Quad modes with support for SDR to read the M4 processor's instructions and for data transfers to/from the PSRAM. The Controller supports inline decryption of encrypted instructions read from the PSRAM before they are passed on to the M4 processor's Instruction Cache. The SPI Controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with PSRAM ICs. The Direct Access mode is used to read instructions and read/write data directly to/from PSRAM. It supports inline decryption using an AES engine for the instructions or data transfer with PSRAM. The Indirect Access mode is used to read and write data/instructions from PSRAM. The two modes - Direct Access and Indirect Access - can be used to access the same PSRAM or two different PSRAM (using CSN0 and CSN1) at a time by enabling hardware controlled mode. The SPI Controllers have independent AHB secondaries for these modes of access.

The features of SPI PSRAM Primary controller is given below.
- Supports Single/Dual/Quad (S/D/Q/O) modes for reading M4 processor instructions and data transfers to/from PSRAM.
- Support for SPI Mode-0.
- Supports full duplex mode in single-bit SPI mode. Support for HOST SPI secondary interface.
- Support for SDR mode PSRAMs
- Supports both 8 and 16-bit PSRAM commands.
- Support both 24 and 32-bit addressing modes
- Supports only AES CTR mode encryption and decryption of PSRAM data with 128-bit and 256-bit key sizes
- Supports up to two PSRAMs connected to CSN0 and CSN1
- Supports Direct mode write
- Supports semi direct mode read operation for PSRAM
- Direct Access Mode:
  - Data transfer from/to PSRAM using the Direct Access mode which does not need any M4 processor involvement after the initial configuration of the Controller. The read/write command used for this mode is programmable depending on the PSRAM used.
  - Direct Access mode supports Wrap / Incremental / Single read operations.
  - Supports prefetch option - enabling this option makes the SPI Controller prefetch the next instruction before the request is posted on the internal AHB bus. If the address for the next instruction is different from the prefetch address, the instruction is scrapped.
  - Supports continuous fetch option to reduce instruction fetch delay from PSRAM - this option makes the SPI controller to post the Command and Address only once on the bus to read contiguous instructions by controlling only the CSN.
  - Supports programmable CSN high time.
- Indirect Access Mode:
  - Configuration of PSRAM and reading/writing data from/to the PSRAM uses the Indirect Access mode which requires the M4 processor to program the SPI controller for each access.
  - Supports reading of up to 32KB bytes of data from PSRAM in a single read operation.
  - In addition to 24 and 32-bit addressing, the SPI Controller supports 9, 10 and 16-bit addressing in this mode.
- Clock Configuration
  - Support for selection of source clock between AHB bus clock and PLL clock.
  - Support for even division factors up to 64 to generate the SPI clock from the source clock.
- Each phase of a Read operation (Command, Address, Dummy Byte, Extra Byte, Read Data) can be in any of the S/D/Q/O modes depending on the PSRAM requirements.
- The number of dummy bytes is programmable and can be programmed as per the instruction and the mode of operation.
- Supports DMA flow control and programmable FIFO thresholds
- Supports configurable memory ranges on which we can save code in encrypted form and the execution will happen with inline decryption.
- Supports dual PSRAM mode - reading and writing from/to two PSRAM simultaneously
- Supports interrupt generation based on different events

The SPI Controllers in the MCU has been designed with programmable options for most of the single and multi-bit operations so that it can interface with PSRAM ICs from multiple vendors. The list of supported PSRAMs and vendors is given below:

Table 5.5. PSRAMs

S.No.	Vendor	Part #	Flash Density (in Mbit)	Vcc	Bus Width
1	AP memory	APS1604M-SQR	16	1.65-1.95	1/2/4-bit
2	AP memory	APS6404L-SQRH	64	1.65-1.95	1/2/4-bit
3	ISSI	IS66/67WVS2M8ALL	16	1.65-1.95	1/2/4-bit
4	ISSI	IS66/67WVS4M8ALL	32	1.65-1.95	1/2/4-bit
5	ISSI	IS66/67WVS2M8BLL	16	1.65-1.95	1/2/4-bit
6	ISSI	IS66/67WVS4M8BLL	32	1.65-1.95	1/2/4-bit

5.4.1.19 Watchdog Timer

The WatchDog Timer is used to generate an interrupt on timeout and a reset in case of system failure which can be caused by an external event like ESD pulse or due to a software failure. Also the Interrupt can be used as a Wakeup source for transitioning from SLEEP/STANDBY to ACTIVE states.

- Independent watchdog timer.
- Interrupt is generated before the system reset is applied which can be used as a wakeup source.
- Generates reset upon Lockup indication from M4 processor.
- Configurable low frequency clock (32KHz RO, RC and Xtal).
- Configurable timeout period.
- Able to operate when CPU is in SLEEP state during power-save applications
- Individually controllable power domain for low-power applications.

5.4.1.20 Calendar

Calendar block acts a RTC with time in seconds, minutes, hours, days, months, years and centuries. The real-time can also be read through APB with accuracy less than a second by reading the millisecond count value and further less also by reading the number of counts of APB clock in 1 millisecond of RTC clock. Accuracy is high.

- Calendar block can provide a seconds trigger and also a msec trigger.
- Calendar block takes care of no. of days in each month and also leap years. It can count up to 4 centuries.
- Real time is readable through APB and also programmable through APB.
- Option to choose either RC clock RO clock as calendar clock.

5.4.1.21 General Purpose Timers

The MCU Timer block supports four 32-bit timers, which can be used to generate various timing events for the software. Each of the four timers can be independently programmed to work in periodic or one-shot mode and can be configured either as a microsecond timer or as a counter.

- Four independent 32bit timers
- Supports per timer enable and disable.
- Option to configure each timer as a 32-bit counter or 32-bit microsecond timer.
- Supports 1µs mode and 256µs modes per timer.
- Accounts for integral and fractional value of the time units programmed.
- Microsecond timer supports two modes:
  - 1 Microsecond mode: The time unit is 1µs. Number of microseconds required to be counted has to be programmed.
  - 256microsecond mode: The time unit is 256µs. Number of 256µs units required to be counted has to be programmed. This is useful when the timer is being used for counting large time values and microsecond based tracking not required.
- One shot and periodic modes per timer.
- Option to interrupt the M4 processor on timeout.

5.4.1.22 Secure Storage

The Block is used for storing configuration values with data protection feature.

- MCU has 3 set's for storage block
  - First chunk is 64 bits
  - Second chunk is 64 bits
  - Third Chunk is 128 bits
- Each chunk is a power domain.
- Secure mode is available for first and second Chunk.
- Storage space can be used for storing Configuration values

5.4.1.23 MVP

The Matrix Vector Processor (MVP) accelerates floating point operations, particularly matrixed complex floating point multiplies and additions. The MVP was designed to offload the major computations of the Angle-of-Arrival (AoA) MUSIC algorithm, although the architecture can generally be used to accelerate other heavily floating-point computational problems such as Machine Learning (ML), Eigen, or BLAS acceleration.

- General purpose instruction set tailored towards algorithms built out of ALU, loop, and load/store instructions
- Enables many high-level array functions, e.g.:
  - Matrix multiplication
  - Element-wise matrix multiplication
  - Matrix addition
  - Power series generation
  - Convolution
- Program flexibility allows efficient iteration over N-D Array elements, including in-place processing of special Matrix views:
  - Element-wise Negate/Conjugate
  - Transpose/Adjoint/Reverse
  - Matrix Blocks (i.e., rectangular parts of matrix)
  - Matrix Slices (i.e., taking rows, columns, or elements uniformly spaced within a matrix)
  - Row-major or column-major ordering
  - Arithmetic Logic Unit (ALU)
- Three 32-bit floating-point input operands, interpreted as real or complex numbers
- Partial integer input support
- One 32-bit floating-point output operands, interpreted as real or complex numbers
- Register bank to hold all input/output operands
- Includes 8 registers for temporary storage and/or accumulation
- Hardware to support 1 complex floating point multiply-accumulate (MAC) per cycle
- Four single-precision floating-point multipliers and adders
- Operations supported at a rate of one operation per cycle:
  - Complex addition, multiplication, and MAC operations
  - Parallel Real multiplication and MAC
  - Parallel Real addition
  - Sum of 4 reals
  - Squared-magnitude of complex/real
  - Integer-to-float conversion
  - Conditional computation
  - Input transformations (per real/complex part of each input)
  - Negation (complex conjugate)
  - Zero-masking (real/imag part decomposition)
- Load/Store Unit (LSU)
- Controls data streaming from Memory to ALU and vice versa
- Pipelined architecture to support two simultaneous 32-bit memory reads and one 32-bit memory write per cycle
- Supports int8/uint8 conversion for both load and store operations
- First-party Direct Memory Access ports (i.e., bus primaries)
- Used by load/store unit for handling accesses to external (system) memory addresses
- Three independent 32-bit AHB primary ports for supporting 2 read channels and 1 write channel simultaneously
- Sequencer
- Coordinates all MVP blocks to execute a sequence of instructions provided via the programming interface
- Handles Array iteration according to instruction sequence and static Array configuration
- Handles Loop iteration according to instruction sequence and static Loop configuration
- Programming interface
- Control registers for starting/stopping engine
- Status registers about ongoing and finished instruction sequences
- Fault status
- Useful information for debug

- Breakpoint and Stepping Controls for Debug
- Interrupts and faults
- Instruction sequence completion
- Bus faults
- Loop faults
- Array faults
- Array configuration registers
- Loop configuration registers
- Instruction queue registers
- Array iteration
- ALU operations
- Looping

5.4.1.24 SYSRTC

The SYSRTC (System Real Time Clock) is a highly configurable RTC capable of serving multiple cores. It contains up to 8 groups, where the number of compare- and capture-channels within each group is parameterized individually. Each group has it's own interrupt- and configuration-registers. The main idea is to save power by letting all groups share a single counter.

- 32-bit counter
- 32 kHz / 1kHz intended operation
- Low energy mode and wake-up
- Up to 8 groups
- 1-2 compare channels per group
- 0-1 capture channel per group
- Optional debug halting
- Optional alternate interrupt/wake-up per group
- Software Reset

5.4.2 Analog Peripherals and Interfaces

5.4.2.1 Capacitive Touch

- 8 input channels - all the input channels are shared with GPIOs
- 1 shield channel - To reduce sensitivity to mesh capacitance
- Capacitive input and resistor input are connected to two GPIOs each
- Programmable input clock source from the available clocks in the chip
- Controls the rate of scanning for all sensors with configurable inter sensor scan ON time
- Supports both samples streaming and cumulative average mode
- DMA capable
- 8, 16 and 32-bit pseudo-random number for generating two non overlapping streams with configurable delay
- Programmable polynomial and seed values for pseudo-random number generator
- Provides wake up indication after capacitive touch sensing

5.4.2.2 Analog to Digital Converter (ADC)

The ADC with up to 12 bits of resolution at 5 MSPS
- 12 bit ADC Output in 2's complement representation
- GPIOs in High Power mode for ADC Operation
  - Signal Ended Mode
    - 17 External configuration selection
    - 5 Internal configuration selection
      - Internal Temperature sensor
      - 3 Opamp Outputs
      - DAC output for internal reference
  - Differential Mode
    - 8 external differential mode configuration selection
    - 4 Internal configuration selection.
      - 3 Opamp Outputs
      - DAC output for internal reference
- GPIOs in Low Power mode for ADC Operation
  - Signal Ended Mode
    - 11 External configuration selection.
    - 5 Internal configuration selection.
      - Internal Temperature sensor.
      - 3 Opamp Outputs
      - DAC output for internal reference
  - Differential Mode
    - 5 external differential mode configuration selection.
    - 4 Internal configuration selection.
      - 3 Opamp Outputs
      - DAC output for internal reference
- 10MHz to 32KHz allowed ADC_CLK
- Configurable DMA to support 16 channels for storing AUXADC data in ULP SRAM.
- Measurement range 0 to AUXADC_VREF(1.8v to 3.3v)

The ADC has five modes of operation:
- Single ended input with noise averaging
- Single ended input without noise averaging
- Differential input with noise averaging
- Differential input without noise averaging
- Shutdown mode.

5.4.2.3 Digital to Analog Converter (DAC)

DAC can take 10 bit digital inputs and convert them into analog voltage within range 5*vdd/36 to 31*vdd/36. Vdd can vary from 1.8 volts to 3.63 volts.
- 10-bit resolution
- Single ended DAC
- Monotonic by design
- Max sampling frequency is 5MHz for DAC_CLK
- Supports Operational mode and Shutdown modes

5.4.2.4 OPAMP

- 3 general purpose Operational Amplifiers (OPAMP) offering rail-to-rail inputs and outputs.
- Each of the three opamps has 2 inputs (inp, inn) and 1 output.
- opamps can take inputs from GPIOs and their outputs can be seen on GPIOs
- configured in either low power mode or high power mode
- opamps can be configured as:
  - Unity gain amplifier
  - Trans-Impedance Amplifier(TIA)
  - Non-inverting Programmable Gain Amplifier (PGA)
  - Inverting Programmable Gain Amplifier
  - Non-inverting Programmable hysteresis comparator
  - Inverting Programmable hysteresis comparator
  - Cascaded Non-Inverting PGA
  - Cascaded Inverting PGA
  - Two opamps Differential Amplifier
  - Instrumentation Amplifier

5.4.2.5 Analog Comparators

Analog comparators peripheral consists of two analog comparators, a reference buffer, a scaler and a resistor bank. Both comparators can take inputs from GPIOs.

The comparator compares analog inputs p and n to produce a digital output, cmp_out according to:

p > n, cmp_out = 1

p < n, cmp_out = 0

The following cases of comparison are possible
- Compare external pin inputs
- Compare external pin input to internal voltages.
- Compare internal voltages.

The inputs of 2 comparators can be programmed independently. The reference buffer, scaler and resistor bank are shared between the two comparators and can be enabled only when atleast one of the comparators is enabled.

5.4.2.6 Temperature Sensor

There are two independent temperature sensors integrated. Ring Oscillator (RO) based temperature sensor and BJT based temperature sensor.

BJT based sensor works for temperature range from -40° to 125° and voltage variation from 1.8V to 3.63V. It outputs the digital word having resolution of nearly 1 degree C. The conversion time is 2 clock cycles of ADC after turning ON the temperature sensor.

RO based sensor outputs 2 clocks.

The temperature reading of the sensor is accessed by configuring the ADC inputs to temperature sensor

5.4.2.7 IR Decoder

This is a general purpose Infrared receiver, which can decode all IR protocol (RC5, NEC,.. etc) with Software intervention. It takes IR pulses from external IR sensor connected through GPIO's
- IR Decoder clocked by a low power 32 KHz RC clock
- Programmable Active and Sleep window duration for IR data monitoring

  Wakeup source to existing low power sleep state

5.5 Bootloader

The Bootloader controls the initial operation of the device after any form of reset. The Bootloader supports Flash programming and initial startup of the application code. Bootloader supports following features:

- Two Bootloaders - Security Bootloader and Application Bootloader
- Support for ISP (In-System Programming) through multiple interfaces - UART, SPI and SDIO
- Auto-detection of ISP interface. The host interfaces are the external peripheral interfaces over which Bootloader can receive commands or firmware when in ISP mode. The Bootloader supports UART, SPI and SDIO interfaces. Bootloader in ISP mode waits for data on any of these interfaces and can automatically detect which interface the data is being received.
- Support for secure boot
- Support for secure firmware upgrade using PUF based Roots-of-Trust (RoT)
- Anti-rollback protection. This feature prevents the firmware version from being downgraded. A new firmware is allowed to be upgraded only if it is be equal to or greater than the current firmware.
- Secure Key Management and Protection
- Support for different flash protection levels and write-protected Flash
- Secure XIP from Flash
- Fail-proof migration of current active firmware to new (update) firmware
- Public key cryptography (digital signature) based authentication

The SiWG917 includes two Bootloaders - Security Bootloader and Application Bootloader. The Security Bootloader runs on the Security processor and the Application Bootloader runs on the Cortex M4 processor. On any reset, execution will always start in Security Bootloader, which is responsible for all security features, ISP and firmware upgradation. Once the Security Bootloader finishes its tasks, it enables the Application Bootloader. The Application bootloader will load and execute the application and also execute wakeup sequence on wakeup from sleep.

The following are the sources, which can trigger the Bootloader:
- Primary reset (RESET_N_PAD)
- Power on reset (POC_IN)
- Watchdog reset
- Black out monitor
- Reset request through SYSRESETREQn bit in the Cortex-M4 processor
- Wake-up from Sleep

5.6 Security

5.6.1 Security Features

- Secure Boot
- Secure OTA Firmware update
- TRNG : Generates high-entropy random numbers based on RF noise, increasing the effort/time needed to expose secret keys
- Secure Zone
- Secure Key storage : HW device identity and key storage with PUF
- Secure Debug
- Anti Rollback : Firmware downgrade to a lower version is prohibited through OTP to prevent the use of older, potentially vulnerable FW version
- Secure XIP from flash with XTS/CTR mode
- Secure Attestation : Allows a device to authenticate its identity using a cryptographically signed token and exchange of secret keys
- Hardware Accelerators: AES128/256/192, SHA256/384/512, HMAC, RNG, CRC, SHA3, AES-GCM/ CMAC, ChaCha-poly
- Software Accelerators: RSA and ECC
- Programmable Secure Hardware Write protect for Flash sectors

5.6.2 Secure Bootup

Key Features
- Ensures your device runs authentic code in the boot and OTA update to eliminate malware insertion threats
- Secure Immutable Bootloader in ROM.
- Authenticates signatures of all other SW using public keys.
- Protocol and Application flash images can be encrypted with separate keys.

On reset, the Security Bootloader configures the module hardware based on the configuration present in the eFuse. It also passes the required information from the eFuse to the Application Bootloader. The Security Bootloader validates the integrity and authenticity of the firmware in the Flash and invokes the Application Bootloader. It detects and prevents execution of unauthorized software during the boot sequence. The Bootloader uses public & private key based digital signatures to recognize authentic software. The Security Bootloader provides provision for inline execution (XIP) of encrypted firmware from Flash. The Bootloader provides 3 flash protection levels which can be used to secure different sections of the Flash for different purposes:

- Protection level 1: Stored at manufacturing, not allowed to modify by the Security Bootloader
- Protection level 2: Allowed to modify by the Bootloader only, usually used to maintain secure information used/consumed by Bootloader
- Protection level 3: Allowed to modify by the Bootloader only, usually used to maintain protected firmware images.

The protection levels are written to Flash during the manufacturing process. The write-protection feature prevents the application program from changing the Flash protection levels.

The Security configurations can be enabled or disabled during the manufacturing process.

5.6.3 Secure XiP

- Execute SW directly from Flash instead of copying it into RAM
- Images are saved in encrypted format and decrypted using device-specific PUF intrinsic keys while executing. In-line decryption based on-the-fly AES engine (based on PUF keys). Multiple protection levels can be set for flash, including unmodifiable. XTS/CTR modes supported.

5.6.4 Secure Firmware Upgrade

Secure firmware upgrade via host interface :

The secure firmware upgrade feature of the Bootloader checks the authenticity of the new firmware image along with its integrity. The Bootloader automatically detects the host interface in use and configures the host interface hardware accordingly. The Bootloader updates the image only after successfully validating the authenticity and integrity of the image. It prevents downgrade to a lower version of firmware using the anti-rollback feature, if it is enabled. The Bootloader also supports transparent migration to a wirelessly updated image and protection against failures by providing recovery mechanisms.

Secure OTA :

- Secure OTA update to eliminate malware insertion threats.
- Wireless and Application image transfer over the air.
- Wireless processor authenticates the signatures of OTA image using public keys
- Bootloader copies the OTA image to primary firmware location upon sucessful authentication .

5.6.5 Secure Zone

Key Features
- Barrier between the Security/Protocol core and Application core.
- No access to the security processor, memory, and HW registers from external peripherals, including the Cortex-M4

The Secure Zone is hardware enforced isolation between the trusted and non-trusted modules in the system. Secure zone protects the secure assets residing in secure execution environment by restricting direct access. It also provides a secure execution environment to store confidential data. The Bootloader configures Secure Zone, secure firmware upgrade and secure bootup in "Secure Zone enabled" mode. This mode is programmed during the manufacturing process.

5.6.6 In-System Programming (ISP)

In System Programming (ISP) is programming or reprogramming of the flash through boot loader using UART, SPI, and SDIO (GPIO-25 to GPIO-30) interfaces. This can be done after the part is integrated on end-user board. Boot loader can be requested to boot in ISP mode by pulling down a specific GPIO pin. This pin has to be left unconnected during reset for the boot loader to bypass ISP and execute the code that is present in flash. ISP mode can be used to reprogram the flash, if the application codes use JTAG pins for functional use. On boot up, if the application code goes into a state where JTAG interface is not functioning, ISP mode can be used to gain the control and to reprogram the flash.

5.6.7 Debug Lock

Key Features

- Debug ports are disabled in HW by default.
- It can be enabled in SW using cryptographically secure host interface commands validated by immutable bootloader
- It allows the device's JTAG ports to be locked and unlocked.

5.7 Debug Support

MCU implements complete hardware debug solution. This provides high system visibility of the M4 processor and memory through either a traditional JTAG port or a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices.

In Serial Wire Viewer (SWV) mode, a one-bit serial protocol is used and this reduces the number of output signal to one. When combining SWV with Serial-Wire debug protocol, the Text Data Output (TDO) pin normally used for Joint Test Action Group (JTAG) protocol can be shared with SWV.

The Embedded Trace Macrocell (ETM) provides high bandwidth instruction trace via four dedicated trace. The MCU_CLK_OUT frequency must be in the range of 40Mhz to 90MHz to Instruction trace using ETM component.

5.8 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
- Support for 20 MHz channel bandwidth for 802.11n and 802.11ax.
- Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi + BLE
- Wi-Fi 6 Features: Individual Target wake-up time (iTWT), Broadcast TWT (bTWT),SU extended range (ER), DCM (Dual Carrier Modulation), DL MU-MIMO, DL/UL OFDMA, MBSSID, BFRP, Spatial Re-use, BSS Coloring, and NDP feedback up to 4 antennas
- Integrated PA
- Data Rates—802.11b: up to 11 Mbps; 802.11g: up to 54 Mbps; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
- Operating Frequency Range [MHz]: 2412-2462 (North America, default), 2412-2472 (Europe, and other countries where applicable), 2412-2484 (Japan)

5.8.1 MAC

- Conforms to IEEE 802.11b/g/n/j/ax standards for MAC
- Hardware accelerators for AES
- WPA, WPA2, WPA3 and WMM support
- AMPDU aggregation for high performance
- Firmware downloaded from host based on application
- Hardware accelerators for DH (for WPS) and ECDH

5.8.2 Baseband Processing

- Supports 11b: DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates
  - 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
  - 802.11ax, 802.11n: MCS 0 to MCS 7
- High-performance multipath handling in OFDM, DSSS, and CCK modes

5.9 Bluetooth

Key Features
- Transmit power up to +16.5 dBm with integrated PA
- Receive sensitivity — LE: -95 dBm, LR 125 Kbps: -106 dBm
- Operating Frequency Range — 2.402 GHz - 2.480 GHz
- Supports Bluetooth® Low Energy (LE): High Speed (1 Mbps and 2 Mbps) and Long Range (LE Coded PHYs, 125 Kbps and 500 Kbps)
- Advertising extensions
- Data length extensions
- LL privacy
- LE dual role
- BLE acceptlist
- BLE 2 peripheral & 2 central connections or 1 central & 1 peripheral connection, 8 peripheral & 2 central
- BLE Mesh (4 nodes) for limited switch use case.

5.9.1 MAC

Link Manager
- Creation, modification & release of physical links
- Connection establishment between Link managers of two Bluetooth devices
- Link supervision is implemented in Link Manager
- Link power control is done depending on the inputs from Link Controller
- Enabling & disabling of encryption & decryption on logical links
- Support for security using AES hardware accelerator

Link Controller
- Encodes and decodes header of BLE packets
- Manages flow control, acknowledgment, re-transmission requests, etc.
- Stores the last packet status for all physical transports
- Indicates the success status of packet transmission to upper layers
- Indicates the link quality to the LMP layer

Device Manager
- Executes HCI Commands
- Controls Scan & Connection processes
- Controls all BLE Device operations except data transport operations
- BLE Controller state transition management
- Anchor point synchronization & management
- Scheduler

5.9.2 Baseband Processing

- Supports BLE 1Mbps, 2Mbps and long range 125kbps, 500kbps

5.10 RF Transceiver

- The SiWG917 features two highly configurable RF transceivers supporting WLAN 11b/g/n/ax and Bluetooth LE wireless protocols. Both RF transceivers together operating in multiple modes covering High Performance (HP) and Low Power (LP) operations. List of operating modes are given in Section 5.10.1 Receiver and Transmitter Operating Modes.
- It contains two fully integrated fractional-N frequency synthesizers having reference from internal oscillator with 40MHz crystal. One of the synthesizer is a low power architecture which also caters single-bit data modulation feature for Bluetooth LE protocols.

5.10.1 Receiver and Transmitter Operating Modes

The radio is highly configurable. The available radio operating modes are

- WLAN HP TX - WLAN High-Performance Transmitter
- WLAN HP RX - WLAN High-Performance Receiver
- WLAN LP RX - WLAN Low-Power Receiver
- BLE HP TX - Bluetooth LE High-Performance Transmitter
- BLE HP RX - Bluetooth LE High-Performance Receiver
- BLE LP TX - Bluetooth LE Low-Power Transmitter
- BLE LP RX - Bluetooth LE Low-Power Receiver

5.11 Embedded Wi-Fi Software

- The wireless software package supports Embedded Wi-Fi (802.11 b/g/n/ax) Client mode, Wi-Fi Access point mode (up to 4 clients), and Enterprise Security in client mode.
- The software package includes complete firmware and application profiles.
- It has a wireless coexistence manager to arbitrate between protocols.

5.11.1 Security

Wireless software supports multiple levels of security capabilities available for the development of IoT devices.

- Accelerators: AES128/256
- WPA/WPA2/WPA3-Personal, WPA/WPA2 Enterprise for Client

5.12 Low Power Modes

It supports Ultra-low power consumption with multiple power modes to reduce system energy consumption.

- Dynamic Voltage and Frequency Scaling
- Deep sleep (ULP) mode with only the sleep timer active – with and without RAM retention
- Wi-Fi standby associated mode with automatic periodic wake-up
- Automatic clock gating of the unused blocks or transit the system from Normal to ULP mode.

5.12.1 ULP Mode

In Ultra Low Power mode, the deep sleep manager has control over the other subsystems and M4 processors and controls their active and sleep states. During deep sleep, the always-on logic domain operates on a lowered supply and a 32 KHz low-frequency clock to reduce power consumption. The ULP mode supports the following wake-up options:

- Timeout wakeup - Exit sleep state after programmed timeout value.
- GPIO Based Wakeup: Exit sleep state when GPIO goes High/Low based on programmed polarity.
- Analog Comparator Based wakeup - Exit sleep state on an event at the analog comparator.
- RTC Timer wakeup - Exit Sleep state on timeout of RTC timer
- WatchDog Interrupt based wakeup - Exit Sleep state upon watchdog interrupt timeout.

5.13 Wireless Subsystem Memory

5.13.1 On-Chip Memory

The multi-threaded processor has the following memory:
- On-chip SRAM of 672/480/416/352Kbytes based on chip configuration
- 448Kbytes of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks and security functions
- 16Kbytes of Instruction cache enabling eXecute In Place (XIP) with quad SPI flash memory.
- eFuse of 1024 bytes (used to store primary boot configuration, security and calibration parameters)

The Following memory configuration between MCU and Wireless Sub-system are possible:

Table 5.6. Possible Memory Configurations between MCU and Wireless Sub-system

No.	MCU memory size	Wireless Subsystem memory size	Config Name	Comments
1.	320K	352K	Config-6	ULP mode is possible (PS4 and PS2)
2.	256K	416K	Config-4	ULP mode is not possible (PS4 only) MCU 320k RAM Retention not possible
3.	192K	480K	Config-2	ULP mode is not possible (PS4 only) MCU 320k RAM Retention not possible

Note: SiWG917 parts have on-chip flash memory

5.14 Pad Configuration

There are multiple processor sub-systems containing SZP (Secure Zone Processor), MCU HP (High Performance) and MCU ULP (Ultra Low Power) which share these common set of GPIO pads. These GPIO pads are controllable by either SZP, MCU HP or MCU ULP. PAD selection register has to be programmed to control the PAD behavior for each GPIO. The SZP and MCU HPGPIOs are available only in PS4/PS3 power states whereas MCU ULP GPIOs are available in all the power states except sleep modes. The UULP Vbat GPIOs are available in all power states.

The SZP, MCU HP and MCU ULP GPIOs PAD are programmable, multi-voltage (1.8V, 3.3V) general purpose, bi-directional I/O buffer with a selectable LVCMOS (Low Voltage CMOS) input or LVCMOS Schmitt trigger input and programmable pull-up/pull-down. In the full-drive mode, this buffer can operate in excess of 100MHz frequency with 15pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 200MHz can be achieved under small capacitive loads.

The following PAD configurations can be controlled by software for SZP, MCU HP and MCU ULP GPIOs.
- Bi-directional IO capability
- Multi-voltage DVDD capability (1.8V, 3.3V)
- Power-on-Start (POS) capable
- Optimized for EMC (low di/dt switching supply noise) with SSO (Simultaneous Switching Output) factor of 8
- Four (4) Programmable output drive strengths (rated 2mA, 4mA, 8mA, and 12mA)
- Selectable output slew-rate (slow / fast)
- Open drain output mode (Logic low or high on input and use OEN as data input)
- LVCMOS/LVTTL compatible input with selectable hysteresis
- Programmable input options (pull-up, pull-down, repeater, or plain input)
- No power sequence requirements, I/Os are tri-stated when core power is not valid (POC control). These are tri-stated even if the system is under reset or in the deep sleep power state.

The following PAD configurations can be controlled by software for UULP Vbat GPIOs.
- Bi-directional IO capability
- Multi-voltage DVDD capability (1.8V, 3.3V)

5.15 Interrupts

- Nested vectored interrupt controller (NVIC) for interrupts handling
- Supports 99 interrupts
- Flexible exception and interrupt management
- Nested exception/interrupt support
- Vectored exception/interrupt entry
- Interrupt configurations, prioritization, and interrupt masking

6. Pin Definitions

6.1 Pin Diagram
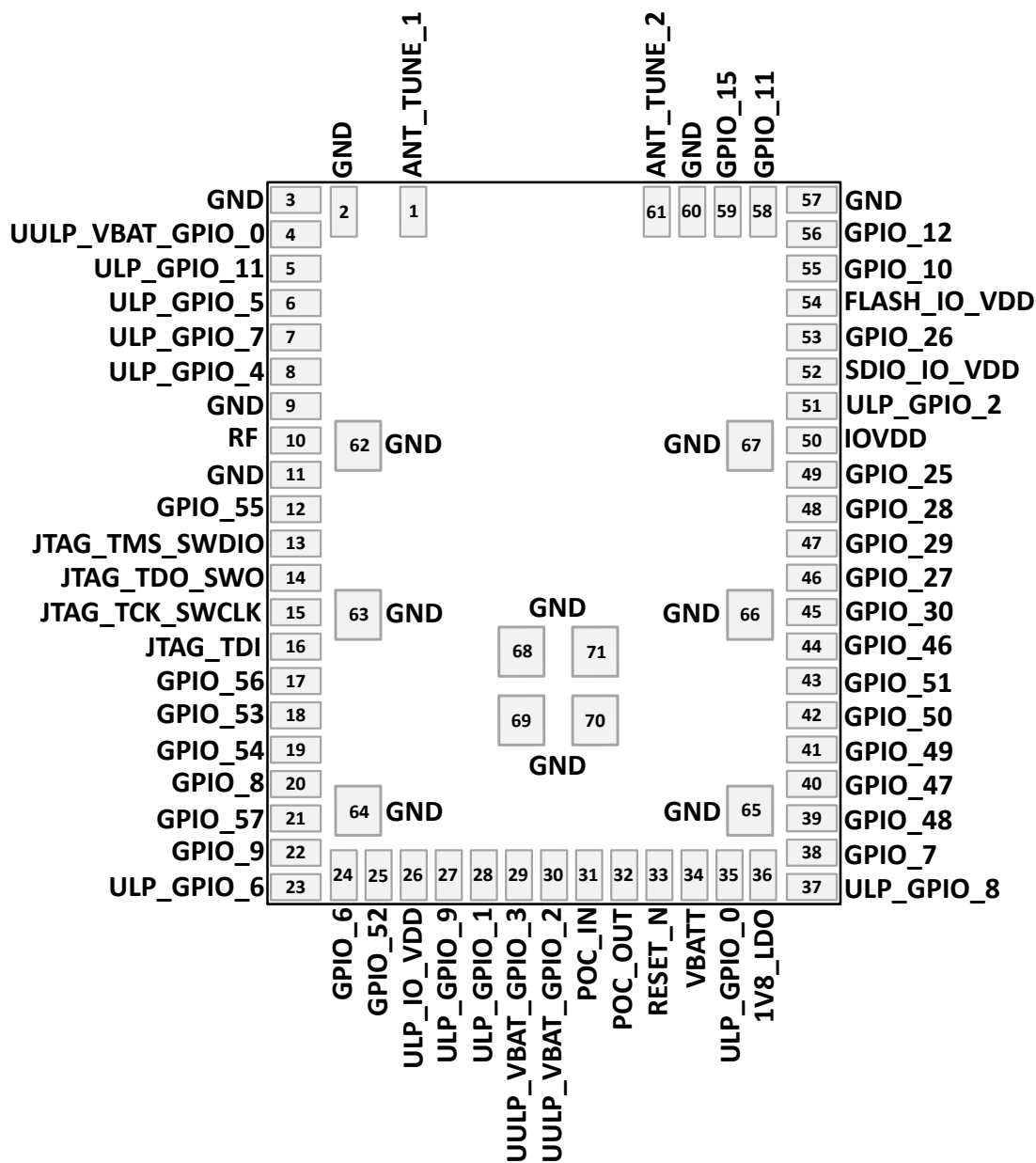
Figure 6.1. SiWG917 Pin Diagram

6.2 Pin Description

Table 6.1. List of Pins Not Available in the Modules

Pin Name	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
RF_BLETX	RF_AVDD	Output	NA	BLE 8 dBm RF Output
ULP_GPIO_10	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
XTAL_32KHZ_P	NA	Inout	NA	Analog Pin. 32KHZ XTAL Connection
NC				No-Connect
XTAL_32KHZ_N	NA	Inout	NA	Analog Pin. 32KHZ XTAL Connection
UULP_VBAT_GPIO_1	VBATT	Inout	HighZ	Default: High Sleep: High Refer to Section 6.3 GPIO Pin Multiplexing for configuration

6.2.1 RF and Control Interfaces

Table 6.2. Chip Packages - RF and Control Interfaces

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
ANT_TUNE_1	1	N/A	Input	N/A	**SiW917Y1GA:** External fine-tuning option for the integral antenna; connect same tuning circuit on both ANT_TUNE1 and ANT_TUNE2 pins; leave floating if no fine-tuning is desired on the integral antenna; **SiW917Y1GN:** leave this pin floating
RF	10	VBATT	Inout	N/A	Connect to antenna with a 50-Ω impedance as per the reference schematics
POC_IN	31	VBATT	Input	NA	This is an input to the chip. It should be made high only after supplies are valid to ensure the module is in safe state until valid power supply is available.
POC_OUT	32	VBATT	Output	NA	This is internally generated. Initially, it is low. But it becomes high when the supply (VBATT) is valid.
RESET_N	33	VBATT	Inout	NA	Active-low reset asynchronous reset signal. RESET_N will be pulled low if POC_IN is low.
ANT_TUNE_2	61	N/A	Input	N/A	**SiW917Y1GA:** External fine-tuning option for the integral antenna; connect same tuning circuit on both ANT_TUNE1 and ANT_TUNE2 pins; leave floating if no fine-tuning is desired on the integral antenna; **SiW917Y1GN:** leave this pin floating

6.2.2 Power and Ground Pins

Table 6.3. Chip Packages - Power and Ground Pins

Pin Name	Pin No.	Type	Direction	Description
ULP_IO_VDD	26	Power	Input	I/O supply for ULP I/Os. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
VBATT	34	Power	Input	Power supply for the module.
1V8_LDO	36	Power	Output	Output of 1.8V LDO which is used for Flash supply.
IOVDD	50	Power	Input	I/O Supply for I/Os. Refer to Section 6.3 GPIO Pin Multiplexing for details on which GPIOs have this as the I/O supply.
SDIO_IO_VDD	52	Power	Input	I/O Supply for SDIO I/Os. Refer to Section 6.3 GPIO Pin Multiplexing for details on which GPIOs have this as the I/O supply.
FLASH_IO_VDD	54	Power	Input	I/O Supply for IC stacked Flash. Connect to 1V8_LDO as per Reference Schematics.
GND	2, 3, 9, 11, 57, 60, 62-71	Ground		Common ground pins.

6.2.3 Peripheral Interfaces

Table 6.4. Chip Packages - Perpheral Interfaces

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
UULP_VBAT_GPIO_0	4	VBATT	Output	High	**Default**: EXT_PG_EN **Sleep**: EXT_PG_EN Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_11	5	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_5	6	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_7	7	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_4	8	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_55	12	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
JTAG_TMS_SWDIO	13	IO_VDD	Input	Pullup	JTAG interface Test Mode Select signal. Bi-directional data pin for SWD interface.

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
JTAG_TDO_SWO	14	IO_VDD	Output	Pullup	JTAG interface output data. Serial wire output for SWD Interface.This pin can also be used as ISP_ENABLE. Pull down to enable ISP mode. In System Programming (ISP) is programming or reprogramming of the flash through boot loader using UART (GPIO_8,GPIO_9), SPI (GPIO_25 to GPIO_28) and SDIO (GPIO_25 to GPIO_30) interfaces. This can be done after the part is integrated on end user board. Boot loader can be requested to boot in ISP mode by pulling down JTAG_TDO_SWO pin. This pin has to be left unconnected during reset for the boot loader to bypass ISP and execute the code that is present in flash. ISP mode can be used to reprogram the flash, if the application codes uses JTAG pins for other multiplexed functionalities. On boot up, if the application code goes into a state where JTAG interface is not functioning, ISP mode can be used to gain the control and to reprogram the flash.
JTAG_TCK_SWCLK	15	IO_VDD	Input	Pullup	JTAG interface clock or serial wire clock
JTAG_TDI	16	IO_VDD	Input	Pullup	JTAG interface input data
GPIO_56	17	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_53	18	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_54	19	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_8	20	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_57	21	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
GPIO_9	22	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_6	23	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ PTA_PRIO: "PTA Priority" input signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. If PTA feature is enabled, use it as PTA_PRIO. If PTA feature is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration.
GPIO_6	24	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_52	25	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_9	27	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_1	28	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ PTA_REQ: "PTA Request" input signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. If PTA feature is enabled, use it as PTA_REQ. If PTA feature is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration.
UULP_VBAT_GPIO_3	29	VBATT	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
UULP_VBAT_GPIO_2	30	VBATT	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
ULP_GPIO_0	35	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_8	37	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_7	38	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ PTA_GRANT: "PTA Grant" output signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. If PTA feature is enabled, use it as PTA_GRANT. If PTA feature is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration.
GPIO_48	39	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration.
GPIO_47	40	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_49	41	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_50	42	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_51	43	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_46	44	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
GPIO_30	45	SDIO_IO_VDD	Inout	Pullup	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_27	46	SDIO_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_29	47	SDIO_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_28	48	SDIO_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_25	49	SDIO_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_2	51	ULP_IO_VDD	Input	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_26	53	SDIO_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_10	55	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_12	56	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_11	58	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
GPIO_15	59	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration

6.3 GPIO Pin Multiplexing

Note:

1. The SiWG917 has the support for 43 GPIOs. These GPIOs are grouped into SoC GPIOs, ULP GPIOs, and UULP GPIOs.
2. The possible GPIO combinations for each Peripheral Interface are listed in Section 6.4 Valid GPIO Sets for Peripherals.
3. The digital GPIOs SOCPERH_ON_ULP_GPIO_0 to SOCPERH_ON_ULP_GPIO_11 are mapped onto physical ULP GPIOs for SoC Peripheral functionality and digital GPIOs ULPPERH_ON_SOC_GPIO_0 to ULPPERH_ON_SOC_GPIO_11 are mapped onto physical SoC GPIOs for ULP Peripheral functionality. Refer to Section 6.3.5 Digital Functions for peripheral mapping on these GPIOs

6.3.1 SoC GPIOs

The SoC GPIOs below (GPIO_6 to GPIO_57) are available in the normal mode of operation (Power-states 4 and 3). Default mode is mode0 (Mode = 0) if not explicitly mentioned.For a description of power-states, refer to the Hardware Reference Manual. Each of these GPIOs Pin function is controlled by the GPIO Mode register mentioned in SoC GPIOs section of the Hardware Reference Manual.

Table 6.5. SoC GPIO Pin Multiplexing

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 11	GPIO Mode = 12	GPIO Mode = 13	GPIO Mode = 14	GPIO Mode = 15
GPIO_6	GPIO_6	SIO_0	USART1_CTS	SSI_MST_DATA2	I2C1_SDA	I2C2_SCL	UART2_RX	I2S_2CH_DIN_1	PMU_TEST_1	ULPPERH_ON_SOC_GPIO_0	PWM_1L	M4SS_QSPI_D0		M4SS_TRACE_CLKIN		NWP_GPIO_6
GPIO_7	GPIO_7	SIO_1	USART1_DTR	SSI_MST_DATA3	I2C1_SCL	I2C2_SDA	UART2_TX	I2S_2CH_DOUT_1	PMU_TEST_2	ULPPERH_ON_SOC_GPIO_1	PWM_1H	M4SS_QSPI_CSN0	M4SS_QSPI_CSN1	M4SS_TRACE_CLK		
GPIO_8	GPIO_8	SIO_2	USART1_CLK	SSI_MST_CLK	GSPI_MST1_CLK	QEI_IDX	UART2_RS485_RE	I2S_2CH_CLK	SSI_SLV_CLK	ULPPERH_ON_SOC_GPIO_2	PWM_2L	M4SS_QSPI_CLK	SCT_OUT_2	M4SS_TRACE_D0		NWP_GPIO_8
GPIO_9	GPIO_9	SIO_3	USART1_RTS	SSI_MST_CS0	GSPI_MST1_CS0	QEI_PHA	UART2_RS485_DE	I2S_2CH_WS	SSI_SLV_CS		PWM_2H	M4SS_QSPI_D1	SCT_OUT_3	M4SS_TRACE_D1		NWP_GPIO_9

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 11	GPIO Mode = 12	GPIO Mode = 13	GPIO Mode = 14	GPIO Mode = 15
GPIO_10	GPIO_10	SIO_4	USART1_RX	SSI_MST_CS1	GSPI_MST1_CS1	QEI_PHB	UART2_RTS	I2S_2CH_DIN_0	SSI_SLV_MOSI	ULPPERH_ON_SOC_GPIO_4	PWM_3L	M4SS_QSPI_D2	SSI_MST_DATA1	M4SS_TRACE_D2		NWP_GPIO_10
GPIO_11	GPIO_11	SIO_5	USART1_DSR	SSI_MST_DATA0	GSPI_MST1_MISO	QEI_DIR	UART2_CTS	I2S_2CH_DOUT_0	SSI_SLV_MISO	ULPPERH_ON_SOC_GPIO_5	PWM_3H	M4SS_QSPI_D3	MCU_CLK_OUT	M4SS_TRACE_D3		NWP_GPIO_11
GPIO_12	GPIO_12		USART1_DCD	SSI_MST_DATA1	GSPI_MST1_MOSI		UART2_RS485_EN		MCU_CLK_OUT	ULPPERH_ON_SOC_GPIO_6	PWM_4L					NWP_GPIO_12
GPIO_15	GPIO_15	SIO_7	UART2_TX	SSI_MST_CS2	GSPI_MST1_CS2		M4SS_TRACE_CLKIN		MCU_CLK_OUT	ULPPERH_ON_SOC_GPIO_7	PWM_4H					NWP_GPIO_15

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 11	GPIO Mode = 12	GPIO Mode = 13	GPIO Mode = 14	GPIO Mode = 15
GPIO_25	GPIO_25	SIO_0	USART1_CLK	SSI_MST_CLK	GSPI_MST1_CLK	QEI_IDX		I2S_2CH_CLK	SSI_SLV_CS	SCT_IN_0	PWM_FAULTA	ULPPERH_ON_SOC_GPIO_6	SOC_PLL_CLOCK	USART1_IR_RX	TopGPIO_0	
GPIO_26	GPIO_26	SIO_1	USART1_CTS	SSI_MST_DATA0	GSPI_MST1_MISO	QEI_PHA	UART2_RS485_EN	I2S_2CH_WS	SSI_SLV_CLK	SCT_IN_1	PWM_FAULTB	ULPPERH_ON_SOC_GPIO_7	INTERFACE_PLL_CLOCK	USART1_IR_TX	TopGPIO_1	
GPIO_27	GPIO_27	SIO_2	USART1_RI	SSI_MST_DATA1	GSPI_MST1_MOSI	QEI_PHB	UART2_RTS	I2S_2CH_DIN_0	SSI_SLV_MOSI	SCT_IN_2	PWM_TMR_EXT_TRIG_1	ULPPERH_ON_SOC_GPIO_8	I2S_PLL_CLOCK	USART1_RS485_EN	TopGPIO_2	
GPIO_28	GPIO_28	SIO_3	USART1_RTS	SSI_MST_CS0	GSPI_MST1_CS0	QEI_DIR	UART2_RTS	I2S_2CH_DOUT_0	SSI_SLV_MISO	SCT_IN_3	PWM_TMR_EXT_TRIG_2	ULPPERH_ON_SOC_GPIO_9	XTAL_ON_IN	USART1_RS485_RE	TopGPIO_3	

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 11	GPIO Mode = 12	GPIO Mode = 13	GPIO Mode = 14	GPIO Mode = 15
GPIO_29	GPIO_29	SIO_4	USART1_RX	SSI_MST_DATA2	GSPI_MST1_CS1	I2C2_SCL	UART2_RX	I2S_2CH_DIN_1	PMU_TEST_1	SCT_OUT_0	PWM_TMR_EXT_TRIG_3	ULPPERH_ON_SOC_GPIO_10	USART1_DCD	USART1_RS485_DE	TopGPIO_4	
GPIO_30	GPIO_30	SIO_5	USART1_TX	SSI_MST_DATA3	GSPI_MST1_CS2	I2C2_SDA	UART2_TX	I2S_2CH_DOUT_1	PMU_TEST_2	SCT_OUT_1	PWM_TMR_EXT_TRIG_4	ULPPERH_ON_SOC_GPIO_11	PMU_TEST_1	PMU_TEST_2	TopGPIO_5	
JTAG_TCK_SWCLK	GPIO_31											I2C1_SDA	UART2_RTS	QEI_IDX		
JTAG_TDI	GPIO_32											I2C1_SCL	UART2_CTS	QEI_PHA		
JTAG_TMS_SWDIO	GPIO_33											I2C2_SCL	UART2_RX	QEI_PHB		
JTAG_TDO_SWO	GPIO_34											I2C2_SDA	UART2_TX	QEI_DIR		

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 11	GPIO Mode = 12	GPIO Mode = 13	GPIO Mode = 14	GPIO Mode = 15
GPIO_46	GPIO_46	M4SS_QSPI_CLK	USART1_RI	QEI_IDX	GSPI_MST1_CLK		M4SS_TRACE_CLKIN	I2S_2CH_CLK	SSI_SLV_CS	ULPPERH_ON_SOC_GPIO_8	SOC_PLL_CLOCK	M4SS_PSRAM_CLK				NWP_GPIO_46
GPIO_47	GPIO_47	M4SS_QSPI_D0	USART1_IR_RX	QEI_PHA	GSPI_MST1_MISO		M4SS_TRACE_CLK	I2S_2CH_WS	SSI_SLV_CLK	ULPPERH_ON_SOC_GPIO_9	INTERFACE_PLL_CLOCK	M4SS_PSRAM_D0				NWP_GPIO_47
GPIO_48	GPIO_48	M4SS_QSPI_D1	USART1_IR_TX	QEI_PHB	GSPI_MST1_MOSI		M4SS_TRACE_D0	I2S_2CH_DIN_0	SSI_SLV_MOSI	ULPPERH_ON_SOC_GPIO_10	I2S_PLL_CLOCK	M4SS_PSRAM_D1				NWP_GPIO_48
GPIO_49	GPIO_49	M4SS_QSPI_CSN0	USART1_RS485_EN	QEI_DIR	GSPI_MST1_CS0		M4SS_TRACE_D1	I2S_2CH_DOUT_0	SSI_SLV_MISO	ULPPERH_ON_SOC_GPIO_11	MCU_QSPI_CSN0	M4SS_PSRAM_CSN0				NWP_GPIO_49

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 11	GPIO Mode = 12	GPIO Mode = 13	GPIO Mode = 14	GPIO Mode = 15
GPIO_50	GPIO_50	M4SS_QSPI_D2	USART1_RS485_RE	SSI_MST_CS2	GSPI_MST1_CS1	I2C2_SCL	M4SS_TRACE_D2	I2S_2CH_DIN_1	PWM_TMR_EXT_TRIG_4	UART2_RTS	MEMS_REF_CLOCK	M4SS_PSRAM_D2				NWP_GPIO_50
GPIO_51	GPIO_51	M4SS_QSPI_D3	USART1_RS485_DE	SSI_MST_CS3	GSPI_MST1_CS2	I2C2_SDA	M4SS_TRACE_D3	I2S_2CH_DOUT_1	PWM_TMR_EXT_TRIG_1	UART2_CTS	PLL_TESTMODE_SIG	M4SS_PSRAM_D3				NWP_GPIO_51
GPIO_52	GPIO_52		USART1_CLK	SSI_MST_CLK	GSPI_MST1_CLK	QEI_IDX	M4SS_TRACE_CLKIN	I2S_2CH_CLK	SSI_SLV_CLK	M4SS_QSPI_CLK	SOC_PLL_CLOCK		M4SS_PSRAM_CLK			
GPIO_53	GPIO_53	M4SS_QSPI_CSN1	USART1_RTS	SSI_MST_CS0	GSPI_MST1_CS0	QEI_PHA	M4SS_TRACE_CLK	I2S_2CH_WS	SSI_SLV_CS	M4SS_QSPI_D0	INTERFACE_PLL_CLOCK	M4SS_PSRAM_CSN1	M4SS_PSRAM_D0			
GPIO_54	GPIO_54	M4SS_QSPI_D4	USART1_TX	SSI_MST_DATA2	GSPI_MST1_CS1	I2C2_SCL	M4SS_TRACE_D0	I2S_2CH_DIN_1	PWM_TMR_EXT_TRIG_2	M4SS_QSPI_D1	I2S_PLL_CLOCK	M4SS_PSRAM_D4	M4SS_PSRAM_D1			

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 11	GPIO Mode = 12	GPIO Mode = 13	GPIO Mode = 14	GPIO Mode = 15
GPIO_55	GPIO_55	M4SS_QSPI_D5	USART1_RX	SSI_MST_DATA3	GSPI_MST1_CS2	I2C2_SDA	M4SS_TRACE_D1	I2S_2CH_DOUT_1	PWM_TMR_EXT_TRIG_3	M4SS_QSPI_CSN0		M4SS_PSRAM_D5	M4SS_PSRAM_CSN0			
GPIO_56	GPIO_56	M4SS_QSPI_D6	USART1_CTS	SSI_MST_DATA0	GSPI_MST1_MISO	QEI_PHB	M4SS_TRACE_D2	I2S_2CH_DIN_0	SSI_SLV_MOSI	M4SS_QSPI_D2	MEMS_REF_CLOCK	M4SS_PSRAM_D6	M4SS_PSRAM_D2			
GPIO_57	GPIO_57	M4SS_QSPI_D7	USART1_DSR	SSI_MST_DATA1	GSPI_MST1_MOSI	QEI_DIR	M4SS_TRACE_D3	I2S_2CH_DOUT_0	SSI_SLV_MISO	M4SS_QSPI_D3	XTAL_ON_IN	M4SS_PSRAM_D7	M4SS_PSRAM_D3			

Note:

1. GPIOs 25 to 30 can be used for Analog functions when GPIO Mode = 14. Multiple Analog functions are available on each pin as shown in Table 6.8 Analog Functions for SoC/ULP GPIOs on page 68. These analog functions are enabled and disabled through programming - refer to the Hardware Reference Manual for more details.
2. NWP GPIOs can be used for Network Processor functions when GPIO Mode = 15.

6.3.2 ULP GPIOs

The ULP GPIOs listed in the table below (ULP_GPIO_0 to ULP_GPIO_11) are available in the normal mode of operation (Power-states 4 and 3) and also in Ultra-low power mode of operation of the Microcontroller (Power-states 2 and 1). For a description of power-states, refer to the Hardware Reference Manual. Each of these GPIO's Pin function is controlled by the GPIO Mode register mentioned in ULP GPIO's section of the Hardware Reference Manual.

Table 6.6. ULP GPIO Pin Multiplexing

ULP_GPIO	ULP GPIO Mode = 0	ULP GPIO Mode = 1	ULP GPIO Mode = 2	ULP GPIO Mode = 3	ULP GPIO Mode = 4	ULP GPIO Mode = 5	ULP GPIO Mode = 6	ULP GPIO Mode = 7	ULP GPIO Mode = 8	ULP GPIO Mode = 9	ULP GPIO Mode = 10	ULP GPIO Mode = 11
ULP_GPIO_0	ULP_EGPIO_0	ULP_SPI_CLK	ULP_I2S_DIN	ULP_UART_RTS	ULP_I2C_SDA		SOCPERH_ON_ULP_GPIO_0	AGPIO_0				
ULP_GPIO_1	ULP_EGPIO_1	ULP_SPI_DOUT	ULP_I2S_DOUT	ULP_UART_CTS	ULP_I2C_SCL	Timer2	SOCPERH_ON_ULP_GPIO_1	AGPIO_1				
ULP_GPIO_2	ULP_EGPIO_2	ULP_SPI_DIN	ULP_I2S_WS	ULP_UART_RX		COMP1_OUT	SOCPERH_ON_ULP_GPIO_2	AGPIO_2				
ULP_GPIO_4	ULP_EGPIO_4	ULP_SPI_CS1	ULP_I2S_WS	ULP_UART_RTS	ULP_I2C_SDA	AUX_ULP_TRIG_1	SOCPERH_ON_ULP_GPIO_4	AGPIO_4	ULP_SPI_CLK	Timer0	IR_INPUT	

ULP_GPIO	ULP GPIO Mode = 0	ULP GPIO Mode = 1	ULP GPIO Mode = 2	ULP GPIO Mode = 3	ULP GPIO Mode = 4	ULP GPIO Mode = 5	ULP GPIO Mode = 6	ULP GPIO Mode = 7	ULP GPIO Mode = 8	ULP GPIO Mode = 9	ULP GPIO Mode = 10	ULP GPIO Mode = 11
ULP_GPIO_5	ULP_EGPIO_5	IR_OUTPUT	ULP_I2S_DOUT	ULP_UART_CTS	ULP_I2C_SCL	AUX_ULP_TRIG_0	SOCPERH_ON_ULP_GPIO_5	AGPIO_5	ULP_SPI_DOUT	Timer1	IR_OUTPUT	
ULP_GPIO_6	ULP_EGPIO_6	ULP_SPI_CS2	ULP_I2S_DIN	ULP_UART_RX	ULP_I2C_SDA		SOCPERH_ON_ULP_GPIO_6	AGPIO_6	ULP_SPI_DIN	COMP1_OUT	AUX_ULP_TRIG_0	
ULP_GPIO_7	ULP_EGPIO_7	IR_INPUT	ULP_I2S_CLK	ULP_UART_TX	ULP_I2C_SCL	Timer1	SOCPERH_ON_ULP_GPIO_7	AGPIO_7	ULP_SPI_CS0	COMP2_OUT	AUX_ULP_TRIG_1	NPSS_TEST_MODE_0
ULP_GPIO_8	ULP_EGPIO_8	ULP_SPI_CLK	ULP_I2S_CLK	ULP_UART_CTS	ULP_I2C_SCL	Timer0	SOCPERH_ON_ULP_GPIO_8	AGPIO_8				

ULP_GPIO	ULP GPIO Mode = 0	ULP GPIO Mode = 1	ULP GPIO Mode = 2	ULP GPIO Mode = 3	ULP GPIO Mode = 4	ULP GPIO Mode = 5	ULP GPIO Mode = 6	ULP GPIO Mode = 7	ULP GPIO Mode = 8	ULP GPIO Mode = 9	ULP GPIO Mode = 10	ULP GPIO Mode = 11
ULP_GPIO_9	ULP_EGPIO_9	ULP_SPI_DIN	ULP_I2S_DIN	ULP_UART_RX	ULP_I2C_SDA	NPSS_TEST_MODE_0	SOCPERH_ON_ULP_GPIO_9	AGPIO_9				
ULP_GPIO_11	ULP_EGPIO_11	ULP_SPI_DOUT	ULP_I2S_DOUT	ULP_UART_TX	ULP_I2C_SDA	AUX_ULP_TRIG_0	SOCPERH_ON_ULP_GPIO_11	AGPIO_11				

Note:

1. All the ULP GPIOs can be used for Analog functions when ULP GPIO Mode = 7. Multiple Analog functions are available on each pin as shown in Table 6.8 Analog Functions for SoC/ULP GPIOs on page 68. These analog functions are enabled and disabled through programming - refer to the Hardware Reference Manual for more details.
2. All the ULP GPIO's can be used for Digital functions when ULP GPIO Mode = 6. The digital functions available on these GPIOs is shown in Table 6.9 Digital Functions for SoC/ULP GPIOs on page 69.

6.3.3 UULP VBAT GPIOs

The UULP VBAT GPIOs listed in the table below (UULP_VBAT_GPIO_0 to UULP_VBAT_GPIO_3) are available in the normal mode of operation (Power-states 4 and 3), in Ultra-low power mode of operation (Power-states 2 and 1) and also in the retention and deep sleep mode of operation (Retention and Power-state 0). For a description of power-states, refer to the Hardware Reference Manual. Each of this UULP VBAT GPIO's Pin function is controlled by the GPIO Mode register mentioned in UULP VBAT GPIO's section of the Hardware Reference Manual.

Table 6.7. UULP VBAT GPIO Pin Multiplexing

UULP VBAT GPIO	UULP VBAT GPIO Mode = 0	UULP VBAT GPIO Mode = 1	UULP VBAT GPIO Mode = 2	UULP VBAT GPIO Mode = 3	UULP VBAT GPIO Mode = 4	UULP VBAT GPIO Mode = 5	UULP VBAT GPIO Mode = 6	UULP VBAT GPIO Mode = 7	Default
UULP_VBAT_GPIO_0	UULP_VBAT_GPIO[0]	EXT_PG_EN	MCU_GPIO0_WAKEUP	SYSRTC_PRS_IN_G0	SYSRTC_PRS_OUT_G0_1	NPSS_32KHZ_XTAL_CLK	NPSS_TEST_MODE_0		EXT_PG_EN
UULP_VBAT_GPIO_2	UULP_VBAT_GPIO[2]	NWP_GPIO0_WAKEUP	MCU_GPIO2_WAKEUP	MCU_GPIO_TOGGLE	NPSS_32KHZ_XTAL_CLK	SYSRTC_PRS_OUT_G1_1	NPSS_TEST_MODE_1	VOLT_SENSE	NWP_GPIO0_WAKEUP
UULP_VBAT_GPIO_3	UULP_VBAT_GPIO[3]	NWP_GPIO1_WAKEUP	MCU_GPIO3_WAKEUP	SYSRTC_PRS_OUT_G0_0	MCU_GPIO_TOGGLE	NPSS_32KHZ_XTAL_CLK	NPSS_TEST_MODE_2	COMP_P	UULP_VBAT_GPIO[3]

6.3.4 Analog Functions

Analog functions are available on pins ULP_GPIO_0 to ULP_GPIO_11 and GPIO_25 to GPIO_30. AGPIO_0 to AGPIO_11 is mapping to ULP_GPIO_0 to ULP_GPIO_11. TopGPIO_0 to TopGPIO_5 is mapping to GPIO_25 to GPIO_30.

Table 6.8. Analog Functions for SoC/ULP GPIOs

GPIO	ADC Function	Touch Function	DAC Function	Comparator Function	OpAmp Function
AGPIO_0	ADCP0	TOUCH6		COMP1_P0	OPAMP1_IN<2>
AGPIO_1	ADCP10 / ADCN0	TOUCH0		COMP1_N0	
AGPIO_2	ADCP1	C_int_res_in		COMP2_P0	OPAMP1_IN<3>
AGPIO_3	ADCP11 / ADCN1	TOUCH5		COMP2_N0	
AGPIO_4	ADCP2		DAC0	COMP1_N1	OPAMP1OUT0
AGPIO_5	ADCP12 / ADCN2	res_out		COMP1_P1	OPAMP2_IN<1>
AGPIO_6	ADCP3	TOUCH4			OPAMP1_IN<4>
AGPIO_7	ADCP15 / ADCN5	TOUCH3			OPAMP1_IN<1>
AGPIO_8	ADCP4	SHIELD_ELECTRODE			OPAMP1_IN<5>
AGPIO_9	ADCP14 / ADCN4	TOUCH1			OPAMP2OUT0
AGPIO_11	ADCP13 / ADCN3	TOUCH7			OPAMP2_IN<0>
TopGPIO_0	ADCP6				
TopGPIO_1	ADCP16 / ADCN6				
TopGPIO_2	ADCP7	TOUCH_VREF_EXT		COMP2_P1	OPAMP3OUT0 / OPAMP1_IN<0>
TopGPIO_3	ADCP17 / ADCN7			COMP2_N1	
TopGPIO_4	ADCP8				OPAMP3_IN<1>
TopGPIO_5	ADCP18 / ADCN8		DAC1		OPAMP1OUT1

Note:

1. Software can program above different functions.
2. Please refer to the Hardware Reference Manual for software programming information.
3. Please refer to Software Reference Manual for software programming information.

6.3.5 Digital Functions

The ULP GPIOs below are configured for SoC peripheral functionality (SOCPERH_ON_ULP_GPIO_0 to SOC-PERH_ON_ULP_GPIO_11) and are available only in the normal mode of operation (Power-states 4 and 3). For a description of power-states, refer to the Hardware Reference Manual. Each of these GPIO's Pin function is controlled by the GPIO Mode register mentioned in SoC GPIO's section of the Hardware Reference Manual.

Table 6.9. Digital Functions for SoC/ULP GPIOs

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode =3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 11	GPIO Mode = 12	GPIO Mode = 13
SOCPERH_ON_ULP_GPIO_0	GPIO_64	SIO_0	USART1_CLK	QEI_IDX	I2C1_SDA	I2C2_SCL	UART2_RS485_EN	SCT_IN_0	PWM_1L	UART2_RTS		USART1_IR_RX	PWM_1L	PMU_TEST_1
SOCPERH_ON_ULP_GPIO_1	GPIO_65	SIO_1	USART1_RX	QEI_PHA	I2C1_SCL	I2C2_SDA	UART2_RS485_RE	SCT_IN_1	PWM_1H	UART2_CTS		USART1_IR_TX	PWM_1H	PMU_TEST_2
SOCPERH_ON_ULP_GPIO_2	GPIO_66	SIO_2		QEI_PHB	I2C1_SCL	I2C2_SCL	UART2_RS485_DE	SCT_IN_2	PWM_2L	UART2_RX	PMU_TEST_1			
SOCPERH_ON_ULP_GPIO_4	GPIO_68	SIO_4	USART1_TX	QEI_IDX			UART2_RX	SCT_OUT_0	PWM_3L	SCT_IN_0	PWM_FAULTA	USART1_RI	PWM_2L	SCT_OUT_4

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode =3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 11	GPIO Mode = 12	GPIO Mode = 13
SOC-PERH_ON_ULP_GPIO_5	GPIO_69	SIO_5	USART1_RTS	QEI_PHA			UART2_TX	SCT_OUT_1	PWM_3H	SCT_IN_1	PWM_FAULTB	USART1_RS485_EN	PWM_2H	SCT_OUT_5
SOCPERH_ON_ULP_GPIO_6	GPIO_70	SIO_6	USART1_CTS	QEI_PHB	USART1_RX	I2C2_SCL	UART2_RTS	SCT_OUT_2	PWM_4L	SCT_IN_2	PWM_TMR_EXT_TRIG_1	USART1_RS485_RE	PMU_TEST_1	SCT_OUT_6
SOCPERH_ON_ULP_GPIO_7	GPIO_71	SIO_7	USART1_IR_RX	QEI_DIR	USART1_TX	I2C2_SDA	UART2_CTS	SCT_OUT_3	PWM_4H	SCT_IN_3	PWM_TMR_EXT_TRIG_2	USART1_RS485_DE	PMU_TEST_2	SCT_OUT_7
SOCPERH_ON_ULP_GPIO_8	GPIO_72	SIO_0	USART1_IR_TX	QEI_IDX			UART2_RX	SCT_OUT_4	PWM_SLP_EVENT_TRIG	UART2_RTS	PWM_TMR_EXT_TRIG_3			
SOCPERH_ON_ULP_GPIO_9	GPIO_73	SIO_1	USART1_RS485_EN	QEI_PHA			UART2_TX	SCT_OUT_5	PWM_FAULTA	UART2_CTS	PWM_TMR_EXT_TRIG_4			

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode =3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 11	GPIO Mode = 12	GPIO Mode = 13
SOCPERH_ON_ULP_GPIO_10	GPIO_74	SIO_2	USART1_RS485_RE	QEI_PHB	I2C1_SDA		UART2_RS485_RE	SCT_OUT_6	PWM_FAULTB	UART2_RX	PMU_TEST_1			
SOCPERH_ON_ULP_GPIO_11	GPIO_75	SIO_3	USART1_RS485_DE	QEI_DIR	I2C1_SCL		UART2_RS485_DE	SCT_OUT_7	PWM_TMR_EXT_TRIG_1	UART2_TX	PMU_TEST_2			

The SoC GPIOs below are configured for ULP peripheral functionality (ULPPERH_ON_SOC_GPIO_0 to ULP-PERH_ON_SOC_GPIO_11) and are available only in the normal mode of operation (Power-states 4 and 3). For a description of power-states, refer to the Hardware Reference Manual. Each of these GPIO's Pin function is controlled by the GPIO Mode register mentioned in ULP GPIO's section of the Hardware Reference Manual.

Table 6.10. ULP GPIO Pin Multiplexing

ULP_GPIO	ULP GPIO Mode = 0	ULP GPIO Mode = 1	ULP GPIO Mode = 2	ULP GPIO Mode = 3	ULP GPIO Mode = 4	ULP GPIO Mode = 5	ULP GPIO Mode = 6	ULP GPIO Mode = 7	ULP GPIO Mode = 8	ULP GPIO Mode = 9	ULP GPIO Mode = 10	ULP GPIO Mode = 11
ULPPERH_ON_SOC_GPIO_0	ULP_EGPIO[0]	ULP_SPI_CLK	ULP_I2S_DIN	ULP_UART_RTS	ULP_I2C_SDA							

ULP_GPIO	ULP GPIO Mode = 0	ULP GPIO Mode = 1	ULP GPIO Mode = 2	ULP GPIO Mode = 3	ULP GPIO Mode = 4	ULP GPIO Mode = 5	ULP GPIO Mode = 6	ULP GPIO Mode = 7	ULP GPIO Mode = 8	ULP GPIO Mode = 9	ULP GPIO Mode = 10	ULP GPIO Mode = 11
ULPPERH_ON_SOC_GPIO_1	ULP_EGPIO[1]	ULP_SPI_DOUT	ULP_I2S_DOUT	ULP_UART_CTS	ULP_I2C_SCL	Timer0						
ULPPERH_ON_SOC_GPIO_2	ULP_EGPIO[2]	ULP_SPI_DIN	ULP_I2S_WS	ULP_UART_RX		COMP1_OUT						
ULPPERH_ON_SOC_GPIO_4	ULP_EGPIO[4]	ULP_SPI_CS1	ULP_I2S_WS	ULP_UART_RTS	ULP_I2C_SDA		NPSS_TEST_MODE_1		ULP_SPI_CLK	Timer0	IR_INPUT	
ULPPERH_ON_SOC_GPIO_5	ULP_EGPIO[5]	IR_OUTPUT	ULP_I2S_DOUT	ULP_UART_CTS	ULP_I2C_SCL	AUX_ULP_TRIG_0	NPSS_TEST_MODE_2		ULP_SPI_DOUT	Timer1	IR_OUTPUT	

ULP_GPIO	ULP GPIO Mode = 0	ULP GPIO Mode = 1	ULP GPIO Mode = 2	ULP GPIO Mode = 3	ULP GPIO Mode = 4	ULP GPIO Mode = 5	ULP GPIO Mode = 6	ULP GPIO Mode = 7	ULP GPIO Mode = 8	ULP GPIO Mode = 9	ULP GPIO Mode = 10	ULP GPIO Mode = 11
ULPPERH_ON_SOC_GPIO_6	ULP_EGPIO[6]	ULP_SPI_CS2	ULP_I2S_DIN	ULP_UART_RX	ULP_I2C_SDA				ULP_SPI_DIN	COMP1_OUT	AUX_ULP_TRIG_0	
ULPPERH_ON_SOC_GPIO_7	ULP_EGPIO[7]	IR_INPUT	ULP_I2S_CLK	ULP_UART_TX	ULP_I2C_SCL	Timer1			ULP_SPI_CS0	COMP2_OUT	AUX_ULP_TRIG_1	NPSS_TEST_MODE_0
ULPPERH_ON_SOC_GPIO_8	ULP_EGPIO[8]	ULP_SPI_CLK	ULP_I2S_CLK	ULP_UART_CTS	ULP_I2C_SCL	Timer0						
ULPPERH_ON_SOC_GPIO_9	ULP_EGPIO[9]	ULP_SPI_DIN	ULP_I2S_DIN	ULP_UART_RX	ULP_I2C_SDA	COMP1_OUT						

ULP_GPIO	ULP GPIO Mode = 0	ULP GPIO Mode = 1	ULP GPIO Mode = 2	ULP GPIO Mode = 3	ULP GPIO Mode = 4	ULP GPIO Mode = 5	ULP GPIO Mode = 6	ULP GPIO Mode = 7	ULP GPIO Mode = 8	ULP GPIO Mode = 9	ULP GPIO Mode = 10	ULP GPIO Mode = 11
ULPPERH_ON_SOC_GPIO_10	ULP_EGPIO[10]	ULP_SPI_CS0	ULP_I2S_WS	ULP_UART_RTS	IR_INPUT		NPSS_TEST_MODE_0					
ULPPERH_ON_SOC_GPIO_11	ULP_EGPIO[11]	ULP_SPI_DOUT	ULP_I2S_DOUT	ULP_UART_TX	ULP_I2C_SDA	AUX_ULP_TRIG_0						

6.4 Valid GPIO Sets for Peripherals

Functions can be split pin wise across all GPIOs except for the following restrictions. For synchronous interfaces there are some restrictions on clubbing of GPIOs into synchronous buses to ensure the timings mentioned in Section 7. Electrical Specifications. For example single synchronous interface cannot be split across ULP & SOC GPIOs. The following table provides all possible pin combinations for all Functions. For GPIO mode related information refer to Section 6.3 GPIO Pin Multiplexing .

ULP SSI (Synchronous Serial Interface) Primary		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_SPI_CLK	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_8	GPIO_6/GPIO_46
ULP_SPI_CS0	ULP_GPIO_7	GPIO_48
ULP_SPI_CS1	ULP_GPIO_4	GPIO_10
ULP_SPI_CS2	ULP_GPIO_6	GPIO_12
ULP_SPI_DIN	ULP_GPIO_6 / ULP_GPIO_9	GPIO_8 / GPIO_47
ULP_SPI_DOUT	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_11	GPIO_7 / GPIO_49
ULP I2S Primary/Seondary		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_I2S_CLK	ULP_GPIO_7 / ULP_GPIO_8	GPIO_15 / GPIO_46
ULP_I2S_WS	ULP_GPIO_4	GPIO_8/GPIO_10/GPIO_48
ULP_I2S_DIN	ULP_GPIO_0 / ULP_GPIO_6 / ULP_GPIO_9	GPIO_6/GPIO_12/GPIO_47
ULP_I2S_DOUT	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_11	GPIO_7/GPIO_11/GPIO_49
ULP I2C INTERFACE		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_I2C_SCL	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_7 / ULP_GPIO_8	GPIO_7/GPIO_11/GPIO_15/GPIO_46
ULP_I2C_SDA	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_6 / ULP_GPIO_9 / ULP_GPIO_11	GPIO_6/GPIO_10/GPIO_12/GPIO_47 / GPIO_49
ULP UART INTERFACE		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_UART_TX	ULP_GPIO_7 / ULP_GPIO_11	GPIO_15/GPIO_49

ULP_UART_RX	ULP_GPIO_6 / ULP_GPIO_9	GPIO_8/GPIO_12/GPIO_47
ULP_UART_CTS	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_8	GPIO_7/GPIO_11/GPIO_46
ULP_UART_RTS	ULP_GPIO_0 / ULP_GPIO_4	GPIO_6/GPIO_10/GPIO_48
IR Interface		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
IR_INPUT	ULP_GPIO_4 / ULP_GPIO_7	GPIO_15/GPIO_48
IR_PG_EN	ULP_GPIO_5	GPIO_11
Timer Interrupt Interface		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
Timer0	ULP_GPIO_4 / ULP_GPIO_8	GPIO_46
Timer1	ULP_GPIO_5 / ULP_GPIO_7	GPIO_15
Timer2	ULP_GPIO_1	GPIO_7
MCU SSI (Synchronous Serial Interface) Primary[1]		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
SSI_MST_CLK	GPIO_8 / GPIO_25 / GPIO_52	
SSI_MST_CS0	GPIO_9 / GPIO_28 / GPIO_53	
SSI_MST_CS1	GPIO_10	
SSI_MST_CS2	GPIO_15 / GPIO_50	
SSI_MST_CS3	GPIO_51	
SSI_MST_DATA0	GPIO_11 / GPIO_26 / GPIO_56	
SSI_MST_DATA1	GPIO_12 / GPIO_27 / GPIO_57	
SSI_MST_DATA2	GPIO_6 / GPIO_29 / GPIO_54	
SSI_MST_DATA3	GPIO_7 / GPIO_30 / GPIO_55	
MCU SSI (Synchronous Serial Interface) Secondary[1]		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
SSI_SLV_CLK	GPIO_8 / GPIO_26 / GPIO_47 / GPIO_52	
SSI_SLV_CS	GPIO_9 / GPIO_25 / GPIO_46 / GPIO_53	

| SSI_SLV_MISO | GPIO_11 / GPIO_28 / GPIO_49 / GPIO_57 | |
| SSI_SLV_MOSI | GPIO_10 / GPIO_27 / GPIO_48 / GPIO_56 | |

GSPI (General SPI) Interface[2]		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
GSPI_MST1_CLK	GPIO_8 / GPIO_25 / GPIO_46 / GPIO_52	
GSPI_MST1_CS0	GPIO_9 / GPIO_28 / GPIO_49 / GPIO_53	
GSPI_MST1_CS1	GPIO_10 / GPIO_29 / GPIO_50 / GPIO_54	
GSPI_MST1_CS2	GPIO_15 / GPIO_30 / GPIO_51 / GPIO_55	
GSPI_MST1_MISO	GPIO_11 / GPIO_26 / GPIO_47 / GPIO_56	
GSPI_MST1_MOSI	GPIO_6 / GPIO_12 / GPIO_27 / GPIO_48 / GPIO_57	

I2S Primary/Secondary		
IO Functionality	Combinations possible on SoC GPIOs	
I2S_2CH_CLK	GPIO_8 / GPIO_25 / GPIO_46 / GPIO_52	
I2S_2CH_WS	GPIO_9 / GPIO_26 / GPIO_47 / GPIO_53	
I2S_2CH_DIN_0	GPIO_10 / GPIO_27 / GPIO_48 / GPIO_56	
I2S_2CH_DIN_1	GPIO_6 / GPIO_29 / GPIO_50 / GPIO_54	
I2S_2CH_DOUT_0	GPIO_11 / GPIO_28 / GPIO_49 / GPIO_57	
I2S_2CH_DOUT_1	GPIO_7 / GPIO_30 / GPIO_51 / GPIO_55	

I2C1 INTERFACE		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
I2C1_SCL	GPIO_7 / JTAG_TDI	ULP_GPIO_1 / ULP_GPIO_11
I2C1_SDA	GPIO_6 / JTAG_TCK_SWCLK	ULP_GPIO_0

I2C2 INTERFACE		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
I2C2_SCL	GPIO_6 / GPIO_29 / JTAG_TMS_SWDIO / GPIO_50 / GPIO_54	ULP_GPIO_0 / ULP_GPIO_6

| I2C2_SDA | GPIO_7 / GPIO_30 / JTAG_TDO_SWO / GPIO_51 / GPIO_55 | ULP_GPIO_1 / ULP_GPIO_7 |

PWM Interface

IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
PWM_1H	GPIO_7	ULP_GPIO_1
PWM_1L	GPIO_6	ULP_GPIO_0
PWM_2H	GPIO_9	ULP_GPIO_5
PWM_2L	GPIO_8	ULP_GPIO_2 / ULP_GPIO_4
PWM_3H	GPIO_11	ULP_GPIO_5
PWM_3L	GPIO_10	ULP_GPIO_4
PWM_4H	GPIO_13	ULP_GPIO_7
PWM_4L	GPIO_12	ULP_GPIO_6
PWM_FAULTA	GPIO_25	ULP_GPIO_4 / ULP_GPIO_9
PWM_FAULTB	GPIO_26	ULP_GPIO_5
PWM_SLP_EVENT_TRIG		ULP_GPIO_8
PWM_TMR_EXT_TRIG_1	GPIO_27 / GPIO_51	ULP_GPIO_6 / ULP_GPIO_11
PWM_TMR_EXT_TRIG_2	GPIO_28 / GPIO_54	ULP_GPIO_1 / ULP_GPIO_7
PWM_TMR_EXT_TRIG_3	GPIO_29 / GPIO_55	ULP_GPIO_8
PWM_TMR_EXT_TRIG_4	GPIO_30 / GPIO_50	ULP_GPIO_9

QEI Interface

IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
QEI_DIR	GPIO_11 / GPIO_28 / JTAG_TDO_SWO / GPIO_49 / GPIO_57	ULP_GPIO_7 / ULP_GPIO_11
QEI_IDX	GPIO_8 / GPIO_25 / JTAG_TCK_SWCLK/ GPIO_46 / GPIO_52	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_8
QEI_PHA	GPIO_9 / GPIO_26 / JTAG_TDI / GPIO_47 / GPIO_53	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_9
QEI_PHB	GPIO_10 / GPIO_27 / JTAG_TMS_SWDIO / GPIO_48 / GPIO_56	ULP_GPIO_6

SIO

IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
SIO_0	GPIO_6 / GPIO_25	ULP_GPIO_0 / ULP_GPIO_8
SIO_1	GPIO_7 / GPIO_26	ULP_GPIO_1 / ULP_GPIO_9
SIO_2	GPIO_8 / GPIO_27	
SIO_3	GPIO_9 / GPIO_28	ULP_GPIO_11

SIO_4	GPIO_10 / GPIO_29	ULP_GPIO_4
SIO_5	GPIO_11 / GPIO_30	ULP_GPIO_5
SIO_6		ULP_GPIO_6
SIO_7	GPIO_15	ULP_GPIO_7

USART1		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
USART1_CLK	GPIO_8 / GPIO_25 / GPIO_52	ULP_GPIO_0
USART1_CTS	GPIO_6 / GPIO_26 / GPIO_56	ULP_GPIO_6
USART1_RTS	GPIO_9 / GPIO_28 / GPIO_53	ULP_GPIO_5
USART1_DCD	GPIO_12 / GPIO_29	
USART1_DSR	GPIO_11 / GPIO_57	
USART1_DTR	GPIO_7	
USART1_IR_RX	GPIO_25 / GPIO_47	ULP_GPIO_0 / ULP_GPIO_7
USART1_IR_TX	GPIO_26 / GPIO_48	ULP_GPIO_1 / ULP_GPIO_8
USART1_RI	GPIO_27 / GPIO_46	ULP_GPIO_4
USART1_RS485_DE	GPIO_29 / GPIO_51	ULP_GPIO_7 / ULP_GPIO_11
USART1_RS485_EN	GPIO_27 / GPIO_49	ULP_GPIO_5 / ULP_GPIO_9
USART1_RS485_RE	GPIO_28 / GPIO_50	ULP_GPIO_6
USART1_RX	GPIO_10 / GPIO_29 / GPIO_55	ULP_GPIO_1 / ULP_GPIO_6
USART1_TX	GPIO_15 / GPIO_30 / GPIO_54	ULP_GPIO_4 / ULP_GPIO_7

SCT		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
SCT_IN_0	GPIO_25	ULP_GPIO_0 / ULP_GPIO_4
SCT_IN_1	GPIO_26	ULP_GPIO_1 / ULP_GPIO_5
SCT_IN_2	GPIO_27	ULP_GPIO_6
SCT_IN_3	GPIO_28	ULP_GPIO_7
SCT_OUT_0	GPIO_29	ULP_GPIO_4
SCT_OUT_1	GPIO_30	ULP_GPIO_5
SCT_OUT_2		ULP_GPIO_6
SCT_OUT_3		ULP_GPIO_7
SCT_OUT_4		ULP_GPIO_8
SCT_OUT_5		ULP_GPIO_9
SCT_OUT_7		ULP_GPIO_11

| UART2 INTERFACE | | |

IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
UART2_TX	GPIO_7 / GPIO_30	ULP_GPIO_5 / ULP_GPIO_9 / ULP_GPIO_11
UART2_RX	GPIO_6 / GPIO_29	ULP_GPIO_4 / ULP_GPIO_8
UART2_CTS	GPIO_11 / GPIO_28 / GPIO_51	ULP_GPIO_7 / ULP_GPIO_1 / ULP_GPIO_9
UART2_RTS	GPIO_10 / GPIO_27 / GPIO_50	ULP_GPIO_6 / ULP_GPIO_0 / ULP_GPIO_8
UART2_RS485_EN	GPIO_12	ULP_GPIO_0
UART2_RS485_RE	GPIO_8	ULP_GPIO_1
UART2_RS485_DE	GPIO_9	ULP_GPIO_11
M4SS TRACE		
M4SS_TRACE_CLKIN	GPIO_6 / GPIO_15 / GPIO_46 / GPIO_52	
M4SS_TRACE_CLK	GPIO_7 / GPIO_47 / GPIO_53	
M4SS_TRACE_D0	GPIO_8 / GPIO_48 / GPIO_54	
M4SS_TRACE_D1	GPIO_9 / GPIO_49 / GPIO_55	
M4SS_TRACE_D2	GPIO_10 / GPIO_50 / GPIO_56	
M4SS_TRACE_D3	GPIO_11 / GPIO_51 / GPIO_57	
Miscellaneous Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
MCU_CLK_OUT	GPIO_11 / GPIO_12 / GPIO_15	

Note:

1. For SSI (Synchronous Serial Interface) use the combinations on SoC GPIOs from these set of GPIOs only – GPIO_8 to GPIO_15, GPIO_25 to GPIO_30, GPIO_46 to GPIO_51 and GPIO_52 to GPIO_57.
2. For GSPI (General SPI) use the combinations on SoC GPIOs from these set of GPIOs only – GPIO_8 to GPIO_15, GPIO_25 to GPIO_30, GPIO_46 to GPIO_51 and GPIO_52 to GPIO_57

6.5 Functional Description

6.5.1 Digital Functions

Pin Name	Direction	Description
GSPI (General SPI) Interface		
GSPI_MST1_CLK	Output	Output Clock from the GSPI primary to external secondary
GSPI_MST1_CS0 to GSPI_MST1_CS2	Output	Active Low CSN. GSPI primary can select a maximum of 3 secondaries.
GSPI_MST1_MISO	Input	Input data to primary from external secondaries

Pin Name	Direction	Description
GSPI_MST1_MOSI	Output	Output data from primary to external secondary
I2C (Inter-integrated Circuit) Interface		
I2Cx_SCL, ULP_I2C_SCL	Inout	I2C Serial Clock x= 1, 2
I2Cx_SDA, ULP_I2C_SDA	Inout	I2C Serial Data x= 1, 2
2 Channel I2S (Inter-IC Sound) Interface		
I2S_2CH_CLK ULP_I2S_CLK	Output/ Input	I2S Clock Output in Primary Mode and Input in Secondary Mode
I2S_2CH_WS ULP_I2S_WS	Output/ Input	Active high I2S Word Select Output in Primary Mode and Input in Secondary Mode
I2S_2CH_DIN_0 to I2S_2CH_DIN_1 ULP_I2S_DIN	Input	I2S Input Data
I2S_2CH_DOUT_0 to I2S_2CH_DOUT_1 ULP_I2S_DOUT	Output	I2S Output Data
QSPI (Quad SPI) Interface		
MCU_QSPI_CLK	Output	Output clock to the external SPI secondary.
MCU_QSPI_CSN0 to MCU_QSPI_CSN1	Output	Active Low Chip Select to select a maximum of two secondaries.
MCU_QSPI_D0 to MCU_QSPI_D7	Inout	QSPI Data. Supports both QUAD and OCTA Data. In Quad Mode, only Bits M4SS_QSPI_D0 to M4SS_QSPI_D3 are valid. In Octa Mode, all the bits are valid
QSPI_PSRAM		
M4SS_PSRAM_CLK	Output	Output clock to the external PSRAM.
M4SS_PSRAM_CSN0	Output	Active Low Chip Select to select a maximum of two secondaries.
M4SS_PSRAM_D0 to M4SS_PSRAM_D3	Inout	QSPI Data. Supports QUAD Data only. In Quad Mode, only Bits M4SS_QSPI_D0 to M4SS_QSPI_D3 are valid.
PWM (Pulse Width Modulation) Interface		
PWM_xH	Output	PWM output signals. The output pins are grouped in pairs, to facilitate driving the low side and high side of a power half-bridge. x = 1,2,3,4
PWM_xL	Output	
PWM_FAULTA	Input	External fault signal A
PWM_FAULTB	Input	External fault signal B
PWM_SLP_EVENT_TRIG	Output	Special event trigger for synchronizing analog to digital conversions.
PWM_TMR_EXT_TRIG_1 to PWM_TMR_EXT_TRIG_4	Input	External trigger for base timers to increment. Each Channel has separate trigger input.
QEI (Quadrature Encode Interface)		
QEI_DIR	Output	Position counter direction. '1' means counter direction is positive. '0' means counter direction is negative.

Pin Name	Direction	Description
QEI_IDX	Input	QE Index. Index pulse occurs once per mechanical revolution and is used as a reference to indicate an absolute position.
QEI_PHA	Input	QE Phase A input
QEI_PHB	Input	QE Phase B input
SCT (State Configurable Timer) Interface		
SCT_IN_0 to SCT_IN_3	Input	Timer input event
SCT_OUT_0 to SCT_OUT_7	Output	Timer output event
SIO (Serial Input Output) Interface		
SIO_0 to SIO_7	Inout	Serial Input-Output Data
SSI (Synchronous Serial Interface) Primary		
SSI_MST_CLK ULP_SPI_CLK	Output	Output clock from SSI Primary
SSI_MST_CS0 to SSI_MST_CS3 ULP_SPI_CS0 to ULP_SPI_CS2	Output	Active Low Chip select
SSI_MST_DATA0 to SSI_MST_DATA1	Inout	Bidirectional Data
ULP_SPI_DOUT	Output	Primary Output Data
ULP_SPI_DIN	Input	Primary Input Data
SSI (Synchronous Serial Interface) Secondary		
SSI_SLV_CLK	Input	Input clock to SSI Secondary
SSI_SLV_CS	Input	Active Low Chip select
SSI_SLV_MISO	Output	Secondary Output Data
SSI_SLV_MOSI	Input	Secondary Input Data
SysRTC Interface		
SYSRTC_PRS_IN_G0	Input	Group 0 input to trigger capture operation
SYSRTC_PRS_IN_G1	Input	Group 1 input to trigger capture operation
SYSRTC_PRS_OUT_G0_0	Output	Group 0 compare 0 match interrupt
SYSRTC_PRS_OUT_G0_1	Output	Group 0 compare 1 match interrupt
SYSRTC_PRS_OUT_G1_0	Output	Group 1 compare 0 match interrupt
SYSRTC_PRS_OUT_G1_1	Output	Group 1 compare 1 match interrupt
UART Interface		
UART2_CTS, ULP_UART_CTS	Input	Active low Clear to Send
UART2_RTS, ULP_UART_RTS	Output	Active low Request to Send
UART2_RS485_DE	Output	Driver Enable. Polarity is programmable.
UART2_RS485_EN	Output	Active high RS485 Enable
UART2_RS485_RE	Output	Receiver Enable. Polarity is programmable.

Pin Name	Direction	Description
UART2_RX, ULP_UART_RX	Input	Serial Input
UART2_TX, ULP_UART_TX	Output	Serial Output
USART Interface		
USART1_CLK	Inout	Serial interface clock
USART1_CTS	Input	Active low Clear to Send
USART1_RTS	Output	Active low Request to Send
USART1_DCD	Input	Active low Data Carrier Detect
USART1_DSR	Input	Active low Data Set Ready
USART1_DTR	Output	Active low Data Terminal Ready
USART1_IR_RX	Input	IrDA SIR Input
USART1_IR_TX	Output	IrDA SIR Output
USART1_RI	Input	Active low Ring Indicator
USART1_RS485_DE	Output	Driver Enable. Polarity is programmable.
USART1_RS485_EN	Output	Active high RS485 Enable
USART1_RS485_RE	Output	Receiver Enable. Polarity is programmable.
USART1_RX	Input	Serial Input
USART1_TX	Output	Serial Output
Timers Interrupt Interface		
Timer0, Timer1,Timer2	Output	Active-high interrupts from Timers
IR Interface		
IR_INPUT	Input	IR Data Pattern Input
IR_PG_EN	Output	Active-high enable signal to the external IR Sensor.
Miscellaneous Interface		
MCU_CLK_OUT	Output	All the Clocks that are used by Cortex-M4 SoC are multiplexed and connected on this pin
ULP_EGPIO_*	Inout	ULP GPIO's controlled by Cortex M4 Processor. * represents 0, 1, 2, 4, 5, 6, 7, 8, 9, 11
AUX_ULP_TRIG_0, AUX_ULP_TRIG_1	Input	External trigger to ADC.
NWP_GPIO_*	Inout	NWP GPIO's controlled by multi-threaded processor. * represents 6, 8, 9, 10, 11, 12, 15, 46, 47, 48, 49, 50,51
UULP VBAT Pin Interface		
EXT_PG_EN	Output	Reserved
XTAL_32KHZ_IN	Input	Low Frequency clock input from an External 32KHz Crystal oscillator
MCU_GPIO2/3_WAKEUP	Input	GPIOs that can be used as Wakeup interrupt to MCU while in Retention or Deep sleep mode

Pin Name	Direction	Description
TRACE PINS		
M4SS_TRACE_CLKIN	Input	
M4SS_TRACE_CLK	Output	
M4SS_TRACE_D0	Output	Trace Packet, bit 0.
M4SS_TRACE_D1	Output	Trace Packet, bit 1
M4SS_TRACE_D2	Output	Trace Packet, bit 2
M4SS_TRACE_D3	Output	Trace Packet, bit 3

6.5.2 Analog Functions

Pin Name	Direction	Description
ADC Interface		
ADCP0 - ADCP19	Input	The 20 single ended input channels that are multiplexed onto the ADC P0 - P9 can be coupled with N0 - N9 for differential mode of operation of the ADC
ADCN0 - ADCN9	Input	The N pins of the 10 possible differential channels multiplexed onto the ADC
DAC Interface		
DAC0, DAC1	Output	Possible output pins from the internal DAC
OpAmp Interface		
OPAMPxyz	Input	Multiplexed inputs of the three OpAmps. xyz denote the OpAmp number, the terminal and the multiplexing on that pin of the OpAmp x = OpAmp number (1, 2 or 3) y = P or N terminal of OpAmp z = 0, 1, 2, 3, 4, 5 (Multiplexing at OpAmp input pin). Note that OPAMP1P is available at 6 locations, OPAMP2P, 3P and 1N are available at 2 locations each and OPAMP2N and 3N pins are available at only one location
OPAMP1OUT0/1, OPAMP2/3OUT0	Output	Outputs of the three OpAmps. Note that OPAMP1 output is available at two possible pin locations whereas OPAMP2 and 3 outputs are available at a fixed pin
Comparator Interface		
COMPx_yz		Multiplexed inputs of the two Comparators. xyz denote the Comparator number, the terminal and the multiplexing on that pin of the Comparator x = Comparator number (A or B) y = P or N terminal of OpAmp z = 0, 1 (Multiplexing at Comparator Input pin). Note that each input pin of both comparators is available on two possible GPIO pins.
Touch Interface		
TOUCH0/1/2/3/4/5/6/7	Input	Capacitive Touch inputs

7. Electrical Specifications

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and VDD supply at 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

7.1 Absolute Maximum Ratings

Functional operation above maximum ratings are not guaranteed and may damage the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{store}	Storage temperature	-40	+125	ºC
$T_{j(max)}$	Maximum junction temperature		+125	ºC
VBATT	3.3V power supply for the on-chip Buck, RF circuit, and UULP IOs	-0.5	3.63	V
IO_VDD	I/O supply for GPIOs	-0.5	3.63	V
SDIO_IO_VDD	I/O supply for SDIO I/Os	-0.5	3.63	V
FLASH_IO_VDD	I/O supply for QSPI flash signals	-0.5	3.63	V
ULP_IO_VDD	I/O supply for ULP I/Os	-0.5	3.63	V
I_{max}	Maximum Current consumption in TX mode		400	mA

7.2 Recommended Operating Conditions

Table 7.2. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
$T_{ambient}$	Ambient temperature	-40	25	85	ºC
$T_{junction}$	Junction temperature			105	ºC
VBATT	3.3V power supply for the on-chip Buck, RF Power Amplifier, UULP I/Os	3.0	3.3	3.63	V
FLASH_IO_VDD	I/O supply for Flash	1.71	1.8	1.98	V
IO_VDD	I/O supply for GPIOs	1.71	1.8	1.98	V
		2.97	3.3	3.63	
SDIO_IO_VDD	I/O supply for SDIO I/Os	1.71	1.8	1.98	V
		2.97	3.3	3.63	
ULP_IO_VDD	I/O supply for ULP I/Os	1.71	1.8	1.98	V
		2.97	3.3	3.63	

7.3 DC Characteristics

7.3.1 Reset Pin

Table 7.3. Reset Pin

Symbol	Parameter	Min.	Typ.	Max.	Unit
V$_{IH}$	High level input voltage @3.3V	0.8 * VBATT	-		V
V$_{IL}$	Low level input voltage @3.3V		-	0.3 * VBATT	V

7.3.2 Power On Control (POC) and Reset

The power on control has two control options. External source as input or internal loopback i.e. The POC_IN input of the chip can be connected to the internally generated POC_OUT signal. RESET_N will be pulled low if POC_IN is low.

7.3.2.1 POC_OUT Connected to POC_IN

The IC generates a POC (Power On Control) signal - POC_OUT that is distributed to all I/O cells to prevent the I/O cells from powering up in an undesired configuration and is also used inside the IC to safe state the IC till a valid supply is available for proper operation. This power management is functional in both power up and power down sequences.

During power up, until the VBATT reaches 1.6V , the POC_OUT signal stays low. Once the VBATT supply exceeds 1.6V, the POC_OUT becomes high and normal operation of the IC starts.

Once the POC_OUT becomes high, it stays high. But if VBATT becomes lower than the Blackout threshold voltage, POC_OUT becomes low

The following figure illustrates the power up sequence when POC_OUT is connected to POC_IN. As shown in the figure below, the RESET_N is high at least 1.6ms after VBATT supply is stable. The RESET_N signal can be controlled via options like an R/C circuit or another MCU's GPIO.
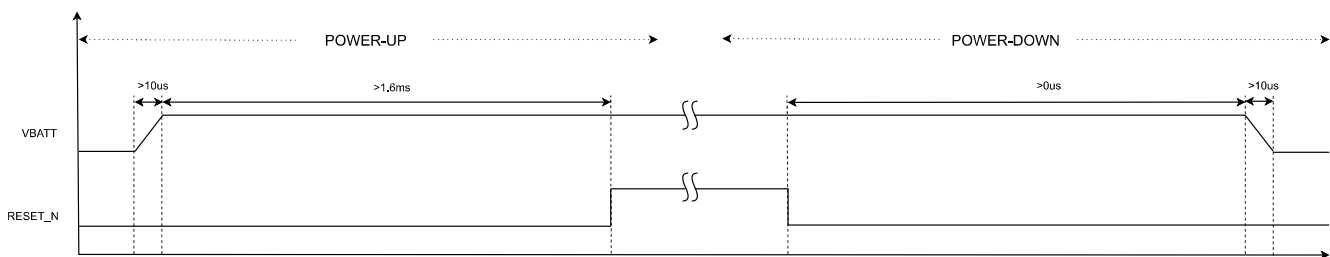
Figure 7.1. Power Up Sequence when POC_OUT is Connected to POC_IN

7.3.2.2 External Control for POC_IN

The POC_IN and RESET_N signals can be controlled from external source like R/C circuits and/or another MCU's GPIOs . The figure below illustrates the requirement for controlling POC_IN and RESET_N with respect to the VBATT supplies.
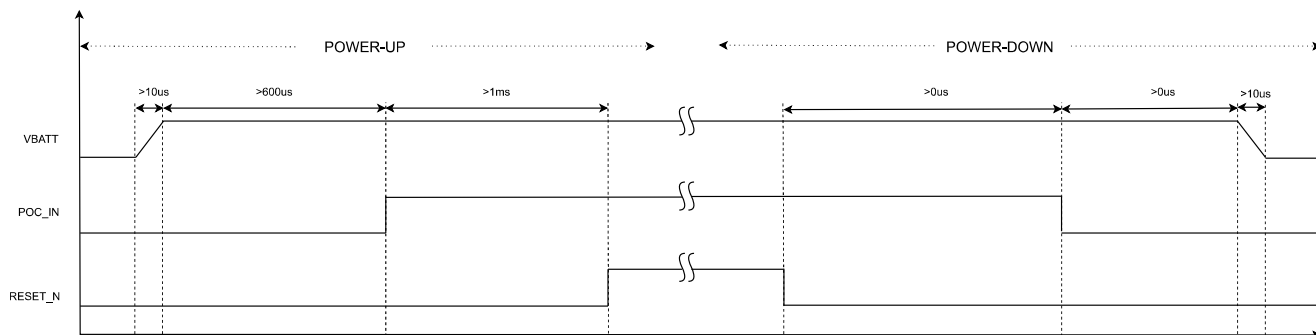

Figure 7.2. Power Up Sequence with External Control for POC_IN

7.3.3 Blackout Monitor

The blackout comparator is enabled by default upon power up. Blackout is typically asserted when the UULP_VBATT_1/2 (VBATT) supply goes lower than 1.6V (see table below), and it is de-asserted when VBATT supply goes higher than 1.625V. Upon a blackout event, the RESET_N signal is autonomously pulled low. The blackout monitor circuit performs this function only when POC_OUT is connected to POC_IN.

Blackout monitor will be disabled after power up. The functionality should be enabled by customer if required. The blackout monitor block should be enabled to monitor the VBATT voltage only in high power modes. In low power modes battery level detection can be implemented using the Nano-Power Brownout detection comparator.

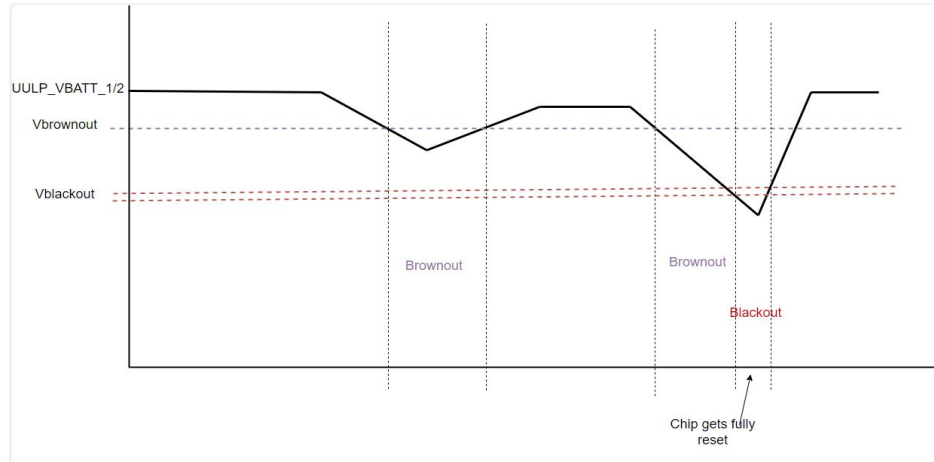When system is in low power mode , the blackout comparator is enabled upon a brownout event.

Figure 7.3. Blackout Monitor

Table 7.4. Blackout Monitor Electrical Specifications

Parameter	Parameter Description	Conditions	Min.	Typ.	Max.	Unit
Blackout VTL	VBATT voltage at which the Blackout monitor resets the IC			1.56	1.65	V
Blackout VTH	VBATT voltage at which the Blackout monitor releases the IC from reset			1.59	1.675	V

7.3.4 Digital Input Output Signals

Table 7.5. Digital I/O Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage @ IOVDD = 3.3V	2.0	-	-	V
	High level input voltage @ IOVDD = 1.8V	1.17	-	-	V
V_{IL}	Low level input voltage @ IOVDD = 3.3V	-	-	0.8	V
	Low level input voltage @ IOVDD = 1.8V	-	-	0.63	V
V_{OL}	Low level output voltage	-	-	0.4	V
V_{OH}	High level output voltage	IOVDD -0.4	-	-	V
I_{OL}	Low level output current	2.0	4.0	12.0	mA
I_{OH}	High level output current	2.0	4.0	12.0	mA
I_{OL} for UULP_GPIO_*	Low level output current	1.0		2.0	mA
I_{OH} for UULP_GPIO_*	High level output current	1.0		2.0	mA

7.3.4.1 Open-Drain I2C Pins

Table 7.6. Open-Drain I2C Pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage	0.7 * IOVDD	-	-	V
V_{IL}	Low level input voltage	-	-	0.3 * IOVDD	V

7.4 AC Characteristics

7.4.1 Clock Specifications

The SiWG917M chipsets require two primary clocks:
- Low frequency 32 kHz clock for sleep manager and RTC
  - Internal 32 kHz RC clock is used for applications with low timing accuracy requirements
  - 32 kHz external clock is used for applications with high timing accuracy requirements
- High frequency 40 MHz clock for the multi-threaded processor, baseband subsystem and the radio
  - 40 MHz clock is integrated inside the module, and no external clock needs to be provided

The chipsets have integrated internal oscillators including crystal oscillators to generate the required clocks. Integrated crystal oscillators enable the use of low-cost passive crystal components. Additionally, in a system where an external clock source is already present, the clock can be reused. The following are the recommended options for the clocks for different functionalities:

32 kHz External Sources:

Option 1: From Host MCU/MPU LVCMOS rail to rail clock input on UULP_VBAT_GPIO_3
Option 2: External Xtal oscillator providing LVCMOS rail to rail clock input on UULPGPIO (Nano-drive clock should not be supplied).

7.4.1.1 Low Frequency Clock

The 32 kHz clock selection can be done through software. RC oscillator clock is not suited for high timing accuracy applications and can increase system current consumption in duty-cycled power modes.

32 kHZ Internal RC Oscillator

Table 7.7. 32 kHz RC Oscillator

Parameter	Parameter Description	Min	Typ	Max	Unit
F_{osc}	Oscillator Frequency		32.0		kHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage		1.2		%

32 kHz External Oscillator

An external 32 kHz low-frequency clock can be fed through the XTAL_32KHZ_IN functionality.
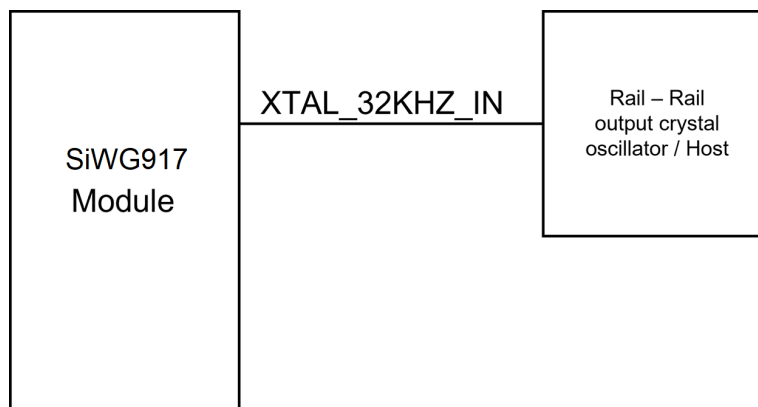
Figure 7.4. External 32 kHz Oscillator - Rail to Rail

Table 7.8. 32 kHz External Oscillator Specifications

Parameter	Parameter Description	Min	Typ	Max	Unit
F_{osc}	Oscillator Frequency		32.768		kHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage	-100		100	ppm
Duty cycle	Input duty cycle	30	50	70	%
V_{AC}	Input AC peak-peak voltage swing at input pin.	-0.3	–	VBATT ±10%	Vpp

7.4.2 SDIO 2.0 Secondary

7.4.2.1 Full Speed Mode

Table 7.9. AC Characteristics - SDIO 2.0 Secondary Full Speed Mode

Parameter	Parameter Description	Min	Typ	Max	Unit
T_{sdio}	SDIO_CLK	–	–	25	MHz
T_s	SDIO_DATA/SDIO_CMD, input setup time	4	–	–	ns
T_h	SDIO_DATA/SDIO_CMD, input hold time	1.2	–	–	ns
T_{od}	SDIO_DATA/SDIO_CMD, clock to output delay	–	–	13	ns
C_L	Output Load	5	–	10	pF
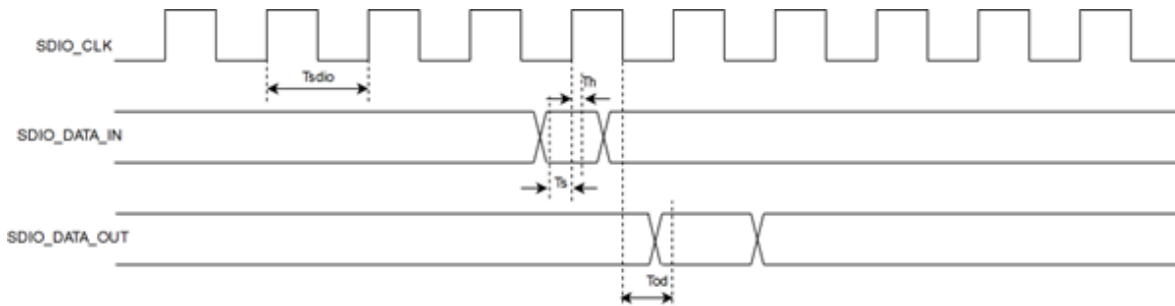
Figure 7.5. Interface Timing Diagram for SDIO 2.0 Secondary Full Speed Mode

7.4.2.2 High Speed Mode

Table 7.10. AC Characteristics - SDIO 2.0 Secondary High Speed Mode

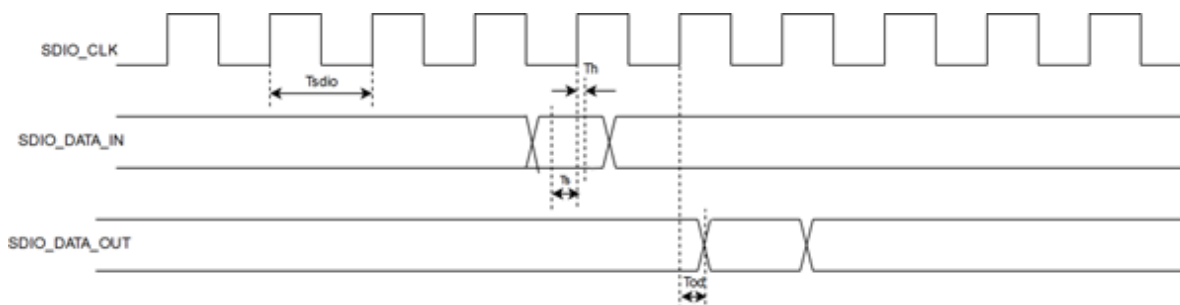| Parameter	Parameter Description	Min	Typ	Max	Unit
T_{sdio}	SDIO_CLK	25	–	50	MHz
T_s	SDIO_DATA/SDIO_CMD, input setup time	4	–	–	ns
T_h	SDIO_DATA/SDIO_CMD, input hold time	1.2	–	–	ns
T_{od}	SDIO_DATA/SDIO_CMD, clock to output delay	2.5	–	13	ns
C_L	Output Load	5	–	10	pF

Figure 7.6. Interface Timing Diagram for SDIO 2.0 Secondary High Speed Mode

7.4.3 SPI Secondary

7.4.3.1 Low Speed Mode

Table 7.11. AC Characteristics - SPI Secondary Low Speed Mode

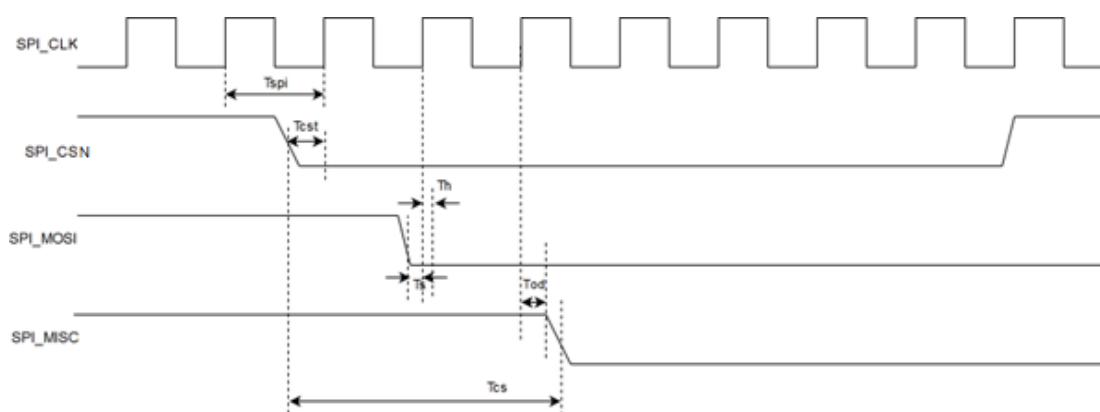| Parameter	Parameter Description	Min	Typ	Max	Unit
T_{spi}	SPI_CLK	0	–	25	MHz
T_{cs}	SPI_CSN to output delay	–	–	7.5	ns
T_{cst}	SPI_CSN to input setup time	4.5	–	–	ns
T_s	SPI_MOSI, input setup time	1.4	–	–	ns
T_h	SPI_MOSI, input hold time	1.5	–	–	ns
T_{od}	SPI_MISO, clock to output delay	–	–	8.75	ns
C_L	Output Load	5	–	10	pF
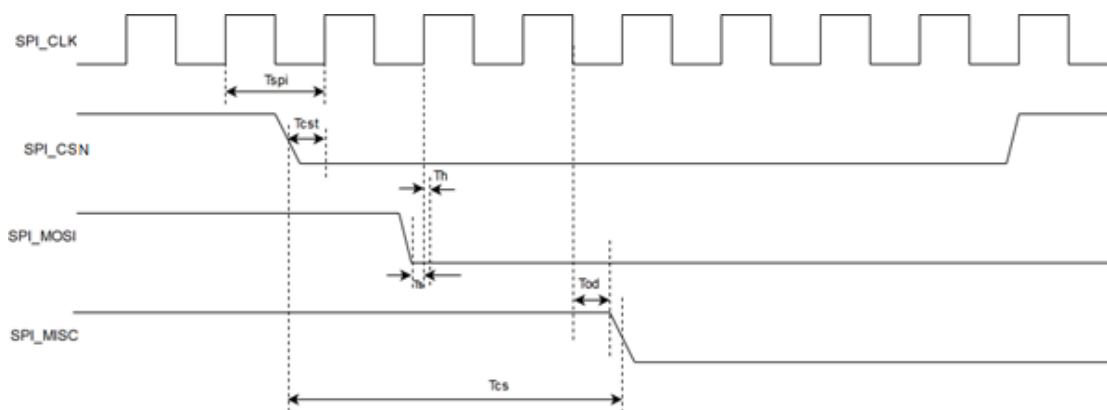
Figure 7.7. Interface Timing Diagram for SPI Secondary Low Speed Mode

7.4.3.2 High Speed Mode

Table 7.12. AC Characteristics - SPI Secondary High Speed Mode

Parameter	Parameter Description	Min	Typ	Max	Unit
T_{spi}	SPI_CLK	25	–	80	MHz
T_{cs}	SPI_CSN to output delay	–	–	7.5	ns
T_{cst}	SPI_CSN to input setup time	4.5	–	–	-
T_s	SPI_MOSI, input setup time	1.4	–	–	ns
T_h	SPI_MOSI, input hold time	1.4	–	–	ns
T_{od}	SPI_MISO, clock to output delay	1.5	–	8.75	ns
C_L	Output Load	5	–	10	pF

Figure 7.8. Interface Timing Diagram for SPI Secondary High Speed Mode

7.4.3.3 Ultra High Speed Mode

Table 7.13. AC Characteristics - SPI Secondary Ultra High Speed Mode

Parameter	Parameter Description	Min	Typ	Max	Unit
T_{spi}	SPI_CLK	80	–	100	MHz
T_s	SPI_MOSI, input setup time	1.4	–	–	ns
T_h	SPI_MOSI, input hold time	1.4	–	–	ns
T_{od}	SPI_MISO, clock to output delay	1.5	–	8.75	ns
C_L	Output Load	5	–	10	pF
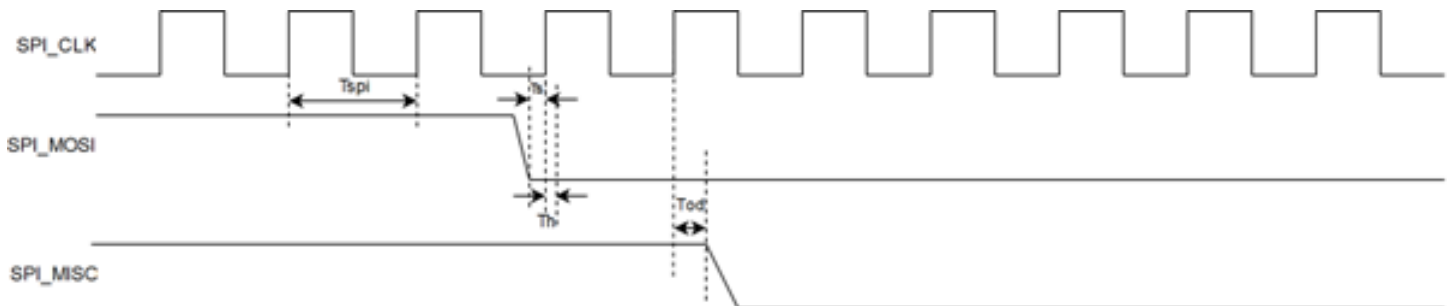
Figure 7.9. Interface Timing Diagram for SPI Secondary Ultra High Speed Mode

7.4.4 UART

Table 7.14. AC Characteristics - UART

Parameter	Parameter Description	Min	Typ	Max	Unit
T_{uart}	CLK			20	MHz
T_{od}	Output delay			10	ns
C_L	Output load			25	pF

7.4.5 GPIO Pins

Table 7.15. AC Characteristics - GPIO Pins

Parameter	Parameter Description	Conditions	Min.	Typ.	Max.	Unit
T_{rf}	Rise time	Pin configured as output; SLEW = 1(fast mode)	1.0	-	4	ns
T_{ff}	Fall time	Pin configured as output; SLEW = 1(fast mode)	0.9	-	4	ns
T_{rs}	Rise time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	5	ns
T_{fs}	Fall time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	5	ns
T_r	Rise time	Pin configured as input	0.3	-	1.3	ns
T_f	Fall time	Pin configured as input	0.2	-	1.2	ns

7.4.6 Flash Memory (Embedded)

Table 7.16. AC Characteristics - Flash Memory

Parameter	Parameter Description	Conditions	Min.	Typ.	Max.	Unit
N_{endu}	Endurance	Sector erase/program	10000	-	-	cycles
		Page erase/program, page in large sector	10000	-	-	cycles
		Page erase/program, page in small sector	10000	-	-	cycles
T_{ret}	Retention time	Powered	10	-	-	years
		Unpowered	10	-	-	years
T_{er}	Block Erase time (32KB)	Page, sector or multiple consecutive sectors	-	150	1400	ms
T_{prog}	Page Programming time		-	0.5	3	ms
T_{ce}	Chip Erase time			20	65	s

7.4.7 QSPI

7.4.7.1 Full Speed Mode (Rising Edge Sampling)

Table 7.17. AC Characteristics - QSPI Full Speed Mode (Rising Edge Sampling)

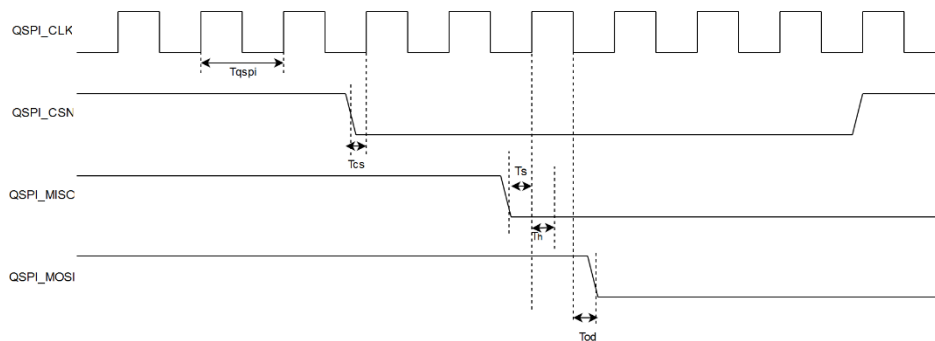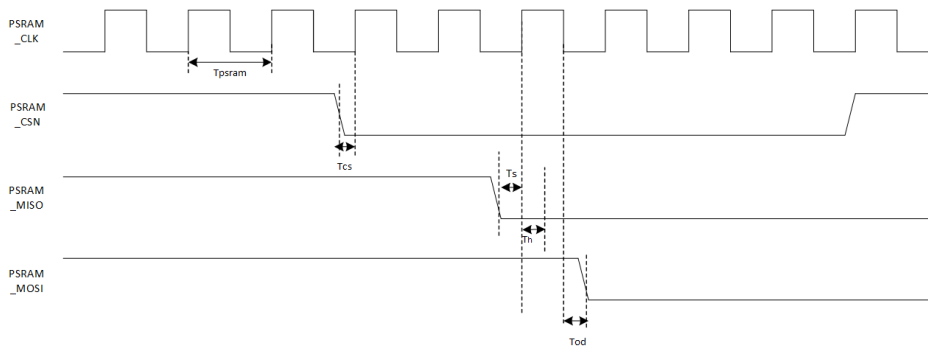| Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{qspi}	qspi_clk	0	-	40	MHz
T_{cs}	qspi_cs, to clock edge(this is achieved functionally)	8.6	-	-	ns
T_s	qspi_miso, setup time	4	-	-	ns
T_h	qspi_miso, hold time	2.5	-	-	ns
T_{od}	qspi_mosi, clock to output valid	-2	-	2	ns
C_L	Output Load	5	-	10	pF

Figure 7.10. Interface Timing Diagram for QSPI Full Speed Mode (Rising Edge Sampling)

7.4.7.2 High Speed Mode (Falling Edge Sampling)

Table 7.18. AC Characteristics - QSPI High Speed Mode (Falling Edge Sampling)

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{qspi}	qspi_clk	0	-	80	MHz
T_{cs}	qspi_cs, to clock edge(this is achieved functionally)	4.3	-	-	ns
T_s	qspi_miso, setup time	4	-	-	ns
T_h	qspi_miso, hold time	2.5	-	-	ns
T_{od}	qspi_mosi, clock to output valid	-2	-	2	ns
C_L	Output Load	5	-	10	pF
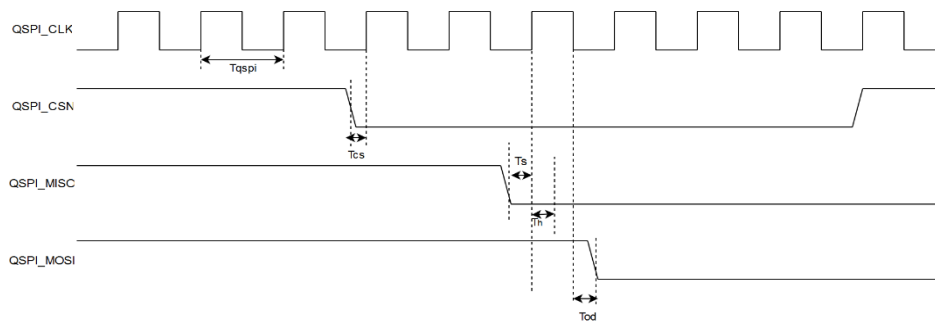
Figure 7.11. Interface Timing Diagram for QSPI High Speed Mode (Falling Edge Sampling)

7.4.8 PSRAM

7.4.8.1 Full Speed Mode (Rising Edge Sampling)

Table 7.19. AC Characteristics - PSRAM Full Speed Mode (Rising Edge Sampling)

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{psram}	psram_clk	0	-	40	MHz
T_{cs}	psram_cs, to clock edge(this is achieved functionally)	8.6	-	-	ns
T_s	psram_miso, setup time	4	-	-	ns
T_h	psram_miso, hold time	2.5	-	-	ns
T_{od}	psram_mosi, clock to output valid	-2	-	2	ns
C_L	Output Load	5	-	10	pF

Figure 7.12. Interface Timing Diagram for PSRAM Full Speed Mode (Rise Edge Sampling)

7.4.8.2 High Speed Mode (Falling Edge Sampling)

Table 7.20. AC Characteristics - PSRAM High Speed Mode (Falling Edge Sampling)

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{psram}	psram_clk	40	-	80	MHz
T_{cs}	psram_cs, to clock edge(this is achieved functionally)	4.3	-	-	ns
T_s	psram_miso, setup time	4	-	-	ns
T_h	psram_miso, hold time	2.5	-	-	ns
T_{od}	psram_mosi, clock to output valid	-2	-	2	ns
C_L	Output Load	5	-	10	pF
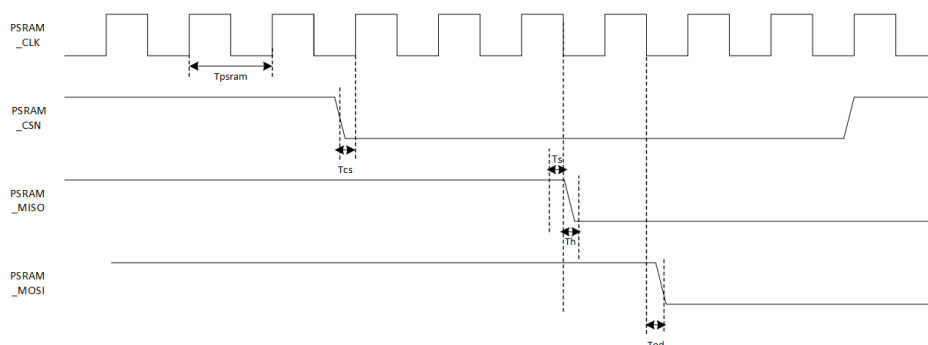
Figure 7.13. Interface Timing Diagram for PSRAM High Speed Mode (Falling Edge Sampling)

7.4.9 I2C

7.4.9.1 Fast Speed Mode

Table 7.21. AC Characteristics - I2C Fast Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2c}	SCL	100	-	400	KHz
T_{low}	clock low period	1.3	-	-	us
T_{high}	clock high period	0.6	-	-	us
T_{sstart}	start condition, setup time	0.6	-	-	us
T_{hstart}	start condition, hold time	0.6	-	-	us
T_s	data, setup time	100	-	-	ns
T_{sstop}	stop condition, setup time	0.6	-	-	us
C_L	Output Load	5	-	10	pF
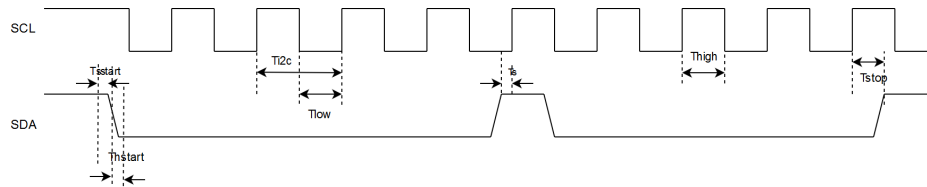
Figure 7.14. Interface Timing Diagram for I2C Fast Speed Mode

7.4.9.2 High Speed Mode

Table 7.22. AC Characteristics - I2C High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2c}	SCL	0.4	-	3.4	MHz
T_{low}	clock low period	160	-	-	ns
T_{high}	clock high period	60	-	-	ns
T_{sstart}	start condition, setup time	160	-	-	ns
T_{hstart}	start condition, hold time	160	-	-	ns
T_{s}	data, setup time	10	-	-	ns
T_{h}	data, hold time	0	-	70	ns
T_{sstop}	stop condition, setup time	160	-	-	ns
C_{L}	Output Load	5	-	10	pF
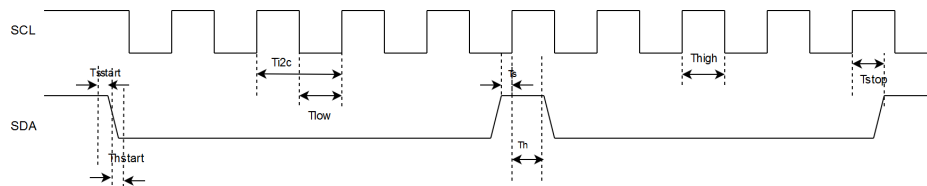
Figure 7.15. Interface Timing Diagram for I2C High Speed Mode

7.4.10 I2S/PCM Primary and Secondary
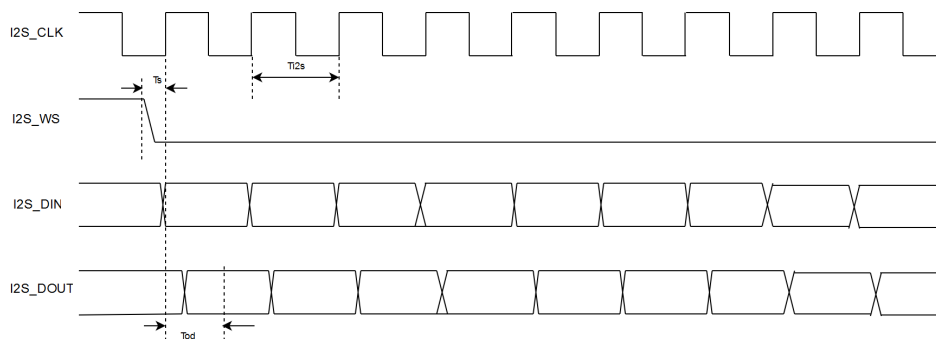
7.4.10.1 Primary Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Table 7.23. AC Characteristics – I2S/PCM Primary Mode

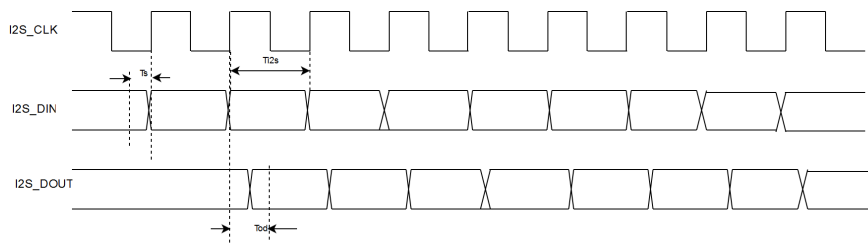| Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	25	MHz
T_s	i2s_din,i2s_ws setup time	10	-	-	ns
T_h	i2s_din,i2s_ws hold time	3	-	-	ns
T_{od}	i2s_dout output delay	0	-	15	ns
C_L	i2s_dout output load	5	-	10	pF
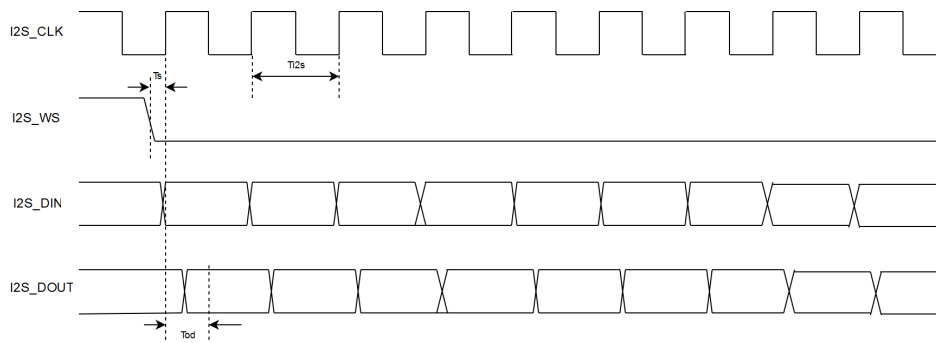
Figure 7.16. Interface Timing Diagram for I2S Primary Mode

7.4.10.2 Secondary Mode

Negedge driving and posedge sampling for I2S

Posedge driving and negedge sampling for PCM

Table 7.24. AC Characteristics - I2S/PCM Secondary Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	25	MHz
T_s	i2s_din,i2s_ws setup time	7.5	-	-	ns
T_h	i2s_din,i2s_ws hold time	2	-	-	ns
T_{od}	i2s_dout output delay	0	-	17	ns
C_L	i2s_dout output load	5	-	10	pF

Figure 7.17. Interface Timing Diagram for I2S Secondary Mode

7.4.11 ULP I2S/PCM Primary and Secondary

7.4.11.1 Primary Mode

Negedge driving and posedge sampling for I2S
posedge driving and negedge sampling for PCM

Table 7.25. AC Characteristics – ULP I2S/PCM Primary Mode

Parameter	Paramter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	10	MHz
T_s	i2s_din,i2s_ws setup time w.r.t negedge	15	-	-	ns
T_h	i2s_din,i2s_ws hold time w.r.t negedge	0	-	-	ns
T_{od}	i2s_dout output delay	0	-	20	ns
C_L	i2s_dout output load	5	-	10	pF

Figure 7.18. Interface timing Diagram for ULP I2S/PCM Primary

7.4.11.2 Secondary Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Table 7.26. AC Characteristics - ULP I2S/PCM Secondary Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	10	MHz
T_s	i2s_din,i2s_ws setup time w.r.t negedge	10	-	-	ns
T_h	i2s_din,i2s_ws hold time w.r.t negedge	3	-	-	ns
T_{od}	i2s_dout output delay	0	-	20	ns
C_L	i2s_dout output load	5	-	10	pF
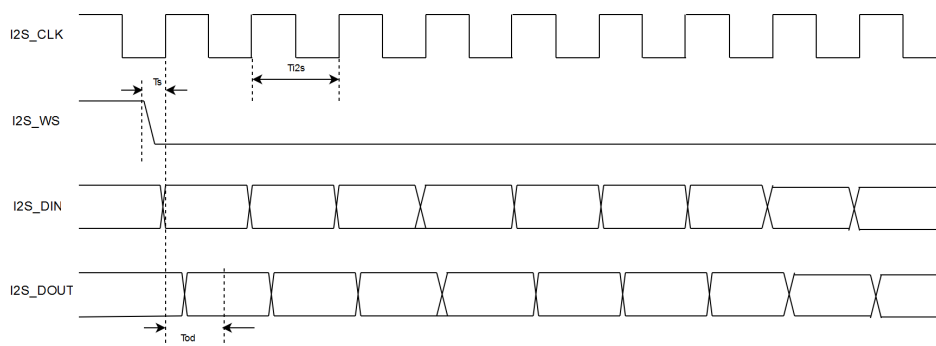
Figure 7.19. Interface Timing Diagram for ULPI2S Secundary

7.4.12 SSI Primary/Secondary

7.4.12.1 Primary Full Speed Mode

Negedge driving and posedge sampling

Table 7.27. AC Characteristics - SSI Primary Full Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{ssi}	SSI_CLK	0	-	20	MHz
T_s	SSI_MISO, input setup time	17	-	-	ns
T_h	SSI_MISO, input hold time	2	-	-	ns
T_{od}	SSI_CS, SSI_MOSI, clock to output valid	0	-	16	ns
C_L	Output Load	5	-	10	pF
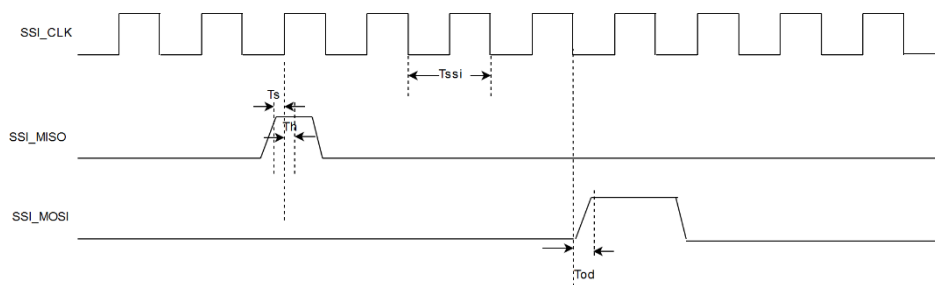
Figure 7.20. Interface Timing Diagram for SSI Primary Full Speed Mode

7.4.12.2 Primary High Speed Mode

Table 7.28. AC Characteristics - SSI Primary High Speed Mode

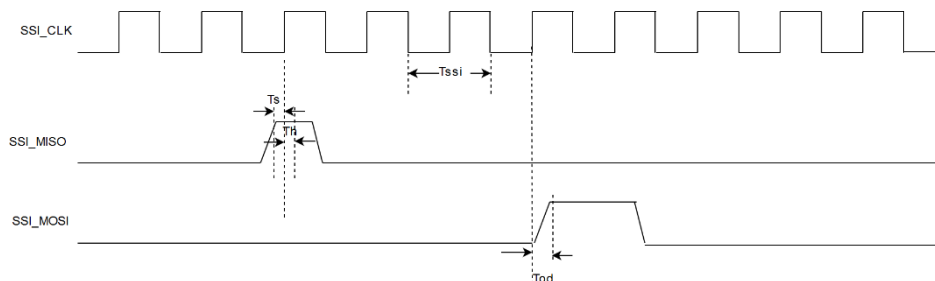| Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{ssi}	SSI_CLK	20	-	40	MHz
T_s	SSI_MISO, input setup time	17	-	-	ns
T_h	SSI_MISO, input hold time	2	-	-	ns
T_{od}	SSI_CS,SSI_MOSI, clock to output valid	1	-	16	ns
C_L	Output Load	5	-	10	pF

Figure 7.21. Interface Timing Diagram for SSI Primary High Speed Mode

7.4.12.3 Secondary Full Speed Mode

Negedge driving and posedge sampling

Table 7.29. AC Characteristics – SSI Secondary Full Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{ssi}	SSI_CLK	0	-	20	MHz
T_s	SSI_MOSI,CS, input setup time	5	-	-	ns
T_h	SSI_MOSI, input hold time	0	-	-	ns
T_{od}	SSI_MISO, clock to output delay	-	-	24	ns
C_L	Output Load	5	-	10	pF
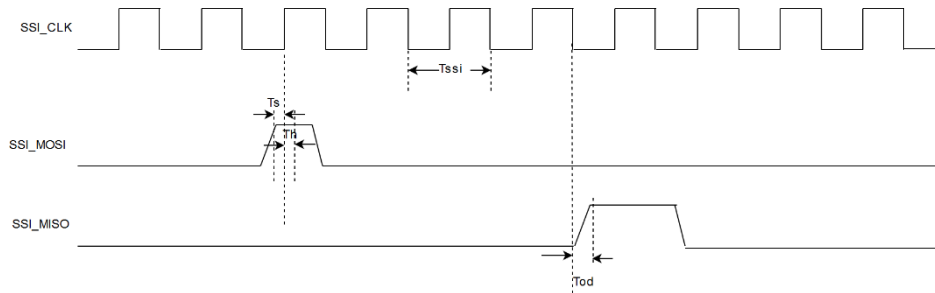
Figure 7.22. Interface Timing Diagram for SSI Secondary Full Speed Mode

7.4.13 ULP SSI Primary

7.4.13.1 Primary Full Speed Mode

Negedge driving and posedge sampling

Table 7.30. AC Characteristics - ULP SSI Primary Full Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{ssi}	SSI_CLK	0	-	10	MHz
T_s	SSI_MISO, input setup time	20	-	-	ns
T_h	SSI_MISO, input hold time	0	-	-	ns
T_{od}	SSI_CS, SSI_MOSI, clock to output valid	0	-	25	ns
C_L	Output Load	5	-	10	pF
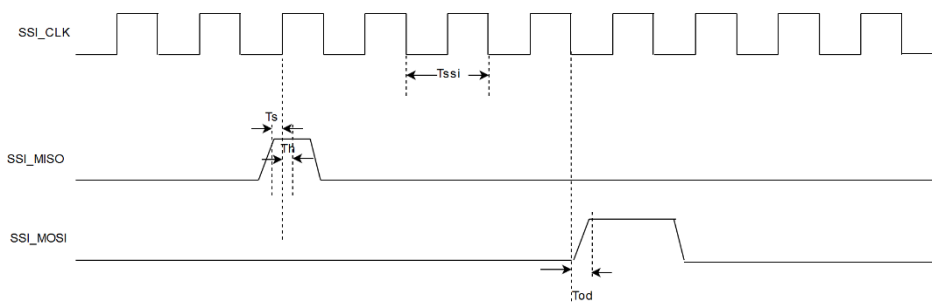
Figure 7.23. Interface Timing Diagram for ULPSSI -- Full Speed Mode

7.4.14 SGPIO/MC-PWM/QEI/SCT Timer/SIO Interfaces

Table 7.31. AC Characteristics – SGPIO/PWM/QEI

Paramter	Parameter Description	Min.	Typ.	Max.	Unit
T_{sct}	CLK	0	-	10	MHz
T_{od}	Output delay	0	-	20	ns
T_s	Input setup time	10	-	-	ns
T_h	Input hold time	1	-	-	ns
C_L	Output load	5	-	10	pF

7.4.15 USART

Table 7.32. AC Characteristics - USART

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{usart}	Interface CLK	0	-	20	MHz
T_{od}	Clock to Output delay	0	-	20	ns
T_s	Input setup time	10	-	-	ns
T_h	Input hold time	1	-	-	ns
C_L	Output load	5	-	10	pF

7.4.16 GSPI Primary

7.4.16.1 Full Speed Mode

Table 7.33. AC Characteristics - GSPI Primary Full Speed Mode

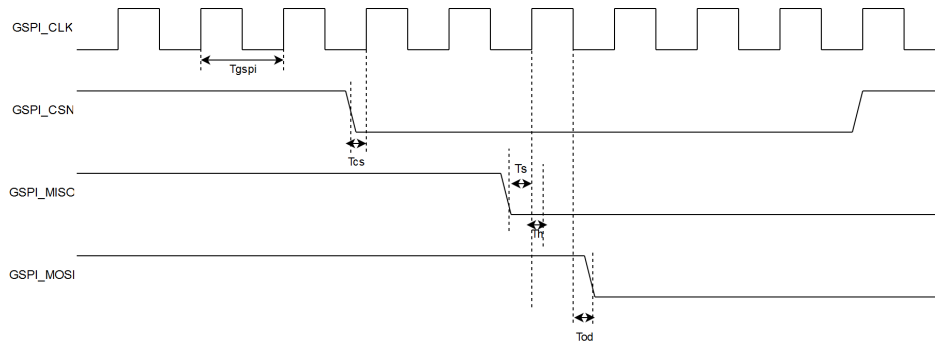| Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{gspi}	gspi_clk	0	-	58	MHz
T_{cs}	gspi_cs, to clock edge(this is achieved functionally)	4.16	-	-	ns
T_s	gspi_miso, setup time	2	-	-	ns
T_h	gspi_miso, hold time	2	-	-	ns
T_{od}	gspi_cs, gspi_mosi, clock to output valid	0	-	8	ns
C_L	Output Load	5	-	10	pF

Figure 7.24. Interface Timing Diagram for GSPI Primary Full Speed Mode

7.4.16.2 High Speed Mode

Table 7.34. AC Characteristics - GSPI Primary High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{gspi}	gspi_clk	58	-	116	MHz
T_{cs}	gspi_cs, to clock edge(this is achieved functionally)	4.16	-	-	ns
T_s	gspi_miso, setup time	2	-	-	ns
T_h	gspi_miso, hold time	2	-	-	ns
T_{od}	gspi_cs, gspi_mosi, clock to output valid	0	-	8	ns
C_L	Output Load	5	-	10	pF
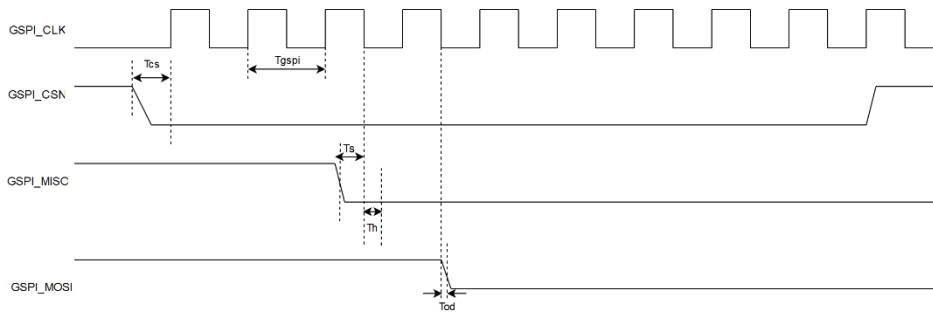
Figure 7.25. Interface Timing Diagram for GSPI Primary High Speed Mode

7.4.17 Cortex-M4 JTAG

Table 7.35. AC Characteristics - Cortex-M4 JTAG

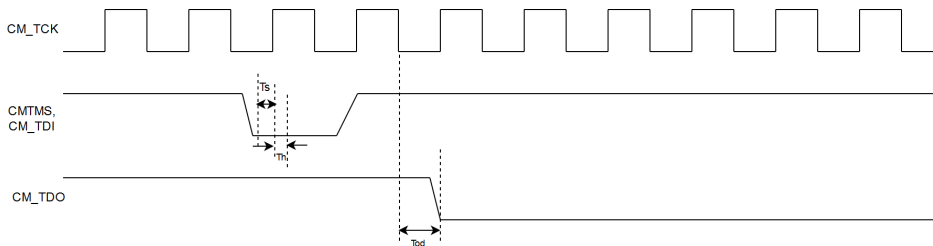| Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{tck}	TCK period	-	-	20	MHz
T_s	Setup	5	-	-	ns
T_h	Hold	4	-	-	ns
T_{od}	Output Delay	0	-	38.5	ns
C_L	Output Load	5	-	10	pF

Figure 7.26. Interface Timing Diagram for Cortex-M4 JTAG

7.4.18 Cortex-M4 Trace

Table 7.36. AC Characteristics - Cortex-M4 Trace

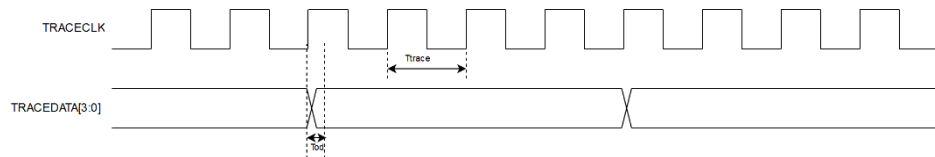| Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{trace}	TRACECLK Period	0	-	100	MHz
T_{od}	Output Delay	1.2	-	8	ns
C_L	Output Load	5	-	10	pF

Figure 7.27. Interface Timing Diagram for Cortex-M4 Trace

7.5 Analog Peripherals

The following analog peripherals are available:
- 2x Analog Comparators
- 3x General purpose Op-Amp
- 16 channel, 12 bit, 5 MSPS Analog to Digital Converter with both single ended and differential modes
- 10 bit, 5 MSPS Digital to Analog Converter

7.5.1 Analog Comparators

Analog comparator is a peripheral circuit that compares two analog voltage inputs and gives a logical output based on comparison.

There are 9 different inputs for each pin of comparator, and 2 of the 9 are external pin inputs.
The following cases of comparison are possible

1. Compare external pin inputs
2. Compare external pin input to internal voltages.
3. Compare internal voltages.

The comparator compares inputs p and n to produce an output, cmp_out.

p > n, cmp_out = 1

p < n, cmp_out = 0

Analog Peripherals consists of 2 comparators whose inputs can be programmed independently. The reference buffer and resistor bank are shared between the two comparators and can be enabled only when at least one of the comparators is enabled.

Table 7.37. Analog Comparator Electrical Specifications

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
V_{ref}	Programmable voltage reference range		0.1		1.1	V
V_{ref_step}	Programmable voltage reference step size			0.1		V
V_{os_comp}	The minimum voltage difference required between inputs to make output high	Typical value corresponds to 1-sigma variation		1.4		mV
V_{hyst_comp}	Hysteresis = 2'd1			60		mV
	Hysteresis = 2'd3			90		mV
ICMR_comp	Input common-mode range		0.15		ULP_IO_VDD-0.15	V
I_{q_comp}	Current consumption on VBATT with all blocks enabled			305		uA

7.5.2 Auxiliary (AUX) LDO

Table 7.38. AUX LDO Electrical Specifications - Regulation Mode

Paramater	Parameter Description	Conditions	Min	Typ	Max	Units
V_{in}	Input Supply Voltage	AUX LDO in Regulation Mode	2.97	3.3	3.63	V
V_{outmax}	Max Output voltage programmable			2.8		V
V_{outmin}	Min Output voltage programmable			1.6		V
V_{step}	Output voltage programmable step size			80		mV
I_{load}	Load current capability				16	mA
I_q	Quiescent current			80		µA

Table 7.39. AUX LDO Electrical Specifications - Bypass Mode

Paramater	Parameter Description	Conditions	Min	Typ	Max	Units
V_{in}	Input Supply Voltage	AUX LDO in Bypass Mode	1.71	1.8	1.98	V
R_{on}	ON Resistance between V_{in} to V_{out} pins of AUX LDO			6.3		Ohm
V_{drop}	Voltage drop from V_{in} to V_{out}	Load = 16mA (Max)		100		mV
V_{out}	$V_{out} = V_{in} - R_{on} * I_{load}$	Load = 16mA at V_{in} = 1.71V		1.61		V

Note:

1. Maximum load current is possible when the three op-amps, two analog comparators, ADC, and DAC are all enabled.
2. Programmable output voltage step, Vstep, can vary up to ±5%.

7.5.3 Analog to Digital Converter

- 12 bit precision ADC
- Single ended mode and differential mode configuration
- Two clock latency

Table 7.40. ADC Electrical Specifications

Parameter	Parameter Description	Conditions	Min	Typ.	Max	Units
N	Resolution of ADC			12		bits
$N_{channel}$	Number of channels – Single ended Mode			16		-
	Number of channels – Differential Mode			8		
f_{ADC}	ADC sampling and input clock frequency				5	MHz
V_{AIN}	Input voltage range – Single ended Mode	Positive terminal	0		AUX_AVDD	V
	Differential Input voltage range – Differential Mode	Positive & negative terminals	0		AUX_AVDD/2	
R_{in}	Input resistance	Single Channel input conversion		100		KΩ
$C_{sampled}$	ADC internal sample and hold capacitor			3		pF
C_{fixed}	Fixed capacitance from multiplexers and ESD protection			2		pF
t_s	Sampling time		0.1			uS
G_{err}	Gain Error		-2		2	%
Offset	Offset		-2		2	mV
ENOB	Effective number of bits			10.1		bits
SNDR	Signal to noise and distortion ratio			62.5		dB
I_{active}	Active current consumption	Input frequency 100kHz at 5Msps		1.5		mA

7.5.4 Digital to Analog Convertor

- 10 bit precision DAC
- Single ended voltage outputs
- 1.71 to 3.63V supply operation.

Table 7.41. DAC Electrical Specifications

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
VOL	Lowest output voltage			0.15*AUX_AVDD		V
VOH	Highest output voltage			0.85*AUX_AVDD		V
R_{load}	Resistive load	Connect to ground	5			KΩ
C_{load}	Load capacitance				50	pF
SNDR	Signal to Noise Ratio	At an input frequency of 100kHz and sampling frequency of 5MHz		50		dB
ENOB	Effective number of Bits	At an input frequency of 100kHz and sampling frequency of 5MHz		8		bits

7.5.5 Op-Amp

There are 3 general purpose Operational Amplifiers (Op-Amps) offering rail-to-rail inputs and outputs.
The Op-Amps can be configured as:

1. Unity gain amplifier
2. Trans-Impedance Amplifier (TIA)
3. Non-inverting Programmable Gain Amplifier (PGA)
4. Inverting Programmable Gain Amplifier (PGA)
5. Non-inverting Programmable hysteresis comparator
6. Inverting Programmable hysteresis comparator
7. Cascaded Non-Inverting PGA
8. Cascaded Inverting PGA
9. Two Op-Amps Differential Amplifier
10. Instrumentation Amplifier

Note:
- In the above list, #7, #8, #9 are configured by cascading 2 Op-Amps
- In the above list, #10 is configured by cascading 3 Op-Amps

Table 7.42. Opamp Electrical Specifications

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
V_{in}	Input Voltage range		0		AUX_AVDD	V
V_{out}	output voltage range	1mA, source or sink	0.1		AUX_AVDD - 0.1	V
I_{out}	output current capability, source or sink	0.5 < Vout < AUX_AVDD-0.5			3	mA
V_{os}	Input offset voltage (1 sigma)	power mode = high C_L=50pF		2.2		mV
		power mode = low C_L=50pF		2.2		mV
Ge1	Gain error, unity gain buffer mode, RL=1Kohm	power mode = high C_L=50pF		1		%
		power mode = low C_L=50pF		1		%
PM	Phase margin, in UGB mode	power mode = high C_L=50pF		59		degrees
		power mode = low C_L=50pF		63		degrees
GBW	Gain-bandwidth product	power mode = high C_L=50pF		17		MHz
		power mode = low C_L=50pF		7.5		MHz
THD_UGB	Total Harmonic Distortion, at 100KHz (UGB mode)	power mode = high C_L=50pF		-64		dB
		power mode = low C_L=50pF		-62		dB

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion, at 10KHz (Non inv amp mode, gain = 51)	power mode = high C_L=50pF		-58		dB
		power mode = low C_L=50pF		-56		dB
PSRR	DC Power supply rejection ratio	power mode = high C_L=50pF		90		dB
		power mode = low C_L=50pF		90		dB
CMRR	DC Common mode rejection ratio	power mode = high C_L=50pF		70		dB
		power mode = low C_L=50pF		71		dB
Idd	Quiescent current - 1 Op-Amp	power mode = high C_L=50pF		0.95		mA
		power mode = low C_L=50pF		315		uA

7.5.6 Temperature Sensor

- Consists of Ring Oscillator (RO) based and BJT based temp sensor.
- Generates PTAT Voltage from BJT based band gap.
- Buffered PTAT voltage is given at ADC Input.
- Output of the ADC is linear function of temperature.
- Generates Temperature dependent and independent clock
- Digital logic to convert the output clock to temperature

Figure 7.28.   Temperature Sensors
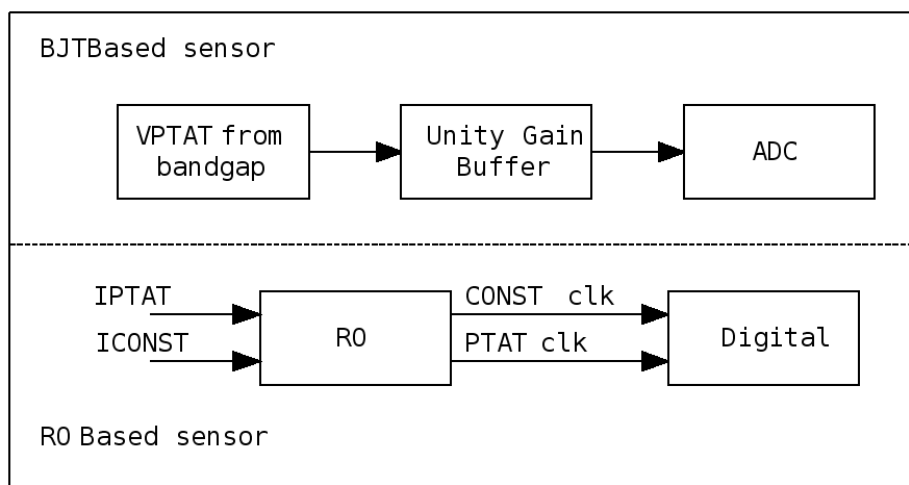
The BJT based sensor works for temperature range from -40ºC to 125ºC and AUX_VDD voltage variation from 1.71V to 3.63V. It outputs the digital word having a resolution of nearly 1ºC. The conversion time is 2 clock cycles of ADC after turning ON the temperature sensor. Typically, the block consumes 110uA of current and leakage current is 800pA.

The RO based sensor will output 2 clocks i.e. one varies linearly with temperature and other is independent of temperature. The PTAT clock cycles are counted in the fixed duration set by the other constant clock and this count value is proportional to the temperature. Current consumption of RO based sensor is 5uA and leakage of nearly 1.15nA.

Table 7.43. BJT Based Temperature Sensor Electrical Specifications

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
Accuracy				5		ºC

7.6 RF Characteristics

All specifications are subject to change. Contact Silicon Labs for final numbers.

Note:

In the sub-sections below,

- All numbers are measured at typical operating conditions unless otherwise stated.
- **PLEASE NOTE THAT THE FOLLOWING NUMBERS ARE PRELIMINARY AND ARE NOT THE FINAL VALUES. EXTENSIVE CHARACTERIZATION FOR THE MODULES ARE UNDERWAY. THERE WILL BE SLIGHT VARIATIONS IN THE FINAL VALUES.**

7.6.1 WLAN 2.4 GHz Transmitter Characteristics

7.6.1.1 Transmitter Characteristics with 3.3V Supply

- TA = 25°C, VBATT = 3.3V. Remaining supplies are at typical operating conditions.
- The transmit power numbers are based on average performance across all channels.

Table 7.44. Transmitter Characteristics with 3.3 V Supply

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power for 20MHz Bandwidth, with EVM limits	DSSS - 1 Mbps	EVM< -9 dB	-	16.5	-	dBm
	CCK - 11 Mbps	EVM< -9 dB	-	16.5	-	dBm
	OFDM - 6 Mbps	EVM< -5 dB	-	17	-	dBm
	OFDM - 54 Mbps	EVM< -25 dB	-	13.5	-	dBm
	HT MCS0 Mixed Mode	EVM< -5 dB	-	16.5	-	dBm
	HT MCS7 Mixed Mode	EVM< -27 dB	-	12.5	-	dBm
	HE MCS0 SU	EVM< -5 dB	-	16	-	dBm
	HE MCS7 SU	EVM< -27 dB	-	12	-	dBm
Transmitter Emissions (6 Mbps @ Maximum Power)	776-794 MHz	CDMA2000	-	-147	-	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	-	-157	-	dBm/Hz
	1450–1495 MHz	DAB	-	-156	-	dBm/Hz
	1570–1580 MHz	GPS	-	-153	-	dBm/Hz
	1592–1610 MHz	GLONASS	-	-133	-	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	-	-152	-	dBm/Hz
	1805–1880 MHz	GSM 1800	-	-149	-	dBm/Hz
	1850–1910 MHz	GSM 1900	-	-148	-	dBm/Hz
	1910–1930 MHz	TDSCDMA, LTE	-	-146	-	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne,WCDMA	-	-142	-	dBm/Hz
	2010–2075 MHz	TDSCDMA	-	-136	-	dBm/Hz
	2110–2170 MHz	WCDMA	-	-128	-	dBm/Hz
	2305–2370 MHz	LTE Band 40	-	-112	-	dBm/Hz
	2370–2400 MHz	LTE Band 40	-	-93	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-105	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-112	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-116	-	dBm/Hz
	5000–5900 MHz	WLAN 5G	-	-156	-	dBm/Hz
Harmonic Emissions (1 Mbps @ Maximum Power)	2nd Harmonic	-	-	-56	-	dBm/MHz
	3rd Harmonic	-	-	-59	-	dBm/MHz

Parameter	Condition	Notes	Min	Typ	Max	Units

Note:

1. There can be a variation of up to 2dB in Tx power across channels at Typical/Room temperature.

2. Each device is tested during manufacturing and set for best power while meeting the IEEE EVM and spectral mask requirements.

3. To meet FCC emission limits, Band-Edge channels (1 and 11) Tx Power will be lowest .Other Channels will be relatively lower compared to middle channels. Refer to Regulatory Certification App note for more details. The radiated power in band edge is a strong function of the antenna properties. The embedded front end has a bandpass filter to meet the regulatory emission standards, including FCC.

4. Channels 1 (2412 MHz) through 11 (2462 MHz) are supported for North America (FCC, ISED). Channels 1 (2412 MHz) through 13 (2472 MHz) are supported for Europe and Japan (CE, MIC). Channel 14 (2484 MHz) is additionally supported for Japan.

7.6.2 WLAN 2.4 GHz Receiver Characteristics on High-Performance (HP) Mode

- TA = 25°C, VBATT = 3.3 V. Remaining supplies are at typical operating conditions.
- All WLAN receiver sensitivity numbers and adjacent channel numbers are at < 10% PER limit for 11g/n/ax rates and <8% PER limit for 11b rates
  - Packet sizes are 1024 bytes for 802.11 b/g data rates and 4096 bytes for 802.11n
  - Packet sizes are 4096 bytes for 802.11ax for SU
- Carrier modulation is non-DCM
- For WLAN ACI cases, the desired signal power is 3 dB (11g/n/ax) and 6dB (11b) above standard defined sensitivity levels respectively

Table 7.45. WLAN 2.4 GHz Receiver Characteristics on HP Mode

Parameter	Condition/Notes	Min	Typ	Max	Unit
Sensitivity for 20MHz Bandwidth[1]	1 Mbps DSSS	-	-94.5	-	dBm
	2 Mbps DSSS	-	-89.5	-	dBm
	5.5 Mbps CCK	-	-89.5	-	dBm
	11 Mbps CCK	-	-86	-	dBm
	6 Mbps OFDM	-	-90	-	dBm
	9 Mbps OFDM	-	-89	-	dBm
	12 Mbps OFDM	-	-88.5	-	dBm
	18 Mbps OFDM	-	-86	-	dBm
	24 Mbps OFDM	-	-83.5	-	dBm
	36 Mbps OFDM	-	-79.5	-	dBm
	48 Mbps OFDM	-	-75.5	-	dBm
	54 Mbps OFDM	-	-74	-	dBm
	HT20 MCS0 Mixed Mode	-	-89	-	dBm
	HT20 MCS1 Mixed Mode	-	-86.5	-	dBm
	HT20 MCS2 Mixed Mode	-	-83.5	-	dBm
	HT20 MCS3 Mixed Mode	-	-81	-	dBm
	HT20 MCS4 Mixed Mode	-	-77.5	-	dBm
	HT20 MCS5 Mixed Mode	-	-73	-	dBm
	HT20 MCS6 Mixed Mode	-	-71.5	-	dBm
	HT20 MCS7 Mixed Mode	-	-69	-	dBm
	HE20 MCSO SU	-	-89.5	-	dBm
	HE20 MCS1 SU	-	-88.5	-	dBm
	HE20 MCS2 SU	-	-84.5	-	dBm
	HE20 MCS3 SU	-	-81	-	dBm
	HE20 MCS4 SU	-	-77	-	dBm
	HE20 MCS5 SU	-	-73	-	dBm
	HE MCS6 SU	-	-71	-	dBm
	HE MCS7 SU	-	-69	-	dBm
	HE MCSO ER	-	-91.5	-	dBm
Maximum Input Level for PER below 10%	802.11 b	-	3	-	dBm
	802.11g	-	-2	-	dBm
	802.11n	-	-4	-	dBm
	802.11ax	-	-2.5	-	dBm

Parameter	Condition/Notes	Min	Typ	Max	Unit
Adjacent Channel Interference	1 Mbps DSSS	-	47	-	dB
	11 Mbps DSSS	-	38	-	dB
	6 Mbps OFDM	-	42	-	dB
	54 Mbps OFDM	-	24	-	dB
	HT20 MCS0 Mixed Mode	-	32	-	dB
	HT20 MCS7 Mixed Mode	-	11	-	dB
	HE MCS0 SU	-	21	-	dB
	HE MCS7 SU	-	6	-	dB
Alternate Adjacent Channel Interference	1 Mbps DSSS	-	51	-	dB
	11 Mbps DSSS	-	44	-	dB
	6 Mbps OFDM	-	51	-	dB
	54 Mbps OFDM	-	32	-	dB
	HT20 MCS0 Mixed Mode	-	51	-	dB
	HT20 MCS7 Mixed Mode	-	31	-	dB
	HE MCS0 SU	-	51	-	dB
	HE MCS7 SU	-	31	-	dB

Note:

1. Rx Sensitivity may be degraded up to 1 dB for channels (1, 2, 3, 4, 5, 9, and 10) at Typical/Room temperature.
2. Rx sensitivity may be degraded up to 2 dB for channels (6, 7, 8, 11, 12, 13, and 14) at Typical/Room temperature.

7.6.3 WLAN 2.4 GHz Receiver Characteristics on Low-Power (LP) Mode

- TA = 25°C, VBATT = 3.3 V. Remaining supplies are at typical operating conditions.
- All WLAN receiver sensitivity numbers and adjacent channel numbers are at < 10% PER limit for 11g/n/ax rates and <8% PER limit for 11b rates
  - Packet sizes are 1024 bytes for 802.11 b/g data rates and 4096 bytes for 802.11n
  - Packet sizes are 4096 bytes for 802.11ax for SU
- Carrier modulation is non-DCM
- For WLAN ACI cases, the desired signal power is 3 dB (11g/n/ax) and 6dB (11b) above standard defined sensitivity levels respectively

Table 7.46. WLAN 2.4 GHz Receiver Characteristics on LP Mode

Parameter	Condition/Notes	Min	Typ	Max	Unit
Sensitivity for 20MHz Bandwidth[1]	1 Mbps DSSS	-	-94.5	-	dBm
	2 Mbps DSSS	-	-89.5	-	dBm
	5.5 Mbps CCK	-	-88.5	-	dBm
	11 Mbps CCK	-	-86	-	dBm
	6 Mbps OFDM	-	-89.5	-	dBm
	9 Mbps OFDM	-	-88.5	-	dBm
	12 Mbps OFDM	-	-88	-	dBm
	18 Mbps OFDM	-	-85.5	-	dBm
	24 Mbps OFDM	-	-83	-	dBm
	36 Mbps OFDM	-	-79	-	dBm
	HT20 MCS0 Mixed Mode	-	-88.6	-	dBm
	HT20 MCS1 Mixed Mode	-	-86	-	dBm
	HT20 MCS2 Mixed Mode	-	-83.5	-	dBm
	HT20 MCS3 Mixed Mode	-	-80.5	-	dBm
	HT20 MCS4 Mixed Mode	-	-77	-	dBm
Maximum Input Level for PER below 10%	802.11 b	-	-6	-	dBm
	802.11g	-	0.5	-	dBm
	802.11n	-	-0.5	-	dBm
Adjacent Channel Interference	1 Mbps DSSS	-	44	-	dB
	11 Mbps DSSS	-	37	-	dB
	6 Mbps OFDM	-	42	-	dB
	36 Mbps OFDM	-	27	-	dB
	HT20 MCS0 Mixed Mode	-	33	-	dB
	HT20 MCS4 Mixed Mode	-	19	-	dB

Parameter	Condition/Notes	Min	Typ	Max	Unit
Alternate Adjacent Channel Interference	1 Mbps DSSS	-	47	-	dB
	11 Mbps DSSS	-	42	-	dB
	6 Mbps OFDM	-	49	-	dB
	36 Mbps OFDM	-	35	-	dB
	HT20 MCS0 Mixed Mode	-	49	-	dB
	HT20 MCS4 Mixed Mode	-	33	-	dB

Note:

1. Rx Sensitivity may be degraded up to 1 dB for channels (1, 2, 3, 4, 5, 9, and 10) at Typical/Room temperature.
2. Rx sensitivity may be degraded up to 2 dB for channels (6, 7, 8, 11, 12, 13, and 14) at Typical/Room temperature.

7.6.4 Bluetooth Transmitter Characteristics on High-Performance (HP) Mode

7.6.4.1 Transmitter Characteristics with 3.3 V Supply

TA = 25°C, VBATT = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are measured at antenna port.[1]

Table 7.47. Bluetooth Transmitter Characteristics on HP Mode 3.3 V

Parameter	Condition	Notes	Min	Typ	Max	Unit
Transmit Power	LE 1Mbps		-	16.5	-	dBm
	LE 2Mbps		-	16.5	-	dBm
	LR 500 Kbps		-	17	-	dBm
	LR 125 Kbps		-	17	-	dBm
Adjacent Channel Power |M-N| = 2	LE		-	-35	-	dBm
Adjacent Channel Power |M-N| > 2	LE		-	-41	-	dBm
BLE Modulation Characteristics @ 1Mbps	Δf1 Avg		-	248	-	kHz
	Δf2 Max		-	250	-	kHz
	Δf2 Avg/Δf1 Avg		-	1.43	-	-
Transmitter Emissions (BLE 1 Mbps @ Maximum Power)	776-794 MHz	CDMA2000	-	-157	-	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	-	-157	-	dBm/Hz
	1450–1495 MHz	DAB	-	-156	-	dBm/Hz
	1570–1580 MHz	GPS	-	-156	-	dBm/Hz
	1592–1610 MHz	GLONASS	-	-156[4]	-	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	-	-155	-	dBm/Hz
	1805–1880 MHz	GSM 1800	-	-153	-	dBm/Hz
	1850–1910 MHz	GSM 1900	-	-152	-	dBm/Hz
	1910–1930 MHz	TDSCDMA, LTE	-	-152	-	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne,WCDMA	-	-150	-	dBm/Hz
	2010–2075 MHz	TDSCDMA	-	-146	-	dBm/Hz
	2110–2170 MHz	WCDMA	-	-139	-	dBm/Hz
	2305–2370 MHz	LTE Band 40	-	-123	-	dBm/Hz
	2370–2400 MHz	LTE Band 40	-	-109	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-117	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-121	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-126	-	dBm/Hz
	5000–5900 MHz	WLAN 5G	-	-156	-	dBm/Hz

Parameter	Condition	Notes	Min	Typ	Max	Unit

Note:

1. There can be up to 2 dB Variation in Tx Power across channels.
2. ETSI Max Power is limited to 10 dBm to meet PSD requirements, because device falls under DTS.
3. In FCC, LR 125kbps Max Power is limited to 13 dBm to meet PSD requirement, because device falls under DTS.
4. Noise-floor is -159dBm/Hz with spurious tone power of -67dBm at 1601.33 MHz when transmitted signal is at 2402 MHz.

7.6.5 Bluetooth Transmitter Characteristics on Low-Power (LP) Mode

TA = 25°C. Parameters are measured at antenna port and applicable to VBATT = 3.3V

Table 7.48. Bluetooth Transmitter Characteristics on LP 0 dBm Mode

Parameter	Condition/Notes	Min	Typ	Max	Unit
Transmit Power	LE 1Mbps	-	-2	-	dBm
	LE 2Mbps	-	-2	-	dBm
	LR 500 Kbps	-	-2	-	dBm
	LR 125 kbps	-	-2	-	dBm
Adjacent Channel Power |M-N| = 2	LE	-	-50	-	dBm
Adjacent Channel Power |M-N| > 2	LE	-	-63	-	dBm
BLE Modulation Characteristics @ 1Mbps	Δf1 Avg	-	248	-	kHz
	Δf2 Max	-	250	-	kHz
	Δf2 Avg/Δf1 Avg	-	1.3	-	-

7.6.6 Bluetooth Receiver Characteristics on High-Performance (HP) Mode

TA = 25°C. Parameters are measured at antenna port and applicable to VBATT = 3.3V

Table 7.49. Bluetooth Receiver Characteristics on HP RF Mode

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity,Dirty TX off[1]	LE (1 Mbps), 37 bytes, PER=30.8%	-	-93.5	-	dBm
	LE (1 Mbps), 255 bytes, PER=30.2%	-	-93	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-90.5	-	dBm
	LE (2 Mbps), 255 bytes, PER=30.2%	-	-90	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-100	-	dBm
	LR (500 Kbps), 255 bytes, PER=30.2%	-	-100	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-104	-	dBm
	LR (125 Kbps), 255 bytes, PER=30.2%	-	-105	-	dBm
Maximum Input Level	LE 1Mbps, 2Mbps, 255 bytes PER=30.2%	-	2	-	dBm
	LR 500kps, 125kbps, 255 bytes PER=30.2%	-	3	-	dBm
C/I Performance	LE 1Mbps, co-channel PER=30.8%	-	-10	-	dB
	LE 1Mbps, adjacent +1 MHz PER=30.8%	-	-5	-	dB
	LE 1Mbps, adjacent -1 MHz PER=30.8%	-	3	-	dB
	LE 1Mbps, adjacent +2 MHz PER=30.8%	-	22	-	dB
	LE 1Mbps, adjacent -2 MHz PER=30.8%	-	24	-	dB
	LE 1Mbps, adjacent +3 MHz PER=30.8%	-	31	-	dB
	LE 1Mbps, adjacent -3 MHz PER=30.8%	-	40	-	dB
	LE 1Mbps, adjacent >= |±4| MHz PER=30.8%	-	39	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	28	-	dB
	LE 1Mbps, +1MHz adjacent to Image channel PER=30.8%	-	35	-	dB
	LE 1Mbps, -1MHz adjacent to Image channel PER=30.8%	-	31	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	-7	-	dB
	LE 2Mbps, adjacent +2 MHz PER=30.8%	-	4	-	dB
	LE 2Mbps, adjacent -2 MHz PER=30.8%	-	4	-	dB
	LE 2Mbps, adjacent +4 MHz PER=30.8%	-	16	-	dB
	LE 2Mbps, adjacent -4 MHz PER=30.8%	-	21	-	dB
	LE 2Mbps, adjacent >= |±6| MHz PER=30.8%	-	34	-	dB
	LE 2Mbps, Image channel PER=30.8%	-	16	-	dB
	LE 2Mbps, +2MHz adjacent to Image channel PER=30.8%	-	28	-	dB
	LE 2Mbps, -2MHz adjacent to Image channel PER=30.8%	-	4	-	dB

Note:

1. BLE, LR: Sensitivities for channels 19,39 are up to 2 dB lower performance.

7.6.7 Bluetooth Receiver Characteristics on Low-Power (LP) Mode

TA = 25°C. Parameters are measured at antenna port and applicable to VBATT=3.3V

Table 7.50. Bluetooth Receiver Characteristics on LP RF Mode

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity,Dirty TX off[1]	LE (1 Mbps), 37 bytes, PER=30.8%	-	-93	-	dBm
	LE (1 Mbps), 255 bytes, PER=30.2%	-	-93	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-90.5	-	dBm
	LE (2 Mbps), 255 bytes, PER=30.2%	-	-90	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-100	-	dBm
	LR (500 Kbps), 255 bytes, PER=30.2%	-	-100	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-104.5	-	dBm
	LR (125 Kbps), 255 bytes, PER=30.2%	-	-105	-	dBm
Maximum Input Level	LE 1Mbps, 2Mbps, 255 bytes, PER=30.2%	-	-4.5	-	dBm
	LR 500kps, 125kbps, 255 bytes, PER=30.2%	-	2.5	-	dBm
C/I Performance	LE 1Mbps, co-channel PER=30.8%	-	-10	-	dB
	LE 1Mbps, adjacent +1 MHz PER=30.8%	-	-5	-	dB
	LE 1Mbps, adjacent -1 MHz PER=30.8%	-	4	-	dB
	LE 1Mbps, adjacent +2 MHz PER=30.8%	-	19	-	dB
	LE 1Mbps, adjacent -2 MHz PER=30.8%	-	22	-	dB
	LE 1Mbps, adjacent +3 MHz PER=30.8%	-	24	-	dB
	LE 1Mbps, adjacent -3 MHz PER=30.8%	-	35	-	dB
	LE 1Mbps, adjacent >= |±4| MHz PER=30.8%	-	37	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	22	-	dB
	LE 1Mbps, +1MHz adjacent to Image channel PER=30.8%	-	34	-	dB
	LE 1Mbps, -1MHz adjacent to Image channel PER=30.8%	-	24	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	-7	-	dB
	LE 2Mbps, adjacent +2 MHz PER=30.8%	-	4	-	dB
	LE 2Mbps, adjacent -2 MHz PER=30.8%	-	2	-	dB
	LE 2Mbps, adjacent +4 MHz PER=30.8%	-	15	-	dB
	LE 2Mbps, adjacent -4 MHz PER=30.8%	-	21	-	dB
	LE 2Mbps, adjacent >= |±6| MHz PER=30.8%	-	35	-	dB
	LE 2Mbps, Image channel PER=30.8%	-	15	-	dB
	LE 2Mbps, +2MHz adjacent to Image channel PER=30.8%	-	28	-	dB
	LE 2Mbps, -2MHz adjacent to Image channel PER=30.8%	-	4	-	dB

Note:

1. BLE, LR: Sensitivities for channels 19, 39 are up to 2 dB lower performance.

7.7 Typical Current Consumption

> PLEASE NOTE THAT THE FOLLOWING NUMBERS ARE PRELIMINARY AND ARE NOT THE FINAL VALUES. EXTENSIVE CHARACTERIZATION FOR THE MODULES ARE UNDERWAY. THERE WILL BE SLIGHT VARIATIONS IN THE FINAL VALUES.

7.7.1 3.3. V
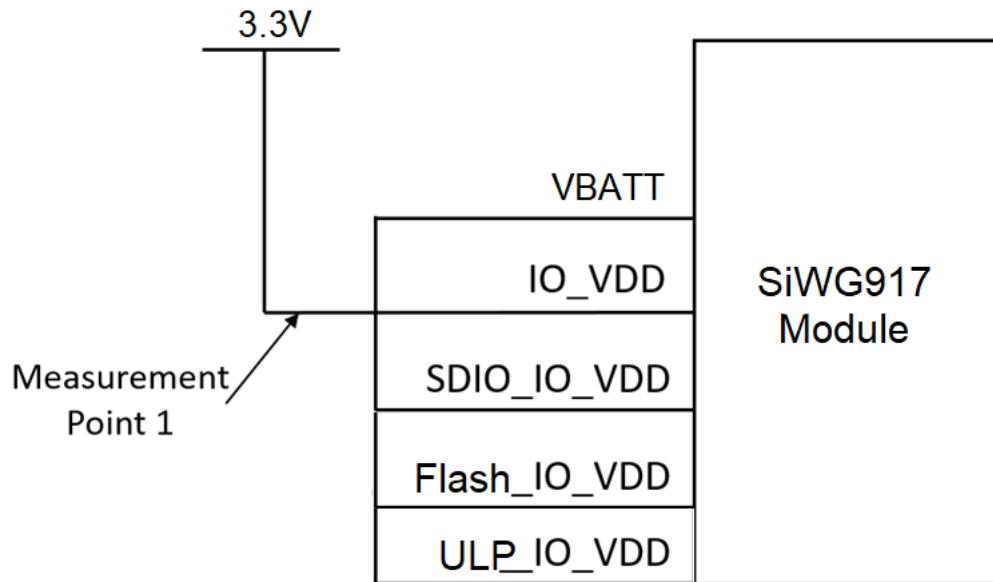
7.7.1.1 WLAN 2.4 GHz

Note: THE FOLLOWING NUMBERS ARE NOT THE FINAL VALUES. THEY ARE STILL UNDER TESTING AND THERE MIGHT BE SLIGHT VARIATIONS IN THE FINAL VALUES.

Parameter	Description	Min	Typ	Max	Units
1 Mbps Listen	LP Mode	-	13	-	mA
1 Mbps RX Active	LP Mode	-	18	-	mA
HT20 MCS0 RX	HP Mode	-	51	-	mA
HT20 MCS7 RX	HP Mode	-	51	-	mA
HE20 MCS0 RX	HP Mode	-	51	-	mA
HE20 MCS7 RX	HP Mode	-	51	-	mA
1 Mbps TX	HP Mode	-	260	-	mA
HT20 MCS0 TX	HP Mode	-	230	-	mA
HT20 MCS7 TX	HP Mode	-	180	-	mA
HE20 MCS0 TX	HP Mode	-	212	-	mA
HE20 MCS7 TX	HP Mode	-	173	-	mA
Deep Sleep with RAM Retention	192K RAM Retained	-	9	-	µA
Standby Associated, DTIM = 10 Without TCP Keep alive	WLAN Keep Alive Every 30 secs with 352K RAM Retained	-	55	-	µA

7.7.1.2 Bluetooth LE

Note: THE FOLLOWING NUMBERS ARE NOT THE FINAL VALUES. THEY ARE STILL UNDER TESTING AND THERE MIGHT BE SLIGHT VARIATIONS IN THE FINAL VALUES.

Parameter	Description	Min	Typ	Max	Units
TX Active Current	LP Mode, Tx Power = 0 dBm	-	10	-	mA
	LP Mode, Tx Power = max transmit power		17		mA
RX Active Current	LP Mode	-	10	-	mA
Advertising, Unconnecta-ble	Advertising on all 3 channels with the Advertising payload 37 bytes @ AI = 1.28s , Tx power @0 dBm and LP Mode	-	37	-	µA
Connected	Connection Interval @200msec, No data and Tx power @ 0 dBm and LP Mode	-	115	-	µA

7.7.1.3 MCU Power States Active and Sleep Currents

Power State	Mode	Min	Typ	Max	Units
PS4	Sleep with 64KB RAM Reten-tion	-	5	-	µA
	Active	-	8.6	-	mA
PS3	Sleep with 64KB RAM Reten-tion	-	5	-	µA
	Active	-	7	-	mA
PS2	Sleep with 64KB RAM Reten-tion	-	5.7	-	uA
	Active	-	660	-	uA
PS1	Sleep with 64KB RAM Reten-tion	-	15	-	uA
	Active	-	240	-	uA
PS0	Sleep with 64KB RAM Reten-tion	-	4.5	-	uA
	Sleep without RAM Retention	-	1.5	-	uA

8. Reference Schematics, BOM and Layout Guidelines

Note:

1. Customers should include provision for programming or updating the firmware at manufacturing.
2. If using UART, we recommend bringing out the SPI lines to test points, so designers could use the faster interface for programming the firmware as needed.
3. If using SPI as host interface, then firmware programming or update can be done through the host MCU, or if designer prefers to program standalone at manufacturing, then it is recommended to have test points on the SPI signals.
4. 3.3 V/1.8 V/VBATT must be supplied by external source.
5. VBATT, SDIO_IO_VDD, IO_VDD, ULP_IO_VDD must be powered using External/On-board Power.
6. FLASH_IO_VDD is powered by 1V8_LDO_OUT output.
7. Place all the Caps closer to the corresponding Module pins.

8.1 SiW917Y1GN Host Schematics

8.1.1 SDIO/SPI/UART

8.1.1.1 Reference Schematics for parts with RF pin

The diagram below shows the typical Host Schematic with SDIO/SPI/UART Host Interface and Internal Flash.
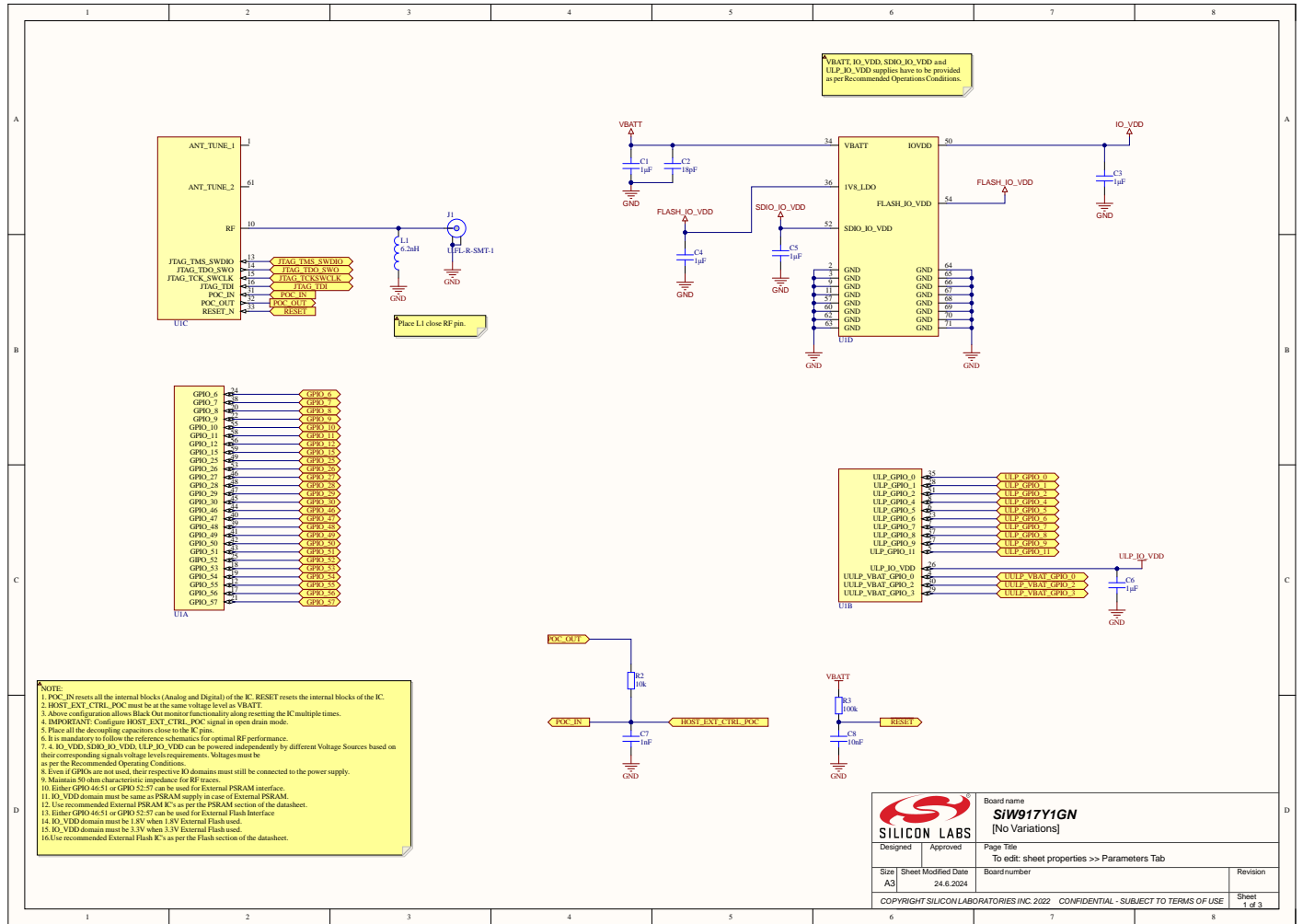
Figure 8.1. Schematics with SDIO/SPI/UART Host Interface for the SiW917Y1GN Module

Note:

1. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Section 7. Electrical Specifications.
2. IO_VDD, SDIO_IO_VDD and ULP_IO_VDD can be driven by a different source irrespective of other sources to support different interfaces.
3. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification, version 2.0.
4. In SPI mode, ensure that the input signals, SPI_CS and SPI_CLK are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset. SPI_INTR is the interrupt signal driven by the Secondary device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required. The following action can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.
   • To use the signal in the Active-high or Active-low mode, ensure that, during the power up of the device, the Interrupt is disabled in the Host processor before deasserting the reset. After deasserting the reset, the Interrupt needs to be enabled only after the SPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.
   • The Host processor needs to be disable the interrupt before the ULP Sleep mode is entered and enable it after SPI interface is reinitialized upon wakeup from ULP Sleep.
5. In UART mode, ensure that the input signals, UART_RX and UART_CTS are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset.
6. L1 must be connected close to the RF port.

8.1.1.2 Bill of Materials

Line No	Quantity	Designator	Value	Description	Tolerance	Rating	Material
1	5	C1, C3, C4, C5, C6	1µF	CAP CER 0402 X5R 1uF 10V 10%	10%	10V	X5R
2	1	C2	18pF	CAP CER 0201 C0G 18pF 25V 2%	2%	25V	C0G
3	1	C7	1nF	CAP CER 0402 X7R 1nF 16V 10%	10%	16V	X7R
4	1	C8	10nF	CAP CER 0402 X7R 10nF 16V 10%	10%	16V	X7R
5	1	J1	U.FL-R-SMT-1	CONN RF 50OHM UFL_2.6x2.6 SMD			
6	1	L1	6.2nH	IND Fixed 0201 6.2nH 300mA 600mOhm 3%	3%	300mA	
7	1	R1	33	RES 0402 33R 1/16W 1% 100ppm	1%	62.5mW	
8	1	R2	10k	RES 0402 10K 1/16W 5% 200ppm	5%	63mW	
9	1	R3	100k	RES 0402 100K 1/16W 1% 100ppm	1%	63mW	
10	1	U1	SiW917Y1GN	PCB Module SiW917Y1GN			

Table 8.1. SiWG917: External Flash Options (these are optional and need not be used for every use-case)

Value	Manufacturer	Manufacturer PN	Description
MX25R6435F	Macronix	MX25R6435FM2IL0	IC Flash 64 Mbit SPI/QUAD 8SOP

8.2 SiW917Y1GA Host Schematics

8.2.1 SDIO/SPI/UART

8.2.1.1 Reference Schematics for Parts with Integral Antenna

The diagram below shows the typical Host Schematic with SDIO/SPI/UART Host Interface and Internal Flash.
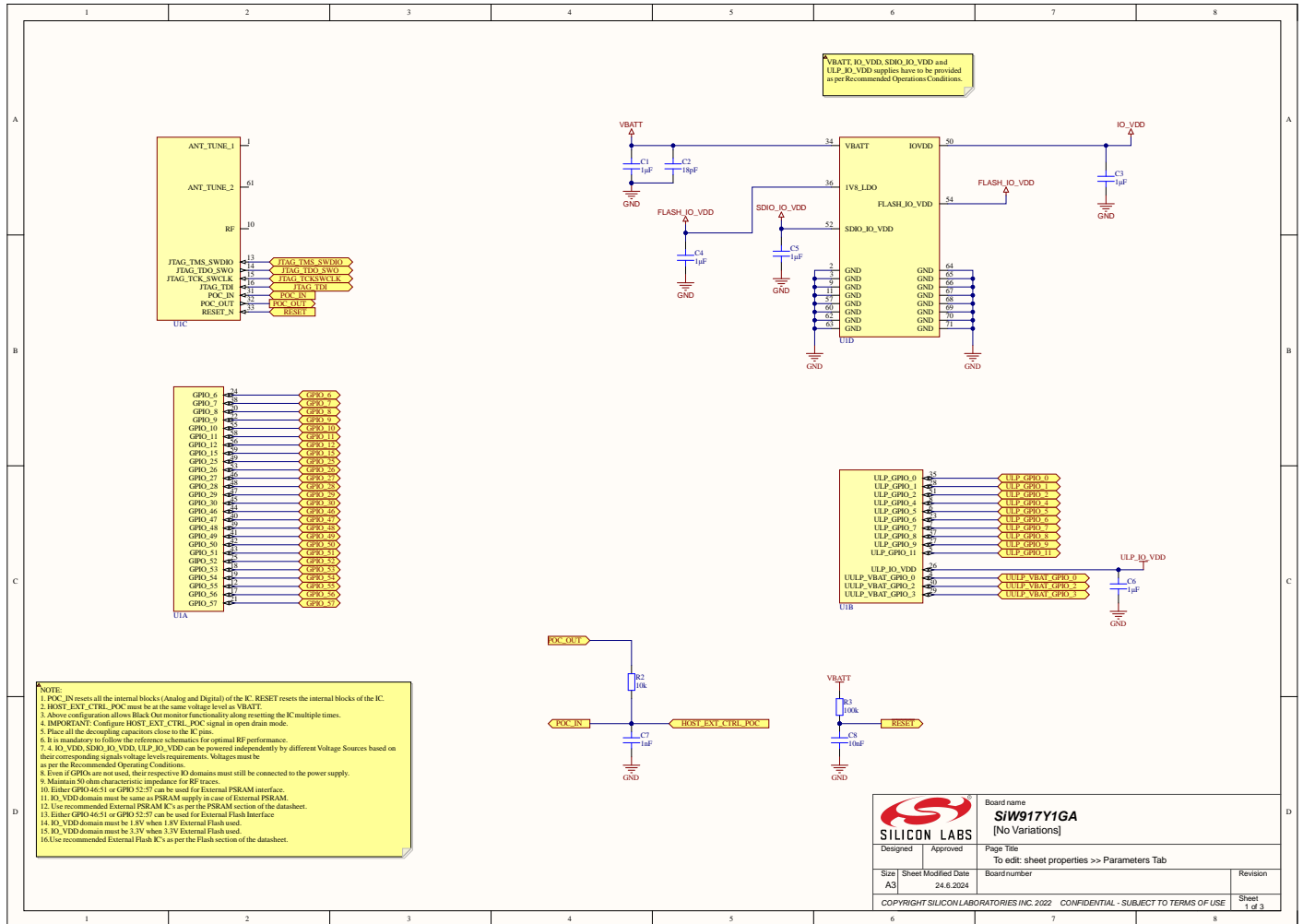
Figure 8.2. Schematics with SDIO/SPI/UART Host Interface for the SiW917Y1GA Module

Note:

1. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Section 7. Electrical Specifications.

2. IO_VDD, SDIO_IO_VDD and ULP_IO_VDD can be driven by a different source irrespective of other sources to support different interfaces.

3. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification, version 2.0.

4. In SPI mode, ensure that the input signals, SPI_CS and SPI_CLK are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset. SPI_INTR is the interrupt signal driven by the Secondary device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required. The following action can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.

   • To use the signal in the Active-high or Active-low mode, ensure that, during the power up of the device, the Interrupt is disabled in the Host processor before deasserting the reset. After deasserting the reset, the Interrupt needs to be enabled only after the SPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.

   • The Host processor needs to be disable the interrupt before the ULP Sleep mode is entered and enable it after SPI interface is reinitialized upon wakeup from ULP Sleep.

5. In UART mode, ensure that the input signals, UART_RX and UART_CTS are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset.

8.2.1.2 Bill of Materials

Line No	Quantity	Designator	Value	Description	Tolerance	Rating	Material
1	5	C1, C3, C4, C5, C6	1µF	CAP CER 0402 X5R 1uF 10V 10%	10%	10V	X5R
2	1	C2	18pF	CAP CER 0201 C0G 18pF 25V 2%	2%	25V	C0G
3	1	C7	1nF	CAP CER 0402 X7R 1nF 16V 10%	10%	16V	X7R
4	1	C8	10nF	CAP CER 0402 X7R 10nF 16V 10%	10%	16V	X7R
5	1	R1	33	RES 0402 33R 1/16W 1% 100ppm	1%	62.5mW	
6	1	R2	10k	RES 0402 10K 1/16W 5% 200ppm	5%	63mW	
7	1	R3	100k	RES 0402 100K 1/16W 1% 100ppm	1%	63mW	
8	1	U1	SiW917Y1GA	PCB Module SiW917Y1GA			

Table 8.2. SiWN917: External Flash Options (these are optional and need not be used for every use-case)

Value	Manufacturer	Manufacturer PN	Description
MX25R6435F	Macronix	MX25R6435FM2IL0	IC Flash 64 Mbit SPI/QUAD 8SOP

8.3 Layout Guidelines

1. The RF (Module Pin No. 10) signal may be directly connected to an on-board chip antenna or terminated in an RF connector of any form factor for enabling the use of external antennas. RF can be left floating if not used.

2. Antenna clearance area is not necessary if you are using an external antenna attached to the RF.

3. The RF trace on RF should have a characteristic impedance of 50 Ohms. Any standard 50 Ohms RF trace (Microstrip or Coplanar wave guide) may be used. The width of the 50 Ohms line depends on the PCB stack, e.g., the dielectric of the PCB, thickness of the copper, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.

4. To evaluate transmit and receive performance like Tx Power and EVM, Rx sensitivity and the like, an RF connector would be required. A suggestion is to place a 'microwave coaxial connector with switch' between RF1 and the antenna.

5. Each GND pin must have a separate GND via. Place the ground vias as close to the ground pads as possible.

6. All decoupling capacitors placement must be as much close as possible to the corresponding power pins, and the trace lengths as short as possible.

7. Ensure all power supply traces widths are sufficient enough to carry corresponding currents.

8. Add GND copper pour underneath IC/Module in all layers, for better thermal dissipation.

9. Add solid GND copper pour underneath Module for better emission performance.

8.3.1 Installation Guide for SiW917Y1GN Module

Figure 8.3 on page 136 below shows the recommended layout for SiW917Y1GN when using an u.fl connector for an external antenna. The short RF trace from the RF pad of the module to the pad of the u.fl connector must be 50 ohm and exactly the same width as the RF pad of the module, i.e., 700 µm. Figure 8.3 SiW917Y1GN Top Layer Application Layer with u.fl Connector on page 136 shows two examples on practical implementations of such a trace. The widths S is fixed to 700 um. The height h depends on the PCB stack-up, and the gap width W is adjusted until the impedance of the trace is exactly 50 ohm. Online calculators for coplanar waveguide with ground can be used to calculate the width W for any specific PCB stack-up. The integrator must consider using a unique connector, such as a "reverse polarity SMA" or "reverse thread SMA", if detachable antenna is offered with the host chassis.

Ground vias underneath the module must be used extensively especially around the rectangular GND pins to enable heat transfer from the bottom of the module to the GND plane of the host board. Routing signal lines elsewhere underneath the module is acceptable.
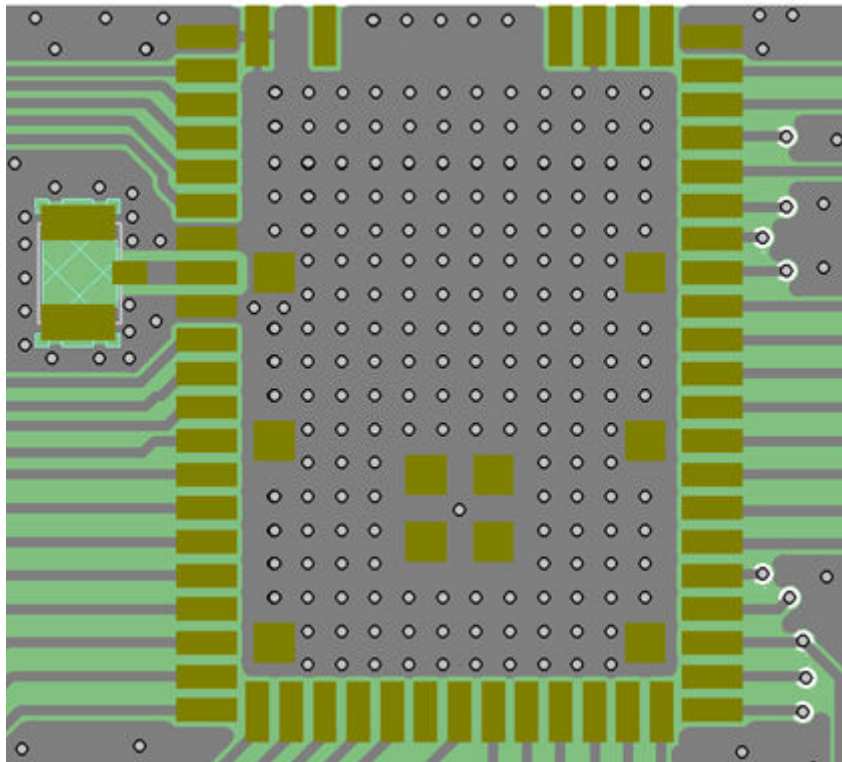
Figure 8.3. SiW917Y1GN Top Layer Application Layer with u.fl Connector

The typical permittivity of PCB laminate is 4.6. If assuming permittivity of 4.6, in the example shown in Figure 8.4 on page 137 the dimensions would be:

S = 700 um

h = 420 um

W = 332 um
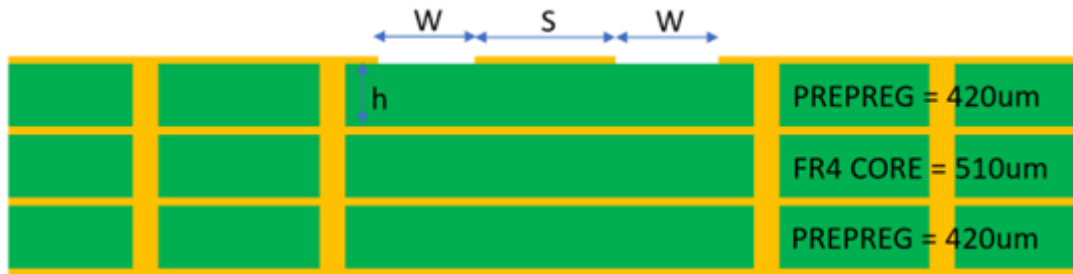
Figure 8.4. Example Implementation of a Co-planar Wave Guide with Ground and Thick Prepeg

Similarly, if assuming permittivity of 4.6, in the example shown in Figure 8.4 on page 137 the dimensions would be:

S = 700 um

h = 730 um

W = 132 um
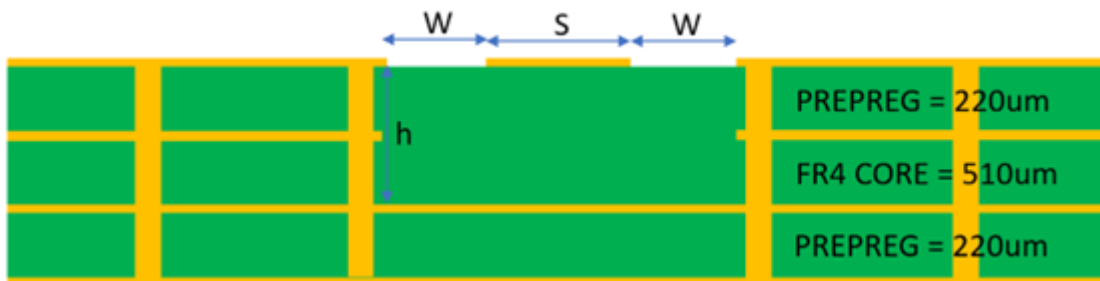
Figure 8.5. Example Implementation of a Co-planar Wave Guide with Ground and Thin Prepeg

8.3.2 Installation Guide for SiW917Y1GA Module

	X-cordinate (mm)	Y-cordinate (mm)
A (Corner of the metal clearance)	-6.5	3.8
B (Corner of the metal clearance)	3.6	3.8
1 (Center point of PAD1)	-4	10.05
3 (Center point of PAD3)	-7.5	10
23 (Center point of PAD23)	-7.5	-10
37 (Center point of PAD37)	7.5	-10
57 (Center point of PAD 57)	7.5	10

Extensive GND stitching underneath the module will help to improve heat transfer from the bottom of the module to the host PCB

Extensive GND stitching of overlapping GND planes will help to avoid unexpected EMC/EMI issues

Figure 8.6. Application Layout of SiW917Y1GA

For optimal performance of the SiW917Y1GA:

- Place the module aligned to the edge of the application PCB, as illustrated in Figure 8.6 on page 138.
- Leave the antenna clearance area void of any traces, components, or copper on all layers of the application PCB.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Avoid plastic or any other dielectric material in direct contact with the antenna.

Figure 8.7 Figure on page 139 shows example layout scenarios which will lead to degraded performance and possible EMC issues with the module.

Ground vias underneath the module must be used extensively especially around the rectangular GND pins to enable heat transfer from the bottom of the module to the GND plane of the host board. Routing signal lines elsewhere underneath the module is acceptable.

Antennas are by nature affected by the surrounding PCB design and in particular the size and shape of the ground surrounding the antenna. The wide band antenna of SiW917Y1GA is designed to operate in various size/shape application boards and the antenna is not sensitive to dielectric material near the antenna. However, in certain extreme circumstances, such as extremely small board or narrow board, the antenna can be detuned enough to have an impact to the range, EVM characteristics and in-band emissions. In such cases it is possible to fine tune the antenna by using one or two external capacitors or inductors connected between the ANT_TUNE1 and GND and/or ANT_TUNE2 and GND. An example is shown in the Figure 8.8 Figure on page 140. Finding the correct value for these components requires empirical testing and measuring the antenna return loss. (See the note below on modular certification.)

The best antenna performance is achieved when the board width is 50mm and the antenna is placed at the center of the board edge. Having wider or narrower PCB will have up to 25% impact to the range. If the board is narrower than 35mm or wider than 100 mm, it is possible that external fine tuning becomes necessary to maintain the EVM performance.

Note: When it comes to modular certifications, following the manufacturer's design guidelines is critical for ensuring that compliance is maintained and modular approvals remain valid, in particular with regards to carrier (host) PCB size, stack-up, and/or module placement. A modular certification is still valid, and, for example, there is no need for a Permissive Change, if no antenna tuning is applied to compensate for reduced performance in terms of range, which may result from sub-optimal carrier PCB size, PCB stack-up, or module placement. Conversely, a custom antenna tuning might invalidate a modular certification, unless it is done to compensate for degradation caused by a deviation from the manufacturer's best-case reference design in terms of size, stack-up, and/or module placement. In such case, a Permissive Change to the modular approval might become necessary, depending on the resulting performance of the

end-product relative to the certified module's test reports, as found during spot-checking. Class 1 Permissive Change (C1PC) is considered if the host PCB modifications do not increase emissions. Class 2 Permissive Change (C2PC) is considered if the modifications degrade the emissions but remain below regulatory limits. In the end, the emission levels established in the module certification are limits for the end device too and determine whether or not a Permissive Change should be considered. Since this is evaluated on a case-by-case basis, customers must consult with the company providing certification services for their product to identify the best approach.
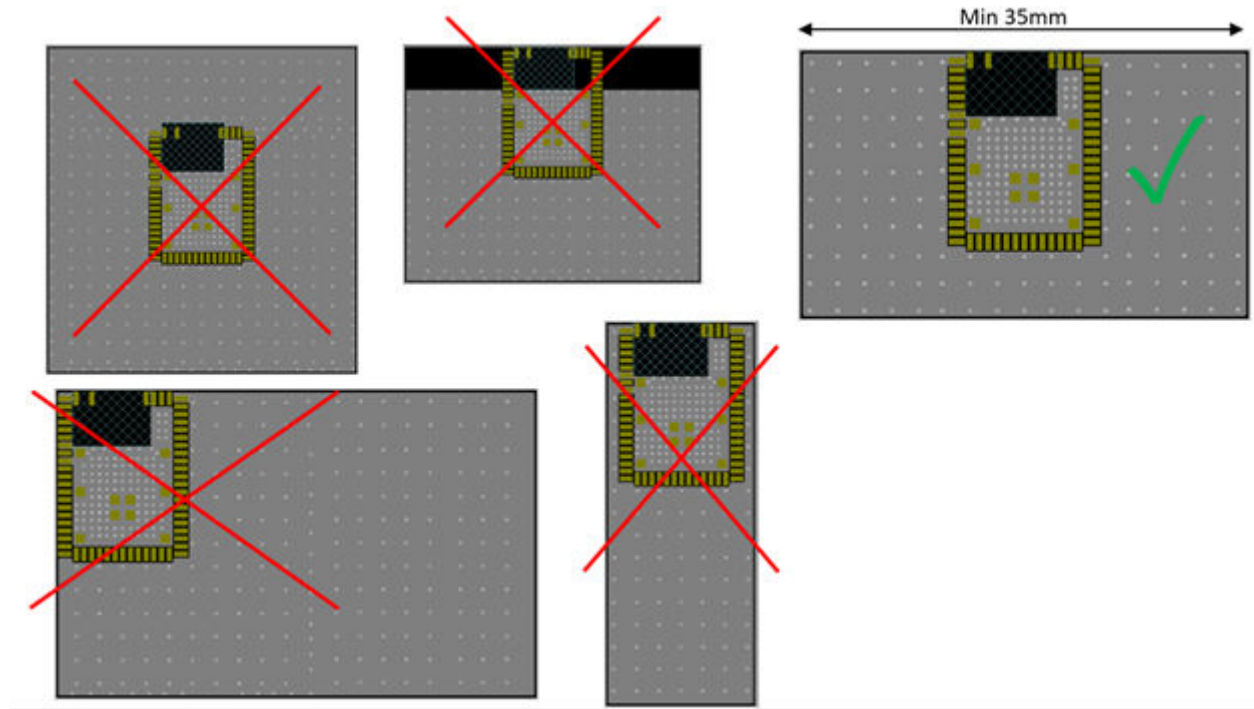
Figure 8.7. Layout Examples

Connect shunt inductor or capacitor to the ANT_TUNE1
and ANT_TUNE2 pads to retune the antenna
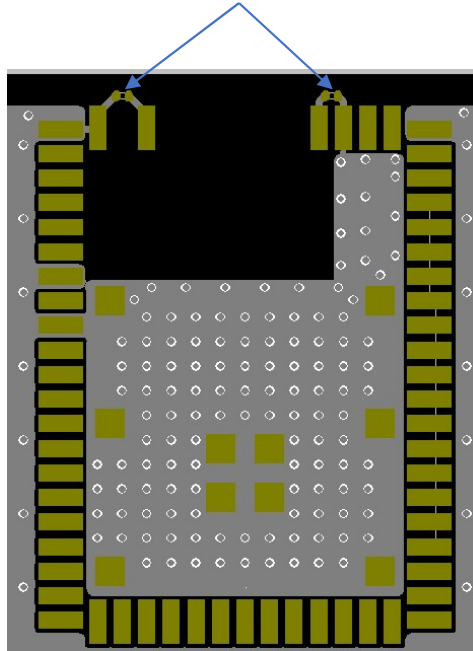
Figure 8.8. External Antenna Fine Tuning Option

8.4 SiW917Y1GA Antenna Radiation and Efficiency

Typical radiation patterns for the built-in antenna under optimal operating conditions are plotted in the figures that follow.

Table 8.3. Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1 dB	Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna. Refer to 8.3.2 Installation Guide for SiW917Y1GA Module for recommendations to archieve optimal antenna performance.
Peak gain	2.26 dBi	
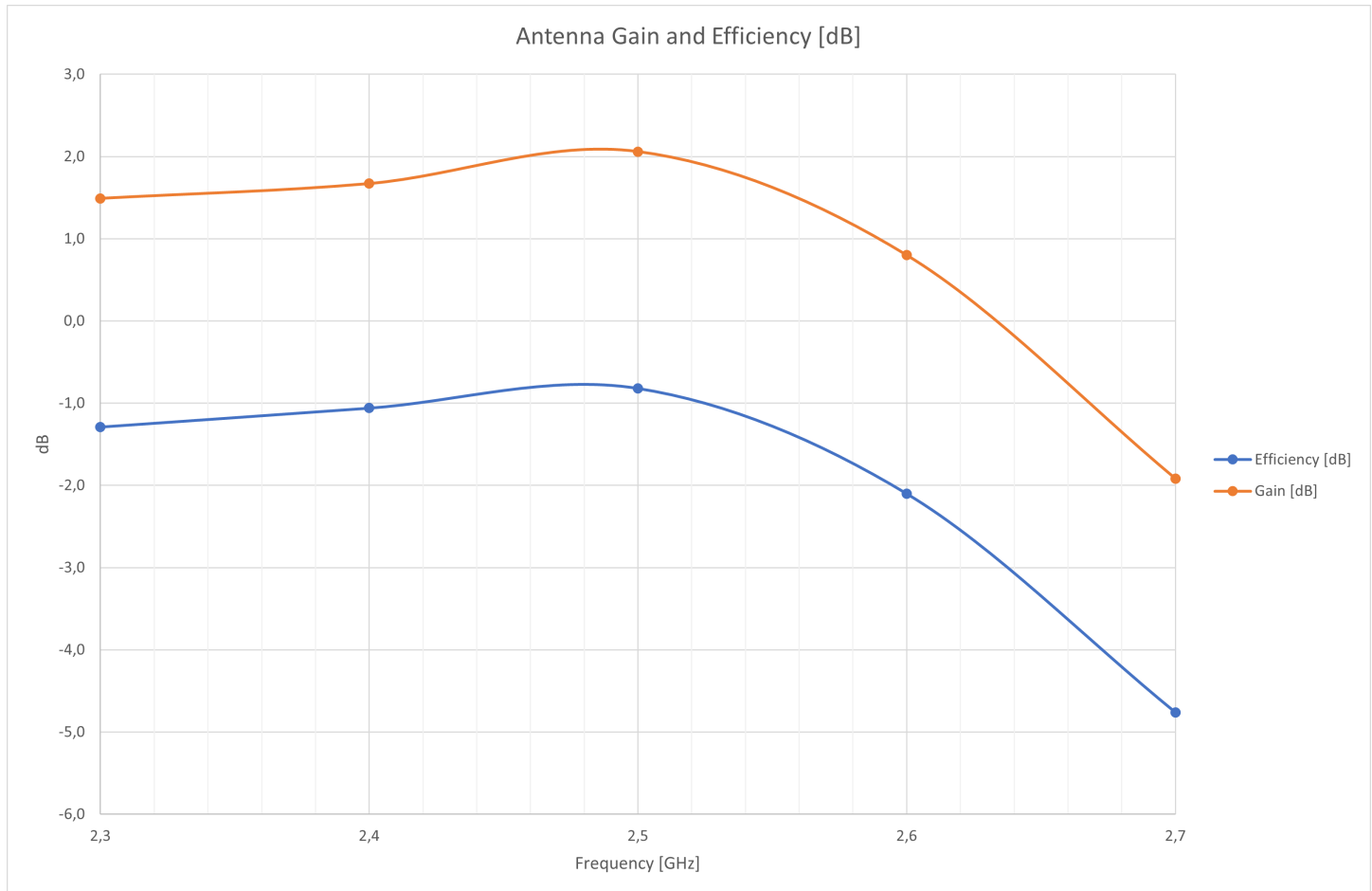
Figure 8.9. Efficiency and Gain of the Built-in Antenna

3D gain pattern @ 2440MHz, View 1
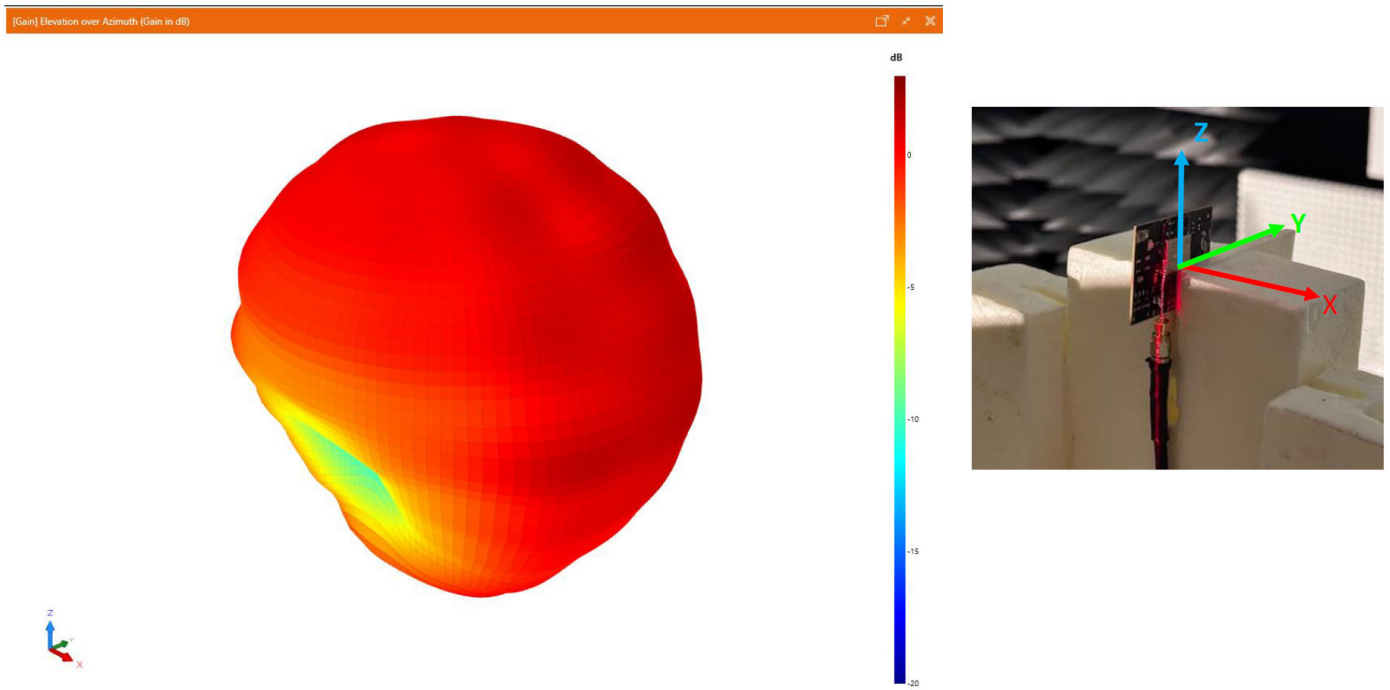
Figure 8.10.   3D Radiation Pattern of the Build-In Antenna

Phi0 Gain cut (dBi)
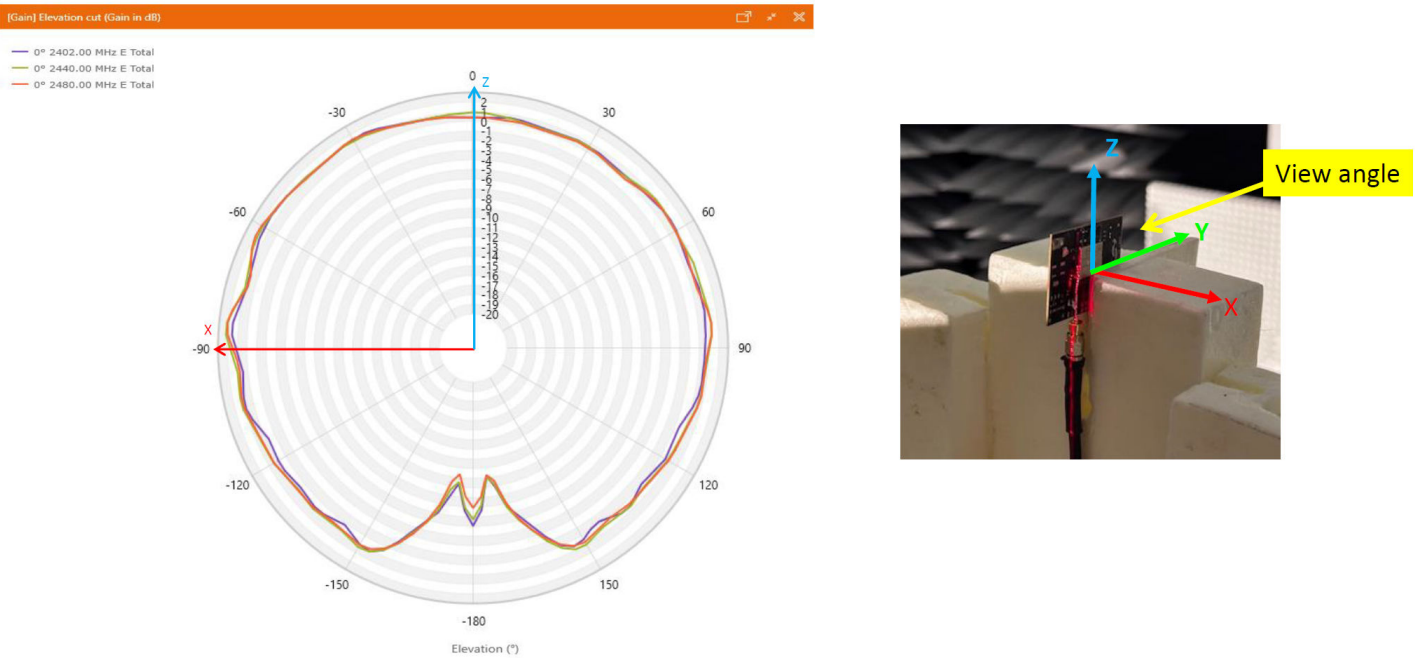
Figure 8.11. Typical 2D Antenna Radiation Patterns - Phi 0º (Side View) Gain (dBi)

Phi90 Gain cut
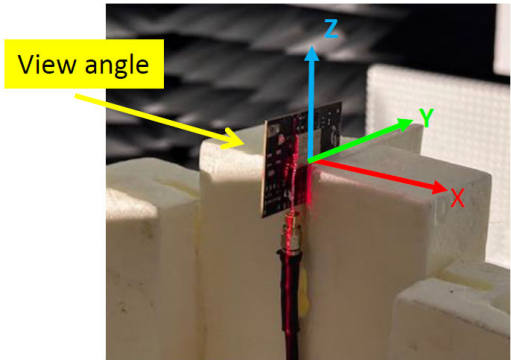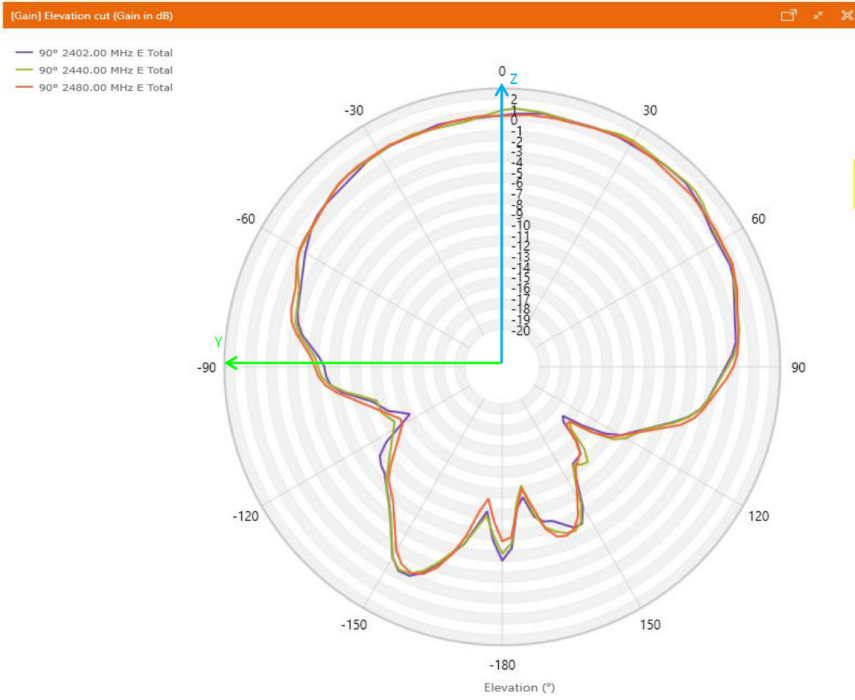
Figure 8.12. Typical 2D Antenna Radiation Patterns - Phi 90º (Top View) Gain (dBi)

Theta90 Gain cut
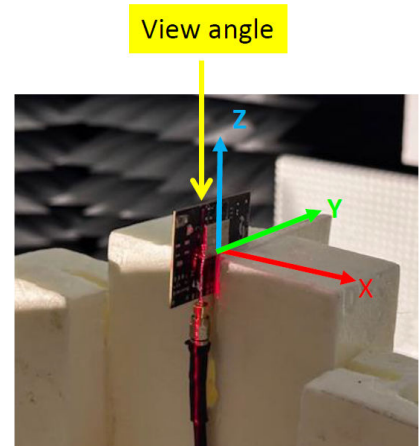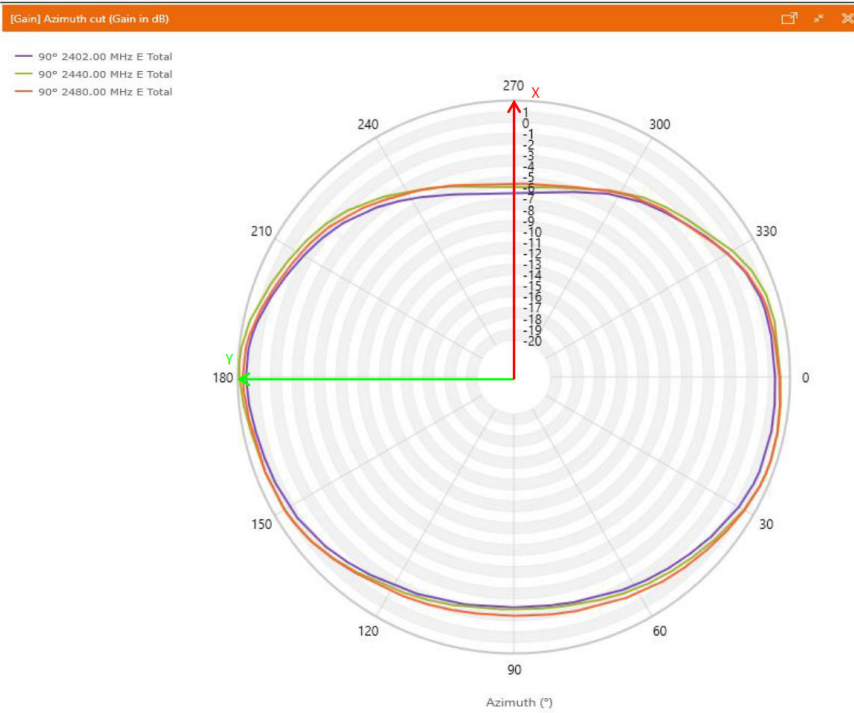
Figure 8.13. Typical 2D Antenna Radiation Patterns - Theta 90º (Front View) Gain (dBi)

8.4.1 Proximity to Other Materials

Avoid placing plastic or any other dielectric material in close proximity to the antenna. Conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region, but this will also negatively impact antenna efficiency and reduce range.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

8.4.2 Proximity to Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

9. Package Specifications

9.1 Dimensions

Table 9.1. Module Dimensions

Parameter	Value (LxWxH)	Units
Module Dimensions	21.10 x 16 x 2.32	mm
Tolerance	±0.2	mm

9.2 Package Outline
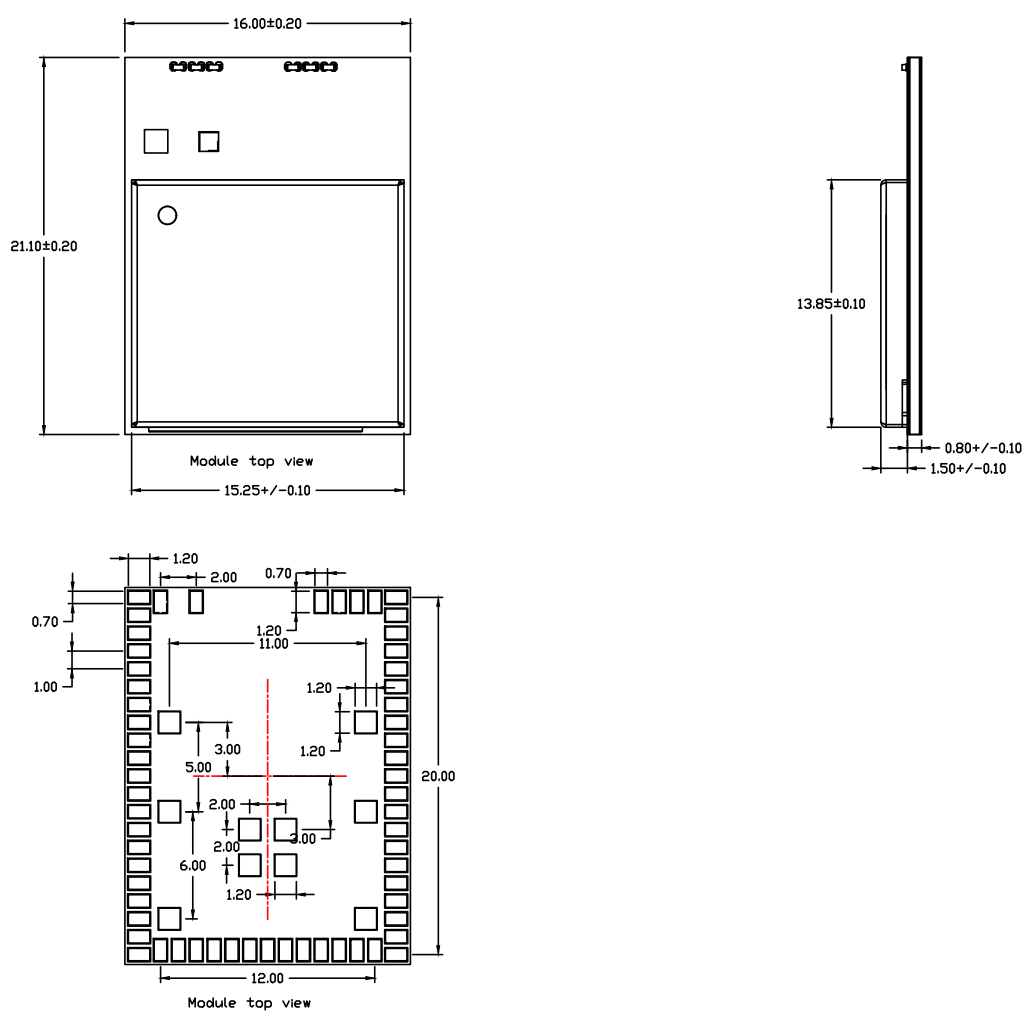
Figure 9.1. Package Outline

9.2.1 Pin Locations

> **Note:** All coordinates in the table below are in millimeters, and in TOP VIEW.

Figure 9.2. Pin Numbering

Table 9.2. Pin Locations

PAD X-Y Coordinates			
Pad #	X	Y	Pad Size
1	-4	9.75	(1.2 x 0.7) mm
2	-6	9.75	
3	-7.2	10	
23	-7.2	-10	
24	-6	-9.75	
36	6	-9.75	
37	7.2	-10	
57	7.2	-10	
58	6	9.75	
61	3	9.75	
62	-5.5	3	(1.2 x 1.2) mm
63	-5.5	-2	
64	-5.5	-8	
65	5.5	-8	
66	5.5	-2	
67	5.5	3	
68	-1	-3	
69	-1	-5	
70	1	-5	
71	1	-3	

9.3 PCB Landing Pattern
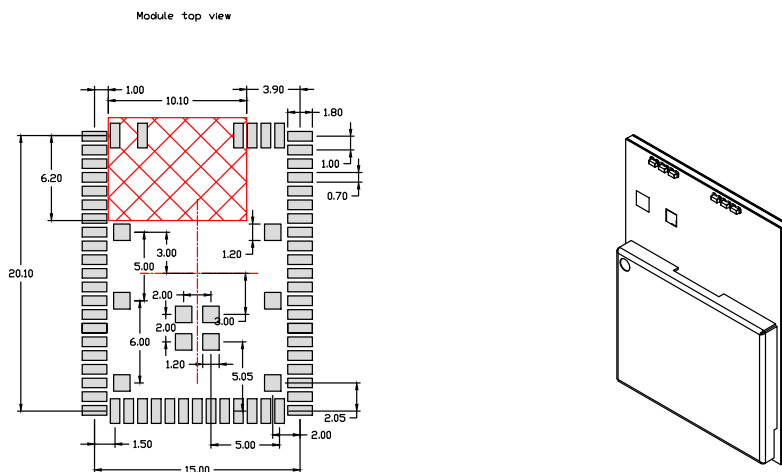
Figure 9.3. PCB Landing Pattern

Table 9.3. PCB Landing Pattern Pin Locations

PAD X-Y Coordinates			
Pad #	X	Y	Pad Size
1	-4	10.05	(1.8 x 0.7) mm
2	-6	10.05	
3	-7.5	10	
23	-7.5	-10	
24	-6	-10.05	
36	6	-10.05	
37	7.5	-10	
57	7.5	10	
58	6	10.05	
61	3	10.05	

PAD X-Y Coordinates			
Pad #	X	Y	Pad Size
62	-5.5	3	(1.2 x 1.2) mm
63	-5.5	-2	
64	-5.5	-8	
65	5.5	-8	
66	5.5	-2	
67	5.5	3	
68	-1	-3	
69	-1	-5	
70	1	-5	
71	1	-3	

9.4 Module Marking Information

The table below illustrates the marking on the Single band module and explains the marking on the module.
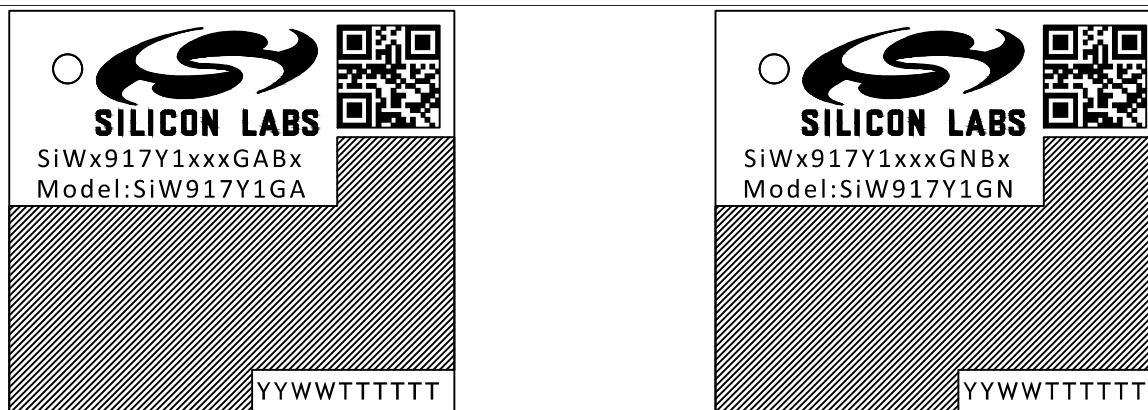
Figure 9.4. Module Marking Information

Marking		Description
Part	SiWx917Y1xxxGABx/ SiWx917Y1xxxGNBx	Orderable Part Number (OPN) designation
Model	SiW917Y1GA/SiW917Y1GN	Model Number designation
QR Code	YYWWMMABCDE	YY – Last two digits of the assembly year
		WW – Two-digit workweek when the device was assembled
		MMABCDE – Silicon Labs unit code
Lot Code	YYWWTTTTTT	YY – Last two digits of the assembly year
		WW – Two-digit workweek when the device was assembled
		TTTTTT – Manufacturing trace code. The first letter is the device revision
Compliance Marks	CE	Certification-related information, such as the CE and Giteki compliance marks, or the FCC and IC IDs, is being engraved on the hatched-out area, and/or printed on the back side of the module (silkscreen), in accordance with the requirements by regulatory bodies.

9.5 Moisture Sensitivity Level

SiWG917 modules are rated MSL3 (Moisture Sensitivity Level 3). Reels are delivered in packing which conforms to MSL3 requirements.

10. Soldering Recommendations

It is recommended that final PCB assembly of the SiWG917 follows the industry standard as identified by the Institute for Printed Circuits (IPC). This product is assembled in compliance with the J-STD-001 requirements and the guidelines of IPC-AJ-820. Surface mounting of this product by the end user is recommended to follow IPC-A-610 to meet or exceed class 2 requirements.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

Note: General SMT application notes are provided in the AN1223 document.

11. Tape and Reel

The SiWG917 modules are delivered to the customer in cut tape (100 pcs) or reel (1000 pcs) packaging having the dimensions below. All dimensions are given in mm unless otherwise indicated.
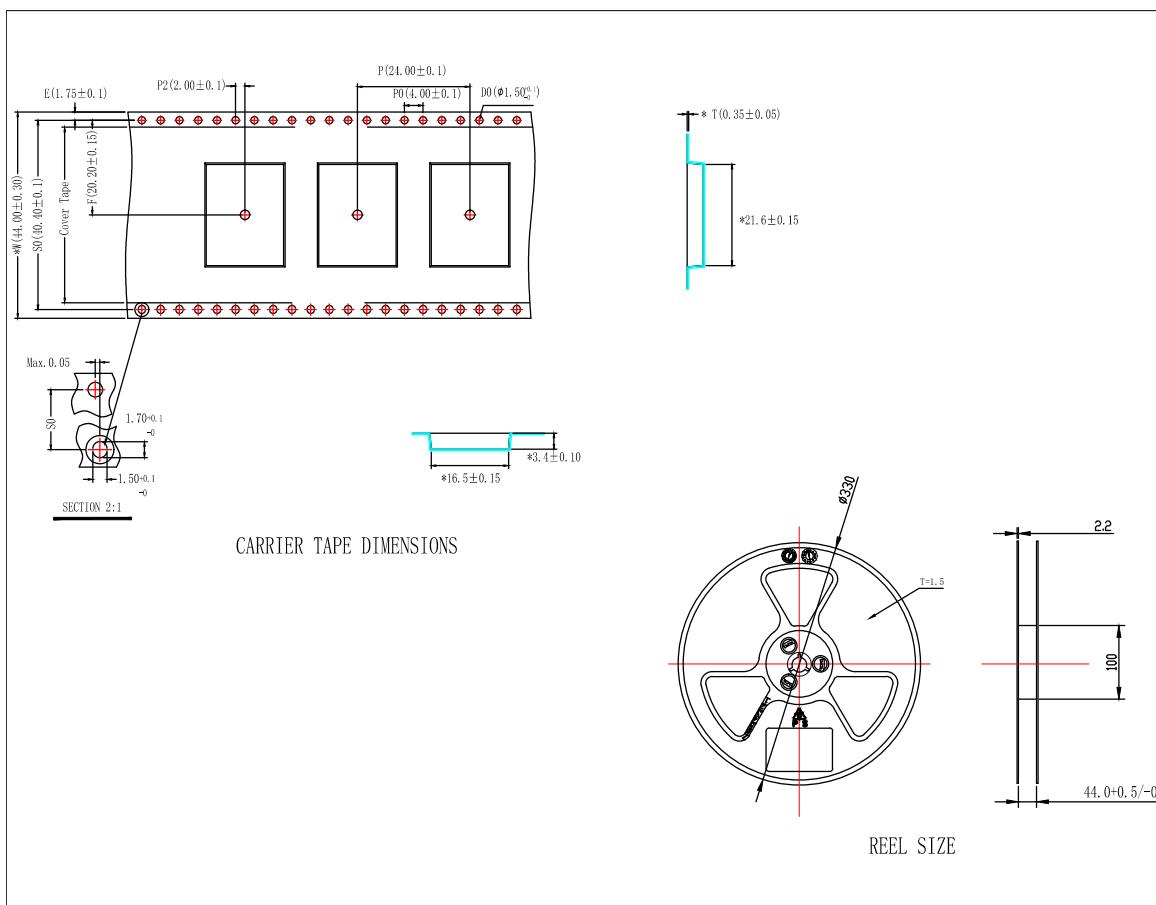
Figure 11.1. Carrier Tape Dimensions

12. Certifications

Note: All regulatory certification-related projects are ongoing at the time of this document's release.

This section details the certification status of the SiW917Y1GA and SiW917Y1GN Connectivity Modules with regards to regional regulatory radio approvals. Where applicable, the status with the qualifications against the specifications of the supported global industrial wireless standards is given too.

The address of the legal manufacturer (technology owner) and certification applicant is:

SILICON LABS / SILICON LABORATORIES FINLAND OY
Alberga Business Park, Bertel Jungin aukio 3,
02600 Espoo, Finland

The SiW917Y1GA and SiW917Y1GN Connectivity Modules have brand name of "SILICON LABS".

"SILICON LABS" (and "Silicon Labs") is a trademark globally owned by the Silicon Laboratories Inc. corporation, and all branches and subsidiaries, including the above applicant, holds the right to use it.

12.1 Qualified Antennas

The SiW917Y1GA and SiW917Y1GN Connectivity Modules have been tested and certified for the use with respectively the built-in integral antenna and a reference external antenna attached to the module's RF pin denoted as RF_PORT. The intended antenna impedance is 50 Ω.

Performance characteristics for the built-in antenna are presented in 8.4 SiW917Y1GA Antenna Radiation and Efficiency. The details of the qualified external antenna(s) are summarized in the table below.

Table 12.1. Qualified External Antenna(s) for the SiW917Y1GN Modules

Manufacturer and Model	Type	Peak Gain	Impedance
TE Connectivity Ltd. (previously Linx Technologies Inc.), ANT-2.4-CW-CT-RPS	Connectorized Coaxial Dipole	+2.8 dBi	50 Ω

Any external antenna of the same general type and of equal or less peak directional gain compared to the one listed in the above table, and having similar in-band and out-of-band characteristics, can be used in the regulatory areas that have modular radio approvals, such as USA and Canada, as long as spot-check testing of the host is performed to verify that no performance changes compromising compliance have been introduced. In the particular FCC case, in order to comply with e-CFR Title 47, Part 15, Subpart C, Section 15.203, the module integrator using an external antenna must ensure it has a unique connector or it is nondetachable.

When using instead an external antenna of a different type (such as a chip antenna, a host PCB trace antenna, or a patch) or having non-similar in-band and out-of-band characteristics, but still with a gain less than or equal to the maximum gain listed in the table above, in principle it can be added to the existing modular grant/certificate by mean of a permissive change, for example with FCC and ISED. Typically, some radiated emission testing is demanded, but no modular or end-product re-certification is required. Please consult your certification house and/or a certification body and/or the module manufacturer for a confirmation of the correct procedures and for any authorization to perform permissive changes.

On the other hand, all products designed to be used with an external antenna having more gain than the maximum gain listed in the table above are very likely to require a full new end-product certification. Since the exact permissive change or registration or re-certification procedure is chosen on a case-by-case basis, please consult your certification house and/or a certification body for understanding the correct approach based on your unique design. You might also want or need to get in touch with Silicon Labs for any authorization letter that your certification body might ask for.

In countries applying the ETSI standards, where manufacturers issue a self-Declaration of Conformity before placing products in the market, like in the EU countries, the radiated emissions are always tested with the end-product and the external antenna type is not critical, but antennas with higher gain may violate some of the regulatory limits.

For Japan, the allowed external antennas are listed in the certificate and/or test report(s). Any other external antenna will have to be formally added to the list of approved antennas by the certificate holder: in this case, please reach out to the module manufacturer to discuss such addition, or consider certifying the end-product itself as an alternative.

12.2 CE and UKCA - EU and UK

The SiW917Y1GA and SiW917Y1GN modules have been tested against the relevant harmonized/designated standards and are in conformity with the essential requirements and other relevant requirements of the EU's Radio Equipment Directive (RED) (2014/53/EU) and of the UK's Radio Equipment Regulations (RER) (S.I. 2017/1206).

Please notice that every end-product integrating the SiW917Y1GA and SiW917Y1GN Connectivity Modules will need to perform the radio EMC tests on the whole assembly, according to the ETSI 301 489-x relevant standards.

Furthermore, it is ultimately the responsibility of the manufacturers to ensure the compliance of their end-products as a whole. The specific product assembly is likely to have an impact to RF radiated characteristics, when compared to the bare module. Hence, manufacturers should carefully consider RF radiated testing with the final product assembly, especially taking into account the gain of the external antenna if any, and the possible deviations in the PSD, EIRP and spurious emissions measurements, as defined in the ETSI EN 300 328 standard.

The modules are entitled to carry the CE and UKCA compliance marks, and the respective formal Declarations of Conformity (DoCs) are available at the product web page which is reachable starting from www.silabs.com.

Each OEM must also consider applying the compliance marks to a visible location on their end-products. In general, module customers assume full responsibility with regards to learning the guidelines and meeting the requirements for the compliance in each country where their end-products are marketed.

12.3 FCC - USA

This device complies with FCC's e-CFR Title 47, Part 15, Subpart C, Section 15.247 (and related relevant parts of the ANSI C63.10 standard) when operating with the built-in integral antenna or with an external antenna type as discussed in chapter 11.1.

Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

FCC RF Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying the RF exposure compliance.

This transmitter meets the Mobile requirements at a distance of 20 cm and above from the human body, in accordance to the limit(s) exposed in the RF Exposure Analysis. This transmitter also meets the Portable requirements at distances equal or above those being reported in Minimum Separation Distances for SAR Evaluation Exemption.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM Responsibilities to Comply with FCC Regulations

This module has been tested for compliance to FCC Part 15.

OEM integrators are responsible for testing their end-product for any additional compliance requirements needed with this module installed (for example, digital device emissions, PC peripheral requirements, etc.)

Additionally, investigative measurements and spot-checking are strongly recommended to verify that the full system compliance is maintained when the module is integrated, even with a module having a full modular approval, in accordance with the "Host Product Testing Guidance" in FCC's KDB 996369 D04 Module Integration Guide V01.

- **General Considerations**

  This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement, which is typically applicable to the final host. The final host will still need to be assessed for compliance to this portion of the rule requirements, if applicable.

- **Manual Information to the End User**

  The OEM integrator has to be aware not to provide information to the end-user regarding how to install or remove this RF module, or how to change RF related parameters, in the user's manual of the final product which integrates this module.

  The end user manual shall include all required regulatory information/warnings as shown in this manual.

- **Host Manufacturer Responsibilities**

  Host manufacturers are ultimately responsible for the full compliance of their host system. The final product is supposed to be assessed against all the essential requirements of the FCC rules, such as FCC Part 15 Subpart B, before it can be placed on the US market. This includes re-assuring the compliance of the radio transmitter with the RF and EMF essential requirements of the FCC rules. The modular radio transmitter must not be incorporated into any other radio-equipped device or system without retesting for compliance as multi-radio and combined equipment.

  Except for minor (cosmetic) modifications, most changes to an FCC certified equipment require preliminary testing to determine whether any of such changes is a Class I or Class II permissive change. For more details about using the Single Modular Transmitter, refer to the following FCC documents:

  • KDB 996369 D01 Transmitter Module Equipment Authorization Guide

  • KDB 996369 D02 Frequently Asked Questions and Answers about Modules

  • KDB 178919 D01 Permissive Change Policy

  • KDB 178919 D02 Permissive Change Frequently-Asked Questions

Separation

- To meet the SAR exemption for portable conditions, the minimum separation distances indicated in Minimum Separation Distances for SAR Evaluation Exemption must be maintained between the human body and the radiator (antenna) at all times.
- This transmitter module is tested in a standalone RF Exposure condition, and in case of any co-located radio transmitter being allowed to transmit simultaneously, or in case of portable use at closer distances from the human body than those allowing the exceptions rules to be applied, a separate additional SAR evaluation, or a reduction in the max output power or in the duty-cycle, might be required for the host, ultimately leading to a Class II Permissive Change, or more rarely to a new grant.
- **Important Note:** In the event that the conditions for the exemption cannot be met, the final product will likely have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the FCC authorization to remain valid, and a permissive change will have to be applied. The SAR evaluation (and/or reconfiguration) is in the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body, following a *Change in ID* authorization by the module's original grant holder.

End Product Labeling

The SiW917Y1GA and SiW917Y1GN modules are labeled with their own FCC ID. In all those cases when the module's label is not visible, for example after the module becomes enclosed inside the end-product casing, or if the FCC ID is printed on the module's PCB silkscreen, then the outside of the device into which the module is installed must also have a label with a reference to the embedded module. In that case, the final product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQ-917AC"

or

"Contains FCC ID: QOQ-917AC"

Final note:

As long as all the conditions in this and all the above chapters are met, further RF testing of the transmitter will not be strictly required. However, still consider the good practice and the FCC strong recommendation to ensure the compliance of the host by spot-checking. Nevertheless, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements which might be mandatory with this module installed.

12.4 ISED - Canada

This radio transmitter (with IC: 5123A-917AC and PMN: *Bluetooth Low Energy and 802.11b/g/n/ax wireless radio module*) has been approved by *Innovation, Science and Economic Development Canada* (*ISED Canada*, formerly *Industry Canada*) to operate with the built-in integral antenna or with the external antenna type(s) listed in Qualified Antennas, having the maximum permissible gain indicated in the table. External antenna types not included in this list, or having a gain greater than the maximum gain listed, are strictly prohibited for use with this device.

This radio-equipped device complies with ISED's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference.
2. This device must accept any interference, including interference that may cause undesired operation of the device.

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

The module meets the requirements for Mobile use cases when the minimum separation distance from the human body is 20 cm or greater, in accordance to the limit(s) exposed in the RF Exposure Analysis.

For Portable use cases, RF exposure or SAR evaluation is not required when the separation distances from the human body are equal or above those reported in Minimum Separation Distances for SAR Evaluation Exemption .

If the separation distance from the human body is less than the values stated in Minimum Separation Distances for SAR Evaluation Exemption, then the OEM integrator is responsible for evaluating the SAR with the end-product, or for the re-configuration of the radio module in the host in terms of lowering the max RF TX power and/or the duty-cycle. A permissive change would be required too, under the responsibility of the host manufacturer, following a *Multiple Listing* authorization by the module's original certificate holder.

OEM Responsibilities to comply with IC Regulations

The SiW917Y1GA and SiW917Y1GN modules have been certified for integration into products only by OEM integrators, under the following conditions:

- The module must be installed in such a way that the intended minimum separation distances are maintained between the radiator (antenna) and all persons at all times. Minimum Separation Distances for SAR Evaluation Exemption indicates the distances in accordance to the use cases.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

Important Note: In the event that the above conditions cannot be met, the final product will have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the ISED authorization to remain valid; a permissive change will have to be applied too. The RF Exposure evaluation (SAR, or possibly a re-configuration) is in the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body, following a *Multiple Listing* authorization by the module's original certificate holder.

End Product Labeling

The SiW917Y1GA and SiW917Y1GN modules are labeled with their own IC ID. In all those cases when the module's label is not visible, for example after the module becomes enclosed inside the end-product casing, or if the IC ID is printed on the module's PCB silkscreen, then the outside of the device into which the module is installed must also have a label with a reference to the embedded module. In that case, the final product must be labeled in a visible area with the following:

"**Contains Transmitter Module IC: 5123A-917AC**"

or

"**Contains IC: 5123A-917AC**"

Final notes:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end-product.

As long as all the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.)

ISED (Français)

Le présent émetteur radio (IC: 5123A-917AC, PMN: *Bluetooth Low Energy and 802.11b/g/n/ax wireless radio module*) a été approuvé par *Innovation, Sciences et Développement Économique Canada* (*ISED Canada*, anciennement *Industrie Canada*) pour fonctionner avec l'antenne intégrée et le ou les types d'antenne énumérés à la section Qualified Antennas, avec le gain maximal admissible indiqué. Les types d'antenne non inclus dans cette liste, ayant un gainsupérieur au gain maximal indiqué, sont strictement interdits d'utilisation avec cet appareil.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage;
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Déclaration d'exposition RF

Les exceptions aux limites de l'évaluation SAR sont données dans le numéro 5 de la publication RSS-102.

Le module répond aux exigences pour les cas d'utilisation Mobile lorsque la distance minimale de séparation du corps humain est de 20 cm ou plus, conformément à la (aux) limite(s) exposée(s) dans l'analyse de l'exposition RF.

Pour les cas d'utilisation portables, l'évaluation de l'exposition RF ou l'évaluation SAR n'est pas requise lorsque les distances de séparation du corps humain sont égales ou supérieures à celles indiquées dans Minimum Separation Distances for SAR Evaluation Exemption.

Si la distance de séparation du corps humain est inférieure aux valeurs indiquées dans Minimum Separation Distances for SAR Evaluation Exemption, l'intégrateur OEM est responsable de l'évaluation du SAR avec le produit final, ou de la reconfiguration du module radio dans l'hôte en termes de réduction de la puissance RF TX maximale et/ou du rapport cyclique. Une modification permissive serait également nécessaire, sous la responsabilité du fabricant de l'hôte, suite à une autorisation de cotation multiple par le titulaire du certificat du module d'origine.

Responsabilités du fabricant de se conformer à la réglementation IC

Le module a été certifié pour l'intégration dans les produits uniquement par les intégrateurs OEM dans les conditions suivantes:

- Le module émetteur doit être installée de manière à maintenir une distance de séparation minimale, comme indiqué ci-dessus, entre le radiateur (antenne) et toutes les personnes à tout moment.
- Le module émetteur ne doit pas être localisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

Remarque Importante: au cas où ces conditions ne pourraient pas être remplies, le produit final devra être soumis à des tests supplémentaires pour évaluer l'exposition RF, ou passer par une reconfiguration de la puissance de sortie maximale et/ou du rapport cyclique, afin que l'autorisation ISED reste valable; une modification permissive devra également être appliqué. L'évaluation de l'exposition aux radiofréquences (SAR, ou éventuellement une reconfiguration) est sous la responsabilité du fabricant du produit final, ainsi que le changement permissif qui peut être effectué avec l'aide de l'organisme de certification des télécommunications du client, après autorisation de cotation multiple par le titulaire de la certification du module.

Étiquetage des produits finis

Les modules SiW917Y1GA / SiW917Y1GN sont étiquetés avec leur propre IC ID. Dans tous ces cas, si l'ID IC n'est pas visible après l'installation du module à l'intérieur d'un autre appareil, alors l'extérieur de l'appareil dans lequel le module est installé doit également afficher une étiquette faisant référence au module inclus. Dans ce cas, le produit final doit être étiqueté dans une zone visible avec les éléments suivants:

"**Contient le module transmetteur IC: 5123A-917AC**"

ou

"**Contient IC: 5123A-917AC**"

Remarques finales:

L'intégrateur OEM doit être conscient de ne pas fournir à l'utilisateur final d'informations sur la procédure d'installation ou de retrait de ce module RF ni sur la modification des paramètres liés à la RF dans le manuel d'utilisation du produit final.

Tant que toutes les conditions ci-dessus sont remplies, aucun test supplémentaire de l'émetteur ne sera nécessaire. Toutefois, l'intégrateur OEM reste responsable de l'essai de son produit final pour déterminer les exigences de conformité supplémentaires requises avec ce module installé (par exemple, émissions d'appareils numériques, exigences relatives aux périphériques PC, etc.)

12.5 MIC - Japan

The SiW917Y1GA and SiW917Y1GN modules are certified in Japan with following certification number:

- 203-JN1379

It is the end-product manufacturer's responsibility to ensure that a module is configured to meet the compliance limits, as documented in the formal certification test report(s) being available at www.silabs.com. Refer to the API reference manual(s) to learn for example how to configure (limit) the maximum RF TX power for the normal operations if need be, and refer as well to the power setting tables in the test report(s) in order to realize the maximum output power allowed for the regulatory compliance in Japan.

Manufacturers integrating a radio module into their host equipment are supposed to make the compliance mark and the certification number visible on the outside of their device. This combination of mark and number, and their relative placement, is depicted in the example Figure 5.1 below, and depending on the overall size it might also appear among the top shield markings of the radio module. The certification mark and certification number must be placed close to the text in the Japanese language which is provided below. This requirement in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

Certification text to be placed on the outside surface of the host equipment:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation of the text:

"This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law."

The "Giteki" compliance mark, together with the actual module's certification number, as shown in the following example figures, must be affixed to an easily noticeable section of the specified radio-enabled host equipment. Note that such section may be required to contain additional information if the end-device embedding the module is also subject to a Telecom approval.

The manufacturer of the final product is also responsible to provide a Japanese language version of the User Manual and/or Installation Instructions as a companion document coming with the final product when placed on the market in Japan. Such a document will have to mention the integrated radio component and the related certification information.

Figure 12.1. Example of GITEKI Mark with Placeholder for Actual Certification Number
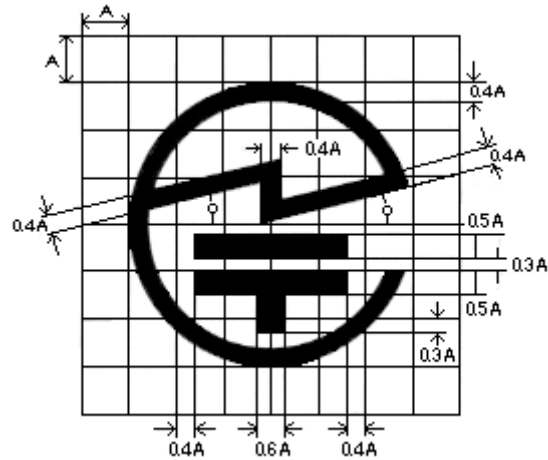
Figure 12.2. Detail of GITEKI Compliance Mark

12.6 KC - South Korea

The SiW917Y1GA and SiW917Y1GN modules have a RF registration for import and use in South Korea.

Registration number is KC ID: R-R-BGT-917AC

These modules are meant to be integrated into end-products, which then become exempted from doing the RF emission testing, as long as the recommended design guidance is followed, and as long as, where applicable, the approved external antennas are used and any additional transmit power backoff is implemented in accordance to the measurements and configurations seen in the formal test report(s).

EMC testing and any other relevant test applicable to the end-product as a whole, plus appropriate labeling of the end-product, might still be required for the full regulatory compliance in the country.

12.7 NCC - Taiwan

The SiW917Y1GA and SiW917Y1GN modules are certified in Taiwan with NCC certification numbers TBD and TBD.

SiW917Y1GA 和 SiW917Y1GN 模塊已在台灣獲得 NCC 認證，認證號為 TBD 和 TBD。

Manufacturers are required to mark their end-products with the following sentence: "This product contains a radio frequency module with certification number TBD."

系統製造商應在平台上放置如下聲明："本產品包含認證號為 TBD 的射頻模塊。"

Note: The outer packaging of the final product must also be marked with the NCC conformity mark by the manufacturer.

注意：最終產品的外包裝也必須由製造商打上 NCC 合格標誌

Additionally, the final product will have to be listed in the NCC database of approved radio-equipped devices. Consequently, the end manufacturer is also supposed to contact the certification house that originally released the modular approval and apply for the registration of their device under the applicable certification number above. Fees might apply, and an authorization by the module manufacturer might also be required.

該平台還需要列入經批准的無線電設備的 NCC 數據庫；因此，平台製造商還應聯繫最初頒發全模塊化批准的認證機構，並根據上述認證編號申請註冊其設備（可能需要付費）。

NCC Statement
For low-power radio frequency equipment that has been certified, companies, firms, or users are not allowed to change the frequency, increase the power, or change the characteristics and functions of the original design without further NCC approval. The use of low-power radio frequency equipment shall not affect flight safety and interfere with legal communications. If interference is found, it shall be immediately stopped, and the equipment can be brought back into use only after it has been improved, so that interference is found no more. The aforementioned legal communication refers to radio communications operating in accordance with the provisions of the Telecommunications Management Act. Low-power radio frequency equipment must withstand interference from legitimate communications or radiating electrical equipment for industrial, scientific, and medical applications.
NCC 警語
取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。 低功率射頻器材之使用不得影響飛航安全及干擾合法通信。 經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。 前述合法通信，指依電信管理法規定作業之無線電通信。 低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

12.8 SRRC - China

The SiW917Y1GA module has a full modular radio type approval for re-use by the OEM integrators:

Certificate number: TBD

CMIIT ID: TBD

The SiW917Y1GN module has a limited modular radio type approval for re-use by the OEM integrators:

Certificate number: TBD

CMIIT ID: TBD

Note for modules with a full modular approval: every end-product integrating the module must be labeled with the following statement, or alternatively the statement will have to go to the end-product's user manual:

本设备包含一个无线电发射器模块，型号核准代码为：CMIIT ID：2023YYXXXX

(Translation: This equipment contains a radio transmitter module with model approval code: CMIIT ID: XXXXYYZZZZ)

中国－SRRC

SiW917Y1GA 模塊具有完整的模塊化認證，可供 OEM 集成商重複使用：
　　認证编号：2024-XXXX
　　CMIIT ID: 2024YYXXXX

SiW917Y1GN 模塊具有有限的模塊化認證，可供 OEM 集成商重複使用：
　　認证编号：2024-ZZZZ
　　CMIIT ID: 2024YYZZZZ

具有完全模塊化批准的模塊注意事項：以下聲明必須出現在嵌入模塊的最終產品的標籤和/或用戶手冊中：

　　本设备包含一个无线电发射器模块，型号核准代码为：CMIIT ID：2023YYXXXX

12.9 Australia (ACMA)

The SiW917Y1GA and SiW917Y1GN modules are in compliance with the Australian RCM requirements, and are labelled with the RCM Compliance Mark. The formal Declaration of Conformity (DoC) is available at www.silabs.com. With the DoC and RCM compliance mark, the modules are also covered for the use in New Zealand (RSM).

12.10 RF Exposure and Proximity to Human Body

When using the SiW917Y1GA and SiW917Y1GN modules in an application where the radio-equipped end-product is located close to the human body, the human RF Exposure must be taken into account. FCC, ISED, and CE/UKCA all have different standards and rules for evaluating the RF Exposure. In particular, each regulator has different requirements when it comes to the exemption from having to perform RF Exposure evaluation and/or SAR (Specific Absorption Rate) measurements, and the minimum separation distances between the module's antenna and the human body varies accordingly. The properties of the SiW917Y1GA and SiW917Y1GN modules allow the minimum separation distances detailed in the table below for the SAR measurement exemption in the Portable use cases (less than 20 cm from the human body). These modules are approved for the Mobile use case (more than 20 cm) without any need for RF Exposure evaluation.

Table 12.2. Minimum Separation Distances for SAR Evaluation Exemption

Certification	SiW917Y1GA	SiW917Y1GN
FCC	BLE: 22 mm 802.11b/g/n/ax: 37 mm All protocols in use (overall): 37 mm	BLE: 23 mm 802.11b/g/n/ax: 39 mm All protocols in use (overall): 39 mm
ISED	BLE: 30 mm 802.11b/g/n/ax: 45 mm All protocols in use (overall): 45 mm	BLE: 30 mm 802.11b/g/n/ax: 45 mm All protocols in use (overall): 45 mm
CE / UKCA	In general, the RF exposure should always be evaluated with the end-product when transmitting with EIRP power levels higher than 20 mW (13 dBm) while operating at distances closer than 20 cm from the human body. With the SiW917Y1GA and SiW917Y1GN modules, this is the case only with the 802.11b/g/n/ax protocols transmitting at full power. In all other cases, modules comply with the requirements of the relevant standard(s).	

The exemption minimum distances above, calculated for reference in the full output power use-case, are based on the rules in force at the time of writing this data sheet. Even though changes happen rarely, always ensure to apply the rules in force at the time of placing the end-product into the market.

In the cases of FCC and ISED, it is allowed to use a module at its max RF TX power in an end-product where the typical separation distance from the human body is smaller than mentioned above, but it requires evaluating the RF Exposure in the final assembly and applying for a *Class 2 Permissive Change* to the FCC and ISED approvals of the module. In order to proceed with the permissive changes, first the module manufacturer should be asked for an authorization to do an FCC's *Change in ID* and an ISED's *Multiple Listing*; then, the new Portable condition will be added to the new parallel grants owned by the end-product manufacturer, for extending the approvals to their unique host under their unique configuration and mode of use.

For those end-products where the embedded module is configured to implement only a single wireless protocol which would allow for the exemption at a shorter distance than the overall minimum distance, there would be no need the evaluate the RF Exposure at such a shorter distance and above. However, a permissive change would still be needed as a mean to notify the FCC / ISED of the reason why in the field the module is allowed to operate at a shorter distance than the overall minimum distance in the table above.

An example of another use case where the module could operate at a shorter distance than in the table above, without having to do the RF Exposure evaluation / SAR measurement, is when the power or the duty-cycle is reduced during normal operation. However, the new minimum distance for the exemption should be re-calculated, and still a permissive change would be needed to notify the regulators of the new conditions.

For the CE/UKCA compliance, RF Exposure must be considered and evaluated by the OEM in all cases (if any) when the end-product is transmitting at higher power level than indicated in the table above.

Note: Placing the module in touch or very close to the human body will have a negative impact on the efficiency of the antenna thus a reduced range is to be expected.

12.11 Bluetooth Qualification

The SiW917Y1GA and SiW917Y1GN modules have the following Qualified Design Listings (QDL) with corresponding Qualified Design Identification (QDID) based on the Bluetooth Core Specification 5.4:

1. **QDID 230044**
   - This Tested Component is for the Low Energy RF-PHY Radio interface.
2. **QDID 226688**
   - This Tested Component is for Host Controller Interface and Low Energy Link Layer.
3. **QDID 227553**
   - This Controller Subsystem combines the above QDID 230044 and QDID 226688. It encompasses the Low Energy RF-PHY Radio interface and the Low Energy Link Layer, plus the Host Controller Interface, for easier integration when doing an End-Product Listing (EPL).

13. Documentation and Support

Silicon Labs offers a set of documents which provide further information required for evaluating, and developing products and applications using SiWG917. These documents will be available on the Silicon Labs website. The documents include information related to Software releases, Evaluation Kits, User Guides, Programming Reference Manuals, Application Notes, and others.

For further assistance, you can contact Silicon Labs Technical Support here.

Resource Location

SiWG917 Document Library : https://docs.silabs.com/wiseconnect/3.1.0/wiseconnect-developing-with-wiseconnect-sdk/

Technical Support : http://www.silabs.com/support/

14. Revision History

Revision 0.51

Work in Progress
- Updated Table 12.2 Minimum Separation Distances for SAR Evaluation Exemption on page 163

Revision 0.5

June, 2024
- Updated Features List
- Update Block Diagrams
- Updated System Overview
- Updated Pin Definitions
- Updated Electrical Specifications
- Updated Reference Schematics, BOM and Layout Guidelines
- Updated Certifications

Revision 0.4

April, 2024

NDA release and full update from previous version.

Revision 0.1

August, 2023

Preliminary version.

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

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