

Hardware Design Document

System Block Diagram of Purpletooth PT-209G Wireless Modem

Document Information

Subject: Hardware Design Document
Title: System Block Diagram of Purpletooth PT-209G Wireless Modem
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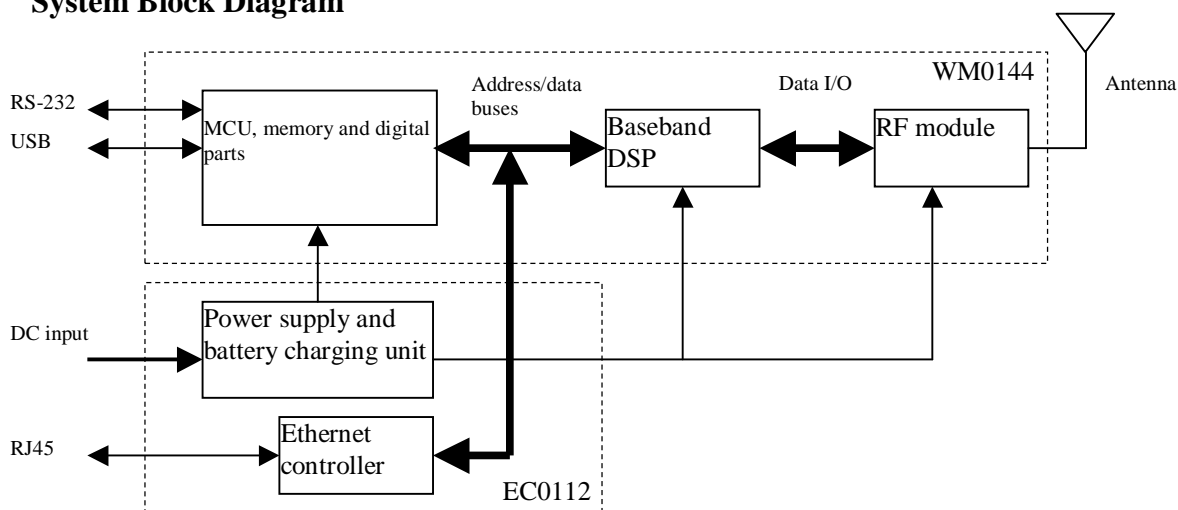
Modifications from V1.0: 1. Add the RF module block diagram.
Modifications from V2.0: 1. Add filter part numbers to RF module block diagram. 2. Add filter characteristics table.
Modification from V2.1: 1. Correct typo in RF block diagram.

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1 Introduction

The following system block diagram describes the system design of Purpletooth PT-209G modem with PCB version WM0144 and EC0112 for modem and charging boards respectively.

2 System Block Diagram



System clock supplies:

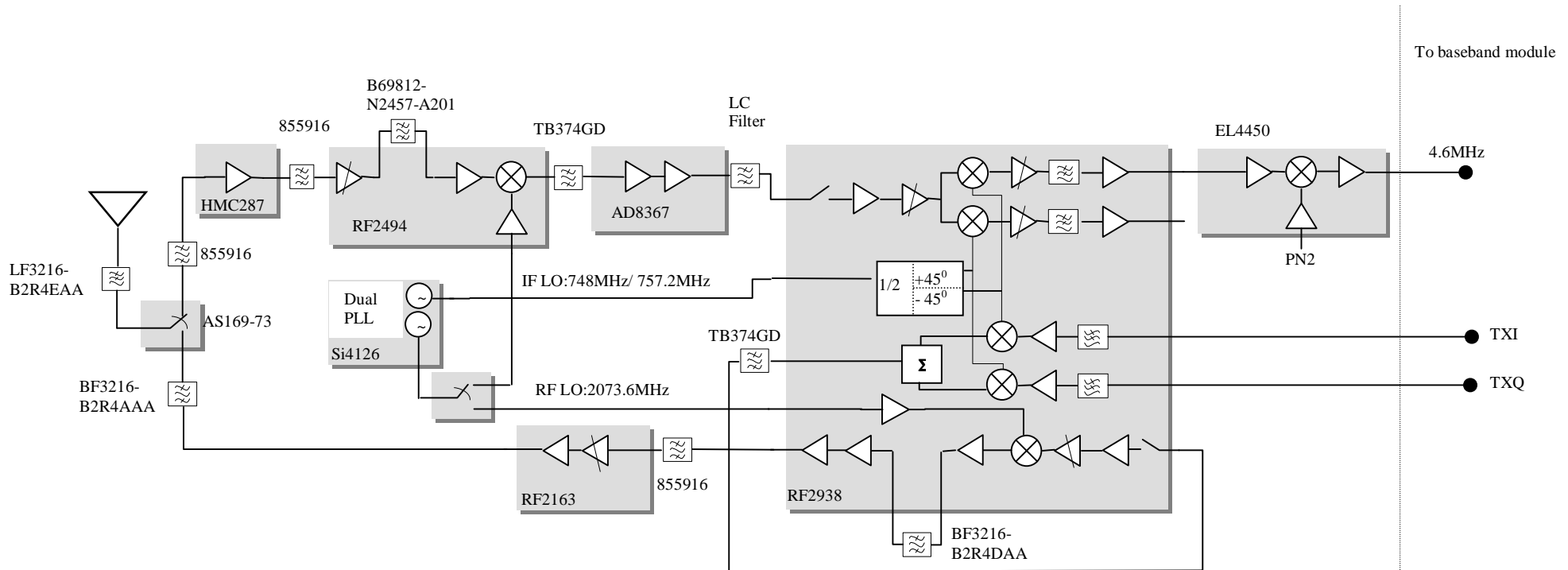
1. MCU oscillator input: 12 MHz
2. Ethernet controller oscillator input: 25 MHz
3. Baseband DSP clock input: 2 MHz (generated from clock divider in 12-MHz driven CPLD)
4. IF LO to RF module: 748 MHz
5. IF carrier at RF module: 374 MHz
6. RF LO to RF module: 2073.6 MHz
7. RF carrier at RF module: 2447.6 MHz

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3 RF Module Block Diagram



Filter characteristics:

Filter	Type	Frequency range/MHz	Center frequency/MHz
LF3216-B2R4EAA	Multi-layer low pass filter	2400 – 2483	2441.5
BF3216-B2R4AAA	Multi-layer band pass filter	2400 – 2500	2450
BF3216-B2R4DAA	Multi-layer band pass filter	2400 – 2500	2450
855916	RF SAW filter	2377.85 – 2507.45	2448.5
B69812-N2457-A201	Ceramic 2-pole filter	2400 – 2500	2450
TB374GD	374MHz SAW filter	362 – 386	374

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