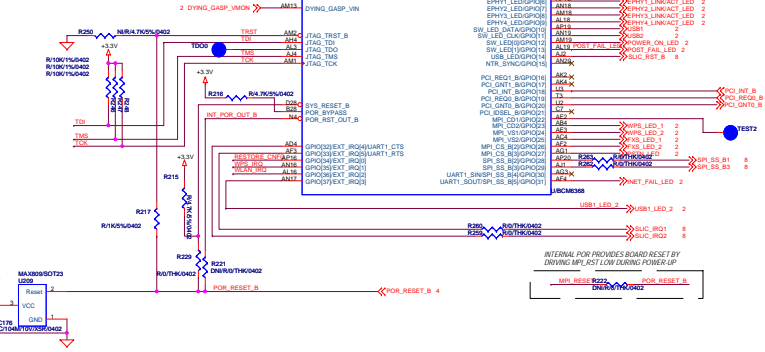
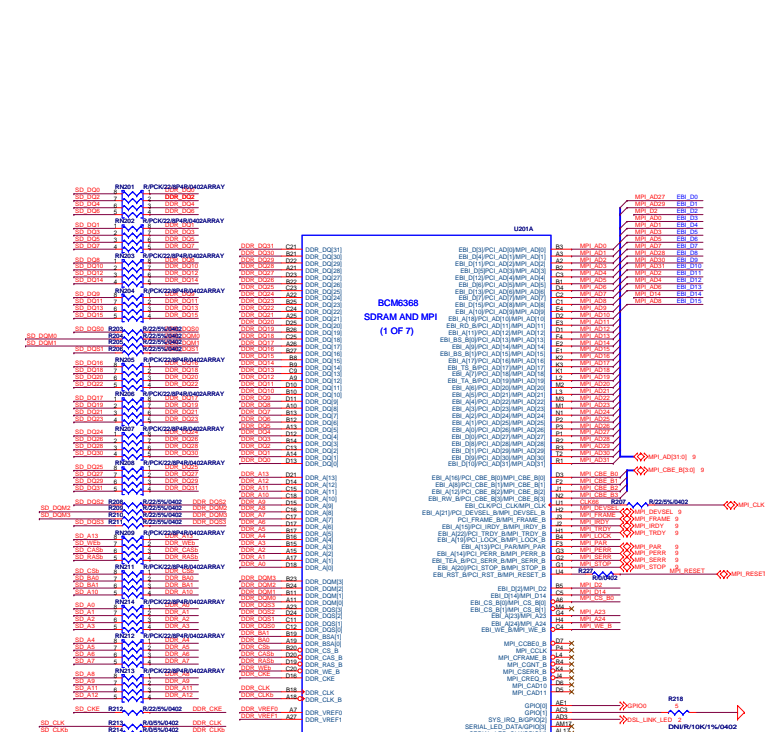
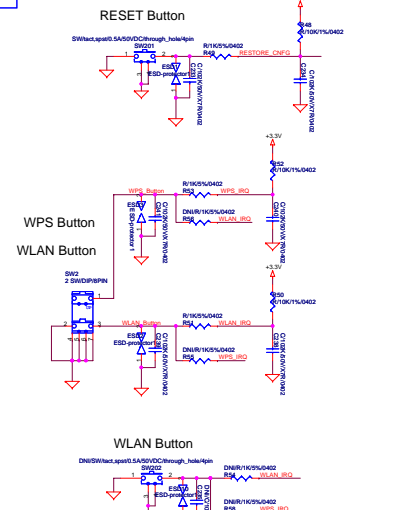
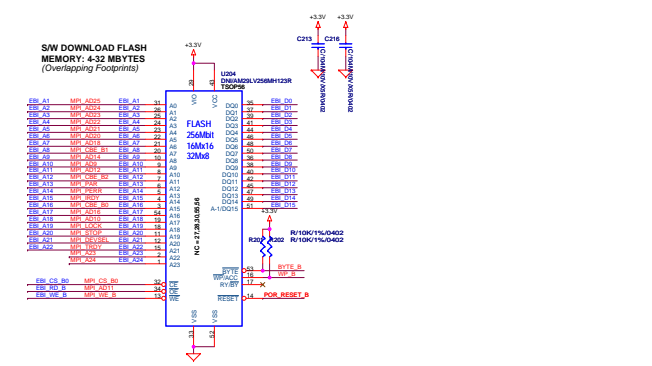


- DDR SDRAM layout rules:**
 All timing is relative to the CLK/CLKB that arrive at the destination DDR SDRAM chip.
- 1) X = CLK/CLKB should be a matched differential pair with a length $\approx 4"$
 - 2) Address and control should be $\times \pm 0.75"$ (or 100 ps)
 - 3) DQS and DQM should be $\times \pm 0.75"$ (or 100 ps)
 - 4) All DQs should match corresponding bank DQS/DQMs within $\pm 0.20"$ (or 30 ps)
 - 5) Trace impedances should be 40 ohms $\pm 10%$ (54 ohms)
 - 6) Route VREF with 30 mil traces and at least 1 high quality ceramic bypass capacitor for each connection to a device.
 - 7) All traces should have a $\mu = 3$ to 1 spacing ratio from the reference GND/PWR layer. (e.g. 15 mil trace to the spacing for a 5 mil dielectric thickness)

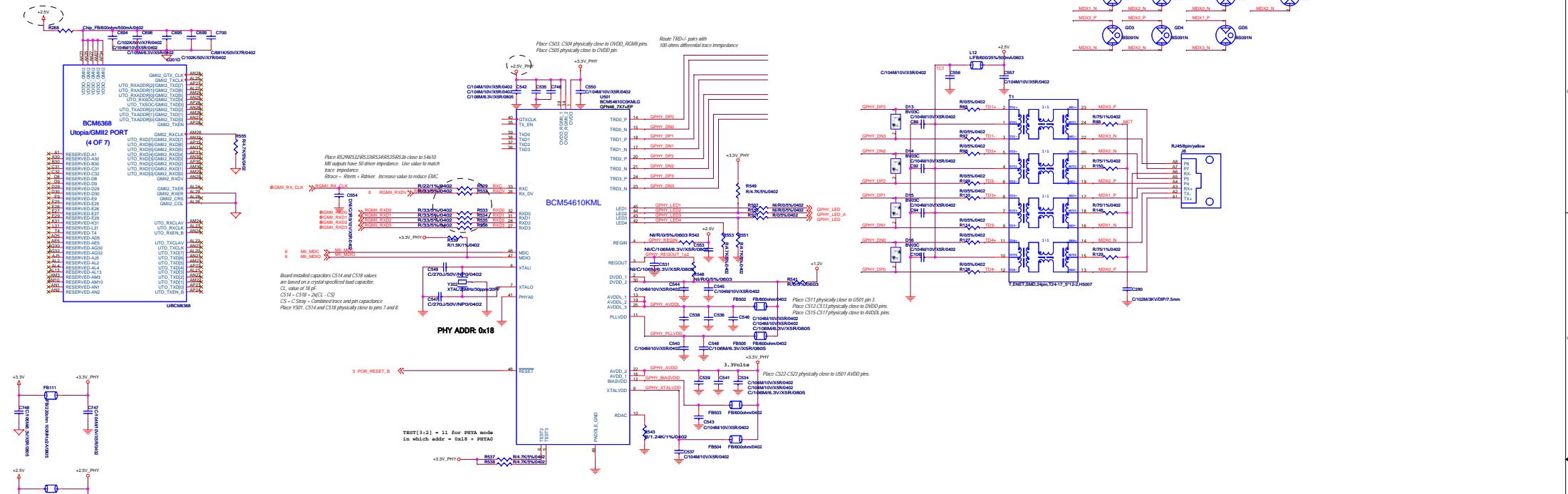


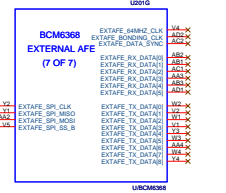
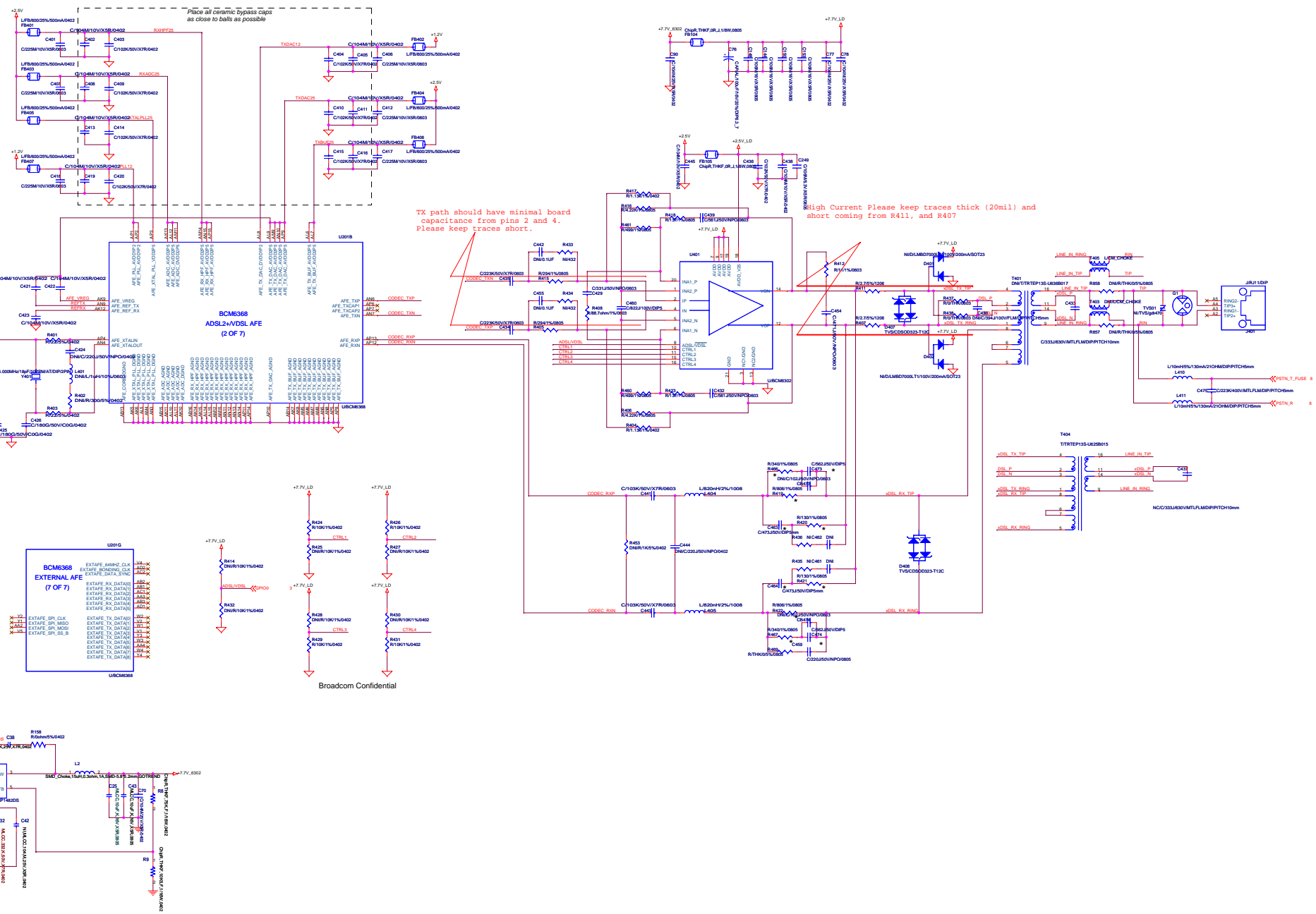
BCM6368 Bootstrap Options

MPI_A0	BOOT_SEL0	R200	DNR1K05U0402	MPI_A1	BOOT_SEL1	R201	DNR1K05U0402	MPI_A2	BOOT_SEL2	R202	DNR1K05U0402
MPI_A3	BOOT_SEL3	R203	DNR1K05U0402	MPI_A4	BOOT_SEL4	R204	DNR1K05U0402	MPI_A5	BOOT_SEL5	R205	DNR1K05U0402
MPI_A6	BOOT_SEL6	R206	DNR1K05U0402	MPI_A7	BOOT_SEL7	R207	DNR1K05U0402	MPI_A8	BOOT_SEL8	R208	DNR1K05U0402
MPI_A9	BOOT_SEL9	R209	DNR1K05U0402	MPI_A10	BOOT_SEL10	R210	DNR1K05U0402	MPI_A11	BOOT_SEL11	R211	DNR1K05U0402
MPI_A12	BOOT_SEL12	R212	DNR1K05U0402	MPI_A13	BOOT_SEL13	R213	DNR1K05U0402	MPI_A14	BOOT_SEL14	R214	DNR1K05U0402
MPI_A15	BOOT_SEL15	R215	DNR1K05U0402	MPI_A16	BOOT_SEL16	R216	DNR1K05U0402	MPI_A17	BOOT_SEL17	R217	DNR1K05U0402
MPI_A18	BOOT_SEL18	R218	DNR1K05U0402	MPI_A19	BOOT_SEL19	R219	DNR1K05U0402	MPI_A20	BOOT_SEL20	R220	DNR1K05U0402
MPI_A21	BOOT_SEL21	R221	DNR1K05U0402	MPI_A22	BOOT_SEL22	R222	DNR1K05U0402	MPI_A23	BOOT_SEL23	R223	DNR1K05U0402
MPI_A24	BOOT_SEL24	R224	DNR1K05U0402	MPI_A25	BOOT_SEL25	R225	DNR1K05U0402	MPI_A26	BOOT_SEL26	R226	DNR1K05U0402
MPI_A27	BOOT_SEL27	R227	DNR1K05U0402	MPI_A28	BOOT_SEL28	R228	DNR1K05U0402	MPI_A29	BOOT_SEL29	R229	DNR1K05U0402
MPI_A30	BOOT_SEL30	R230	DNR1K05U0402	MPI_A31	BOOT_SEL31	R231	DNR1K05U0402	MPI_A32	BOOT_SEL32	R232	DNR1K05U0402



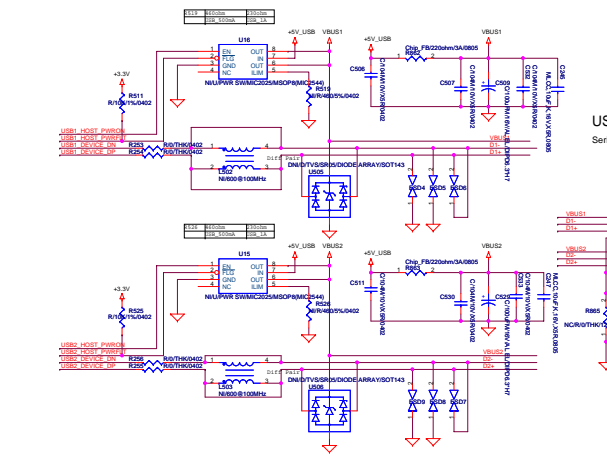
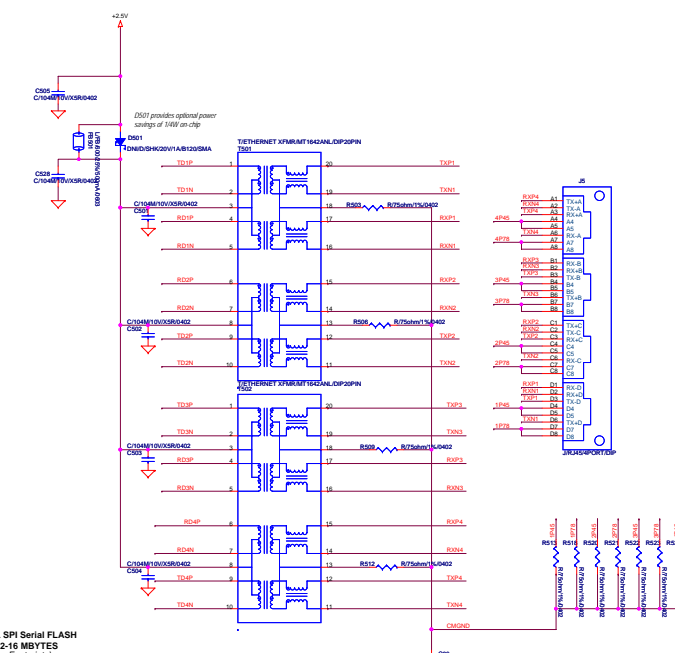
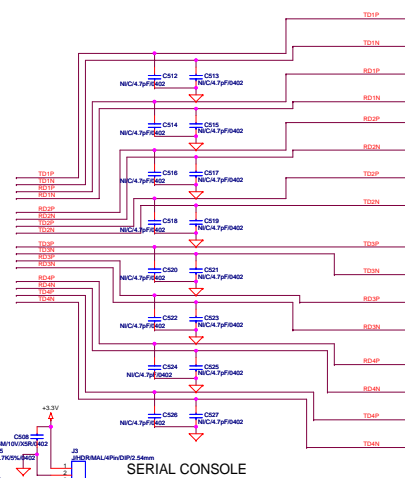
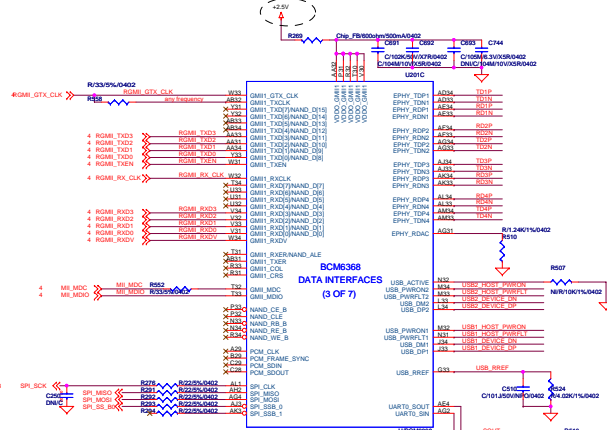
CONNECT VDD0, GM2 TO 3.3V WHEN USED IN GM1, M1 OR UTPOR4 MODE
 CONNECT VDD0, GM2 TO 2.5V WHEN USED IN RGM1 MODE

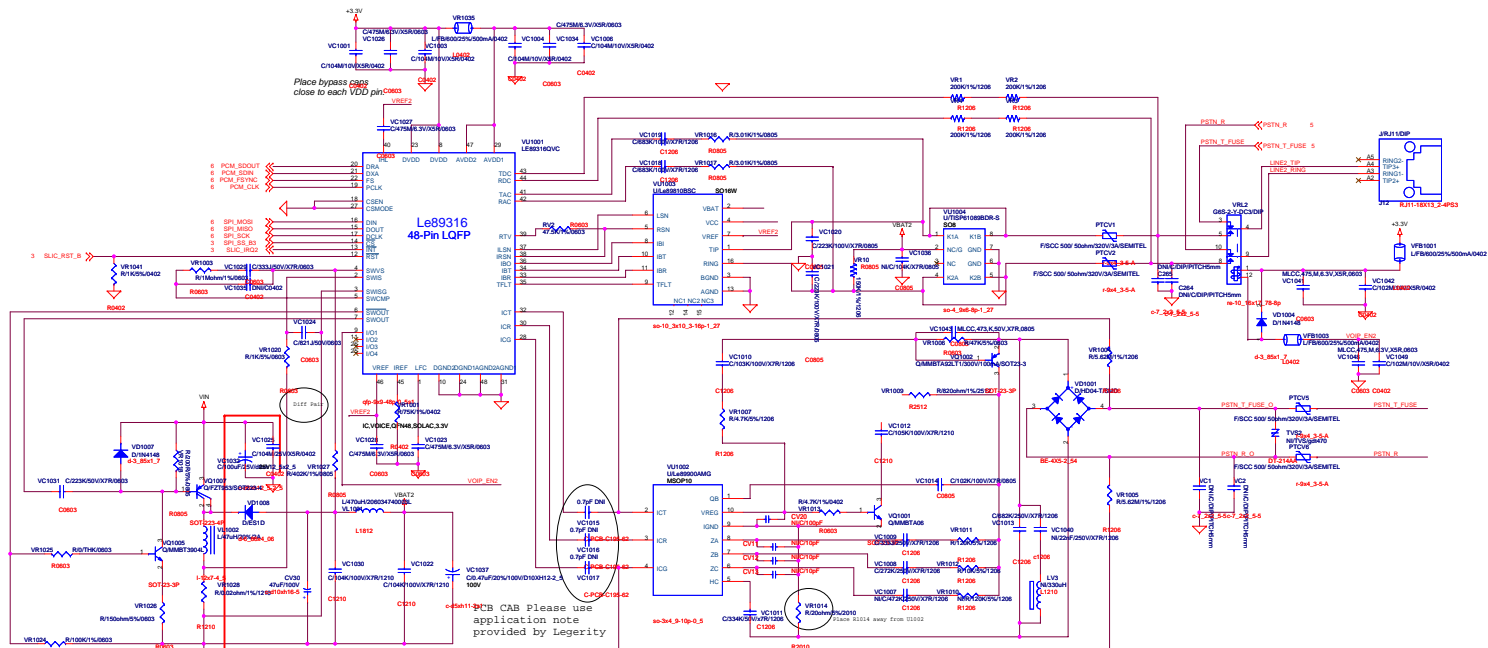




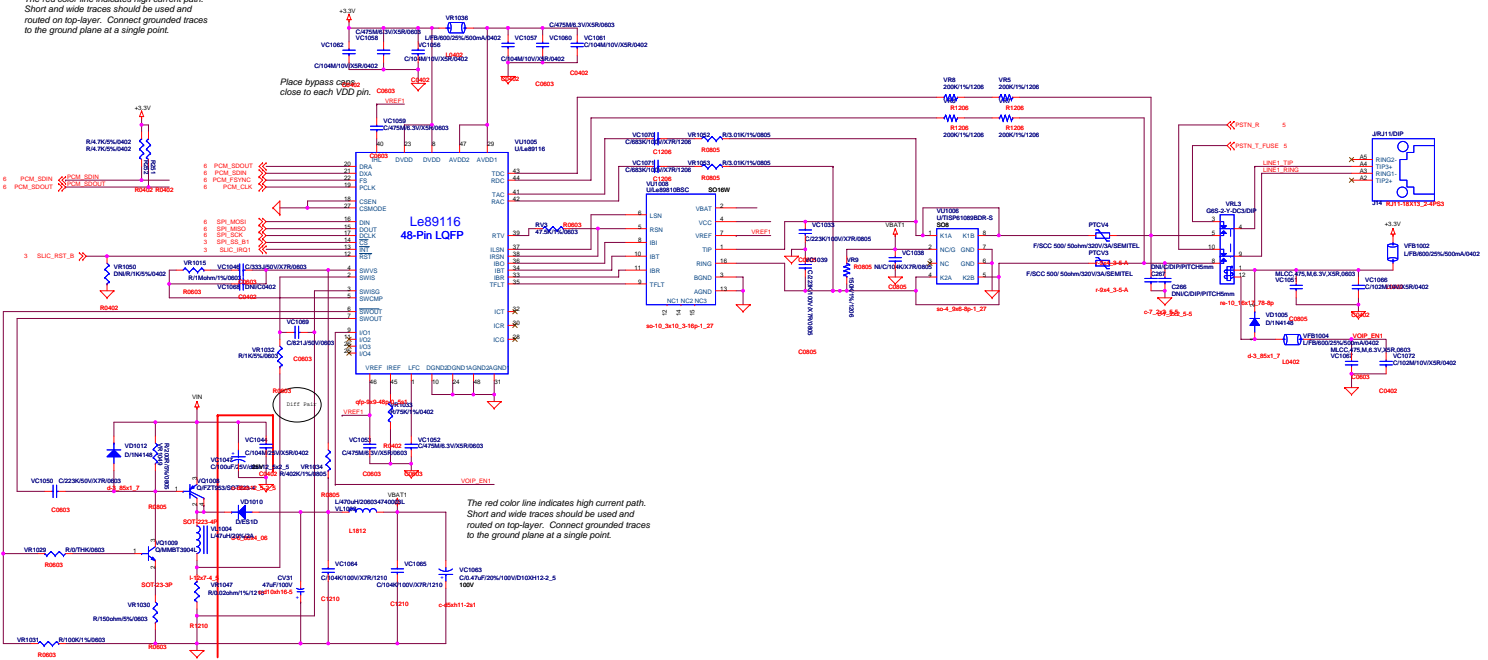
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CONNECT VIDEO_GM1 TO 3.3V WHEN USED IN GM1_M0 OR MAND MODE
 CONNECT VIDEO_GM1 TO 2.5V WHEN USED IN RGMI MODE

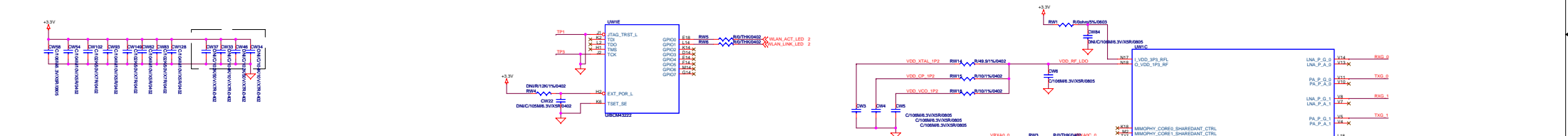
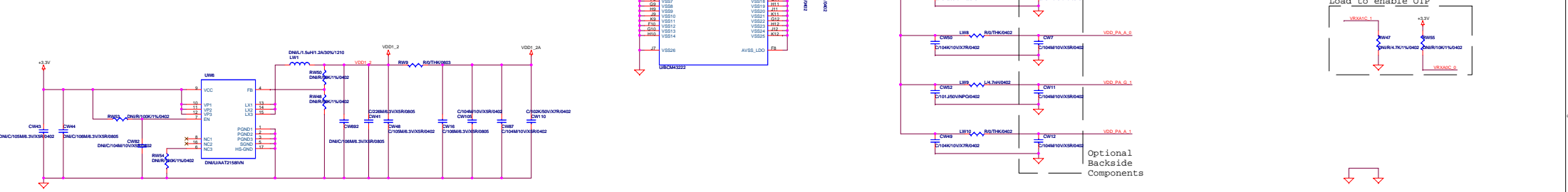
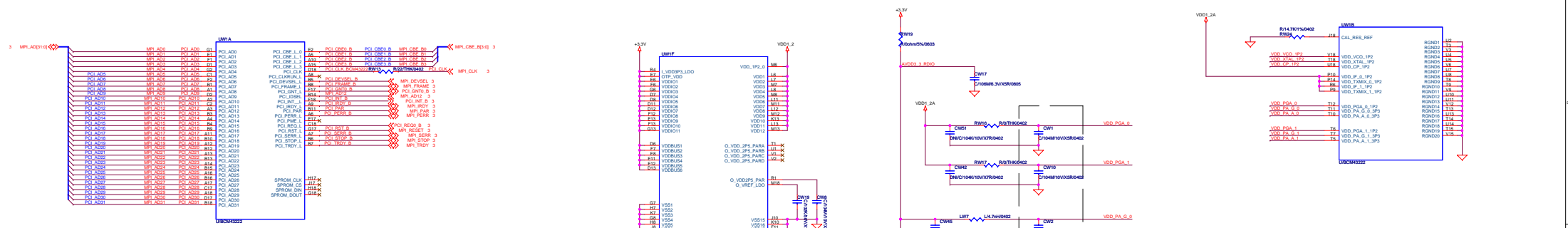




The red color line indicates high current path. Short and wide traces should be used and routed on top-layer. Connect grounded traces to the ground plane at a single point.



The red color line indicates high current path. Short and wide traces should be used and routed on top-layer. Connect grounded traces to the ground plane at a single point.



ANTENNA A0

ANTENNA A1