1 Description of Functional Blocks

1.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of –band blocking specification at the Low Noise Amplifier (LNA) input allows their radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitized. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore2-External to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

1.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-External to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

1.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments.

1.2 RF Transmitter

1.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimize the frequency drift during a transmit timeslot which results in a controlled modulation index. A digital base band transmit filter provides the required spectral shaping.

1.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore2-External to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

1.3 RF synthesizer

The radio synthesizer is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes or LC resonators.

1.4 Base band and Logic

1.4.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data, which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by hardware MMU to minimize the overheads on the processor during data/voice transfers.

1.4.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet form header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimizes the intervention required by the processor during transmission and reception.

1.4.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/ μ -law/linear voice date(from host)
- A-law/ μ -law/Continuously Variable Slope Delta(CVSD)(over the air)
- Voice interpolation for lost packets
- Rate mismatches

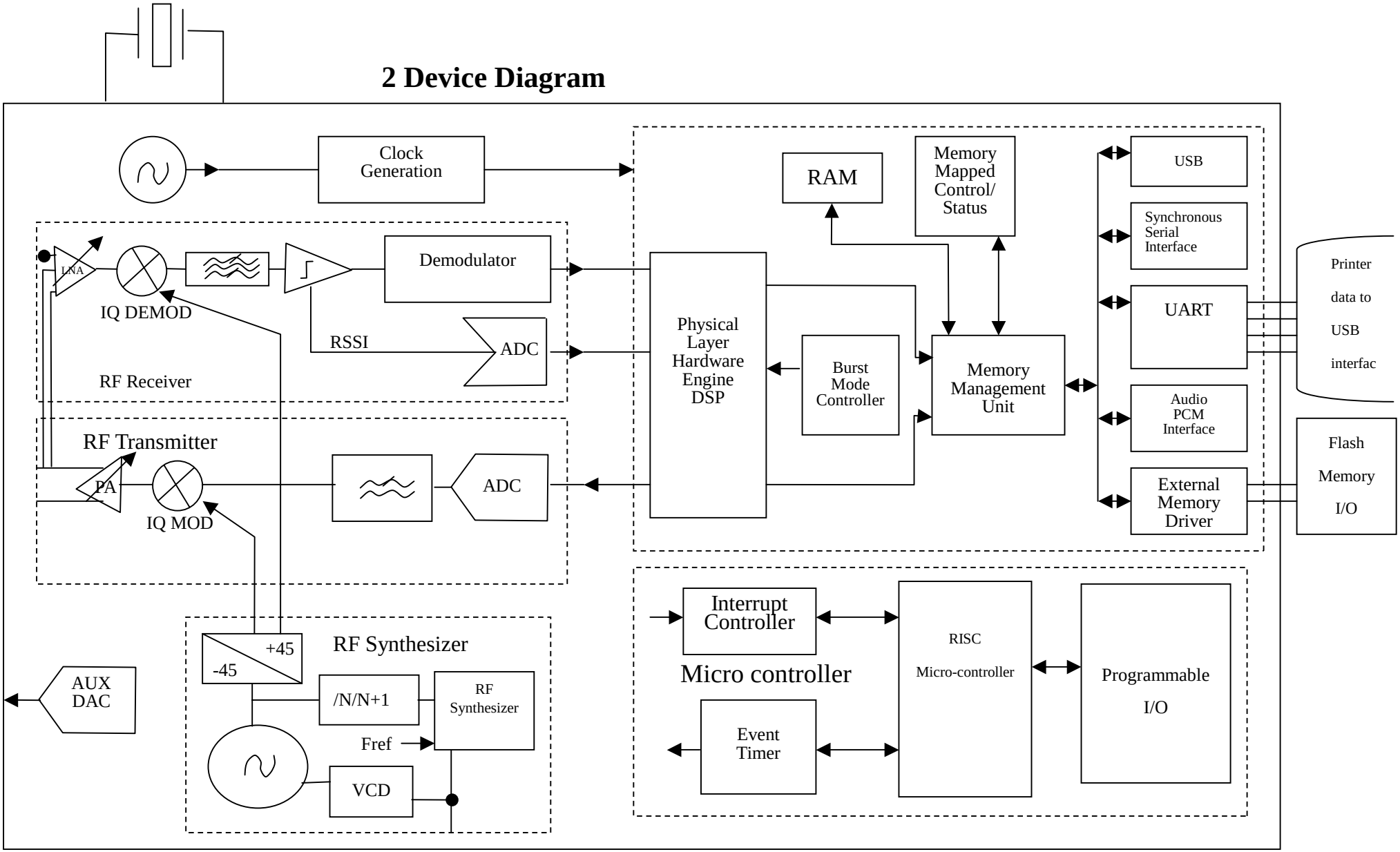
1.4.4 RAM

32Kbytes of on-chip RAM is provided and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

1.4.5 External Memory Driver

The External Memory Driver interface can be used to connect to the external Flash memory and also to the optional external RAM for memory intensive applications.

2 Device Diagram



3 Device Terminal Descriptions

3.1 RF Parts

The BlueCore2-External RF_IN terminal can be configured as either a single-ended or differential input. The operational mode is determined by setting the Persistent Store Key PSKEY_TXRX_PIO_CONTROL (0x209). Using a single-ended RF input to be used for Class 1 operation, as shown in figure3.1.

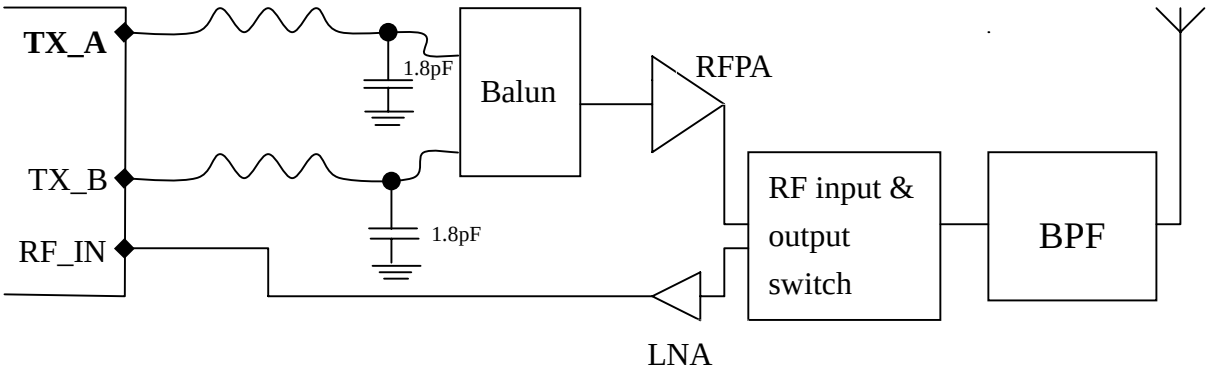


Figure 3.1: RF Parts (Class1)

1. Scope

The BT-PA02A is a low power and high performance communication product which allows laptop PCs and other devices to print data to Printer.
It is especially well-suited for wireless printing, but also can used for general-purpose wireless replacement. The BT-PA02A support Serial Port Profile(Cable Replacement) . This mode allows device that support the bluetooth Serial Port Profile to wirelessly to USB1.1 compliant device. The data is passed unmodified to the receiving device. In this mode, the sending devices look to the software as though they are communicating via a hardwired RS-232 connection. Therefore, the BT-PA02A can be used with any printer that supports printing over the serial port (although the actual physical connection between the BT-PA02A and the printer can be USB interface, the sending device thinks it is communicating to a serial device). With Windows systems, this means that standard printer drivers like the HP LaserJet 930C driver can be used, so no special software needs to be installed on the PC.

2. Block description

ATMEL AT89S52: (in charge of data conversion for serial to parallel)

The AT89S52 is a low-power, high-performance CMOS 8-bit micro-controller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a a versatile 8 bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful micro-controller which provides a highly-flexible and cost effective solution to many embedded control applications.
The AT89S52 provides the following standard features: 8K bytes of Flash, 256bytes of RAM, 32 I/O lines, Watchdog timer, two data pointer, three 16-bit timer/counters, a six-vector two level interrupt architecture, a full duplex serial port, on chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

CYPRESS SL811HS: (In charge of data conversion parallel to USB)

The SL811HS is an Embedded USB Host/Slave Controller capable of communicate with either full-speed USB peripherals The SL811HS can interface to devices such as microprocessors, microcontrollers, DSPs or directly to a variety of buses such as ISA, PCMCIA, and others. The SL811HS USB host controller conforms to USB specification 1.1.

The SL811HS USB Host/Slave Controller incorporates USB serial interface functionality along with internal full-/low speed transceivers. The SL811HS supports and operates in USB full-speed mode at 12 Mbps, or at low-speed 1.5Mbps mode.

The SL811HS data port and microprocessor interface provide an 8-bit data path I/O or DMA bi-directional, with interrupt support to low easy interface to standard microprocessors or microcontrollers such as Motorola or Intel CPUs and many others. Internally, the SL811HS contains a 256-byte RAM data buffer which is used for control registers and data buffer.

DC to DC Converter: (In charge of all the system's power supply)

The DC to DC converter include two parts of power source to supply the system's power. One part of power is converted from 6V to 5V and the others is converted from 5V to 3.3V. This two part of power have low noise and high efficiency.

74HC373: (In charge of address latch)

The main function of 74HC373 is responsible for address latch. When CPU do data transfer, it need two cycle's data phase to complete data transition. One phase is address phase, the others is data phase. If we have no address latch, the address phase will be replaced by the following data phase.

32K bytes SRAM: (In charge of data buffer for conversion)

The 32K bytes SRAM are the buffers for data conversion. When CPU receive the printing data from BT-Module, it store the data in the 32K bytes SRAM. If printer can receive data from PC, the CPU transfer the data from SRAM to SL811HS.

USB Connector:

USB connector is responsible for connection between Printer and BT-PA02A.

6. BT-PA02A Block Diagram