MtW8153 2x3 5GHz MIMO

Wireless Transceiver

Detailed Datasheet

Worldwide Technical Support:

For Technical Support contact information, please visit our web site at:
http://www.mtlk.com

Revision Record Table

Rev	Description of Change	Revision Date	
-	Initial release of detailed datasheet	June 20, 2007	
A	Updates for conditional release	October 3, 2007	
B	Updates for full release	February 28,2008	

Table of Contents

General Description

Overview

The MtW8153 is a fully integrated single chip, triple receiver - dual Transmitter radio frequency integrated circuit (RFIC) designed to support the emerging IEEE 802.11n WLAN standard for MIMO applications. It operates in the 4.9 GHz to 5.9 GHz World Band frequency range (802.11a/n). That is making it compatible with both the new 802.11n and legacy 802.11a standards. By implementing real MIMO technology, the MtW8153 supports Phy rates in excess of 300Mbps and two to eight times extended reach. Additionally, MtW8153 offers true performance scalability to support higher rates and significantly better cost efficiency as compared to multiple-device MIMO RF solutions.

MtW8153 features all the necessary circuitry to form 2x3 MIMO radio frequency (RF) transceiver matrix: Three full receive paths and two full transmit paths, phase locked loop (PLL) synthesizer, receiver and transmitter gain control, receive signal strength indicator (RSSI) and loopback paths for calibration.

MtW8153 employs a Zero-IF, direct-conversion architecture, eliminating the need for external SAW filters by implementing on-chip, tunable baseband filtering. The RSSI enables accurate automatic gain control (AGC) setting as well as best-in-class rejection of interferers.
MtW8153 is fabricated in a mature Silicon Germanium (SiGe) process packed in an 10 x 10 x1 mm, 0.4mm pitch QFN Package (QFN88), and uses a single operating voltage.

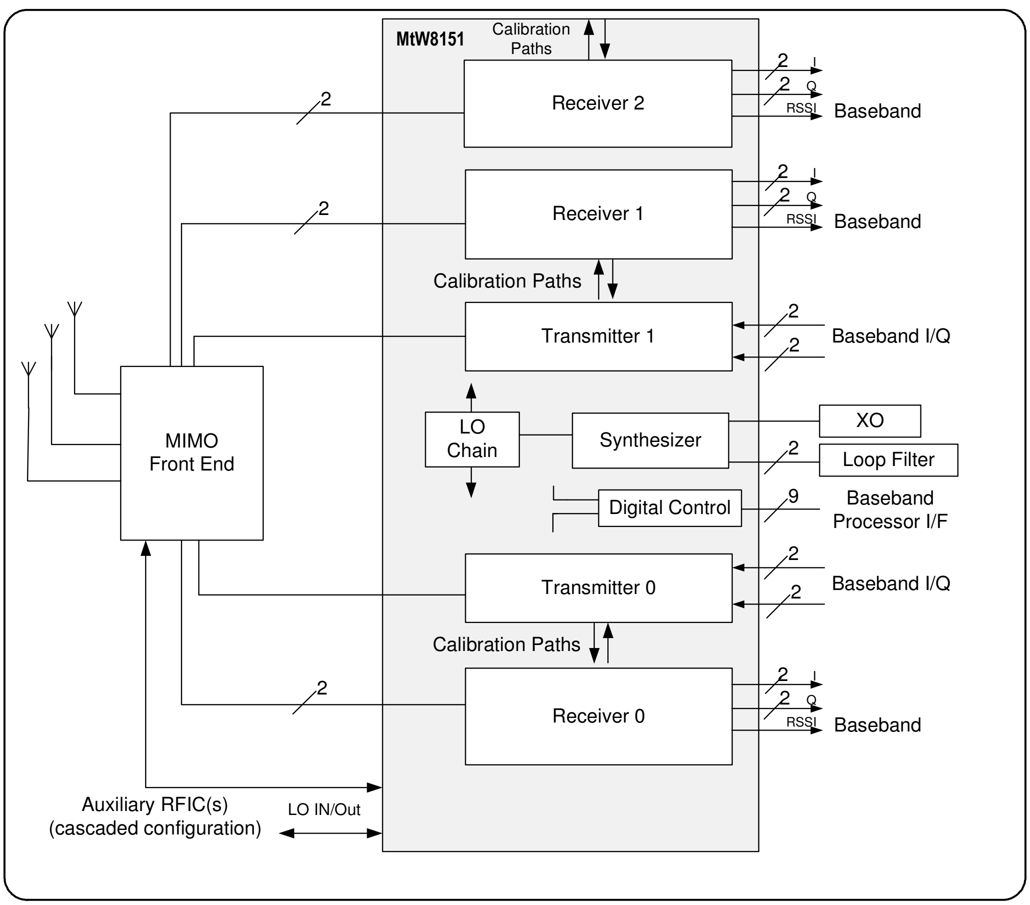


Figure 1: Functional Block Diagram

Key Features

- 2 x 3 real MIMO RFIC for WLAN in a single state-of-the-art chip
- Best-in-class spectrum utilization: two independent data chains enable using spatial multiplexing to receive and transmit separate data streams over the same frequency channel
- 4.9 GHz to 5.9 GHz World-Band operation
- Supports Phy rates in excess of 300Mbps
- Channel bonding: supports both 20MHz channels and 40MHz bonded channels for extended throughput.
- Supports Smart-Antenna techniques such as SDMA (beamforming), STBC, diversity, antenna loading
- Tunable baseband filtering in the receiver
- Receive signal strength indicator (RSSI) enables fast and accurate automatic gain control (AGC) settings and improved interferer rejection
- Fast switching between receive and transmit modes
- Single operating voltage
- 10 x 10 x 1 mm, 0.4mm pitch QFN88 package
- Compliant with IEEE 802.11n and IEEE 802.11a standards
- Supports BPSK, QPSK, 16-QAM and 64-QAM OFDM
- On-chip integrated synthesizer and VCO
- Fast and simple digital control parallel interface
- Zero-IF direct conversion: No external SAW filters required
- Integrated loopback paths for Tx/Rx calibration
- Separate controls for each RF chain
- Mature SiGe process

1 Pinout Descriptions

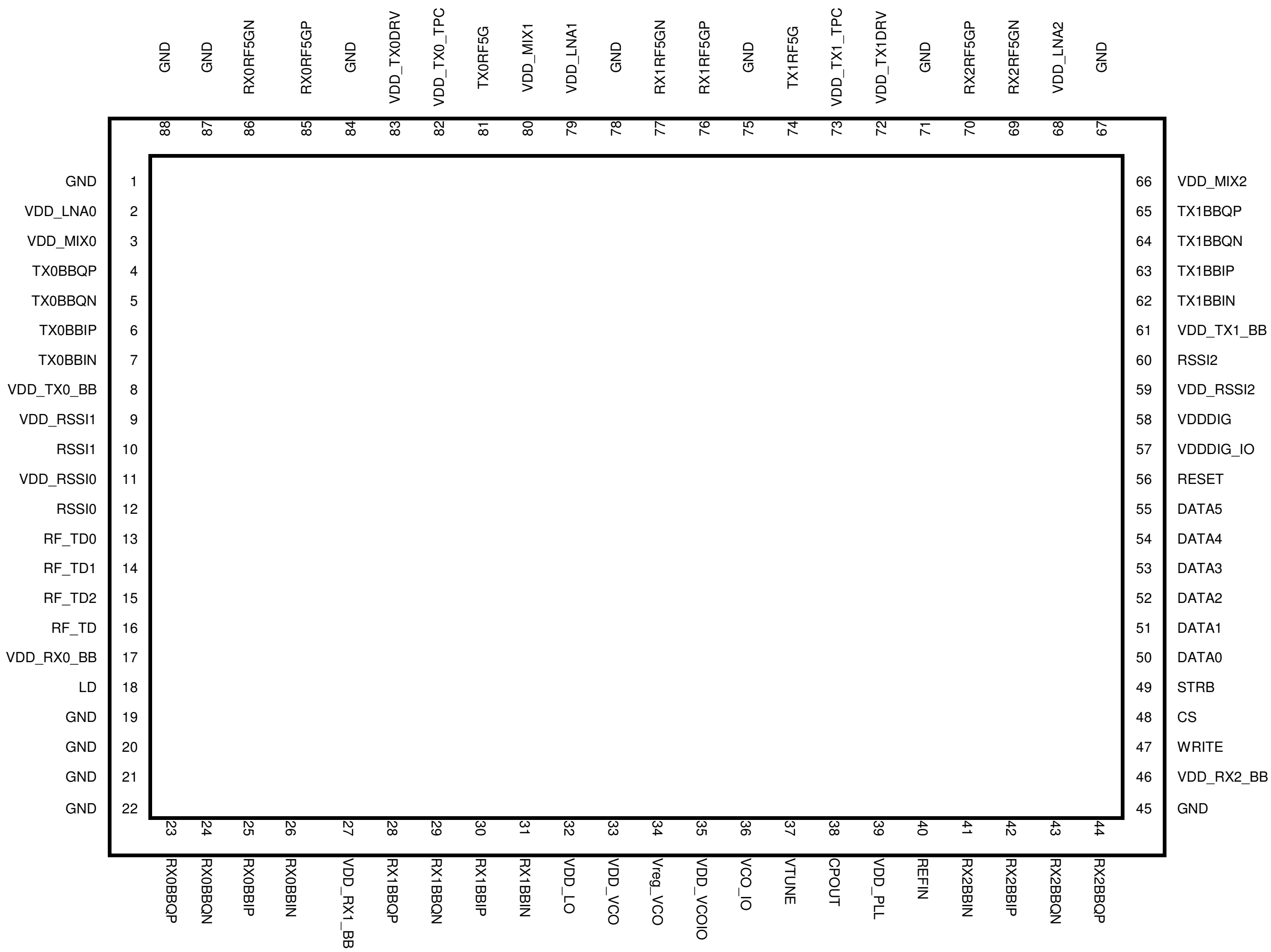


Figure 2 - MtW8153 Pinout Map

Table 1: Pin Descriptions

Pin No.	Name	Type	Description
1	GND	Ground	
2	VDD_LNA0	RF power supply	
3	VDD_MIX0	RF power supply	
4	TX0BBQP	Analog Input	Transmitter 0 base band input Q+
5	TX0BBQN	Analog Input	Transmitter 0 base band input Q-
6	TX0BBIP	Analog input	Transmitter 0 base band input I+
7	TX0BBIN	Analog input	Transmitter 0 base band input I-
8	VDD_TX0_BB	Analog power supply	
9	VDD_RSSI1	Analog power supply	
10	RSSI1	Analog output	Receiver 1 RSSI output
11	VDD_RSSI0	Analog power supply	
12	RSSI0	Analog output	Receiver 0 RSSI output
13	RF_TD0	Digital output	For future use
14	RF_TD1	Digital output	For future use
15	RF_TD2	Digital output	For future use
16	RF_TD	Digital output	For future use
17	VDD_RX0_BB	Analog power supply	
18	LD	Digital output	Lock Detect
19	GND	Ground	
20	GND	Ground	
21	GND	Ground	
22	GND	Ground	
23	RX0BBQP	Analog output	Receiver 0 base band output Q+
24	RX0BBQN	Analog output	Receiver 0 base band output Q-
25	RX0BBIP	Analog output	Receiver 0 base band output I+
26	RX0BBIN	Analog output	Receiver 0 base band output I-
27	VDD_RX1_BB	Analog power supply	
28	RX1BBQP	Analog output	Receiver 1 base band output Q+
29	RX1BBQN	Analog output	Receiver 1 base band output Q-
30	RX1BBIP	Analog output	Receiver 1 base band output I+
31	RX1BBIN	Analog output	Receiver 1 base band output I-
32	VDD_LO	RF power supply	
33	VDD_VCO	RF power supply	
34	VREG_VCO	RF power supply	VCO 2.4V power supply. Can either come from Internal

Pin No.	Name	Type	Description
			regulator (connect bypass capacitor to this pin) or from external 2.4V regulator
35	VDD_VCOIO	RF power supply	
36	VCO_IO	RF bidirectional	VCO auxiliary input/output
37	VTUNE	Analog input	PLL frequency control voltage, connect to loop filter output.
38	CPOUT	Analog output	PLL Charge pump output connect to loop filter input
39	VDD_PLL	RF power supply	
40	REFIN	Analog input	40MHz eeference clock input
41	RX2BBIN	Analog output	Receiver 1 base band output I-
42	RX2BBIP	Analog output	Receiver 1 base band output I+
43	RX2BBQN	Analog output	Receiver 1 base band output Q-
44	RX2BBQP	Analog output	Receiver 1 base band output Q+
45	GND	Ground	
46	VDD_RX2_BB	Analog power supply	
47	WRITE	Digital input	Parallel control interface write/read
48	CS	Digital input	Parallel control interface chip select
49	STRB	Digital input	Parallel control interface strobe
50	DATA0	Digital I/O	Parallel control interface data bus
51	DATA1	Digital I/O	Parallel control interface data bus
52	DATA2	Digital I/O	Parallel control interface data bus
53	DATA3	Digital I/O	Parallel control interface data bus
54	DATA4	Digital I/O	Parallel control interface data bus
55	DATA5	Digital I/O	Parallel control interface data bus
56	RESET	Digital Input	Reset input
57	VDDDIG_IO	Digital power supply	
58	VDDDIG	Digital power supply	
59	VDD_RSSI2	Analog power supply	
60	RSSI2	Analog output	Receiver 2 RSSI output
61	VDD_TX1_BB	Analog power supply	
62	TX1BBIN	Analog input	TX0 base band input I-
63	TX1BBIP	Analog input	TX0 base band input I+
64	TX1BBQN	Analog input	TX0 base band input Q-
65	TX1BBQP	Analog input	TX0 base band input Q+
66	VDD_MIX2	RF power supply	
67	GND	RF input	Ground
68	VDD_LNA2	RF power supply	

Pin No.	Name	Type	Description
69	RX2RF5GN	RF input	Receiver 2 5GHz differential negative input
70	RX2RF5GP	RF input	Receiver 2 5GHz differential positive input
71	GND	RF output	Ground
72	VDD_TX1DRV	RF power supply	
73	VDD_TX1_TPC	RF power supply	
74	TX1RF5G	RF output	Transmitter 1 5GHz single ended output
75	GND	Ground	
76	RX1RF5GP	RF input	Receiver 1 5GHz differential positive input
77	RX1RF5GN	RF input	Receiver 1 5GHz differential negative input
78	GND	Ground	
79	VDD_LNA1	RF power supply	
80	VDD_MIX1	RF power supply	
81	TX0RF5G	RF output	Transmitter 0 5GHz single ended output
82	VDD_TX0_TPC	RF power supply	
83	VDD_TX0DRV	RF power supply	
84	GND	RF output	Ground
85	RX0RF5GP	RF input	Receiver 0 5GHz differential positive input
86	RX0RF5GN	RF input	Receiver 0 5GHz differential negative input
87	GND	RF input	Ground
88	GND	Ground	

2 Electrical specifications

2.1 Absolute Maximum Ratings

Stress levels beyond the figures listed below may cause permanent damage to the device.

Parameters	Conditions	Units	Min	Typ	Max
Supply Voltage	Pins to GND	V	-0.2		+4.0
Digital I/O	Pins to GND	V	-0.2		V_{cc}+0.2V
Analog I/O	Pins to GND	V	-0.2		V_{cc}+0.2V
RF Input Power		dBm			+10
Storage Ambient Temperature		ºC	-40		125

Table 2 – Absolute Maximum Ratings

This circuit can be damaged by ESD. It is recommended that you take appropriate precautions when handling all integrated circuits. Failure to observe proper handling procedures may result in ESD damage which ranges from subtle performance degradation to complete device failure. Precision integrated circuits are more susceptible to ESD damage because very small parametric changes can cause the device not to meet its published specifications.

2.2 Operating Conditions[1]

The typical current consumption is based on a typical RFIC at Ta=25ºC

Parameters	Conditions	Units	Min	Typ	Max
Operating, DC Electrical Requirements					
Supply Voltage		V	2.8	3.0	3.6
Current Consumption	Transmit	mA		320	390
	Receive[2]			305	355
	RSSI			50	60
	Standby			50	
	Power-Down			1	

Table 3 - Operating Conditions

2.3 Thermal Conditions

Parameters	Conditions	Units	Min	Typ	Max
Ta	Operating Ambient Temperature[3]	ºC	0		85
Tj	Junction Temperature	ºC	0		125
Θ Ja	Junction-to-ambient Thermal Resistance parameter[4]	ºC/W	15.9		
ΨJt	Junction-to-top-center Thermal Characteristic parameter[5]	ºC/W	0.2		

Table 4 - Thermal Conditions

1 Worst case specifications trough the datasheet are based on the power supply range as described in table 3 and Ta=0 ºC to 85ºC ambient.

2 Not including RSSI current, which is active only for AGC purpose

3 Ambient temperature as defined by JESD51-2, is the natural convection air (still air).

4 Junction to ambient thermal resistance parameter is defined by JESD51-5 using a 76.2x114.3mm PCB, 2ps2, 1.6mm thick.

5 Thermal characterization parameter as defined by JESD51-2, and can be used to estimate the junction temperature in an actual environment using: ψjt = (Tj – Ttop)/P, Ttop = temperature on top center of the package, P = total power dissipation.

3 Receiver Specifications

Typical conditions (unless otherwise specified): Vcc=3.0v, baseband output signal: 65mV rms OFDM 64QAM, T_A=25°.

Parameters Receiver RF Input to	Conditions Baseband I/Q Outputs	Units	Min	Typ	Max
Receive Chains	Full chains, Zero-IF, RF to baseband		3		
RF Input Frequency Range	Full range	GHz	4.9-5.9		
Noise Figure	Max Gain	dB		5.5	
Maximum receive signal	Min Gain, EVM=28dB	dBm		-16	
Ultimate EVM	With Optimal Gain Setting and I/Q mismatch calibration	dB		-34.5	-33

Table 5 - Receiver Specifications

4 Transmitter Specifications

Typical conditions (unless otherwise specified): Vcc=3.0v, ,baseband input signal: 54mV rms OFDM 64QAM, T_A=25°.

Parameters	Conditions	Units	Min	Typ	Max
Transmit Chains	Full chains, baseband to RF		2		
RF Output Frequency Range	Full Range	GHz	4.9 to 5.9		
Nominal Output Power	Calibrated	dBm		-5	
Ultimate EVM	At nominal transmit power	dB		-35	-32
TPC Range	For 1dB steps	dB		11	
TPC Step		dB		0.5	1
Output 1dB Compression Point	CW Signal	dBm	4.5	8	

Table 6–Transmitter Specifications

5 Synthesizer Specifications

Typical conditions (unless otherwise specified): Vcc=3.0v, baseband input signal: 65mV rms OFDM 64QAM, T_A=25°.

Parameters	Conditions	Unit	Min	Typ	Max
Frequency Synthesizer and LO Generation					
RF Channel Center Frequency		GHz	4.9 to 5.9		
Frequency raster		MHz	5		20
Integrated Phase Noise	10KHz to 10MHz	ºRMS		0.7	

Table 7 - Synthesizer Specifications

Reference Clock					
Reference Input Frequency		MHz		40	
Reference clock input Low level		V_L		0.3	1.2
Reference clock input High level		V_H	2.2	2.2	

Table 8– Reference clock

6 Timing Specifications

Typical conditions (unless otherwise specified): Vcc=3.0v, , baseband input signal: 65mV rms OFDM 64QAM, T_A=25°.

Parameters	Conditions	Unit	Min	Typ	Max
Digital Interface Timing					
Data bus turnaround	Digital Read cycle, Input to Output	ns		2	
	Digital Read cycle, Output to Input	ns		2	
Rise/Fall Time	Digital Read cycle	ns		1	
AGC Timing					
AGC Gain Change	Any gain step	ns		120	
RSSI Response Time	20dB power step, OFDM signal	ns		150	
Mode Switching					
Switching between TX and RX		ns		285	
Switching between RX and TX		ns		285	
Switching between RX Listen and RX		ns		250	
Switching from Standby to RX		ns		375	
Switching from Standby to TX		ns		245	
Switching from RX or TX to Standby		ns		50	
Switching from Power Down to Standby	Includes PLL lock time	µs		350	
Switching from Standby to Power Down		µs		50	

Table 9 - Timing Specifications

7 Theory of operation

7.1 Overview

The MtW8153 consists of three RF receivers and two RF transmitters that support a 2 x 3 MIMO configuration. Designed for scalability, two or more MtW8153 components can be cascaded to establish a higher rank MIMO.

Each receiver and transmitter can work in either the 4.9-5.9 GHz band or in the 2.4-2.5GHz band.

Fast switching between receive and transmit modes, and receiver or transmitter gain control are achieved using a fast parallel interface. The interface is bi-directional to allow both read and write functionality. The RFIC is fully flexible and allows separate controls of each RF chain and the blocks within it.

7.2 Receive Path

Each MtW8153 receive path consists of a programmable-gain LNA, a pair of I & Q demodulating mixers, fully integrated baseband filters, and a set of programmable-gain amplifiers for automatic gain control.

Each receive path has an independent fast-settling gain setting to accommodate MIMO operation with the different input levels received from the antennas. The three receive antennas can also be used to perform maximum ratio combining (MRC), improving performance for modems supporting this functionality.

A base band Received Signal Strength Indication (RSSI) provides wide-band signal detection to the baseband chip, improving interferer rejection. Loopback paths are provided for I/Q calibration of the chip.

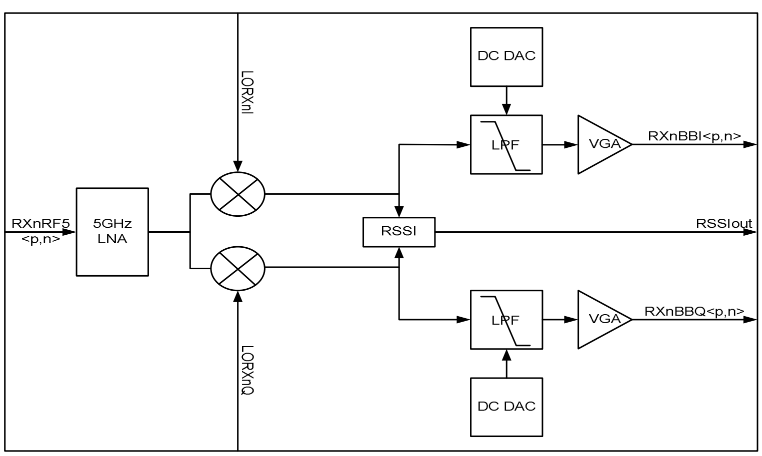


Figure 3 – Receiver block diagram

7.3 Transmit Path

The transmit path includes baseband filters, an I & Q modulator and a programmable-gain power amplifier driver. The baseband filters support both 20MHz channels and 40MHz channel bonding for extended throughput. Superior EVM performance allows support of modulation schemes and MIMO techniques: BPSK, QPSK, 16 QAM and 64QAM OFDM.

Each chain has a separate control of the transmitted power control (TPC) through the parallel interface bus.

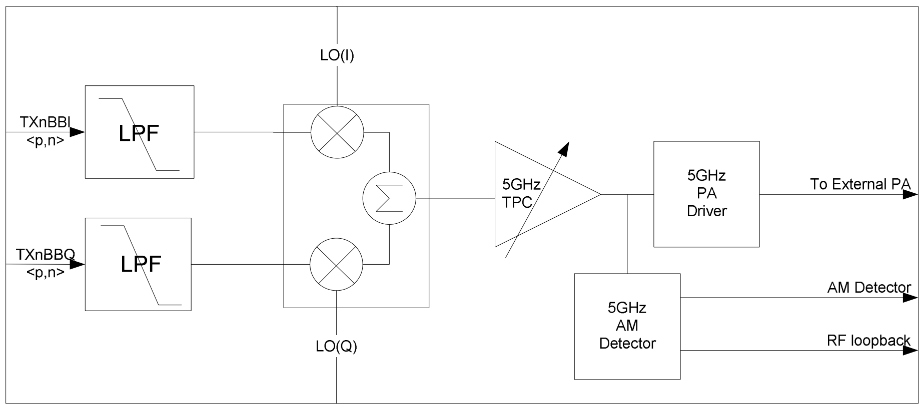


Figure 4 – Transmitter block diagram

7.4 Calibration Circuits

Several calibration circuits are available on-chip, enabling optimum transceiver operation. Imbalance between the I and Q branches is measured and compensated for in a frequency-dependent or constant manner, for each transmitter or receiver.

7.5 Power Modes

Both standby and power-down power-saving modes are available. In power down mode, the MtW8153 is completely shut down except for the digital interface and the reference oscillator. In standby mode, only the on-chip synthesizer is active, enabling minimum power consumption while providing fast response. Transition from this mode to transmit or receive modes takes less than 1µsec.

7.6 Digital Interface

The MtW8153 RFIC employs a parallel interface, which enables fast communication with the chip. This real-time communication is used for fast AGC, TPC, T/R and internal register settings. The interface is asynchronous, with a 6-bit address and 12-bit data bus width. It provides both read and write functionality, at a maximum speed of 60MHz (50ns per access).

The control interface uses nine pins to implement the link:

- Six bi-directional Address/Data bits (DATA0 to DATA5)
- One Write/Read Signal (WR)

- One Interface Strobe (STRB)
- One Chip Select/Enable masking control (CS)

To ensure synchronicity, CS must remain at logical ‘0’ for a duration of 8ns between digital accesses (read or write) to the same RFIC. Multiple RFICs can be controlled using the same bus, requiring only a separate CS line to select the destination RFIC.

A “burst mode” is available for faster control of sets of registers. This feature can be used for fast setting of the gain registers.

7.6.1 Write Cycle Timing and Operation

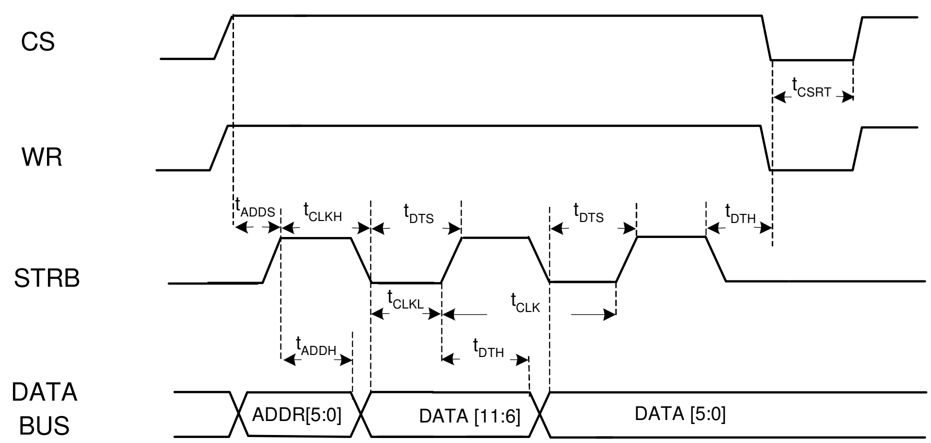


Figure 5 - Digital Interface Write Cycle Timing

7.6.2 Read Cycle Timing and Operation

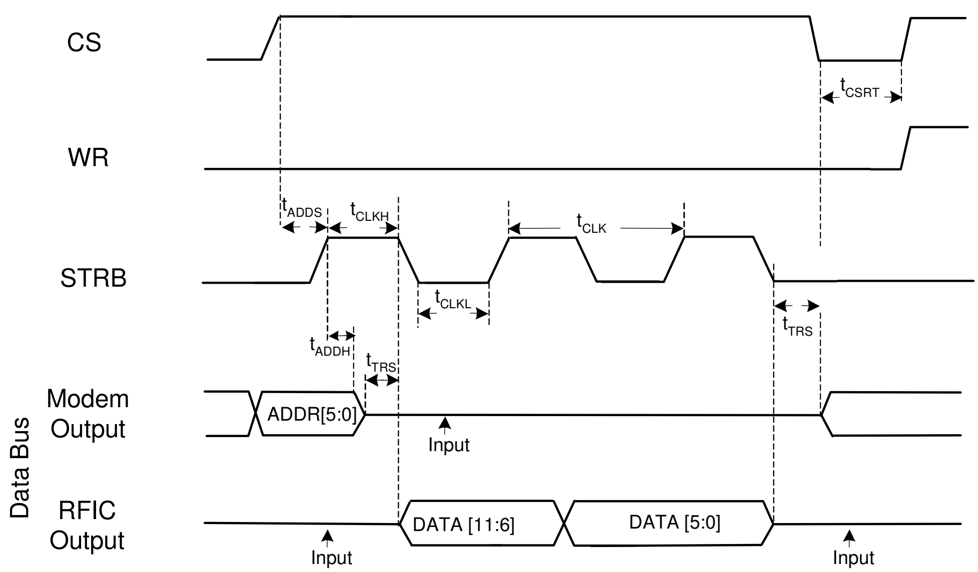


Figure 6 - Digital Interface Read Cycle Timing

In order to prevent collisions, a minimum gap of 4ns is required before the STRB transition to '0', in which the Modem IC must set the data bus I/O pins to their input state.

7.6.3 Digital Interface Timing constraints

Designator	Parameter	Unit	Min	Typ	Max
Read/Write Access Cycle					
t_{CLK}	STRB Cycle Period	ns	16.6		
t_{CLKL}	STRB 'Low' Time	ns	7.5		
t_{CLKH}	STRB 'High' Time	ns	7.5		
t_{ADDS}	Address Setup Time	ns	4.0		
t_{ADDH}	Address Hold Time	ns	4.0		
t_{DTS}	Data Setup Time	ns	4.0		
t_{DTH}	Data Hold Time	ns	4.0		
t_{CSRT}	CS Access Recovery Time	ns	8.0		
t_{TRS}	Collision Avoidance time	ns	4.0		

Table 10 – Timing constraints

8 Typical peripherial circuits

8.1 RF input

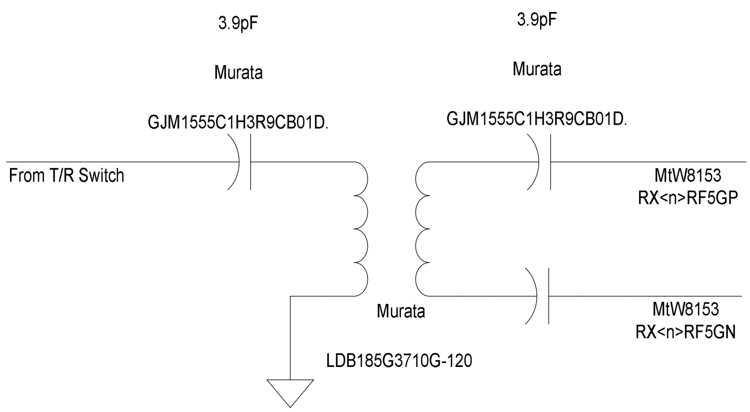


Figure 7 – RF input

8.2 PLL loop filter

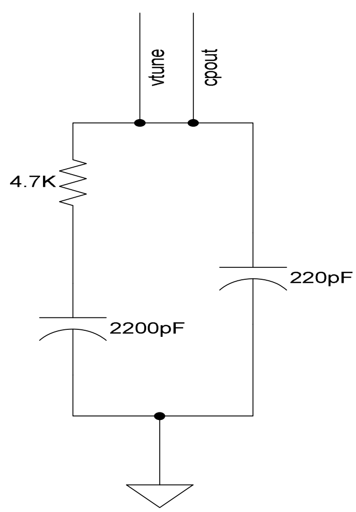
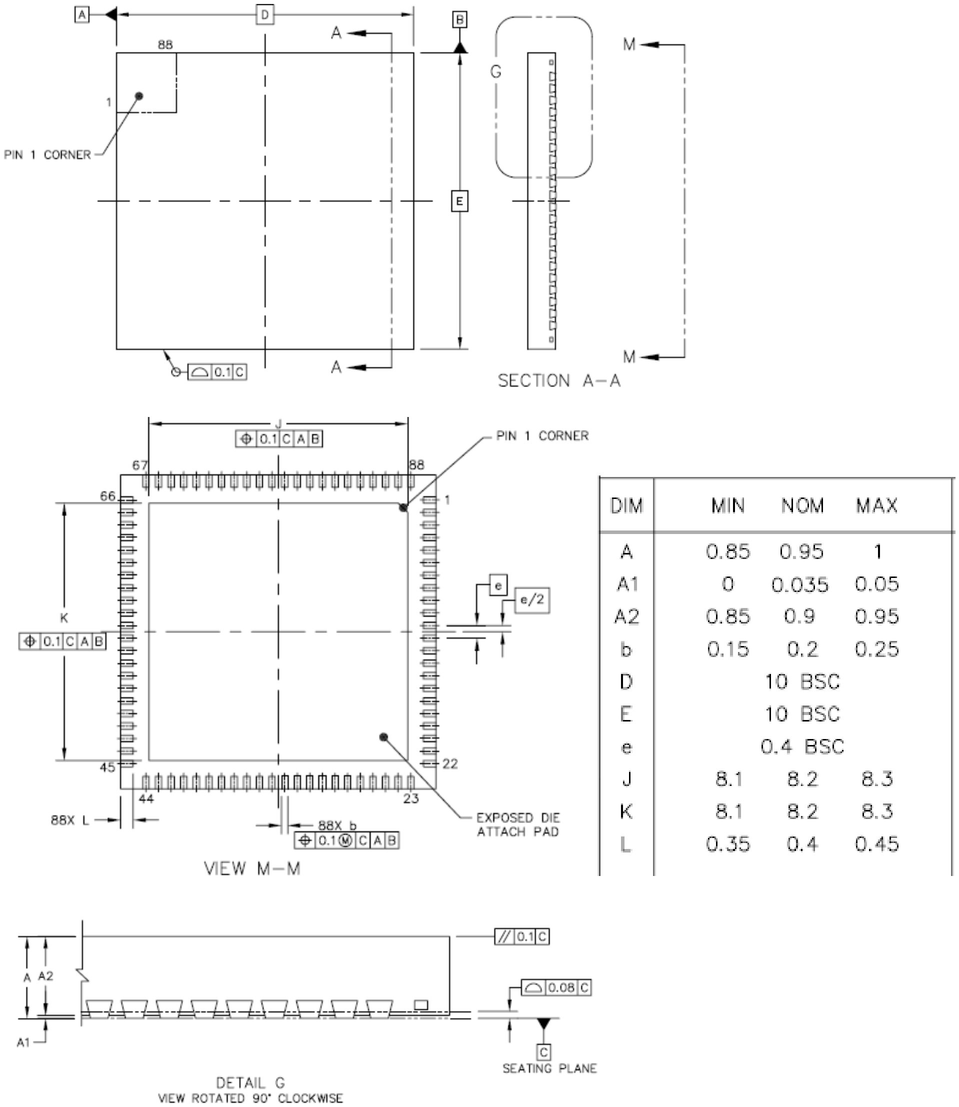


Figure 8 – Loop filter

8.3 Package Outline Drawing

The package is a 88 leads QFN, 10x10x1, 0.4mm pitch.

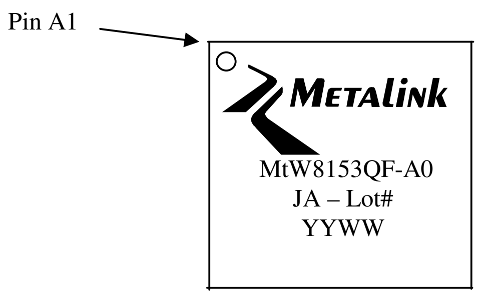


DIM	MIN	NOM	MAX
A	0.85	0.95	1
A1	0	0.035	0.05
A2	0.85	0.9	0.95
b	0.15	0.2	0.25
D		10 BSC	
E		10 BSC	
e		0.4 BSC	
J	8.1	8.2	8.3
K	8.1	8.2	8.3
L	0.35	0.4	0.45

Figure 9: Package Information

8.4 Marking Information

The following diagram illustrates the actual markings on the MtW8153 IC. The location of the marking is not drawn to scale.



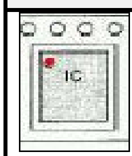
MtW8153QF-A0	Part number, package code, device version
Lot# =	refers to the package manufacturer lot schedule
YY =	Last 2 digits of current year
WW =	Mold work week

9 Ordering Information

The following table lists the pertinent information required to order the MtW8153 chip.

Marking on the Chip	Functionality Description	Ordering Information/ Part Number	Package Type	Ordering Quantities
MtW8153QF-A0	2x3 MIMO RFIC	MtW8153QF-A0	QFN 10X10X1mm, 0.4mm Pitch, 88 pin package.	Sample orders - multiples of 10 units (tray) production orders - multiples of 1000 units (T/R)

The following table lists the Tape and Reel information.

Pin 1 Orientation	Trailer (empty pocket of inner reel)	Trailer (empty pocket of outer reel)	Reel Dimensions (width, pitch)	Wheel Diameter
 Left Up	15	25	24x16mm	180mm

Note:	Ordering information is subject to change. Please contact Metalink for the most updated ordering information table and to confirm that you are in possession of the latest datasheet revision that corresponds to your specific chip.

Note:	Please contact Metalink to confirm that you are in possession of the latest datasheet revision that corresponds to your specific chip revision letter.