

# Vocoder and Controller Boards Detailed Theory of Operation

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### Introduction to This Section

This section of the manual provides a detailed circuit description of the ASTRO Digital XTS 3000 vocoder and controller boards. When reading the theory of operation, refer to your appropriate schematic and component location diagrams located in the back section of this manual. This detailed theory of operation will help isolate the problem to a particular component.

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### General

The controller board is the central interface among the various subsystems of the radio. It is very similar to the digital logic portion of the controllers on many existing Motorola radios. Its main task is to interpret user input, provide user feedback, and schedule events in the radio operation, and includes programming ICs, steering the activities of the DSP, and driving the display.

The vocoder board performs the functions which were previously performed by analog circuitry. This includes all tone signaling, trunking signalling, conventional analog voice, etc. All analog signal processing is done digitally utilizing a DSP56001. In addition, the vocoder board provides a digital voice-plus-data capability, utilizing VSELP or IMBE voice compression algorithms. Vocoder is a general term used to refer to these DSP based systems and is short for voice encoder.

The vocoder and controller boards are connected through a 50-pin compression connector; they provide interconnection among the microcontrol unit (MCU), the DSP, and (on secure-equipped radios) the encryption board.

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### Vocoder Board

Refer to Figure 6 and the appropriate schematic diagram.

The vocoder board consists of a digital signal processor (DSP — U405), 32k x24 static-RAM (SRAMs — U401, U402, and U403), a 256kB FLASH ROM (U404), and an ABACUS/DSP support IC (ADSIC — U406).

The FLASH ROM (U404) contains the program code executed by the DSP. As with the FLASH ROM used on the controller board, the FLASH ROM is reprogrammable, so new features and algorithms can be updated in the field as they become available. Depending on the mode and operation of the DSP, corresponding program code is moved from the FLASH ROM into the faster SRAM, where it is executed at full bus rate.

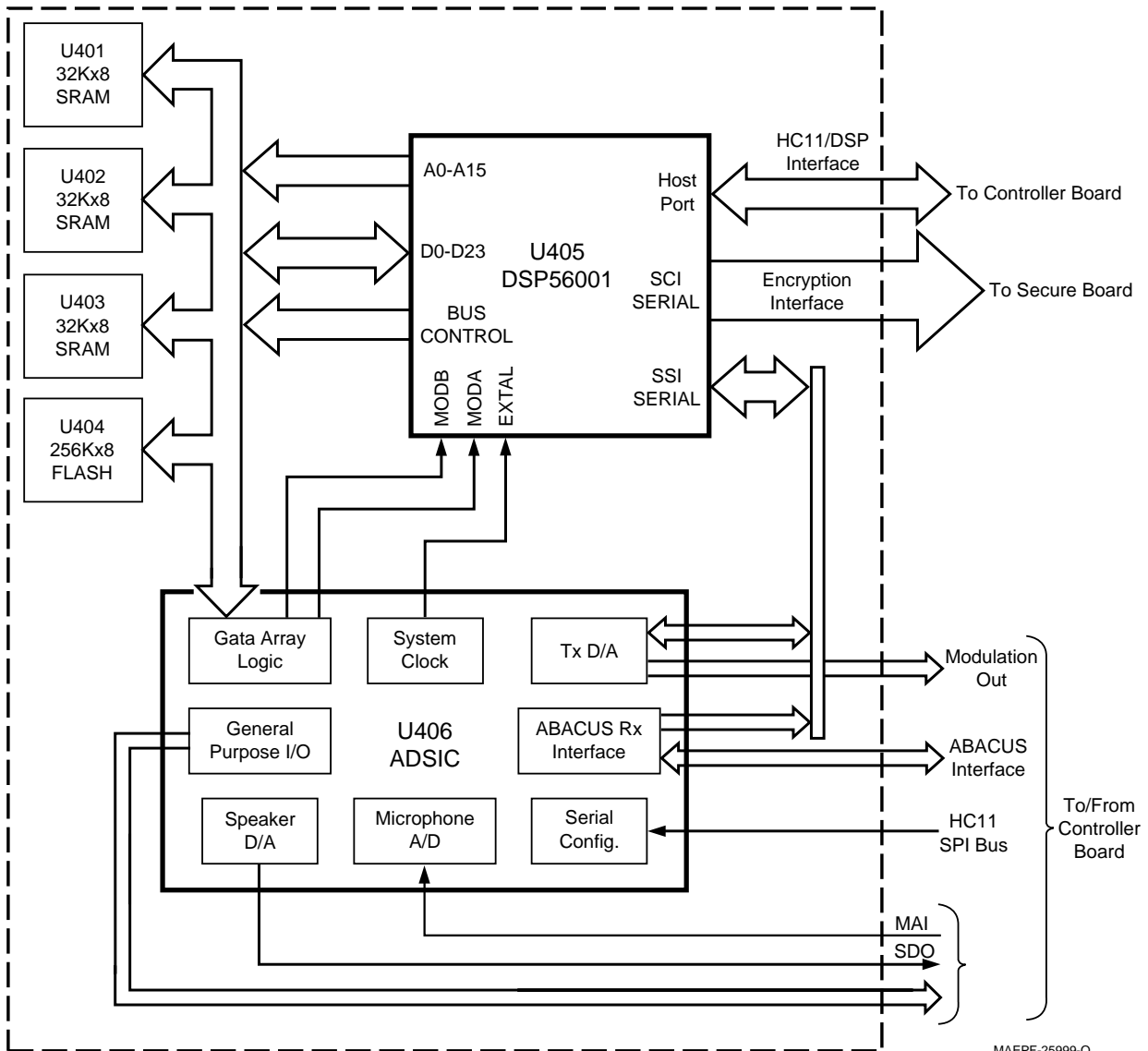


Figure 6 Vocoder Board

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The ADSIC (U406) is basically a support IC for the DSP. It provides, among other things, the interface from the digital world of the DSP to the analog world. The ADSIC also provides interrupt control for the DSP processing algorithms and some memory management. The configuration programming of the ADSIC is performed by the MCU. However, some components of the ADSIC are controlled through a parallel memory mapped register bank by the DSP.

In the receive mode, The ADSIC (U406) acts as an interface with the ABACUS IC, which can provide IF data samples directly to the DSP for processing. Or, the IF data can be filtered and discriminated by the ADSIC and data provided to the DSP as raw discriminator sample data. The latter mode, with the ADSIC performing the IF filtering and discrimination, is the typical mode of operation.

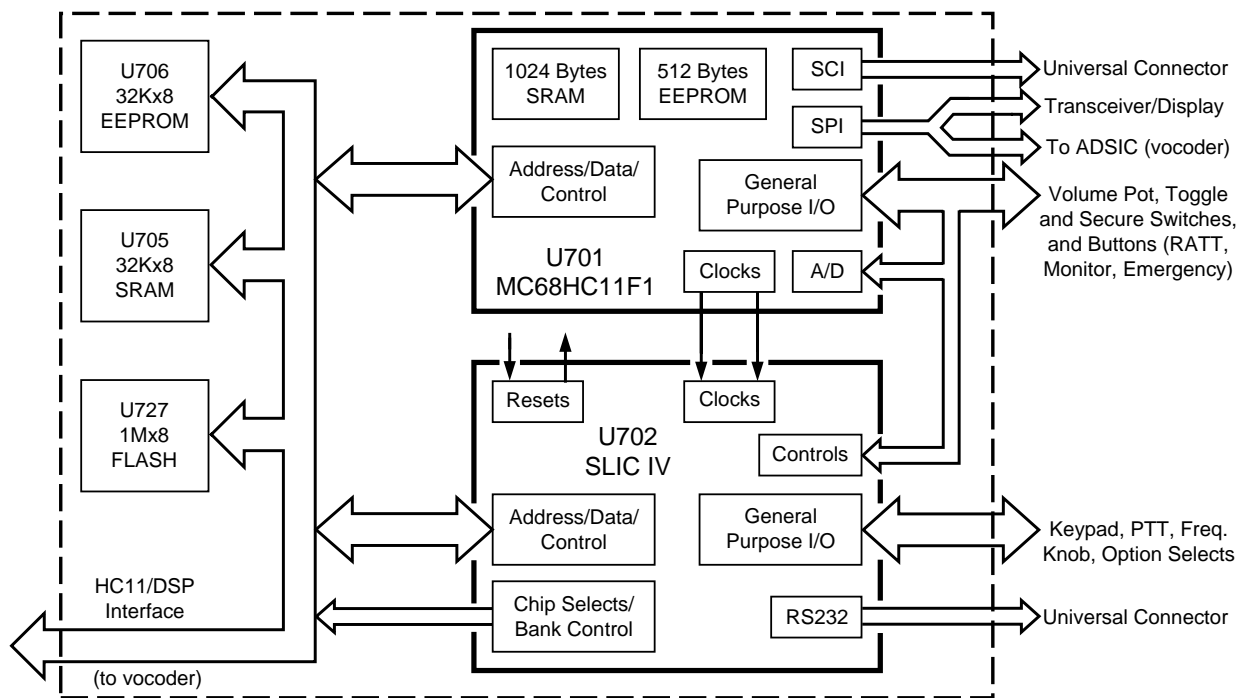
The DSP sends the processed signal back to the ADSIC for D/A conversion. The result is then sent to the audio PA for the speaker output.

In the transmit mode, the ADSIC (U406) provides a serial digital-to-analog (D/A) converter. The data generated by the DSP is filtered and reconstructed as an analog signal, and sent to the VCO as a modulation signal. Both the transmit and receive data paths between the DSP and ADSIC are through the DSP SSI port.

The amplified microphone signal is provided to the ADSIC, which incorporates an analog-to-digital (A/D) converter to translate the analog waveform to a series of data. The data is available to the DSP through the ADSIC parallel registers. In the converse way, the DSP writes speaker data samples to a D/A in the ADSIC, which provides an analog speaker audio signal to the audio PA.

## Controller Board

Refer to Figure 7 and the appropriate schematic diagram



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Figure 7 Controller Board

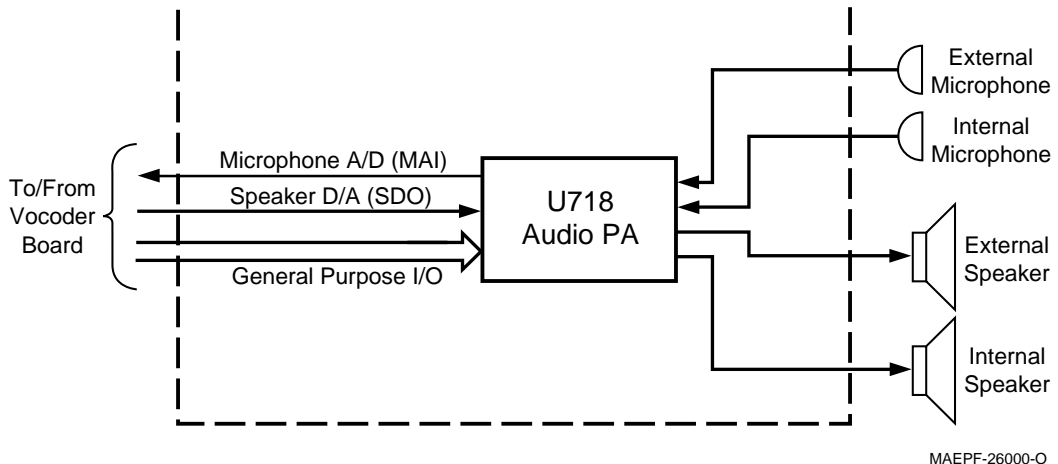
The controller board consists almost entirely of digital logic comprising a microcontrol unit (MCU — U701), a custom support logic IC (SLIC — U702), and memory consisting of: SRAM (U705), EEPROM (U706), and FLASH memory (U727). The board also contains the audio PA (U718) and its associated circuitry.

The MCU's (U701) memory system is composed of a 32k x 8 SRAM (U705), a 32k x 8 EEPROM (U706), and 1M x 8 FLASH ROM (U727). The MCU also contains 1024 bytes of internal SRAM and 512 bytes of internal EEPROM. The EEPROM memory is used to store customer

specific information and radio personality features. The FLASH ROM contains the programs which the HC11F1 executes. The FLASH ROM allows the controller firmware to be reprogrammed for future software upgrades or feature enhancements. The SRAM is used for scratchpad memory during program execution.

The SLIC (U702) performs many functions as a companion IC for the MCU. Among these are expanded input/output (I/O), memory decoding and management, and interrupt control. It also contains the universal asynchronous receiver transmitter (UART) used for the RS232 data communications. The SLIC control registers are mapped into the MCU's (U701) memory space.

The controller board's audio power amplifier (PA) (U718) is the only analog IC on the board. This IC is an audio amplifier for the microphone analog input and speaker analog output. The audio PA allows steering between the internal and external microphone and speaker. Steering is accomplished via four control lines provided by the ADSIC and controlled by the DSP through the ADSIC parallel registers. Refer to Figure 8.



*Figure 8 Audio Power Amplifier Steering*

The controller performs the programming of all peripheral ICs. This is done via a serial peripheral interface (SPI) bus. ICs programmed via this bus include the synthesizer, DAIC, reference oscillator, display, and ADSIC. On secure-equipped models, the encryption board is also controlled through the SPI bus.

In addition to the SPI bus, the controller also maintains two asynchronous serial busses: the SB9600 bus and an RS232 serial bus. The SB9600 bus is for interfacing the controller section with different hardware option boards, some of which may be external to the radio. The RS232 is functions as a common data interface for external devices.

User input is handled by the controller through top rotary controls and side buttons. On models with a display, an additional 3 x 2 (model II) or 3 x 6 keypad (model III) are also read. User feedback is provided

by a single bicolor LED on the top and (on models II and III) a four-line, twelve-character display.

The controller schedules the activities of the DSP through the host port interface. This includes setting the operational modes and parameters of the DSP. The controlling of the DSP is analogous to programming analog signaling ICs on standard analog radios.

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## Switching Regulator

All of the digital circuitry on the vocoder and controller boards is supplied with 5-volt regulated dc by a switched-mode regulator on the controller board (see Figure 4). The fundamental parts of the regulator are U709, L119, C180, D104, C174, C175, and U726. Module U709 is a pulse-width modulating (PWM), switched, regulator controller. Coil L119 is an energy storage element, C180 is an output ripple filter, and D104 is a Schottky diode switch. Capacitors C174 and C175 are added for UNSW\_B+ ripple filtering, and are necessary for the stability of the regulator. Module U726 is a supply supervisory IC, which provides a system reset function when the output of the regulator falls out of regulation, typically around 4.7 Vdc.

This switched-mode regulator works by supplying just sufficient energy to the storage element to maintain the output power of the regulator at 5Vdc. It can be related to a flywheel in the sense that just enough energy can be added to a spinning flywheel to keep it spinning at a constant speed. This is in contrast to a typical linear type regulator, which basically shunts unused current to ground through an active resistive divider. The switched-mode regulator is much more energy efficient. It can be noted that input current to the regulator is less than the load current. In fact, as input voltage to the regulator goes up, current supplied to the regulator actually goes down for a constant load.

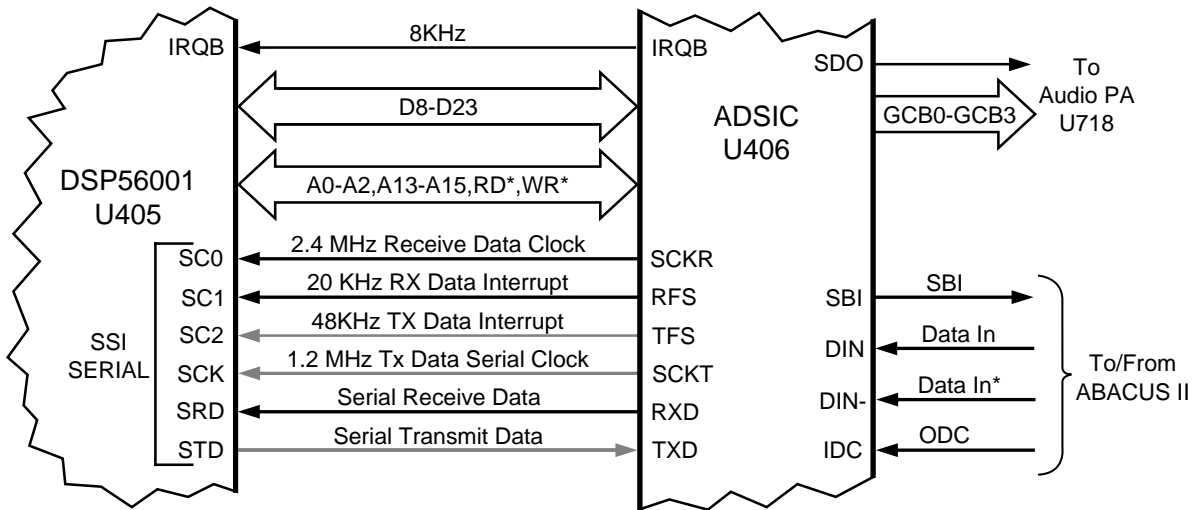
Module U709 works off of a clock with a nominal operating frequency of 160kHz (kit number NCN6128), or 260kHz (kit number NCN6167). This may vary a little, based on the load and input voltage. Regulation is maintained by varying the duty cycle of a clock output driving L119. This signal is referred to as Lx on U709 (refer to *Waveform W1*). As long as the clock output is high, current flows from the supply into L119, allowing energy to be stored. When the clock output goes low, diode D104 conducts, allowing current to continue to flow from ground through L119. A pulse width on the Lx signal can be obtained, which provides the correct amount of energy to keep the output in regulation. Capacitor C180 is an output filter that reduces ripple on the output from the clock transitions.

Module U709 is supplied directly from the unswitched battery supply. It is turned on and off through the control line connected to SHDN\*/ON/OFF\*. This is the same control line from the MCU, which controls the series pass element Q106, that switches SW\_B+. A voltage level of approximately 2 Vdc is required to turn the regulator on.

## RX Signal Path

The vocoder processes all received signals digitally. This requires a unique back end from a standard analog radio. This unique functionality is provided by the ABACUS IC, with the ADSIC (U406) acting as the interface to the DSP. The ABACUS IC, located on the transceiver board, provides a digital back end for the receiver section. It provides a digital output of I (in phase) and Q (quadrature) data words that represent the IF (Intermediate Frequency) signal at the receiver back end (refer to appropriate transceiver section for more details on ABACUS operation). This data is passed to the DSP via an interface with the ADSIC (U406) for appropriate processing.

The ADSIC interface with the ABACUS comprises the four signals: SBI, DIN, DIN\*, and ODC (refer to Figure 9).



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Figure 9 DSP RSSI Port - RX Mode

**NOTE:** An asterisk symbol (\*) next to a signal name indicates a negative or NOT logic true signal.

*SBI* is a programming data line for the ABACUS. This line is used to configure the operation of the ABACUS, and is driven by the ADSIC. The MCU programs many of the ADSIC operational features through the SPI interface. There are 36 configuration registers in the ADSIC, of which four contain configuration data for the ABACUS. When these particular registers are programmed by the MCU, the ADSIC in turn sends this data to the ABACUS through the *SBI*.

*DIN* and *DIN\** are the data lines in which the I and Q data words are transferred from the ABACUS. These signals make up a differentially encoded current loop. Instead of sending TTL-type voltage signals, the data is transferred by flowing current one way or the other through the loop. This helps reduce internally generated spurious emissions on the transceiver board. The ADSIC contains an internal current loop decoder which translates these signals back to TTL logic and stores the data in internal registers.

*ODC* is a clock that ABACUS provides to the ADSIC. Most internal ADSIC functions are clocked by this *ODC* signal at a rate of 2.4 MHz; it is available as soon as power is supplied to the circuitry. This signal initially may be 2.4 or 4.8MHz after power-up. The *ODC* signal is programmed by the ADSIC, via the *SBI* signal, to 2.4MHz when the ADSIC is initialized by the MCU through the SPI bus. For any functionality of the ADSIC to exist, including initial programming, this reference clock must be present.

In the fundamental mode of operation, the ADSIC transfers raw IF data to the DSP. The DSP can perform IF filtering and discriminator functions on this data to obtain a baseband demodulated signal. However, the ADSIC includes a digital IF and discriminator function, and can provide this baseband demodulated signal directly to the DSP; this is the typical mode of operation. The internal digital IF filter is programmable up to 24 taps. These taps are programmed by the MCU via the SPI interface.

The DSP accesses this data through its SSI serial port. This is a six-port, synchronous serial bus. It is actually used by the DSP for both transmit and receive data transfer, but only the receive functions will be discussed here. The ADSIC transfers the data on the *SRD* line to the DSP at a rate of 2.4 MHz. This is clocked synchronously by the ADSIC, which provides a 2.4MHz clock on *SC0*. In addition, a 20kHz interrupt is provided on *SC1*, signalling the arrival of a data packet. This means that a new I and Q sample data packet is available to the DSP at a 20kHz rate, which represents the sampling rate of the received data. The DSP then processes this data to extract audio, signalling, etc., based on the 20kHz interrupt.

In addition to the SPI programming bus, the ADSIC also contains a parallel configuration bus consisting of *D8-D23*, *A0-A2*, *A13-A15*, *RD\**, and *WR\**. This bus is used to access registers mapped into the DSP memory starting at *Y:FFF0*. Some of these registers are used for additional ADSIC configuration controlled directly by the DSP; some of the registers are data registers for the speaker D/A. Analog speaker audio is processed via this parallel bus, in which the DSP outputs the speaker's audio digital data words to the speaker's D/A, and an analog waveform, output on *SDO* (speaker data out), is generated. In conjunction with the speaker D/A, the ADSIC contains a programmable attenuator to set the rough signal attenuation. However, the fine levels and differences among signal types are adjusted through the DSP's software algorithms. The speaker D/A attenuator setting is programmed by the MCU via the SPI bus.

The ADSIC provides an 8kHz interrupt to the DSP on *IRQB* for processing the speaker data samples. *IRQB* is also one of the DSP mode configuration pins at start-up. This 8kHz signal must be enabled through the SPI programming bus by the MCU, and is necessary for any audio processing to occur.

For secure messages, the analog signal data may be passed to the secure module prior to processing speaker data for decryption. The DSP transfers the data to and from the secure module through its *SCI* port, consisting of *TXD* and *RXD*. The *SCI* port is a two-wire, duplex, asynchronous serial port. Configuration and mode control of the secure module is performed by the MCU via the SPI bus.

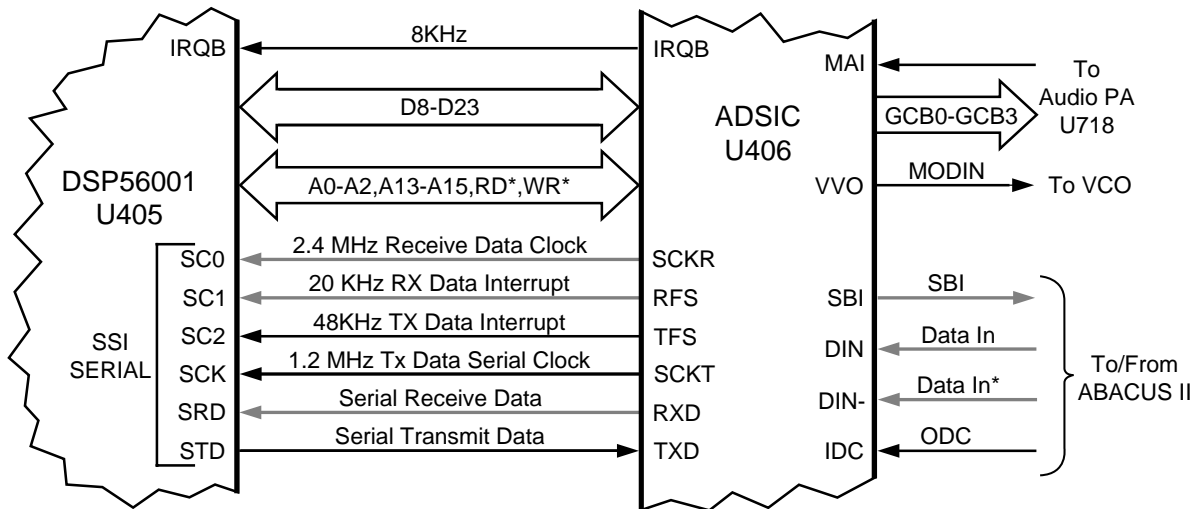
The ADSIC contains four general purpose I/O lines, labeled GCB0 through GCB3. These are connected to the AUDIO PA, and are used for enabling the speaker and microphone amplifiers in the IC and for steering the speaker and microphone audio paths from internal to external. These I/O lines are controlled by the DSP through the ADSIC parallel configuration bus. The DSP then writes speaker data samples, at an 8kHz rate, to the speaker D/A register via the parallel bus, and configures the AUDIO PA enable lines by writing the same bus to the register controlling the I/O.

The audio PA provides about 20dB of gain and a dual-ended differential output: SPKR\_COMMON, and EXT\_SPKR or INT\_SPKR. Internal or external speaker drive is achieved by changing the phase of the outputs on INT\_SPKR and EXT\_SPKR to be either in-phase or out-of-phase with SPKR\_COMMON. The signal which is out-of-phase with SPKR\_COMMON will be driven.

Since all of the audio and signaling is processed in DSP software algorithms, all types of audio and signaling follow this same path.

## TX Signal Path

The transmit signal path follows some of the same design structure as the receive signal path described above under “RX Signal Path” (refer to Figure 10). It is advisable to read through the “RX Signal Path” section prior to reading this section.



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Figure 10 DSP RSSI Port - TX Mode

The ADSIC contains a microphone A/D with a programmable attenuator for coarse level adjustment. As with the speaker D/A attenuator, the microphone attenuator value is programmed by the MCU via the SPI bus. The analog microphone signal from the audio PA (U718) is input to the A/D on MAI (Mic Audio In). The microphone A/D converts the analog signal to a series of data words and stores them in internal registers. The DSP accesses this data through the parallel data bus parallel configuration bus consisting of D8-D23, A0-A2, A13-A15, RD\*, and WR\*. As with the speaker data samples, the DSP reads the microphone samples from registers mapped into its memory



space, starting at Y:FFF0. The ADSIC provides an 8kHz interrupt to the DSP on IRQB for processing these microphone data samples.

As with the received trunking low-speed data, low-speed data is processed by the MCU and returned to the DSP at the DSP SCLK port, connected to the MCU port PA0.

For secure messages, the analog signal may be passed to the secure module for encryption prior to further processing. The DSP transfers the data to and from the secure module through its SCI port, consisting of TXD and RXD. Configuration and mode control of the secure module is performed by the MCU via the SPI bus.

The DSP processes these microphone samples, generates and mixes the appropriate signalling, and filters the resultant data. This data is then transferred to the ADSIC IC on the DSP SSI port. The transmit side of the SSI port consists of SC2, SCK, and STD. The DSP SSI port is a synchronous serial port. SCK is the 1.2MHz clock input derived from the ADSIC, which makes it synchronous. The data is clocked over to the ADSIC on STD at a 1.2MHz rate.

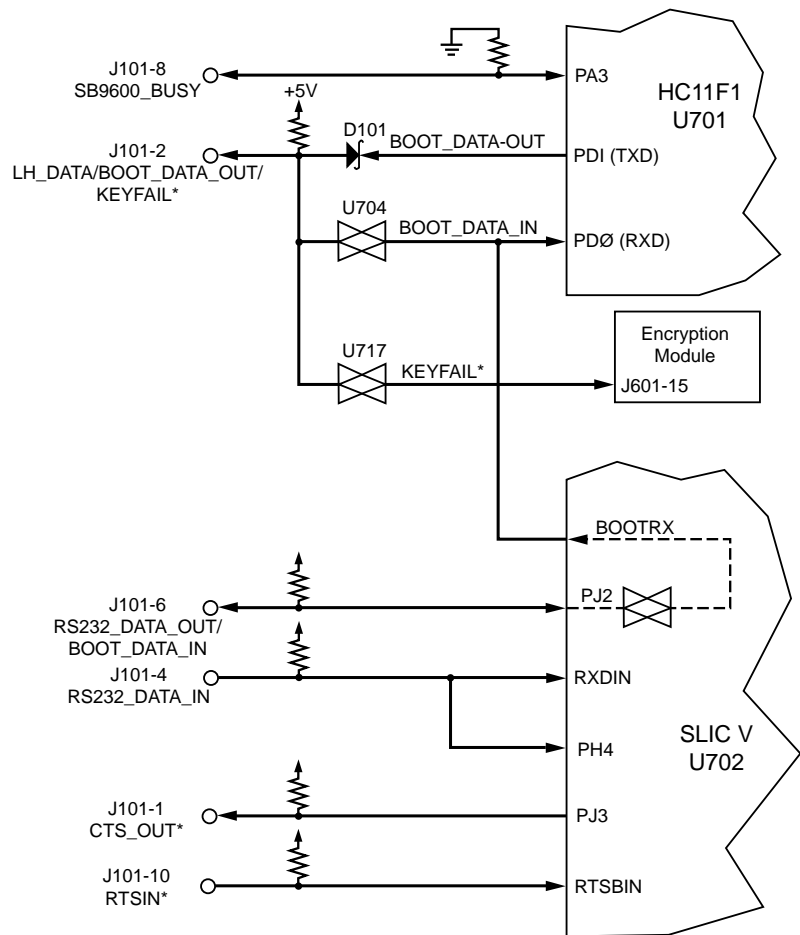
The ADSIC generates a 48kHz interrupt on SC2 so that a new sample data packet is transferred at a 48kHz rate, and sets the transmit data sampling rate at 48ksp. These samples are then input to a transmit D/A converter, which converts the data to an analog waveform. This waveform is actually the modulation out signal from the ADSIC port VVO, and is connected directly to the VCO. The transmit side of the transceiver is virtually identical to a standard analog FM radio.

Also required is the 2.4MHz ODC signal from the ABACUS IC. Although the ABACUS IC provides receiver functions, it is important to note that this 2.4MHz reference is required for all of the ADSIC operations.

## Controller Bootstrap and Asynchronous Buses

The SB9600 bus is an asynchronous serial communications bus utilizing a Motorola proprietary protocol. It provides a means for the MCU to communicate with other hardware devices. In the ASTRO Digital XTS 3000 radio, it communicates with hardware accessories connected to the universal connector.

The SB9600 bus utilizes the UART internal to the MCU, operating at 9600 baud. The SB9600 bus consists of LH\_DATA (J101-2) and SB9600\_BUSY (J101-8) signals. LH\_DATA is actually the SCI TXD and RXD ports (U701 — PD0 and PD1) tied together through the MUX U704 (see Figure 11). This makes the bus a simplex, single-wire system. SB9600\_BUSY (U701 — PA3) is an active low signal that is pulled low when a device wants control of the bus.



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Figure 11 Host SB9600 and RS232 Ports

The same UART internal to the MCU is used in the controller bootstrap mode of operation. This mode is used primarily in downloading new program code to the FLASH ROMs on the vocoder and controller boards. In this mode, the MCU accepts special code, downloaded at 7200 baud via the SCI bus, instead of operating from program code resident in its ROMs. However, it must operate in a two-wire, duplex configuration.

A voltage applied to J101-12 (Vpp) of greater than 10 Vdc will trip the circuit consisting of Q104, and VR119. This circuit sets the MODA and

MODB pins of the MCU to bootstrap mode (logic 0,0) and configures the MUX (U704) to separate the RXD and TXD signals of the MCU SCI port. Now, if the Vpp voltage is raised to 12Vdc required on the FLASH devices for programming, the circuit comprising VR121, Q109, and Q110 will trip supplying Vpp to the FLASH devices U727 and U404. One more complication exists in that the BOOT\_DATA\_IN signal (RXD) is multiplexed with the RS232 data out signal RS232\_DATA\_OUT. This multiplexing occurs in the SLIC IV (U702), which must also be properly configured.

The ASTRO Digital XTS 3000 radio has an additional asynchronous serial bus which utilizes RS232 bus protocol. This bus utilizes the UART in the SLIC IC (U702). It consists of RS232\_DATA\_OUT (J101-6), RS232\_DATA\_IN (J101-4), CTSOUT\* (J101-1), and RTSIN\* (J101-10). It is a two-wire duplex bus, used to connect to external data devices. This bus is used to keyload radios equipped with encryption modules. When keyloading a radio, the RS232\_DIN\* and CTSOUT\* lines are pulled low by the keyloader, and MUX U717 will be enabled by the MCU. The keyloading data (multiplexed with the LH\_DATA/BOOT\_DATA\_OUT line) is sent to the encryption module on the KEYFAIL\* line. This data will be ignored at the MCU's PDI port.

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## Vocoder Bootstrap

The DSP has two modes of bootstrap: from program code stored in the FLASH ROM (U404), or retrieving code from the host port.

During normal modes of operation, the DSP executes program code stored in the FLASH ROM, U404. Unlike the MCU, however, the DSP moves the code from the FLASH ROM into the three SRAMs (U401, U402, and U403), where it is executed from. Since, at initial start-up, the DSP must execute this process before it can begin to execute system code, it is considered a bootstrap process. In this process, the DSP fetches 512 words, 1536 bytes, of code from the FLASH ROM, starting at physical address \$C000, and moves it into internal P memory. This code contains the system vectors, including the reset vector. It then executes this piece of bootstrap code, which basically in turn moves additional code into the external SRAMs.

A second mode of bootstrap allows the DSP to load this initial 512 words of data from the host port, being supplied by the MCU. This mode is used for FLASH programming the DSP ROM when the ROM may initially be blank. In addition, this mode may be used for downloading some diagnostic software for evaluating that portion of the board.

The bootstrap mode for the DSP is controlled by three signals: MODA/IRQA\*, MODB/IRQB\*, and D23 (kit number NTN8250D), or MODC (kit number NTN8250E). All three of these signals are on the DSP (U405). MODA and MODB configure the memory map of the DSP when the DSP reset becomes active. These two signals are controlled by the ADSIC (U406) during power-up, which sets MODA low and MODB high for proper configuration. Later, these lines become interrupts for analog signal processing. D23/MODC controls whether the DSP will look for code from the MCU or will retrieve code from the FLASH ROM. D23 high, or MODC low out of reset, causes the DSP to seek code from the FLASH ROM (U404). For the second mode of bootstrap, the MCU drives BOOTMODE low, causing D23 to go low and MODC to go high.

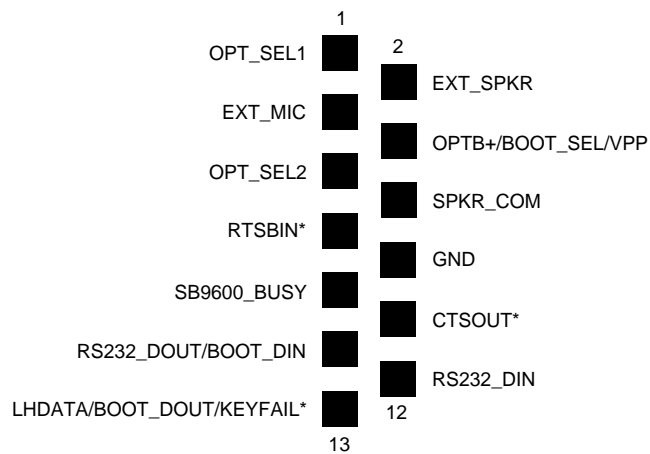
## SPI Bus Interface

This bus is a synchronous serial bus made up of a data line, a clock line, and an individual IC unique select line. Its primary purpose is to configure the operating state of each IC. ICs programmed by this include: display module, ADSIC, fractional-N synthesizer, pendulum reference oscillator, DAIC and, if equipped, the secure module.

The MCU (U701) is configured as the master of the bus. It provides the synchronous clock (SPI\_SCK), a select line, and data (MOSI [Master Out Slave In]). In general, the appropriate select line is pulled low to enable the target IC, and the data is clocked in. Actually, the SPI bus is a duplex bus with the return data being clocked in on MISO (master in slave out). The only place this is used is when communicating with the secure module. In this case, the return data is clocked back to the MCU on MISO (master in slave out).

## Universal Connector and Option Selects

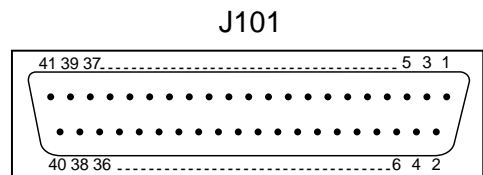
The universal connector is located on the side of the radio. It is the external port or interface to the outside, and is used for programming and interfacing to external accessories. The signals are shown in Figure 12. The universal connector connects to the controller board at J101 through a flex circuit, routed inside the external housing. Connections to the universal connector and J101 on the controller board are shown in Figures 12 and 13.



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Figure 12 Universal (Side) Connector

Signal Name	J101-Pin #
OPT_SEL_1	11
EXT_SPKR	9
EXT_MIC	13
OPT_B+/BOOT_SEL/VPP	12
OPT_SEL_2	7
SPKR_COM	5
RTSIN*	10
GND	3
SB9600_BUSY	8
CTSOUT*	1
RS232_DOUT/BOOT_DIN	6
LH_DATA/BOOT_DOUT/KEYFAIL*	2
RS232_DIN	4



MAEPF-26005-O

Figure 13 Controller Connector — J101

Most of the signals are extensions of circuits described in other areas of this manual. However, there are two option select pins used to configure special modes: Option Select 1 and Option Select 2. These pins are controlled by accessories connected to the universal connector. Table 1 outlines their functions as defined at the universal connector.

*Table 1 Option Select Functions*

	Option Select 1	Option Select 2
External PTT	0	0
No Function (Normal)	1	1
External Speaker	0	1

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## Keypad and Display Module

An optional integral four-line by 12-character LCD display module is available with either a 3 x 2 keypad (model II radios) or 3 x 6 keypad (model III radios). This unit is not considered field repairable. The display module is connected to the controller through flex connector P301.

The display is controlled by the MCU, which programs the display through the SPI bus and DISP\_EN\* (select) line. In addition, display backlighting is provided by two white LEDs controlled by the BL\_EN signal. Digital +5V, routed to the display, is used to power these LEDs, as well as all other circuitry on the display.

The keypad module is connected to the controller through flex connector P107. The keypad is read through a row and column matrix made up of ROW1, ROW2, ROW3, ROW4, ROW5, ROW6, and COL1, COL2, and COL3. These signals are input to I/O ports on the SLIC (U702) and individually pulled to a high state through resistors. When a key is pressed, the respective signals for a single row and a single column are set to logic zero. The MCU reads these ports through the SLIC parallel registers, provides for key debounce, and determines which key has been pressed.

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## Controls and Control Top Flex

The housing assembly top controls include an on/off switch/volume control (S1), a 16-position mode-select switch with programmable two-position concentric switch (U1), a programmable three-position (A,B,C) toggle switch (S2), and a programmable top (orange) button (SW3). The side controls include three programmable, momentary, push button switches (side button 1 [SB2], side button 2 [SB3], and top side button [SB1]) and a PTT switch (SW2). These components are connected through a flex circuit to the controller at J101 (see Figure 14). The assembly also contains the radio's internal speaker and internal microphone.

UNSW\_B+ is routed through switch S1 to provide the B+\_SENSE signal which provides radio power control. Refer to "Radio Power" on page 1 for further details.

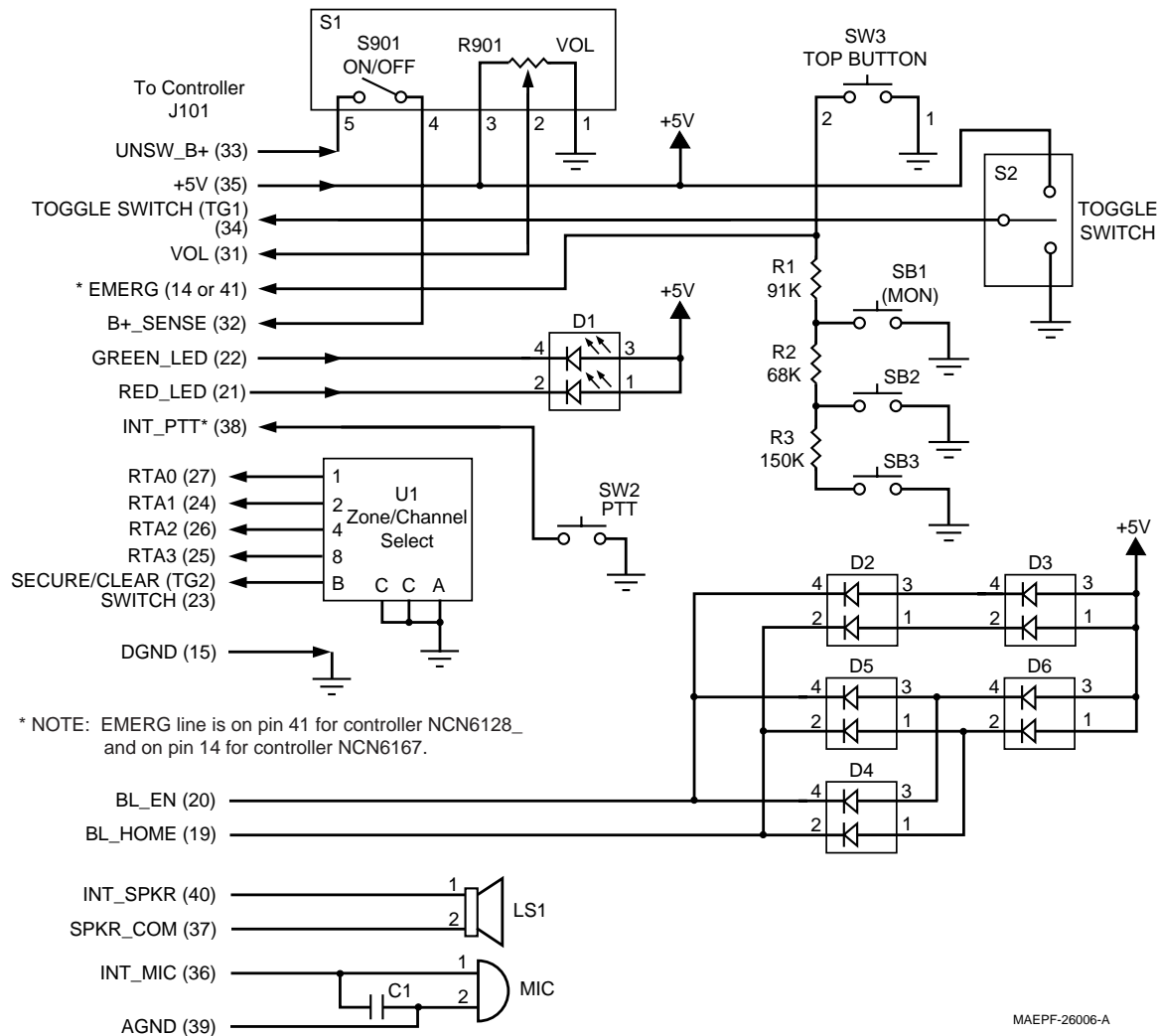


Figure 14 Control Top Flex

Volume control is also provided by S1, which contains a potentiometer biased between +5Vdc and ground. The VOL signal is a voltage level between +5Vdc and 0Vdc, dependent on the position of the rotary knob. VOL is an input to an A/D port on the MCU (U701). The MCU sends the appropriate message to the DSP to adjust speaker volume based on this setting.

Switch S2 is the three-position, programmable toggle switch typically used for expanded zone/channel selection. It is an input to an MCU A/D port with levels of 0Vdc, 2.5Vdc, and 5Vdc.

Programmable top (orange) button SW3 is typically used for emergency. This button, along with programmable side buttons SB1 through SB3, is connected to a resistor divider network, biased between +5Vdc and ground. This network, made up of R1, R2, and R3, provides a voltage level, controlled by which button is pressed, to an A/D port on the MCU. The MCU determines which button has been pressed based on the value at the A/D port.

LED D1 is the TX/RX indicator. LEDs D2 through D6 are used for backlighting the frequency knob.

U1 is a binary-coded switch. The output pins from U1 are connected to I/O ports on the controller, which provides a four-bit binary word to the MCU, indicating which of the 16 positions the rotary is set to. This switch provides an additional output, TG2, which is typically used for coded or clear mode selection. It is an input to a control I/O with a pull-up resistor. Selecting clear mode pulls this signal to logic low.

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## Controller Memory Map

Figure 15 depicts the controller section memory map for the parallel data bus as used in normal modes of operation. There are three maps available for normal operation, but map 2 is the only one used. In bootstrap mode, the mapping is slightly different and will be addressed later.

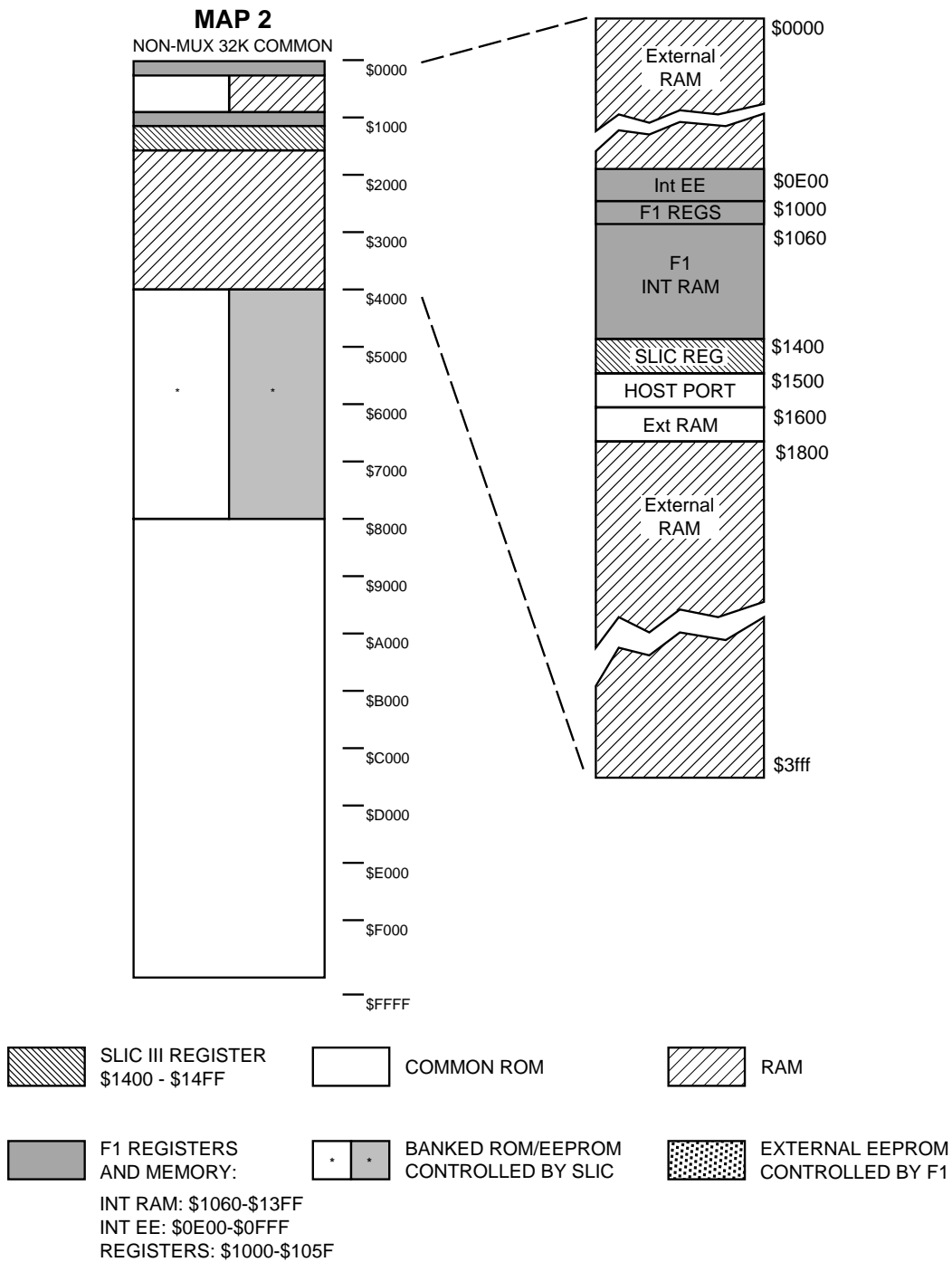
The external bus for the host controller (U701) consists of one 32k x 8 SRAM (U705), one 32k x 8 EEPROM (U706), one 1M x 8 FLASH ROM (U727), and SLIC (U702) configuration registers. In addition, the DSP host port is mapped into this bus through the SLIC address space. The purpose of this bus is to interface the MCU (U701) to these devices.

The MCU executes program code stored in the FLASH ROM. On a power-up reset, it fetches a vector from \$FFFE, \$FFFF in the ROM and begins to execute code stored at this location. The external SRAM, along with the internal 1k x 8 SRAM, is used for temporary variable storage and stack space. The internal 512 bytes of EEPROM, along with the external EEPROM, are used for non-volatile storage of customer-specific information. More specifically, the internal EEPROM space contains transceiver board tuning information and, on power-down, some radio-state information is stored in the external EEPROM.

The SLIC is controlled through sixteen registers mapped into the MCU memory at \$1400-\$14FF. This mapping is achieved by the following signals from the MCU: R/W\*, CSIO1\*, HA0-HA4, HA8, and HA9. Upon power-up, the MCU configures the SLIC including the memory map by writing to these registers.

The SLIC memory management functions, in conjunction with the chip selects provided by the MCU, provide the decoding logic for the memory map that is dependent upon the “map” selected in the SLIC. The MCU provides a chip select, CSGEN\*, which decodes the valid range for the external SRAM. In addition, CSIO1\* and CSProg\* are provided to the SLIC decoding logic for the external EEPROM and FLASH ROM respectively. The SLIC provides a chip select and banking scheme for the EEPROM and FLASH ROM. The FLASH ROM is banked into the map in 16kB blocks, with one 32kB common ROM block. The external EEPROM may be swapped into one of the banked ROM areas. This is all controlled by EE1CS\*, ROM1CS\*, ROM2CS\*, HA14\_OUT, HA15\_OUT, HA16, and HA17 from the SLIC (U702), and D0-D8 and A0-A16 from the MCU (U701).

The SLIC provides three peripheral chip selects: XTSC1B, XTCS2B, and XTCS3B. These can be configured to drive an external chip select when its range of memory is addressed. XTSC1B is used to address the host port interface to the DSP; XTSC2B is used to address a small portion of external SRAM through gate U708; and XTSC3B is used as general purpose I/O for interrupting the secure module.



MAEPF-24346-O

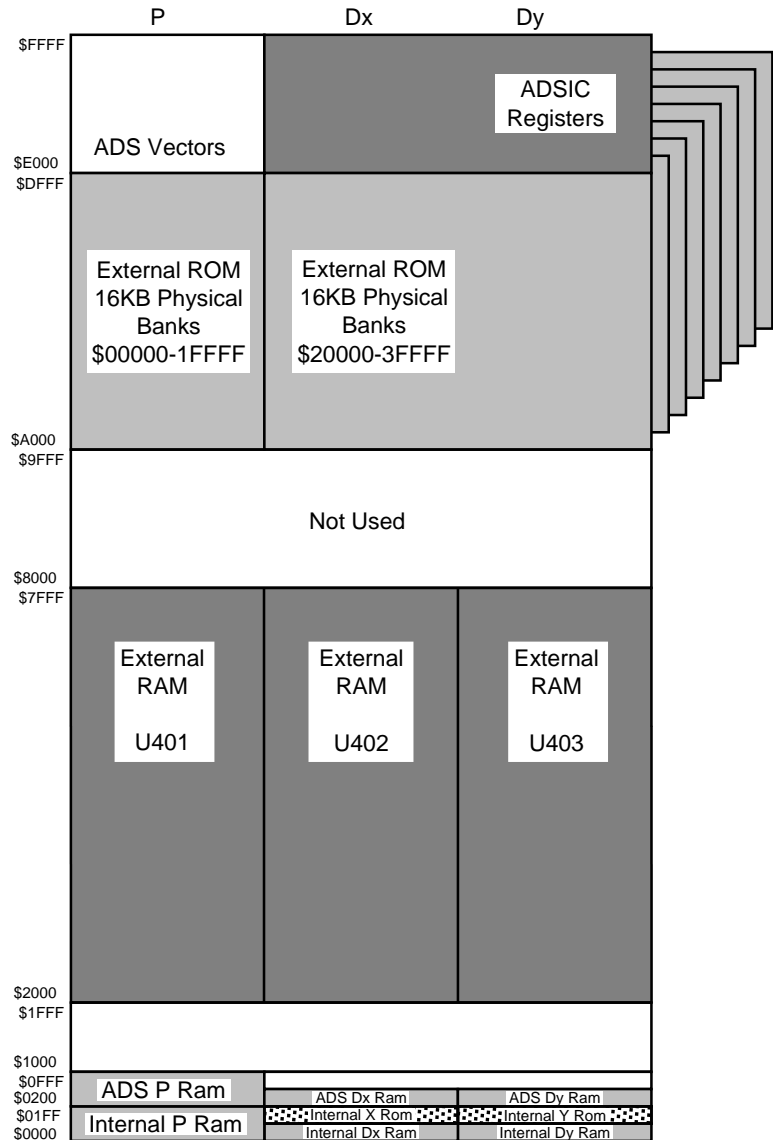
*Figure 15 Controller Memory Mapping*

In bootstrap mode, the memory map is slightly different. Internal EEPROM is mapped at \$FE00-\$FFFF and F1 internal SRAM starts at \$0000-\$03FF. In addition, a special bootstrap ROM appears in the ROM space from \$B600-\$BFFF. For additional information on bootstrap mode, refer to the section “Controller Bootstrap and Asynchronous Buses” on page 10.



# Vocoder Memory Map

The vocoder (DSP) external bus consists of three 32k x 8 SRAMs (U401, U402, and U403), one 256k x 8 FLASH ROM (U404), and ADSIC (U406) configuration registers. Refer to Figure 16.



MAEPF-26007-A

Figure 16 Vocoder Memory Mapping

The DSP56001A (U405) has a 24 bit wide data bus (D0-D23) and a 16 bit wide address bus (A0 - A15). The DSP can address three 64k x 24 memory spaces: P (Program), Dx (Data X), and Dy (Data Y). These additional RAM spaces are decoded using PS\* (Program Strobe), DS\* (Data Strobe), and X/Y\*. RD\* and WR\* are separate read and write strobes.

The ADSIC provides memory decoding for the FLASH ROM (U404). EPS\* provides the logic  $A15 \times (A14 \oplus A13)$  and is used as a select for the ROM. The ADSIC provide three bank lines for selecting 16k byte

banks from the ROM. This provides decoding for 128k bytes from the ROM in the P: memory space. PS\* is used to select A17 to provide an additional 128k bytes of space in Dx: memory space for the ROM.

The ADSIC internal registers are decoded internally and start at \$E000 in Dy:. These registers are decoded using A0-A2, A13-A15, and PS\* from the DSP. The ADSIC internal registers are 16 bits wide, so only D8-D23 are used.

The DSP program code is stored in the FLASH ROM, U404. During normal modes of operation, the DSP moves the appropriate program code into the three SRAMs (U401, U402, and U403) and internal RAM for execution. The DSP never executes program code from the FLASH ROM itself. At power-up after reset, the DSP downloads 512 words (1536 bytes) from the ROM, starting at \$C000, and puts it into the internal RAM, starting at \$0000, where it is executed. This segment of program code contains the interrupt vectors and the reset vector, and is basically an expanded bootstrap code. When the MCU messages the DSP that the ADSIC has been configured, the DSP overlays more code from the ROM into external SRAM and begins to execute it. Overlays occur at different times when the DSP moves code from the ROM into external SRAM, depending on immediate mode of operation, such as changing from transmit to receive.

---

## MCU System Clock

The MCU (U701) system clock is provided by circuitry internal to the MCU and is based on the crystal reference, Y100. The nominal operating frequency is 7.3728MHz. This signal is available as a clock at 4XECLK on U701 and is provided to the SLIC (U702) for internal clock timing. The MCU actually operates at a clock rate of 1/4 the crystal reference frequency or 1.8432MHz. This clock is available at ECLK on U701.

The MCU clock contains a crystal warp circuit comprised of L120, Q102, and C162. This circuit is controlled by an I/O port (PA6) on the MCU. This circuit moves the operating frequency of the oscillator about 250ppM on certain receive channels to prevent interference from the MCU bus noise.

---

## DSP System Clock

The DSP (U405) system clock, DCLK, is provided by the ADSIC (U406). It is based off the crystal reference, Y401, with a nominal operating frequency of 33.0000 MHz. The ADSIC contains an internal clock-divider circuit that can divide the system clock from 33MHz to 16.5MHz or 8.25MHz operation. The DSP controls this divider by writing to the ADSIC parallel registers. The frequency is determined by the processes the DSP is running and, to reduce system power consumption, is generally configured to the slowest operating speed possible.

The additional circuitry of CR402, L401, C416, C417, C419, and C422 make up a crystal warp circuit. This circuit is controlled by the OSCw signal from ADSIC, which is configured by the host through the SPI bus. The crystal warp circuit moves the operating frequency of the oscillator about 400ppM on certain receive channels to prevent interference from the DSP bus noise.

---

## Radio Power-Up/ Power-Down Sequence

Radio power-up begins when the user closes the radio on/off switch on the control top, placing 7.5Vdc on the B+\_SENSE line. This signal enables the pass element Q106 through Q105, enabling SW\_B+ to the controller board and the transceiver board. B+\_SENSE also enables the +5Vdc regulator, U709. When +5Vdc has been established, it is sensed by the supervisory IC, U726, which disables the system reset through the delay circuit R208 and C214.

When the MCU comes out of reset, it fetches the reset vector in ROM at \$FFFE, \$FFFF and begins to execute the code this vector points to. It configures the SLIC through the parallel bus registers. Among other things it enables the correct memory map for the MCU. It configures all the transceiver devices on the SPI bus. The MCU then pulls the ADSIC out of reset and, after a minimal delay, the DSP also. It then configures the ADSIC via the SPI bus, configuring, among other things, the DSP memory map. While this is happening, the DSP is fetching code from ROM U404 into internal RAM and beginning to execute it. It then waits for a message from the MCU that the ADSIC has been configured, before going on.

During this process, the MCU does power diagnostics. These diagnostics include verifying the MCU system RAM, and verifying the data stored in the internal EEPROM, external EEPROM, and FLASH ROMs. The MCU queries the DSP for proper status and the results of DSP self tests. The DSP self tests include testing the system RAM, verifying the program code in ROM U404, and returning the ADSIC configuration register checksum. Any failures cause the appropriate error codes to be sent to the display. If everything is OK, the appropriate radio state is configured and the unit waits for user input.

On power-down, the user opens the radio on/off switch, removing the B+\_SENSE signal from the controller board. This does not immediately remove power, as the MCU holds this line active through B+\_CNTL. The MCU then saves pertinent radio status data to the external EEPROM. Once this is done, B+\_CNTL is released, shutting off SW\_B+ at Q106 and shutting down the 5Vdc regulator U709. When the regulator slumps to about 4.7Vdc, supervisory IC U726 activates a system reset to the SLIC, which in turn resets the MCU.



# Secure Modules

# 7

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## Introduction

The secure modules are designed to digitally encrypt and decrypt voice and ASTRO data in ASTRO Digital XTS 3000 radios. This section covers the following secure modules:

- NTN8253
- NTN8254
- NTN8255
- NTN8256
- NTN8257
- NTN8258
- NTN8259
- NTN8260
- NTN8261
- NTN8326
- NTN8418
- NTN8328
- NTN8329
- NTN8330
- NTN8331
- NTN8705
- 0105956V67

**NOTE:** The secure modules are NOT serviceable. The information contained in this chapter is only meant to help determine whether a problem is due to a secure module or the radio itself.

The secure module uses a custom encryption integrated circuit (IC) and an encryption key variable to perform its encode/decode function. The encryption key variable is loaded into the secure module, via the radio's universal (side) connector, from a hand-held, key variable loader (KVL). The encryption IC corresponds to the particular encryption algorithm purchased. The encryption algorithms and their corresponding kit numbers are:

DES	NTN8253
DES-XL	NTN8254
DES-OFB	NTN8255
DVI-XL	NTN8256
DVP-XL	NTN8257
DES-XL and DES-OFB	NTN8258
DVP-XL and DES-OFB	NTN8259
DES-XL and DVP-XL	NTN8260
DVP-XL and DVI-XL	NTN8261
DVI-XL and DES-OFB	NTN8326
DES and DES-OFB	NTN8418

DVP	NTN8328
DVI-XL and DVP	NTN8329
DES-XL and DVP	NTN8330
DVP-XL and DVP	NTN8331
DES-OFB and DVP	NTN8705
All, except DVP	0105956V67

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## Circuit Description

The secure module operates from three power supplies (UNSW\_B+, SW\_B+, and +5V). The +5V and the SW\_B+ are turned on and off by the radio's on/off switch. The UNSW\_B+ provides power to the secure module as long as the radio battery is in place.

Key variables are loaded into the secure module through connector J601, pin 15. Up to 16 keys (depending on the type of encryption module) can be stored in the module at a time. The key can be infinite key retention or 30-seconds key retention, depending on how the code plug is setup.

The radio's host processor communicates with the Secure Module on the Serial Peripheral Interface (SPI) bus. The host processor is the master on this bus, while the secure module is a slave on the bus. The SPI bus consists of five signal lines. Refer to Table 1 for signal information. A communications failure between the host processor and the secure module will be indicated as an "ERROR 09/10" message on the radio display.

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## Troubleshooting Secure Operations

Refer to "Disassembly/Reassembly Procedures" on page 1. A key variable loader (KVL) and oscilloscope are needed to troubleshoot the secure module.

*NOTE:* The secure module itself is not serviceable. If the secure module is found to be defective, it must be replaced.

## Error 09/10, Error 09/90

The ASTRO Digital XTS 3000 radio automatically performs a self test on every power-up. Should the radio fail the self tests, the display will show "ERROR 09/10" or "ERROR 09/90" accompanied by a short beep. If the display shows "ERROR 09/10" or "ERROR 09/90," the radio failed the secure power-up tests and the host microcontroller was unable to communicate with the secure module via the SPI bus. Turn the radio off and back on. If the radio still does not pass the self tests, then a problem exists with the secure operations of the radio.

Troubleshooting information for "ERROR 09/10" is found in Troubleshooting Chart, "09/10 Secure Hardware Failure." For "ERROR 09/90," see Troubleshooting Chart, "09/90 Secure Hardware Failure."

## Keyload

When the keyloading cable is attached to the ASTRO Digital XTS 3000 radio and "KEYLOADING" is not displayed on the radio's display, then the radio has not gone into KEYLOAD mode. For troubleshooting "KEYLOAD" failure, refer to Troubleshooting Chart, "Key Load Fail."

*NOTE:* ASTRO Digital XTS 3000 radios need a keyloader that has the ability to keyload an ASTRO Digital XTS 3000 radio. The keyloader must be either a "T - - - - CX" or a "T - - - - DX" keyloader.

# Disassembly/Reassembly Procedures

# 8

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## Introduction to this Section

This section gives detailed procedures for disassembling and reassembling the radio. Refer to the diagrams that accompany the text, the exploded view diagrams and parts lists located in the back of this manual, and the ASTRO Digital XTS 3000 Basic Service Manual, Motorola publication 68P81083C85. Items in parentheses ( ) refer to item numbers in the exploded view.

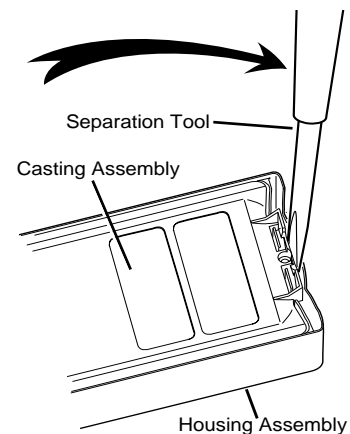
---

## Disassembly

1. Turn off the radio by rotating the on/off/volume control fully counterclockwise until you hear a click.
2. Referring to the Basic Service Manual (68P81083C85), Chapter 6, remove the universal connector cover or any accessory connected to the radio, the antenna, and the battery.

*NOTE:* It is not necessary to remove the volume knob (6) and insert (7) or frequency knob (13) and insert (11) to service the main chassis. However, if any top control is suspected, then the knobs and inserts should be removed prior to removing the chassis from the front cover. Refer to Chapter 6 in the Basic Service Manual.

3. With the back of the radio facing upward, insert the DNT 8193 special tool at the bottom of the radio between the housing assembly (2) and the two tabs on the casting assembly (54). Gently pry upward to free the housing assembly from the casting. Making sure that the antenna bushing has cleared the hole in the control top, carefully lift the casting assembly clear of the housing assembly.



4. While holding the casting assembly (54) in one hand and the housing assembly (2) in the other, unplug the 41-pin connector on the controls flex assembly (18) from the controller board (44).

*NOTE:* This can easily be done using the thumb of the hand holding the housing assembly.

Put the housing assembly aside.

5. Remove the main seal (58) from around the casting assembly (54).
6. If you are disassembling a model II or III radio, continue with step 7; if you are disassembling a model I radio, skip to step 10.
7. With the front of the radio facing upward, lift the LCD module (38), with display locator pad (39), up and off of the four locator posts on the casting (54). Then, flip the LCD module up toward the top of the radio, revealing the display flex attachment bracket (42) and the keypad flex attachment bracket (43).
8. Disengage the display flex attachment bracket (42) by prying it up from the side, releasing the two chassis snaps; note the positioning of the bracket over the flex's "finger." Remove the LCD module (38) and display flex connector bracket (42) and put them aside.
9. Disengage the keypad flex attachment bracket (43) by prying it up from the side, releasing the two chassis snaps.
10. Pry all four controller front shield clips (40) upward, alternating diagonally across the chassis. Remove the controller front shield (41), with keypad flex assembly (37) (models II and III only) and clips still attached, from the chassis.
11. Lift the controller board (44) up and away from the chassis.

*NOTE:* If the radio is equipped with hardware encryption, insert a small (1/8" wide maximum), flat-bladed screwdriver between the lower left portion of the chassis and controller board and gently pry upward on the controller board. This will free the controller board/encryption board (45) connection.
12. Lift out the 50-pin (48) and 20-pin (47) compression connectors.
13. Remove the vocoder board shield (46) by inserting a small (1/8" wide maximum), flat-bladed screwdriver in the removal slot on the right side of the shield, and prying in a counterclockwise direction. Once the shield's retention tab is free of the casting window, lift the shield out. If the encryption board (45) is equipped, it will come out with the shield.
14. Turn the casting assembly over and allow the vocoder board (50) to drop out into the palm of your hand.
15. With the front of the radio facing upward, use your thumb to hold down the clip (40) that secures the upper left portion of the RF shield (49), and pry the clip free. Then, release the two snaps on the right side of the RF shield. Lift the shield out, rotating it around its top edge.
16. Using the RF board coax disengagement tool or needle-nosed pliers, carefully unplug the coaxial cable's connector (55) from the RF board's (51) surface-mount connector.
17. Lift the RF board (51) out of the casting assembly. Inspect the casting to make sure the thermal pad (61) is attached to the casting. If the pad is attached to the RF board, remove it from the board. If the pad is in good condition, reattach it to the casting; if it is not, attach a new pad to the casting and discard the old one.
18. Lift the B+ assembly (52) and B+ seal (53) out of the casting assembly.



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## Reassembly

1. Reinstall the B+ assembly (52) and B+ seal (53), making sure that the seal seats properly in the casting assembly. Inspect the B+ assembly from the back of the casting to ensure that the seal shows evenly around the B+ assembly.
2. Make sure that a thermal pad (61) is attached to the casting. If it is not, attach a new thermal pad to the casting as indicated in the exploded view.
3. With the front of the radio facing upward, drop the RF board (51) in place, tucking the right side of the board in first — under the casting ledge.
4. Plug the coaxial cable's connector (55) into the RF board's (51) surface-mount connector, making sure to lead the coax's connector in on an axis straight into the surface-mount connector. An angled lead-in can damage the surface-mount connector or the center of the coax.
5. Reinstall the RF shield (49). Insert the shield's top edge in first, aligning the two tabs on the shield's top edge with the two slots in the casting, then pivot the shield down into position. Engage the two snaps on the right side first, then insert and snap down the single left side clip (40).
6. Reinstall the vocoder board (50) with the component side of the board facing downward.
7. Reinstall the vocoder board shield (46), engaging the two tabs on the left side first, then snapping down the single right side snap.

If the encryption board (45) is equipped, reinstall it with the shield:

- a. Align the notches on the encryption board's edge with the internal tabs on the vocoder board shield.
  - b. Drop the board in place.
  - c. Slide the board upward until it stops, nested in the shield.
8. Reinstall the 50-pin (48) and 20-pin (47) compression connectors; they can only be inserted in one way. Insert the 50-pin connector with the smallest diameter peg pointing downward on the left side. Insert the 20-pin connector with the two-peg edge pointing downward on the left side.
  9. Reinstall the controller board (44). Tuck the controller board's upper peninsula into the retention slot on the casting, rotate the board into position, and engage the 20- and 50-pin connectors. If the radio is equipped with hardware encryption, make sure that the controller board's connector mates fully with the encryption board's (45) connector.
  10. Reinstall the controller front shield (41), with keypad (models II and III only) and four clips (40) still attached, into the chassis. Snap the controller front shield clips down, alternating diagonally across the shield.
  11. If you are reassembling a model II or III radio, continue with step 11; if you are resassembling a model I radio, skip to step 13.

12. Reinstall the keypad flex attachment bracket (43). Insert the two tabs on the bracket through the two slots in the keypad flex (37) and into the two slots in the controller board (44), then snap down the two casting snaps.
13. Reinstall the LCD module (38), display locator pad (39), and display flex attachment bracket (42). Position the LCD module, with display faces upward, the flex points toward the bottom of the radio, and the locating "finger" on the flex passes through the opening between the middle compression fingers on the bracket. Insert the tab on the bracket through the slot in the flex and into the slot in the controller board (44), then snap down the two chassis snaps. Flip the LCD module down to cover the display flex connector and keypad flex connector brackets. Press the display locator pad (39) down over the three locator tabs on the casting.
14. Reinstall the main seal (58) around the casting assembly (54). Start at the top of the casting and work the seal around the perimeter of the casting until it is completely in place.
15. While holding the casting assembly (54) in one hand and the housing assembly (2) in the other, plug the 41-pin connector on the controls flex assembly (18) into the connector on the controller board (44).

*NOTE:* This can easily be done using the thumb of the hand holding the chassis.
16. With the fronts of both the casting assembly (54) and housing assembly (2) facing upward, carefully insert the top of the casting into the top of the housing assembly. Making sure that the antenna bushing is inside the antenna hole in the control top, pivot the bottom of the housing downward toward the bottom of the casting until they meet. Snap the housing assembly and casting assembly together.
17. Referring to the Basic Service Manual (68P81083C85), Chapter 6, reinstall: the universal connector cover or any accessory connected to the radio, the antenna, and the battery.

*NOTE:* If the volume knob (6) or frequency knob (13) were removed prior to servicing the main chassis, reinstall them.

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## Ensuring Radio Submersibility

### Introduction

ASTRO XTS 3000 R radio models meet the stringent requirements of U. S. MIL-STD-810C, Method 512.1, Procedure I, MIL-STD-810D, Method 512.2, Procedure I, and MIL-STD-810E, Method 512.3, Procedure I, which require the radio to maintain watertight integrity when immersed in three feet of water for two hours @ 27° ΔT. Radios shipped from the Motorola factory have passed the water immersion test and should not be disassembled. If disassembly is necessary, refer to qualified service personnel and service shops capable of restoring the watertight integrity of the radio.



#### **Caution**

It is strongly recommended that maintenance of the radio be deferred to qualified service personnel and service shops. This is of paramount importance as irreparable damage to the radio can result from service by unauthorized persons. If disassembly is necessary, unauthorized attempts to repair the radio may void any existing warranties or extended performance agreements with Motorola. It is also recommended that submersibility be checked annually by qualified service personnel.

If the radio is accidentally dropped in water, shake the radio to remove the excess water from the speaker grille area before operating; otherwise, the sound may be distorted until the water has evaporated from this area.

### General Information

To ensure that the radio is truly a watertight unit, special testing, test procedures, and specialized test equipment are required. The special testing involves a vacuum check of the radio and pressure testing (troubleshooting) for water leaks if the vacuum check fails. The specialized test equipment is needed to perform the vacuum check and pressure testing, if required.

### Specialized Test Equipment

Vacuum Pump Kit,  
NLN9839

The vacuum pump kit includes a vacuum pump with gauge, and a vacuum hose. An adapter with gasket (NTN9279A), which must be ordered separately, connects the vacuum hose to the radio's casting. The vacuum pump kit is also used on Motorola ASTRO SABER R radios. The adapter with gasket is new to the ASTRO XTS 3000 R.

Pressure Pump Kit,  
NTN4265

The pressure pump kit includes a pressure pump with gauge, and a pressure hose; the pressure pump kit is also used on Motorola ASTRO SABER R radios. As with the vacuum pump kit above, the NTN9279A adapter connects the pressure hose to the radio's casting.

Miscellaneous  
Hardware

Other items needed for testing the submersible radio include:

- Large water container.
- Deionized (DI) water
- A supply of replacement seals, o-rings, and gaskets (refer to the ASTRO XTS 3000 R exploded view parts list).

Disassembly and  
Reassembly

*If disassembly and reassembly of the radio is required, refer to the “Disassembly/Reassembly Procedures” in this manual.*

Disassembly

Disassemble the radio according to the “Disassembly” section of this manual.

Reassembly

Reassemble the radio according to the “Reassembly” section of this manual. Tighten all hardware that was loosened or removed. **DO NOT REASSEMBLE THE RADIO WITHOUT FIRST PERFORMING THE FOLLOWING PRELIMINARY INSPECTION PROCEDURE:**

1. Remove the main seal o-ring from the casting.
2. Inspect the seal area around the casting for foreign material that might prevent the main seal o-ring from sealing properly.
3. Install a new main seal o-ring; discard the old o-ring.
4. Reassemble the housing.



The main seal o-ring should not be visible when looking at the back side of the radio. If the seal is visible, it is improperly installed.

**Caution**

Vacuum Test

Refer to the exploded view diagrams and parts lists in this manual.

General

The vacuum test uses a vacuum pump and gauge. The pump creates a vacuum condition inside the radio, and the gauge monitors the radio for a stable vacuum reading; that is, checking for a properly sealed, watertight unit. Before starting the vacuum test:

- Remove the battery.
- Remove the universal connector cover to expose the universal connector.

## Conducting the Test

1. Attach the vacuum hose to the vacuum pump. Check the pump and hose for leaks by blocking off the open end of the hose and operating the pump a few times. The actual reading of the gauge at this point is not important; it is important that the gauge pointer remains steady, indicating no vacuum leaks in the pump.
2. Remove the vacuum test port (see Section 13, page 72, item 62) using a 7/64" Allen key. Remove the O-Ring; item 63.
3. Ensure that a rubber gasket is attached to the hose-to-casting adapter. Screw the adapter into the tapped hole in the casting.
4. Attach the open end of the hose to the adapter.
5. Place the radio on a flat surface with the casting facing upward. Place two or three drops of water on each slot of the label (66) that protects the vent port seal (65) on the casting. This will ensure that no air goes through the seal.
6. Operate the pump a few times until the gauge indicates 5 in. Hg; do not pull more than 7 in. Hg of vacuum on the radio.  
  
Operate the pump again until the gauge indicates 6 in. Hg.
7. Observe the gauge for approximately 1 minute.
  - If the needle falls 1 in. Hg or less (for example, from 6 in. Hg to 5 in. Hg), then the radio has passed the vacuum test and is approved for submersibility. No additional testing will be required.
  - If the needle falls more than 1 in. Hg (for example, from 6 in. Hg to less than 5 in. Hg), then the radio has failed the vacuum test and the radio might leak if submersed. Additional troubleshooting of the radio will be required; complete this procedure, then go to the "Pressure Test" section of this manual.
8. Dry the water from the slots on the label (66) that protects the vent port seal to allow the radio to equalize. The pressure should drop slowly to "0."
9. Remove the vacuum hose and adapter from the radio.
10. Install the o-ring and the vacuum test port plug. Torque the plug to 6 in-lb.

## Pressure Test

*Refer to the exploded view diagrams and parts lists in this manual.*

## General

Pressure testing the radio is necessary only if the radio has failed the vacuum test. Do not perform the pressure test until the vacuum test has been completed. Pressure testing involves creating a positive pressure condition inside the radio, submersing the radio in water, and observing the radio for a stream of bubbles (leak). Since all areas of the radio are being checked, observe the entire unit carefully for the possibility of multiple leaks before completing this test.

## Conducting the Test

1. Remove the vacuum test port (see Section 13, page 72, item 62) using a 7/64" Allen key. Remove the O-Ring; item 63.
2. Screw the adapter (with gasket) into the tapped hole in the casting.
3. Attach one end of the pressure hose to the adapter and the other end to the pressure pump.
4. Cover the vent port seal (65) and label (66) on the back of the casting with your thumb. This will prevent air from going through the seal. Keep the vent port covered with your thumb until the test is complete (through step 8).
5. Operate the pump until the gauge reads approximately 1 psig.



Pressure any greater than 1 psig may push air around the main seal.

### Caution

6. Maintain the pressure at 1 psig and submerge the radio into a water-filled container. Keep the vent port covered with your thumb while the radio is submerged.
7. Watch for any continuous series of bubbles. A stream of bubbles indicates a sign of leakage.  
*NOTE:* Some air entrapment may cause the accumulation of bubbles, especially in the grille area, but the bubbles should not be continuous.
8. Note all of the seal areas that show signs of leakage. Pinpoint the problem(s) to one (or more) of the following areas:
  - housing
  - antenna bushing seal
  - controls seal
  - frequency switch, toggle, and on/off/volume control switch
  - main seal
  - battery contact and battery contact seal
  - keypad
9. Remove the radio from the water container, remove your thumb from the vent port seal, and dry the radio thoroughly. Be especially careful to dry the area around the main seal to prevent contamination of the internal electronics while the unit is open.

To avoid equipment damage, keep the area around the port seal dry by ensuring that there is no water around the casting's vacuum port.

10. Remove the adapter and pressure hose added in steps 1 and 2, above.
11. Install the o-ring and the vacuum test port plug. Torque the plug to 6 in-lb.
12. Inspect the vent port seal (65) to ensure that the seal behind the label's (66) two slots has not been punctured. If it has been punctured, the seal and the label must be replaced.

## Troubleshooting Leak Areas

Before repairing any leak, read all applicable area repair paragraphs. This will help to eliminate unnecessary disassembly and reassembly of a radio with multiple leaks. Troubleshoot only the faulty seal areas listed in the “Pressure Test” section, and, when multiple leaks exist, in the order listed.

*NOTE:* Before reassembling the radio, always install a new main seal o-ring, and new seals in the defective area.

### Housing

1. If a leak occurs at the lens, universal connector, casting/housing interface, or PTT/Ratt button area of the housing, replace the housing. Referring to the Disassembly/Reassembly Procedures:
  - a. Remove the housing assembly from the radio.
  - b. Discard the housing assembly and main seal o-ring.
  - c. Install a new main seal o-ring around the casting assembly.
  - d. Install a new housing assembly to the radio.
  - e. Inspect the main seal for proper seating.
  - f. Observe carefully to ensure that the main seal o-ring is not pinched between the housing and the casting.
2. If the leak occurs at the control top area, remove the knobs, knob inserts and antenna in order to determine the leak location:
  - a. Conduct the Pressure Test.
  - b. Identify the leak location.

### Antenna Bushing Seal

1. Referring to the Disassembly/Reassembly Procedures, remove the housing assembly from the radio.
2. Remove and discard the antenna bushing seal.
3. Inspect the housing seal surface for debris or damage. Remove any debris and replace housing if damaged.
4. Install new antenna bushing seal.
5. Install a new main seal o-ring around the casting assembly.
6. Reassemble the housing assembly to the radio.
7. Inspect the main seal for proper seating. Observe carefully to ensure that the main seal o-ring is not pinched between the housing and the casting.

### Controls Seal

1. Referring to the Disassembly/Reassembly Procedures, remove the housing assembly from the radio.
2. Remove the speaker bracket screw.
3. Remove the speaker bracket.
4. Disconnect the controls flex from the universal connector.
5. Disconnect the controls flex and backer from PTT area of the housing assembly.
6. Referring to the Basic Service Manual (68P81089C80), Chapter 6, remove the frequency knob, frequency insert, secure lever, lightpipe, volume knob, volume insert, and o-ring.

7. Using a pair of needle nose pliers, unsnap the left snap of the controls bracket assembly.
8. Remove the controls bracket assembly.
9. Remove and discard the controls seal.
10. Inspect the housing seal surfaces for debris. Remove any debris.
11. Install a new controls seal.
12. Install a new main seal o-ring around the casting assembly.
13. Reassemble the controls bracket assembly.
14. Referring to the Basic Service Manual (68P81089C80), Chapter 6, install the frequency knob, new frequency escutcheon, new frequency insert, secure lever, lightpipe, volume knob, new volume insert, and o-ring.
15. Reconnect the controls flex to the universal connector and the PTT area of the housing assembly.
16. Reassemble the housing assembly to the radio.
17. Inspect the main seal for proper seating. Observe carefully to ensure that the main seal o-ring is not pinched between the housing and the casting.

Frequency Switch,  
Toggle, and On/Off/  
Volume Control Switch

1. Referring to the Disassembly/Reassembly Procedures, remove the housing assembly from the radio.
2. Remove the speaker bracket screw.
3. Remove the speaker bracket.
4. Disconnect the controls flex from the universal connector.
5. Disconnect the controls flex and backer from the PTT area of the housing assembly.
6. Referring to the Basic Service Manual (68P81089C80), Chapter 6, remove the frequency knob, frequency insert, secure lever, lightpipe, volume knob, volume insert, and o-ring.
7. Using a pair of needle nose pliers, unsnap the left snap of the controls bracket assembly.
8. Remove the controls bracket assembly.
9. Replace the switch that leaks by following the unsoldering and replacement instructions contained in the new switch's instruction sheet.
10. Reassemble the controls bracket assembly.
11. Referring to the Basic Service Manual (68P81089C80), Chapter 6, install the frequency knob, new frequency escutcheon, new frequency insert, secure lever, lightpipe, volume knob, new volume insert, and o-ring.
12. Reconnect the controls flex to the universal connector and the PTT area of the housing assembly.
13. Install a new main seal o-ring around the casting assembly.
14. Reassemble the housing assembly to the radio.



15. Inspect the main seal for proper seating. Observe carefully to ensure that the main seal o-ring is not pinched between the housing and the casting.

## Main Seal

1. Referring to the Disassembly/Reassembly Procedures, remove the housing assembly from the radio.
2. Remove and discard the main seal.
3. Inspect the housing and casting seal surfaces for debris or damage. Remove any debris and replace the housing or casting if damaged.
4. Install a new main seal o-ring around the casting assembly.
5. Reassemble the housing assembly to the radio.
6. Inspect the main seal for proper seating. Observe carefully to ensure that the main seal o-ring is not pinched between the housing and the casting.

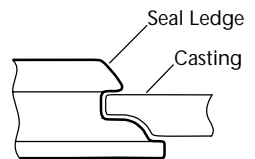
## Battery Contact and Battery Contact Seal

1. Referring to the Disassembly/Reassembly Procedures, remove the housing assembly from the radio.
2. Completely disassemble the casting assembly.
3. Remove and discard the leaking component.
4. Inspect the casting seal surface for debris or damage. Remove any debris and replace casting if damaged.
5. Install a new battery contact and a new battery contact seal if necessary.



### Caution

When installing the battery contact seal, make sure that the ledge around the outside of the seal completely protrudes through the opening in the casting and sits flush with the outside surface of the casting. Also, make sure that the seal's shape is not distorted.



6. Reassemble the casting assembly.
7. Install a new main seal o-ring around the casting assembly.
8. Reassemble the housing assembly to the radio.
9. Inspect the main seal for proper seating. Observe carefully to ensure that the main seal o-ring is not pinched between the housing and the casting.

## Keypad

1. Referring to the Disassembly/Reassembly Procedures, remove the housing assembly from the radio.
2. Remove and discard the keypad.
3. Inspect the housing seal surface for debris or damage. Remove any debris and replace housing if damaged.
4. Install new keypad.
5. Install a new main seal o-ring around the casting assembly.
6. Reassemble the housing assembly to the radio.
7. Inspect the main seal for proper seating. Observe carefully to ensure that the main seal o-ring is not pinched between the

housing and the casting.

#### Vacuum Port Seal

1. Remove the vacuum port plug (see Section 13, page 72, item 62), using a 7/64" hex torque bit; remove the o-ring; item 63.
2. Inspect the casting seal surface for debris or damage. Remove any debris and replace the casting if damaged.
3. Install a new o-ring and reinstall the vacuum port plug to the correct torque as specified in Table 2.

*Table 2 Submersible Radio Torque Specifications*

Application	Torque (in.-lbs)	Torque (N•m)	Torque Bit Part No.
Speaker Bracket Screw	2	0.23	66-80321B79
Vacuum Port Plug	6	0.68	66-80357B82

#### Vent Port Seal

1. Remove the seal label (66) that covers the vent port seal (65).
2. Remove the vent port seal.
3. Ensure that the casting's surfaces are clean and free from any adhesive or other foreign materials.
4. Install a new vent port seal, covering the two vent port holes, in the small recessed area in the casting. Ensure that no oily substances come in contact with the seal.
5. Install a new seal label over the vent port seal in the larger recessed area in the casting. Press down evenly over the label's surface to ensure good adhesion.

# Troubleshooting Procedures

# 9

---

## Introduction to This Section

The purpose of this section is to aid in troubleshooting a malfunctioning ASTRO Digital XTS 3000 radio. It is intended to be detailed enough to localize the malfunctioning circuit and isolate the defective component.



### Caution

Most of the ICs are static sensitive devices. Do not attempt to troubleshoot or disassemble a board without first referring to the following Handling Precautions section.

---

## Handling Precautions

Complementary metal-oxide semiconductor (CMOS) devices, and other high-technology devices, are used in this family of radios. While the attributes of these devices are many, their characteristics make them susceptible to damage by electrostatic discharge (ESD) or high-voltage charges. Damage can be latent, resulting in failures occurring weeks or months later. Therefore, special precautions must be taken to prevent device damage during disassembly, troubleshooting, and repair. Handling precautions are mandatory for this radio, and are especially important in low-humidity conditions. **DO NOT** attempt to disassemble the radio without observing the following handling precautions.

1. Eliminate static generators (plastics, Styrofoam, etc.) in the work area.
2. Remove nylon or double-knit polyester jackets, roll up long sleeves, and remove or tie back loose hanging neckties.
3. Store and transport all static-sensitive devices in ESD-protective containers.
4. Disconnect all power from the unit before ESD-sensitive components are removed or inserted unless otherwise noted.
5. Use a static-safeguarded workstation, which can be accomplished through the use of an anti-static kit (Motorola part number 01-80386A82). This kit includes a wrist strap, two ground cords, a static-control table mat and a static-control floor mat. For additional information, refer to Service and Repair Note SRN-F1052, "Static Control Equipment for Servicing ESD Sensitive Products," available from Literature Distribution.

Motorola  
Literature Distribution  
2290 Hammond Drive  
Schaumburg, IL 60173  
(708) 576-2826

6. Always wear a conductive wrist strap when servicing this equipment. The Motorola part number for a replacement wrist strap that connects to the table mat is 42-80385A59.

---

## Voltage Measurement and Signal Tracing

It is always a good idea to check the battery voltage under load. This can be done by measuring the OPT\_B+ pin at the universal connector on the back of the radio, with the radio keyed. The battery voltage should remain at or above 7.0Vdc. The battery should be recharged or replaced as necessary prior to analyzing the radio.

In most situations, the problem circuit may be identified using a dc voltmeter, RF millivoltmeter, and oscilloscope (preferably with 100MHz bandwidth or more). The “Recommended Test Equipment, Service Aids, and Tools” section in the ASTRO Digital XTS 3000 Portable Radios Basic Service Manual outlines the recommended tools and service aids which would be useful. Of special note is the 8180377E58 Housing Eliminator, which allows the technician to open the radio to probe points while in operation.

In some cases dc voltages at probe points are shown in red on the schematics. In other areas diagrams may be included to show time varying signals which should be present under the indicated circumstances. It is recommended that a thorough check be made prior to replacement of any IC or part. If the probe point does not have a signal reasonably close to the indicated one, a check of the surrounding components should be made prior to replacing any parts.



### Caution

When checking a transistor or module, either in or out of circuit, do not use an ohmmeter having more than 1.5 volts dc appearing across test leads or use an ohms scale of less than x100.

## Power-Up Self-Check Errors

Each time the radio is turned on the MCU and DSP perform some internal diagnostics. These diagnostics consist of checking the programmable devices such as the FLASH ROMs, internal and external EEPROMs, SRAM devices, and ADSIC configuration bus checksum. At the end of the power-up self-check routines, if an error exists, the appropriate error code is displayed on the display. For non-display radios, the error codes may be read using the Radio Service Software (RSS) from the SB9600 bus on the universal connector. Table 3 lists valid checksums, the related failure, and a reference section for investigating the cause of the failure.

*Table 3 Power-Up Self-Check Error Codes*

Error Code	Description	Troubleshooting Chart
01/81	Host ROM Checksum Failure	Chart 6
01/82	External EEPROM Checksum Failure	Chart 7
01/84	SLIC Initialization Failure	Chart 8
01/88	MCU (Host $\mu$ C) External SRAM Failure	Chart 9
01/92	Internal EEPROM Checksum Failure	Chart 10
02/A0	ADSIC Checksum Failure	Chart 11
02/81	DSP ROM Checksum Failure	Chart 12
02/88	DSP External SRAM Failure	Chart 13
02/90	General DSP Hardware Failure	Chart 14
09/10	Secure Hardware Module Not Installed	Chart 15
09/90	Secure Hardware Failure	Chart 16
001	Synthesizer Out of Lock	Chart 29 & Chart 30
002	Block Checksum Failure for Selected Mode	Chart 7

In the case of multiple errors, the codes are logically ORed and the results displayed. As an example, in the case of an ADSIC checksum failure and a DSP ROM checksum failure, the resultant code would be 02/A1. Following is a series of troubleshooting flowcharts which relate to each of these failure codes.

## Power-Up Sequence

Upon RESET\* going active, the MCU begins to execute code which is pointed to by the vector stored at SFFFE, SFFFF in the FLASH ROM. The execution of this code is as follows:

1. Initialize the MCU (U701). Green LED on.
2. Initialize the SLIC (U702).
3. CONFIG register check. If the CONFIG register is not correct, the MCU will repair it and loop.
4. Start ADSIC/DSP:
  - Bring the ADSIC reset line high.
  - Wait 2ms.
  - Bring the DSP reset line high.

5. Start EMC:

- Set the EMC wake-up line low (emc irq line).
- Wait 5ms.
- Set the EMC wake-up line high
- Wait 10ms.
- Set the EMC wake-up line low (emc irq line).
- Wait 5ms.
- Set the EMC wake-up line high.

6. Begin power-up self-tests.

7. Begin RAM tests:

- External RAM (\$1800-\$3FFF).
- Internal RAM (\$1060-\$1300).
- External RAM (\$0000-\$0DFF).
- Display 01/88 if failure.

The radio will get stuck here if the internal RAM is defective. The radio uses the internal RAM for stack. The RAM routines use subroutines. Thus, if the internal RAM is defective, the radio will get lost testing the external RAM.

8. Display "Self Test" (these routines use subroutines too). It is almost impossible to display an error message if the internal RAM is defective.

9. Begin MCU (host  $\mu$ C) ROM checksum test.

- Fail 01/81 if this routine fails.

10. Begin DSP power-up tests. The MCU will try this five times before it fails the DSP test.

- Check for HF2.
  - Fail 02/90 if 100ms.
- Program the ADSIC.
- Wait for the DSP power-up message.
  - Fail 02/90 if 300ms.
  - Fail 02/90 if wrong message from the DSP.
- Wait for the DSP status information.
  - Fail 02/90 if 100ms.
  - Fail 02/88 if DSP RAM fails.
- Wait for the ADSIC checksum.
  - Fail 02/90 if 100ms.

- Fail 02/90 if failure

- Wait for the first part of the DSP version number.

- Fail 02/90 if 100ms.

- Wait for the second part of the DSP version number.

- Fail 02/90 if 100ms.

11. Display errors if a fatal error exists at this point.

12. Checksum the codeplug.

- Test internal codeplug checksums.

- Fail 01/92 if failure.

- Test external codeplug checksums.

- Error 01/82 if non-fatal error; fail 01/82 if fatal error.

13. Power-up the EMC (if it is enabled in the codeplug).

14. Turn off the green LED.

15. Start up operating system.

## Standard Bias Table

Table 4, below, outlines some standard supply voltages and system clocks which should be present under normal operation. These should be checked as a first step to any troubleshooting procedure.

*Table 4 Standard Operating Bias*

Signal Name	Nominal Value	Tolerance	Source
UNSW_B+	7.5Vdc	6.0-9.0Vdc	J101
SW_B+	7.5Vdc	6.0-9.0Vdc	Q106
+5V	5.0Vdc	±10%	U709
+5VA	5.0Vdc	±10%	U710
RESET	5.0Vdc	+0.7, -1.0Vdc	U702
POR*	5.0Vdc	+0.7, -1.0Vdc	U726
DSP_RST*	5.0Vdc	+0.7, -1.0Vdc	U701
ADSIC_RST*	5.0Vdc	+0.7, -1.0Vdc	
DCLK	33.0000MHz <sup>a</sup>	±500ppM	U406
ODC	2.4MHz	±30ppM	ABACUS
ECLK	1.8432MHz	±500ppM	U701
IRQB*	8kHz <sup>b</sup>	±500ppM	U406
+5V	5.0Vdc	±10%	U202
RX_5V <sup>c</sup>	5.0Vdc	±10%	U106

- a. This is number may vary due to the operating mode of the radio when it is measured. The ADSIC contains a divider which may divide the clock by a modulus of 2. Therefore the actual frequency measured may be  $\text{clock}/2^N$ . The most common frequency will be 16.5000MHz nominal.
- b. This 8kHz clock will be present only after the MCU has successfully programmed the ADSIC after power-up. This is a good indication that the ADSIC is at least marginally operational.
- c. Receive mode only.



# Troubleshooting Charts



---

## Introduction to This Section

This section contains detailed troubleshooting flowcharts. These charts should be used as a guide in determining the problem areas. They are not a substitute for knowledge of circuit operation and astute troubleshooting techniques. It is advisable to refer to the related detailed circuit descriptions in the theory section prior to troubleshooting a radio.

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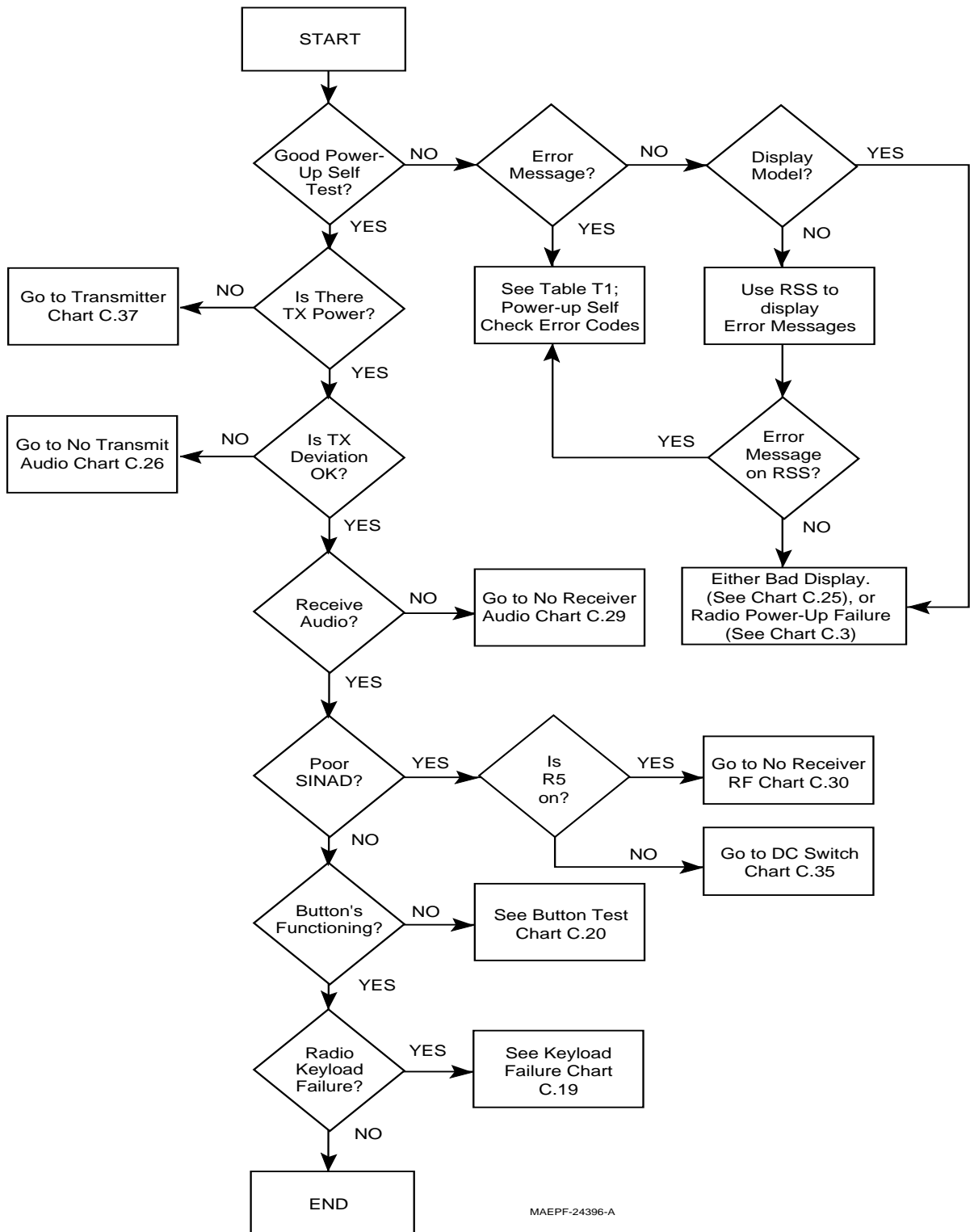
## List of Troubleshooting Charts

Most troubleshooting charts end up by pointing to an IC to replace. **It is not always noted, but it is good practice to verify supplies and grounds to the affected IC and to trace continuity to the malfunctioning signal and related circuitry before replacing any IC.** For instance, if a clock signal is not available at a destination IC, continuity from the source IC should be checked before replacing the source IC.

Chart 1.	800 MHz Radio Main.....	10-3
Chart 2.	VHF/UHF Radio Main.....	10-4
Chart 3.	Radio Power-up Fail.....	10-5
Chart 4.	Bootstrap Fail .....	10-6
Chart 5.	DC Supply Failure.....	10-7
Chart 6.	01/81 Host ROM Checksum Failure.....	10-8
Chart 7.	01/82 or 002, External EEPROM Checksum Failure .....	10-9
Chart 8.	01/84 SLIC Initialization Failure .....	10-10
Chart 9.	01/88 MCU (Host $\mu$ C) External SRAM.....	10-11
Chart 10.	01/92, Internal EEPROM Checksum Failure.....	10-12
Chart 11.	02/A0, ADSIC Checksum Failure.....	10-13
Chart 12.	02/81, DSP ROM Checksum Failure.....	10-14
Chart 13.	02/88, DSP External SRAM FailureU414.....	10-15
Chart 14.	02/90, General DSP Hardware Failure.....	10-16
Chart 15.	09/10, Secure Hardware failure .....	10-17
Chart 16.	09/90, Secure Hardware Failure.....	10-18
Chart 17.	Key Load Fail .....	10-19
Chart 18.	Button Test.....	10-20
Chart 19.	Keypad Error .....	10-21

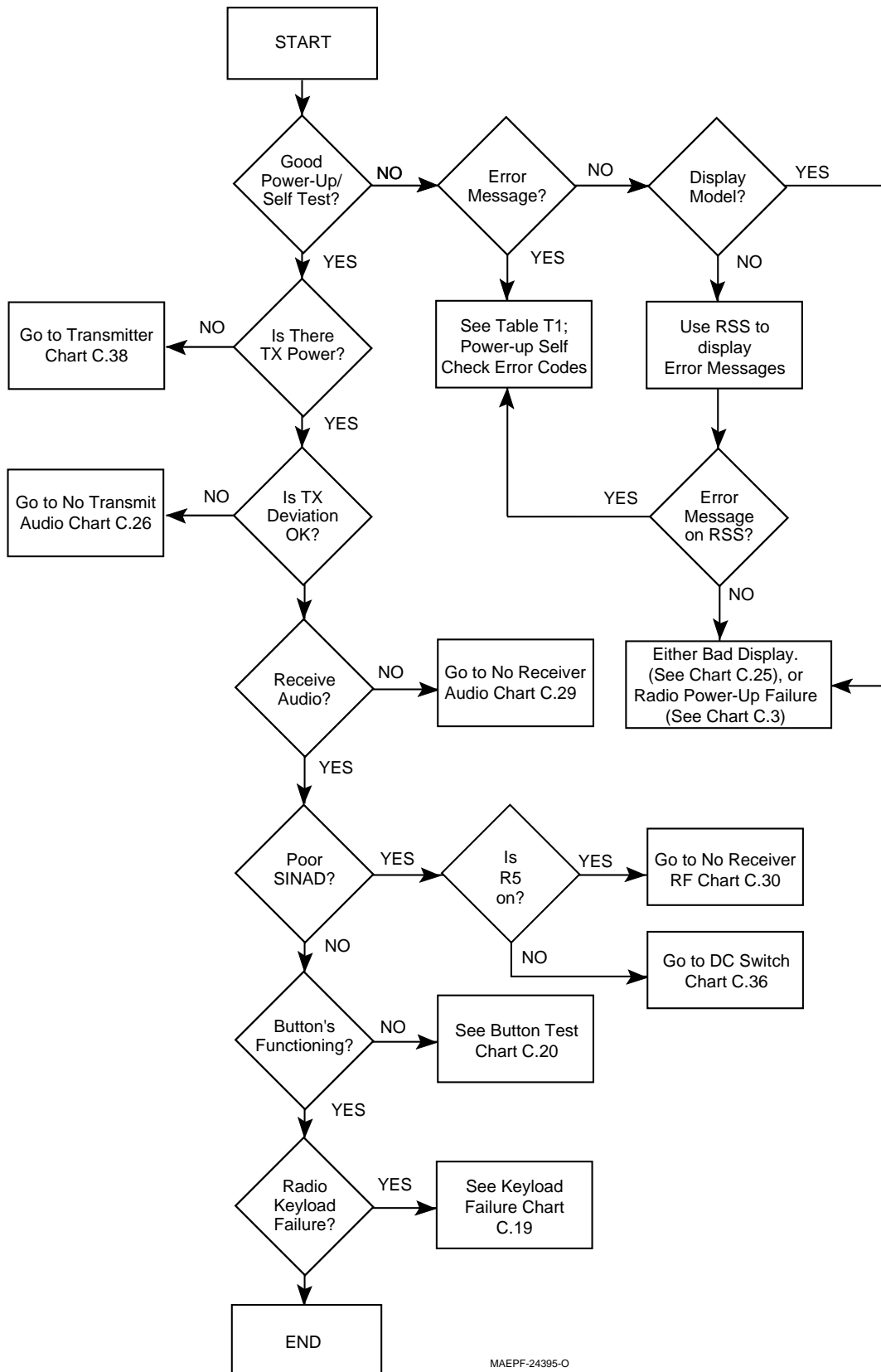
Chart 20. Volume Set Error .....	10-22
Chart 21. Zone/Channel select Error .....	10-23
Chart 22. Top/Side Button Error .....	10-24
Chart 23. Radio Power-up Fail .....	10-25
Chart 24. Bootstrap Fail.....	10-26
Chart 25. 800 MHz No TX Deviation.....	10-27
Chart 26. VHF/UHF No TX Deviation.....	10-27
Chart 27. No RX Audio.....	10-28
Chart 28. VHF/UHF/800 MHz Receiver RF.....	10-29
Chart 29. VHF/UHF Frequency Generation Unit (FGU).....	10-30
Chart 30. 800 MHz Frequency Generation Unit (FGU).....	10-30
Chart 31. VHF/UHF Voltage Controlled Oscillator (VCO) .....	10-31
Chart 32. 800 MHz Voltage Controlled Oscillator (VCO) .....	10-32
Chart 33. 800 MHz DC Switch .....	10-33
Chart 34. VHF/UHF DC Switch .....	10-33
Chart 35. 800 MHz Transmitter RF .....	10-34
Chart 36. VHF/UHF Transmitter RF .....	10-35
Chart 37. VHF/UHF Only, VCO Crossover Frequency Tune .....	10-36

**NOTE:**  $\mu$ C is used in several of the following troubleshooting charts.  
 $\mu$ C = MCU



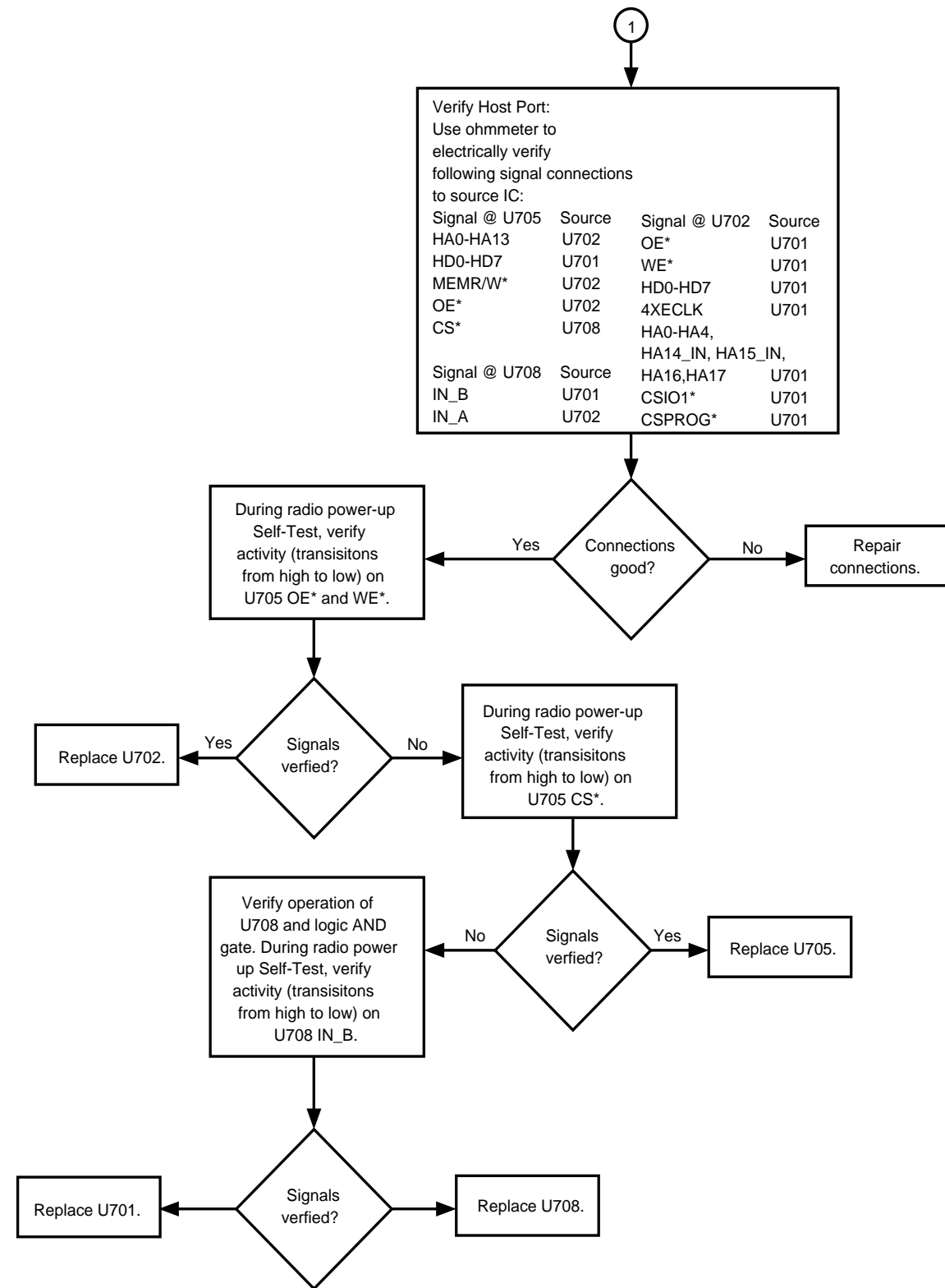
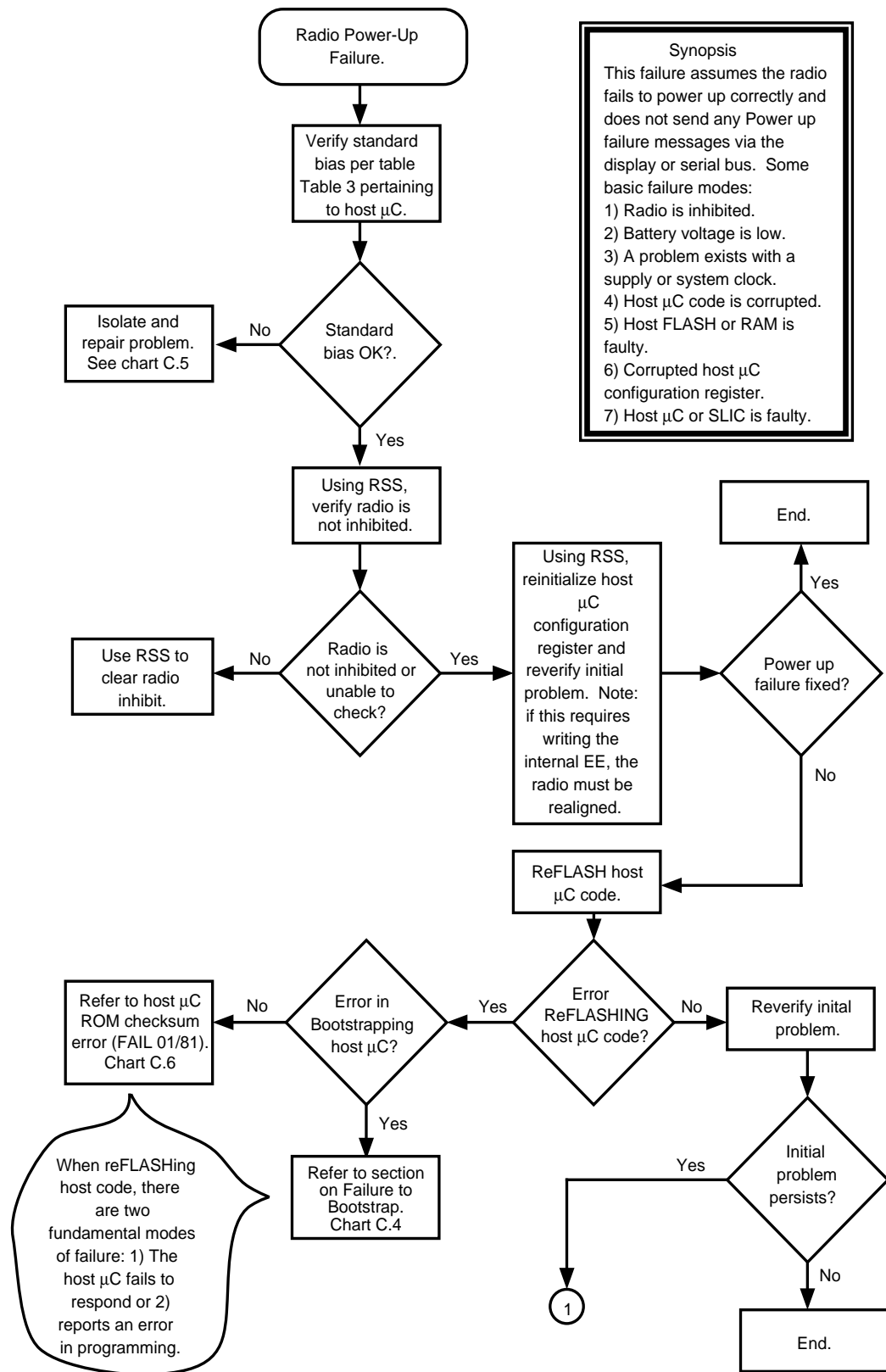
MAEPF-24396-A

Chart 1. 800 MHz Radio Main



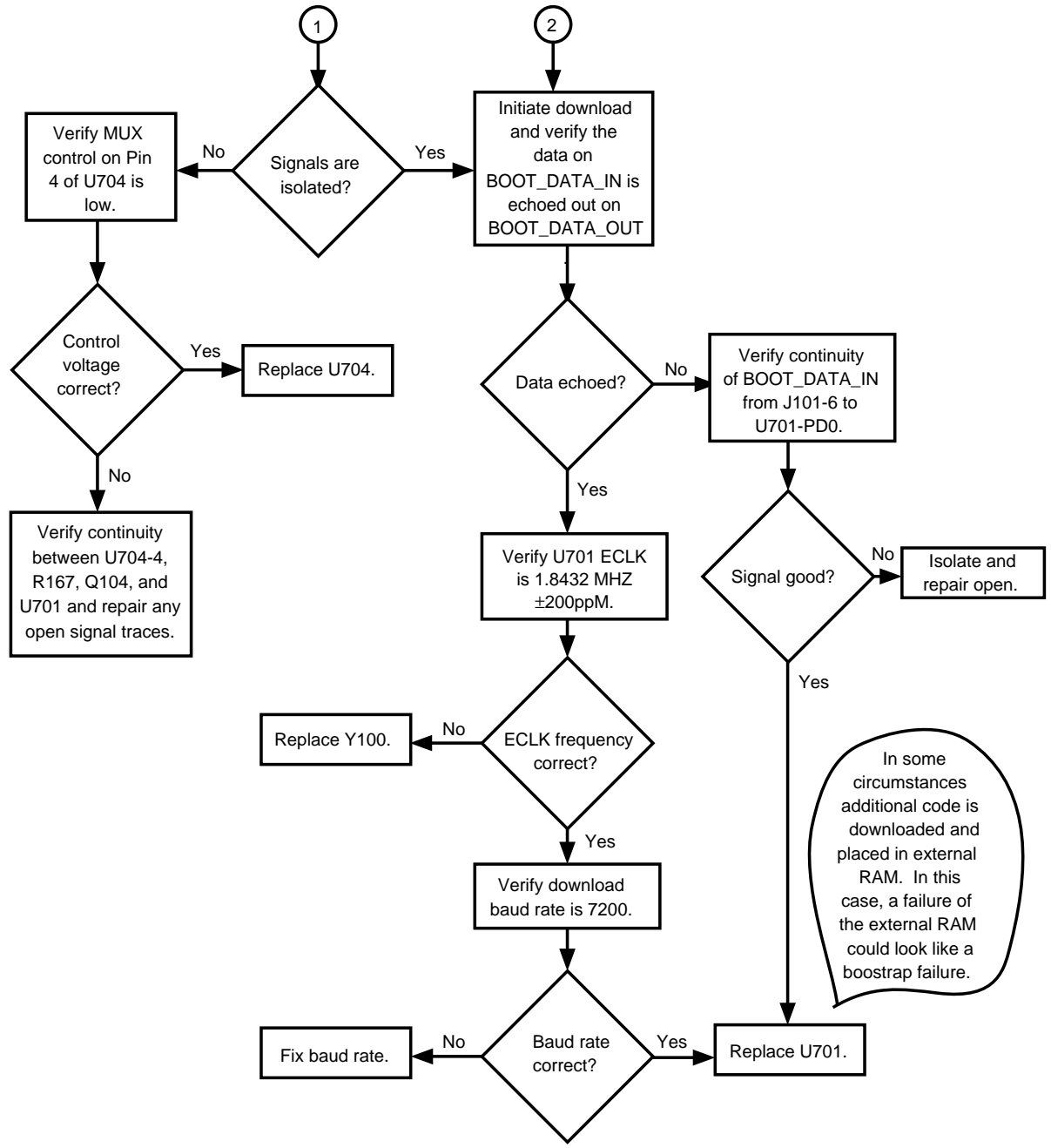
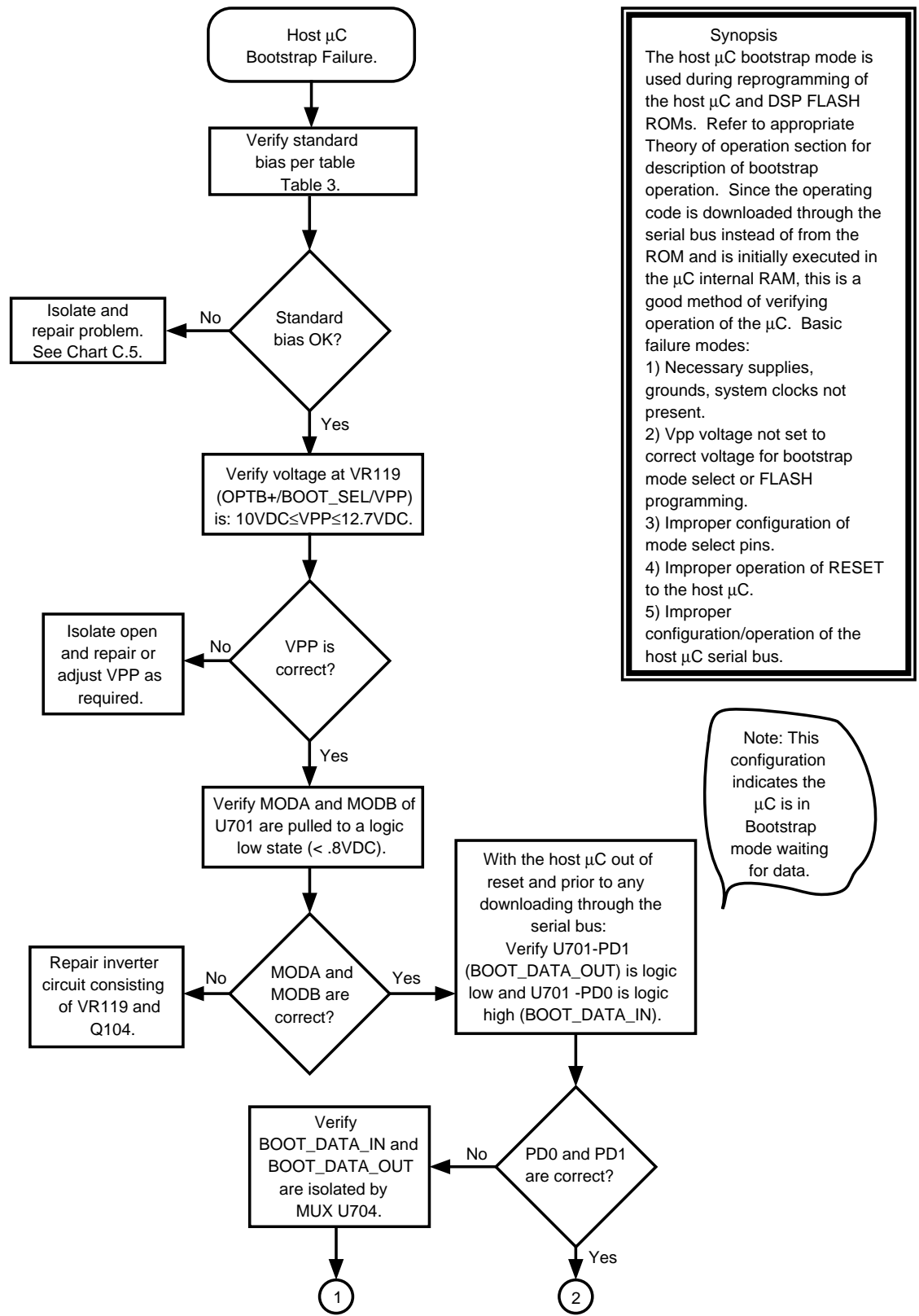
MAEPF-24395-O

Chart 2. VHF/UHF Radio Main



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Chart 3. Radio Power-up Fail



MAEPF-26017-O

Chart 4. Bootstrap Fail

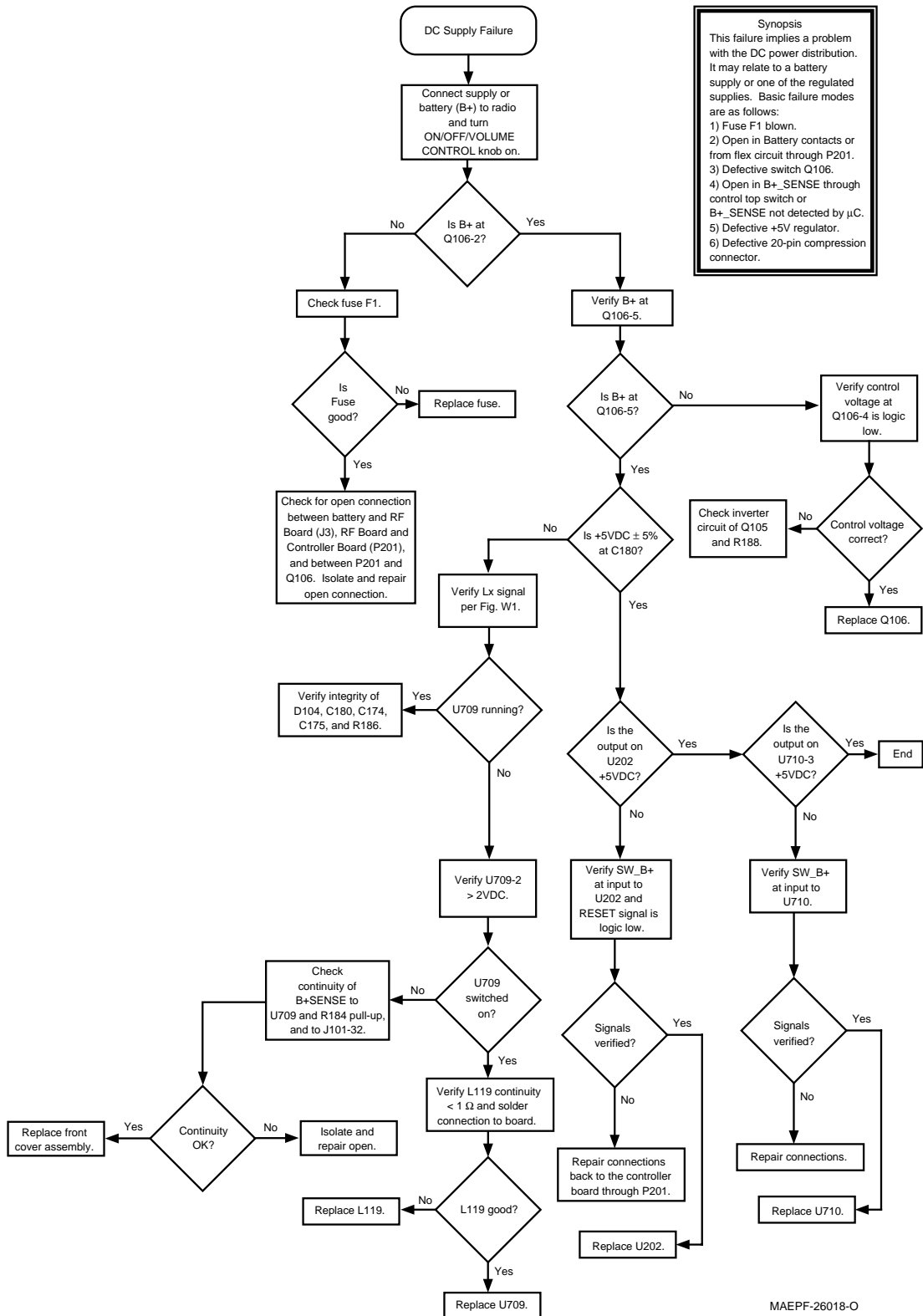
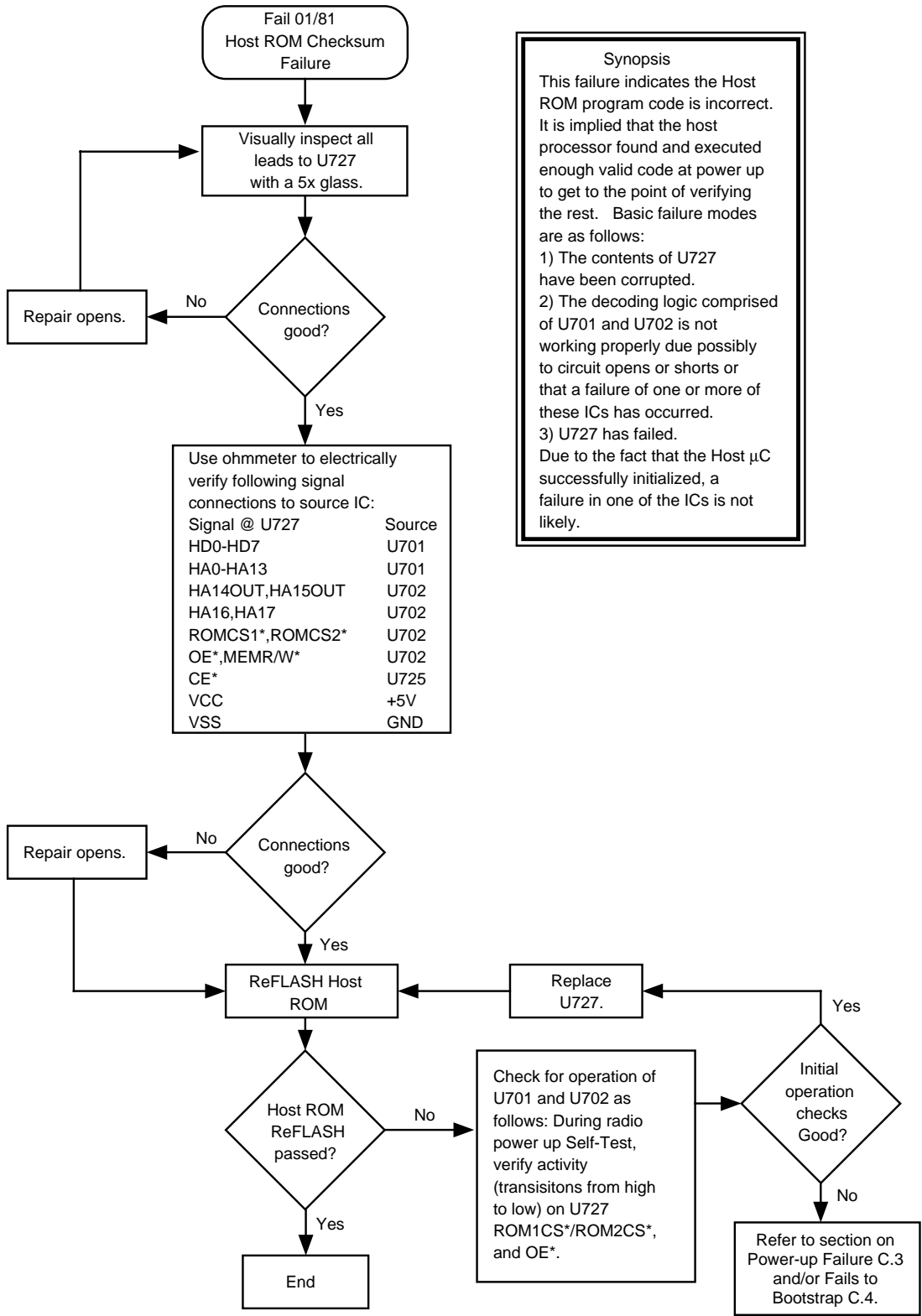


Chart 5. DC Supply Failure



**Synopsis**

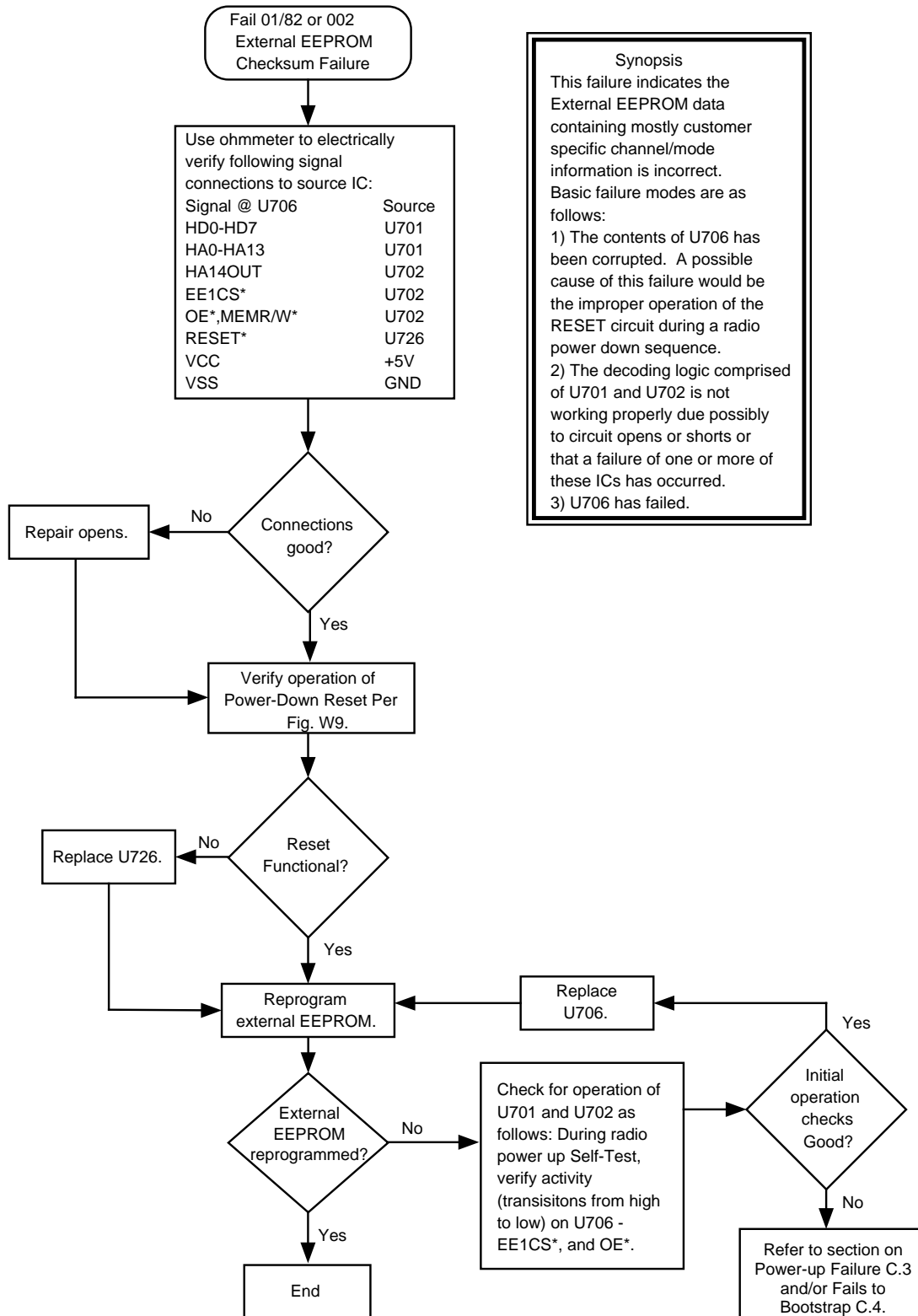
This failure indicates the Host ROM program code is incorrect. It is implied that the host processor found and executed enough valid code at power up to get to the point of verifying the rest. Basic failure modes are as follows:

- 1) The contents of U727 have been corrupted.
- 2) The decoding logic comprised of U701 and U702 is not working properly due possibly to circuit opens or shorts or that a failure of one or more of these ICs has occurred.
- 3) U727 has failed.

Due to the fact that the Host  $\mu$ C successfully initialized, a failure in one of the ICs is not likely.

Chart 6. 01/81 Host ROM Checksum Failure





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Chart 7. 01/82 or 002, External EEPROM Checksum Failure

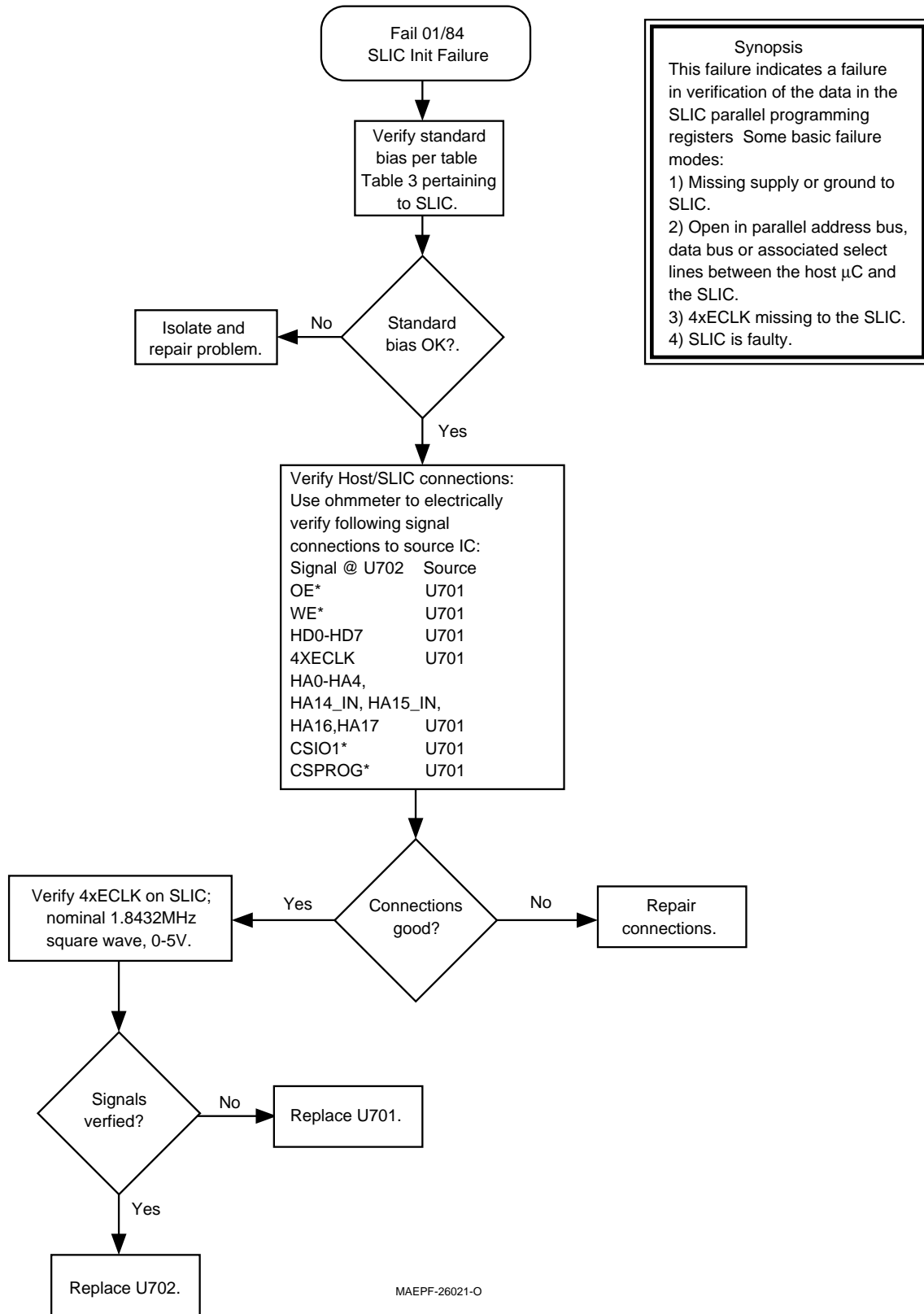
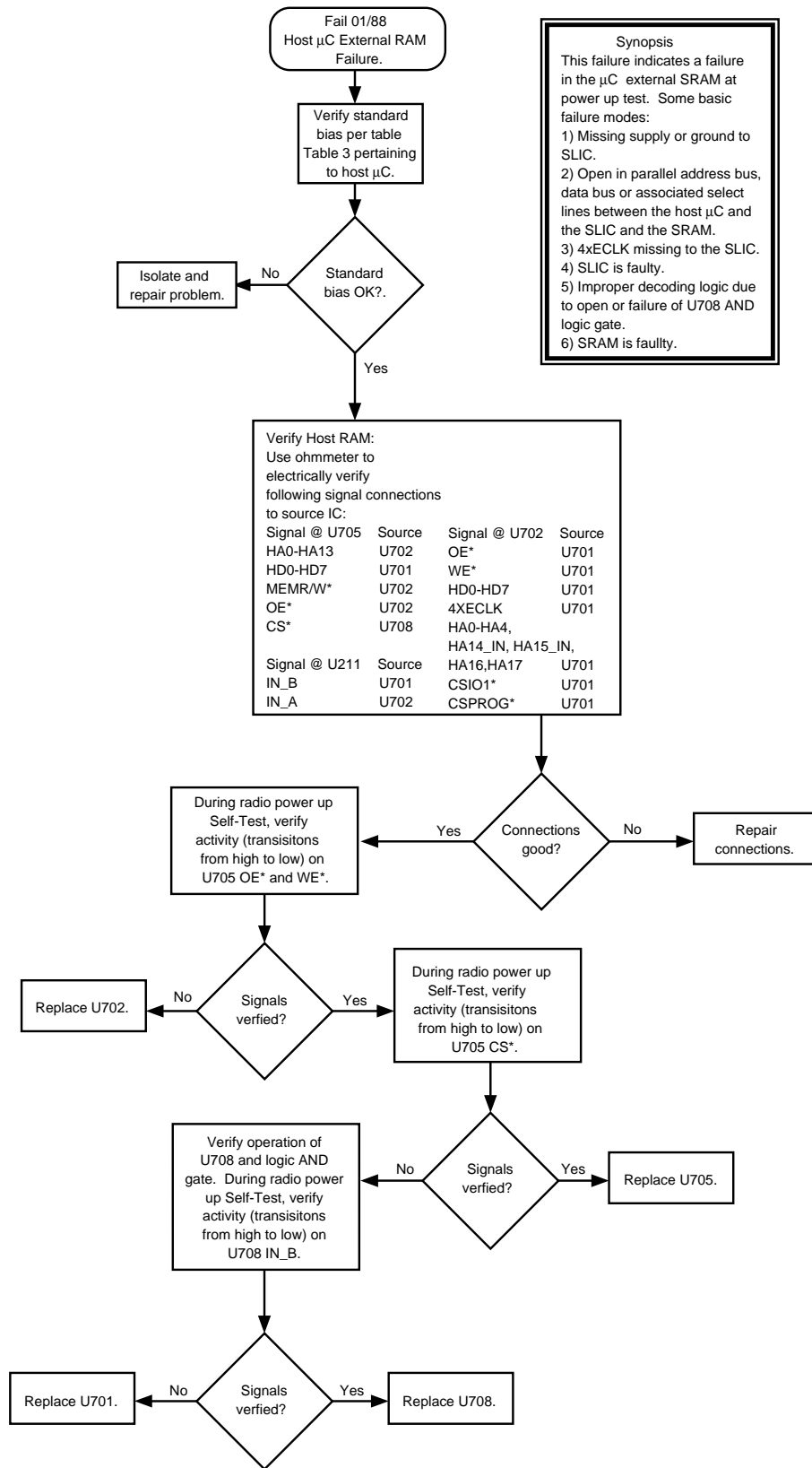
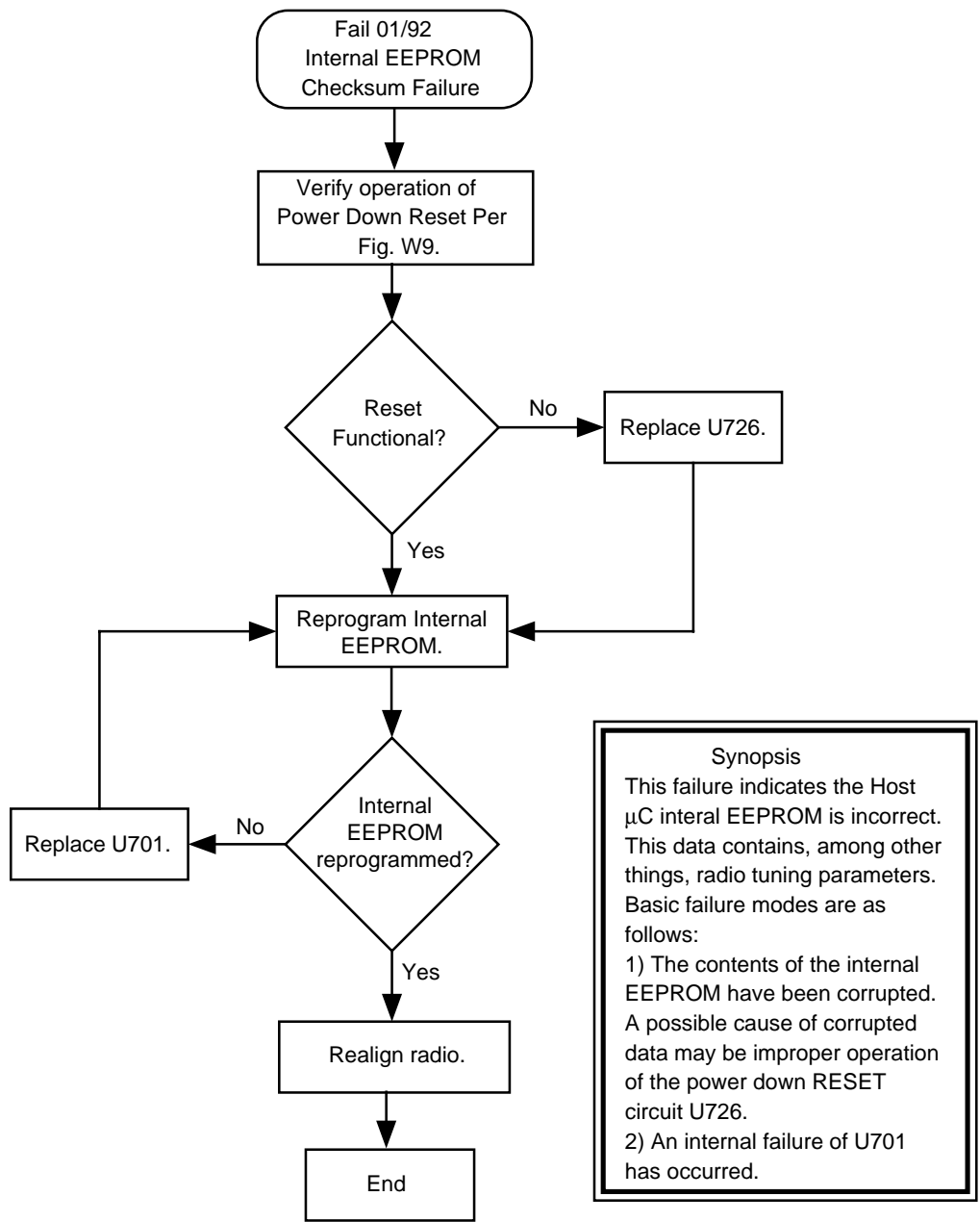


Chart 8. 01/84 SLIC Initialization Failure



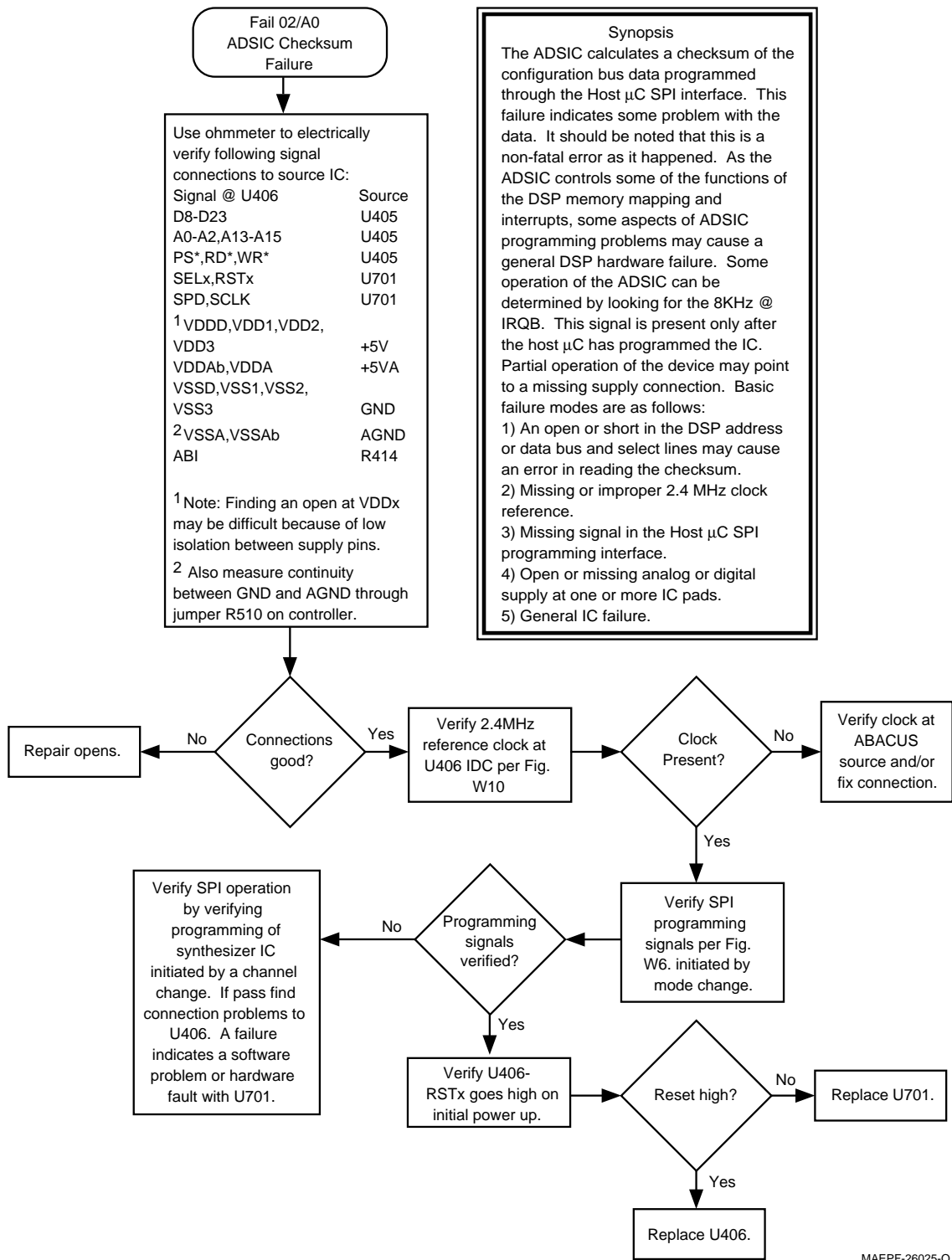
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Chart 9. 01/88 MCU (Host  $\mu$ C) External SRAM



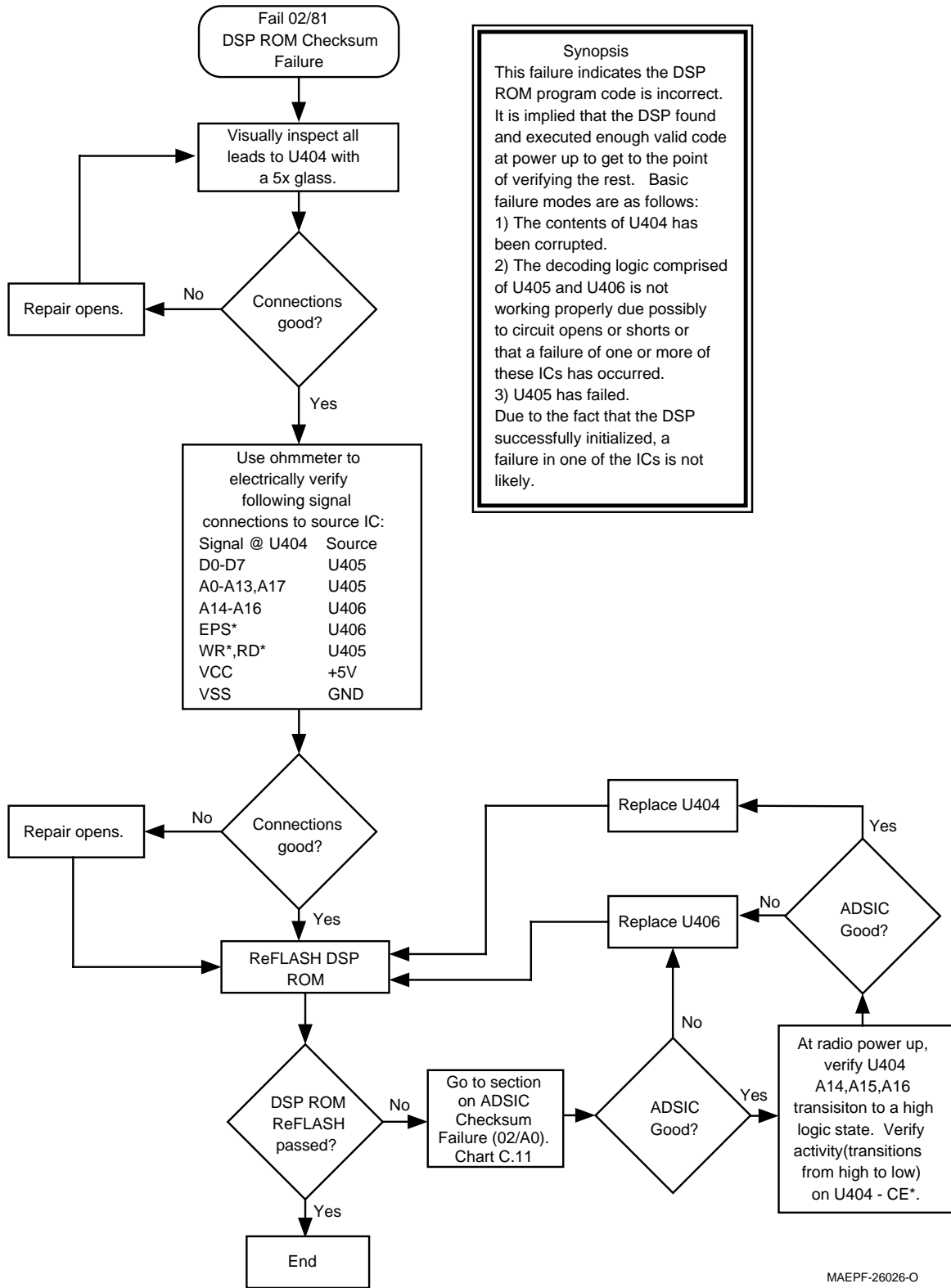
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Chart 10. 01/92, Internal EEPROM Checksum Failure



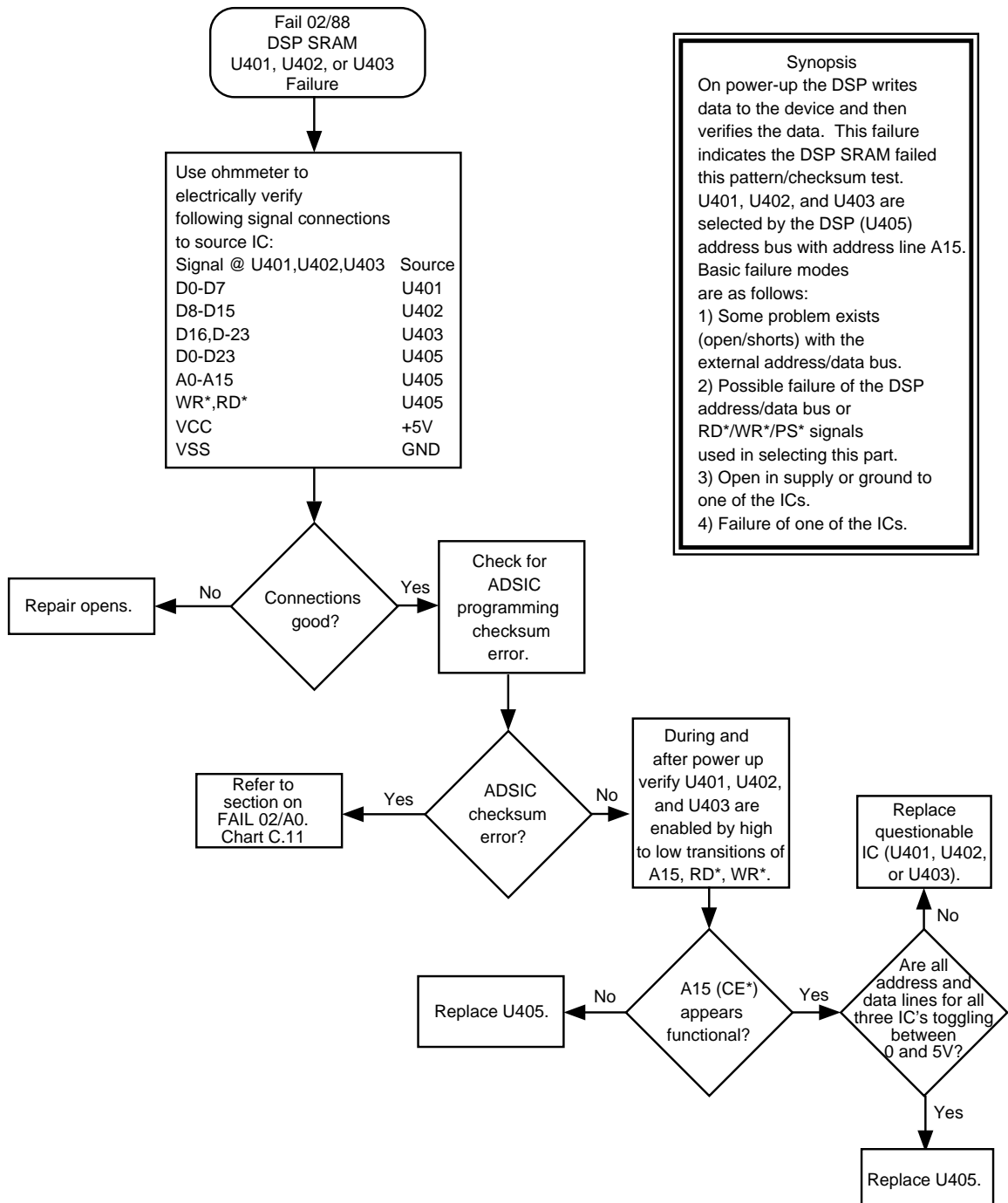
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Chart 11. 02/A0, ADSIC Checksum Failure



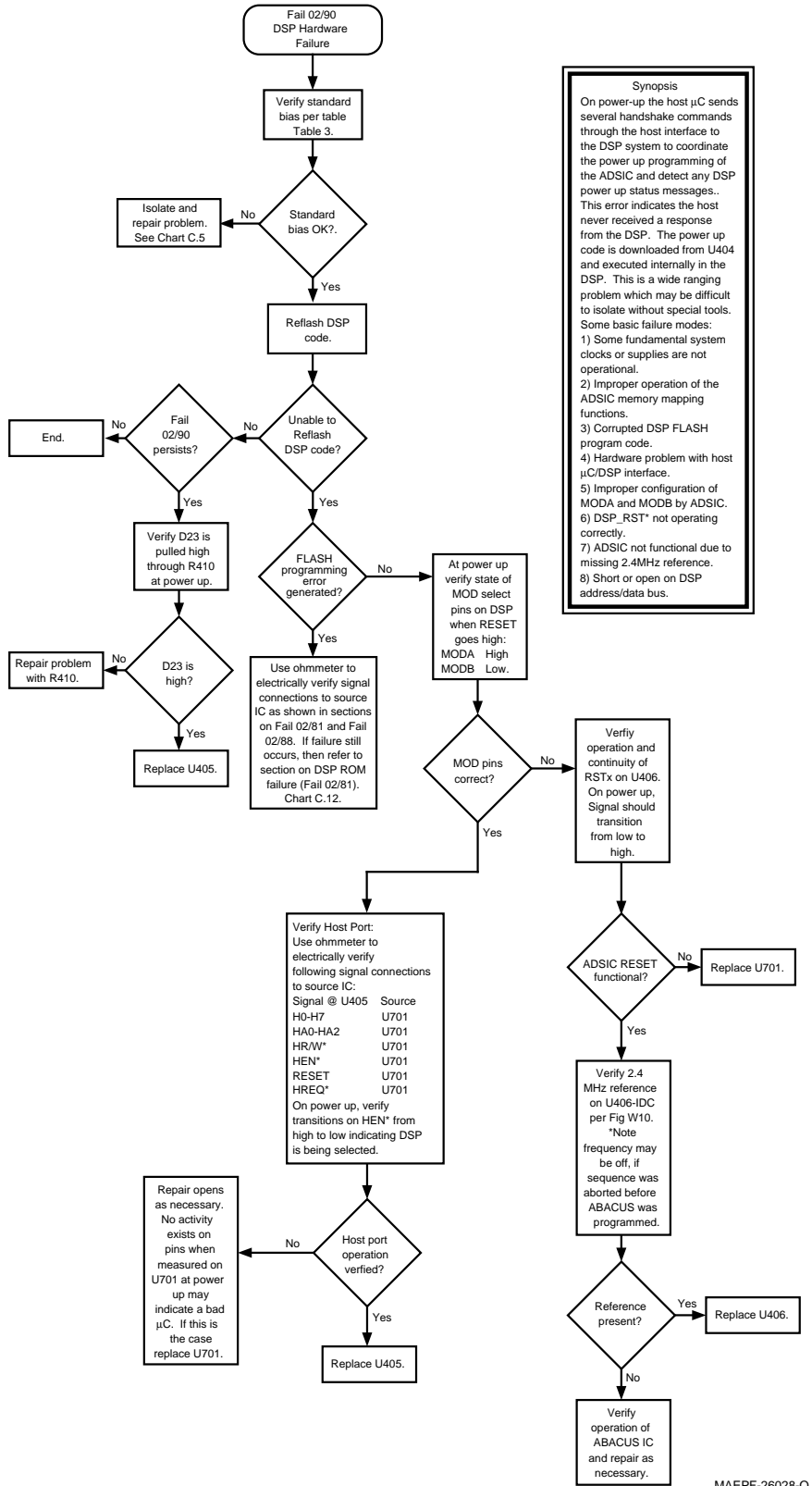
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Chart 12. 02/81, DSP ROM Checksum Failure



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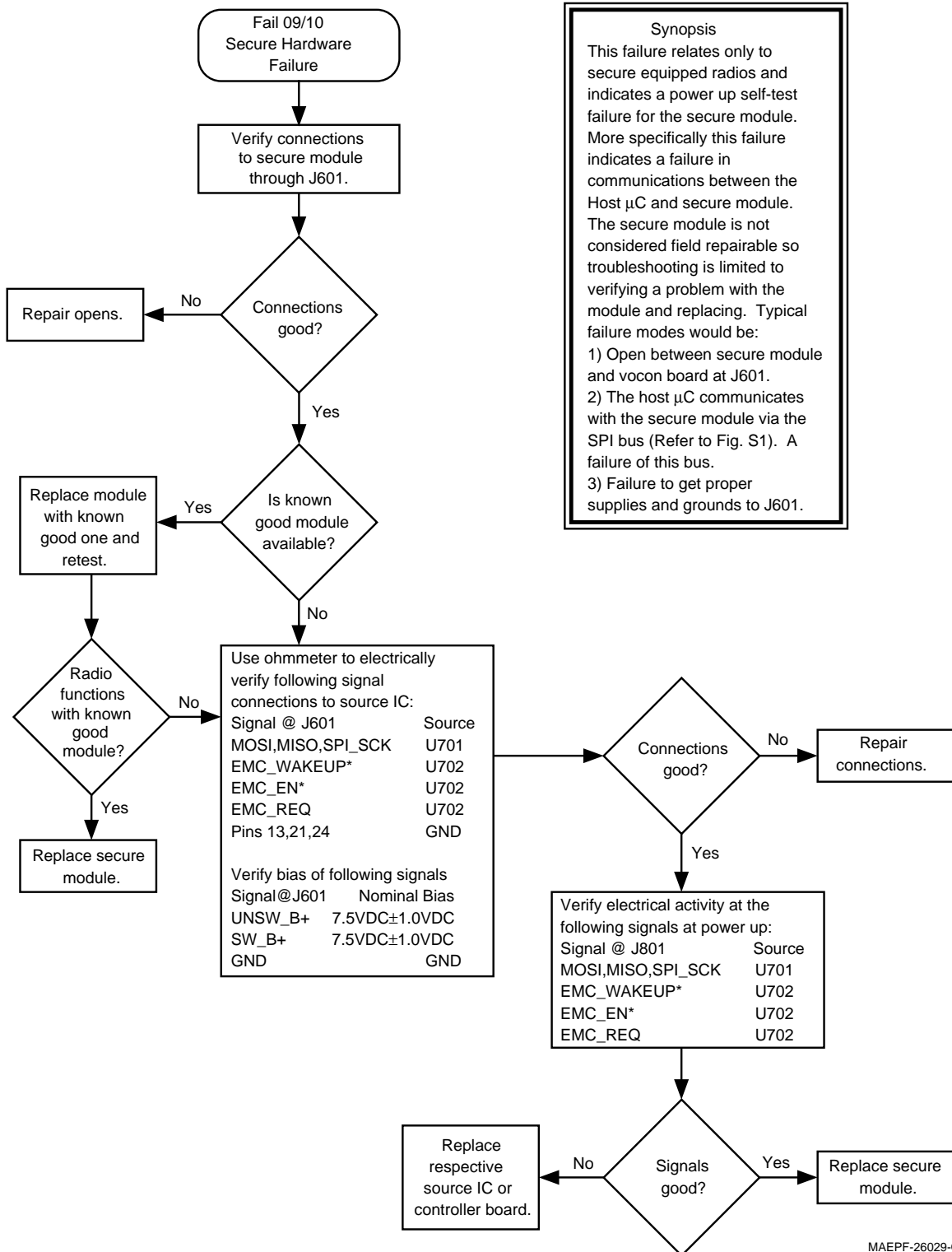
Chart 13. 02/88, DSP External SRAM Failure U414



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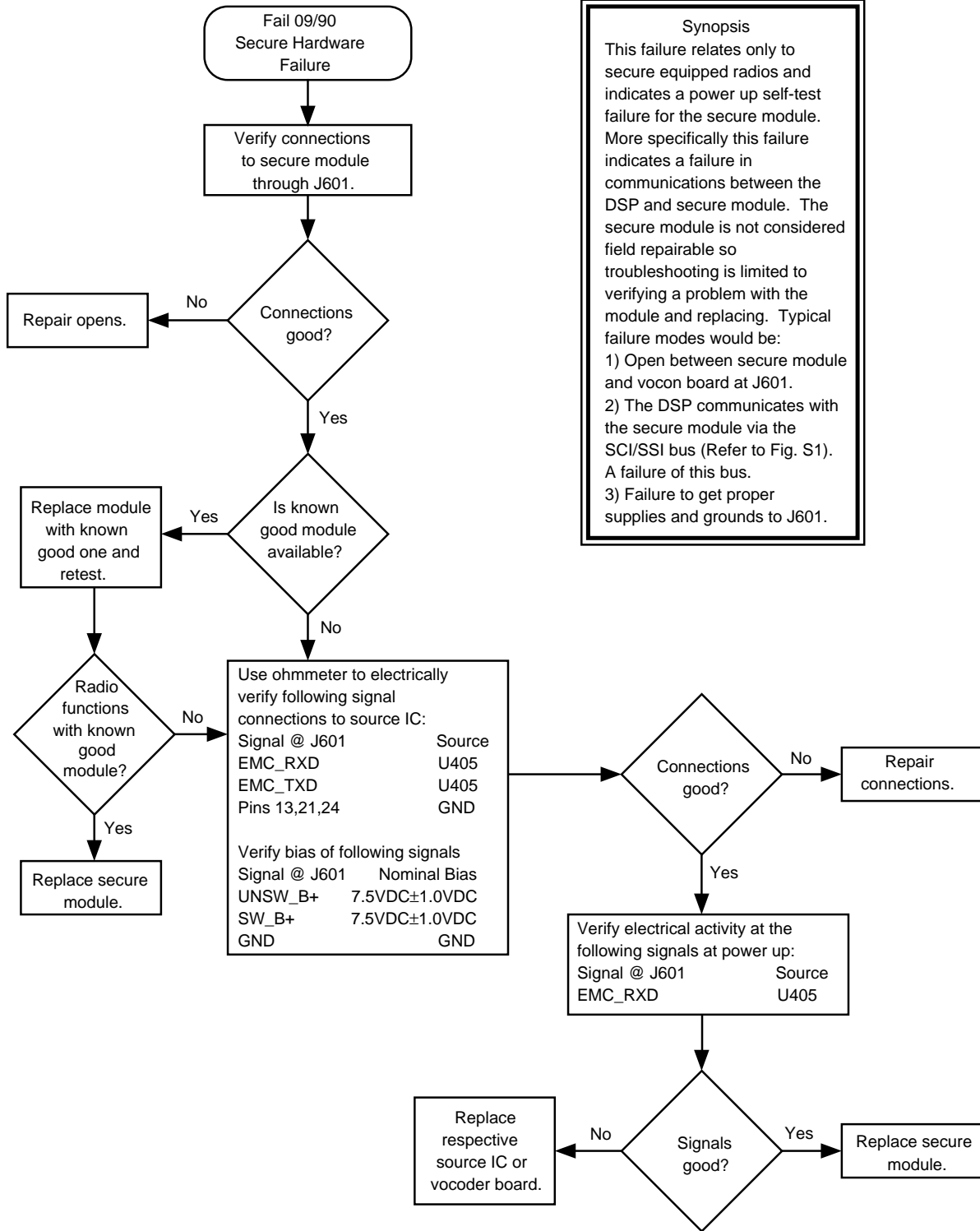
Chart 14. 02/90, General DSP Hardware Failure





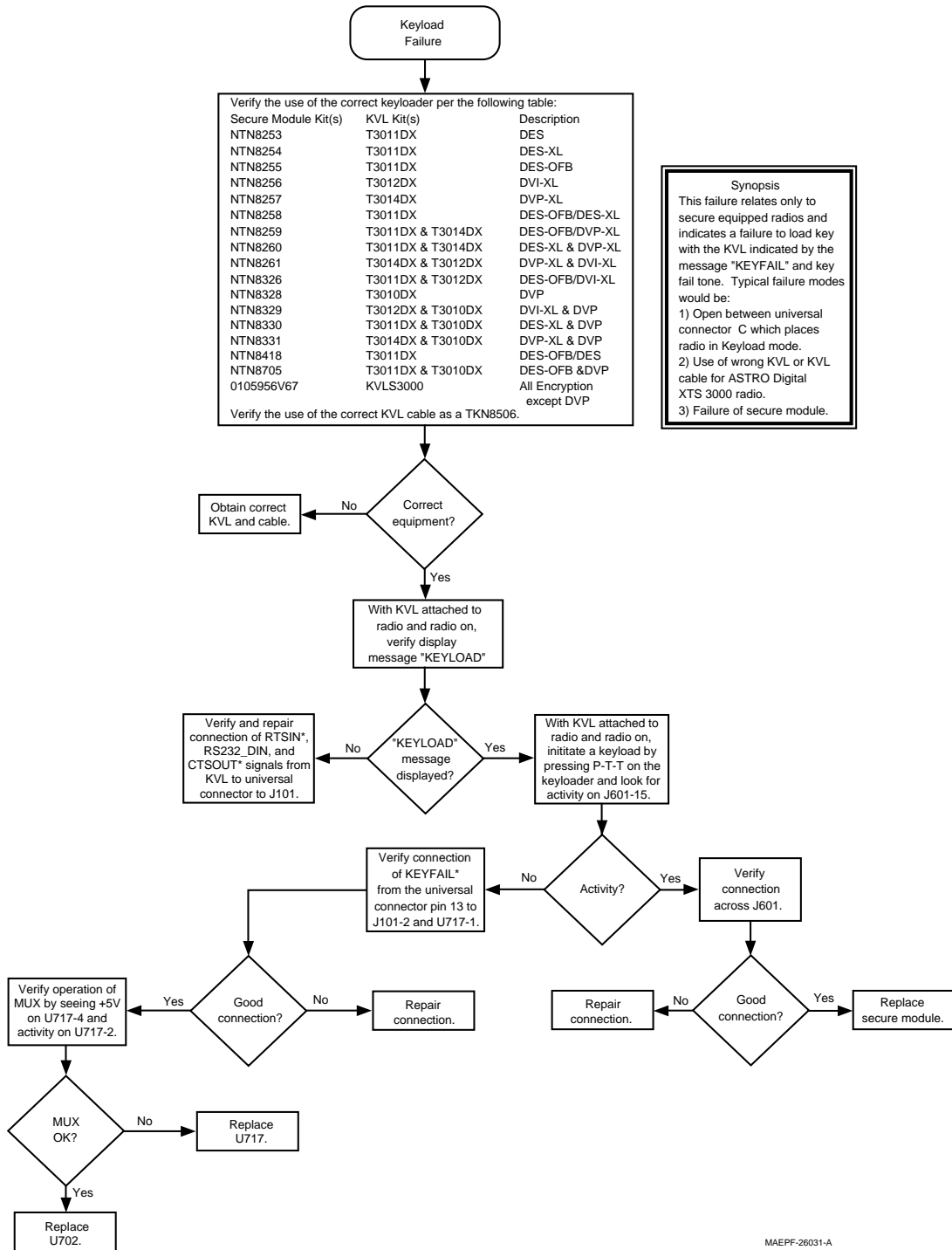
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Chart 15. 09/10, Secure Hardware failure



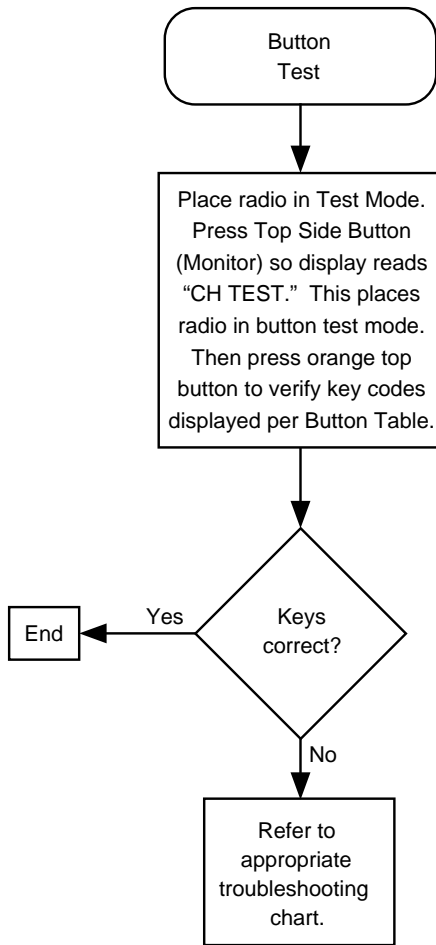
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Chart 16. 09/90, Secure Hardware Failure



MAEPF-26031-A

Chart 17. Key Load Fail

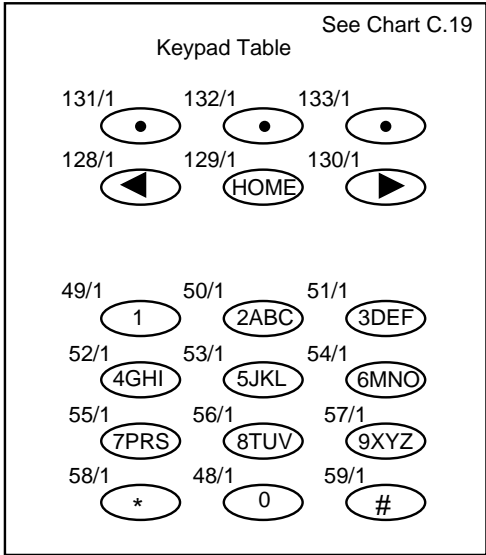


**Synopsis**

This chart relates to a failure in the button functions. Basic Failure modes are as follows:

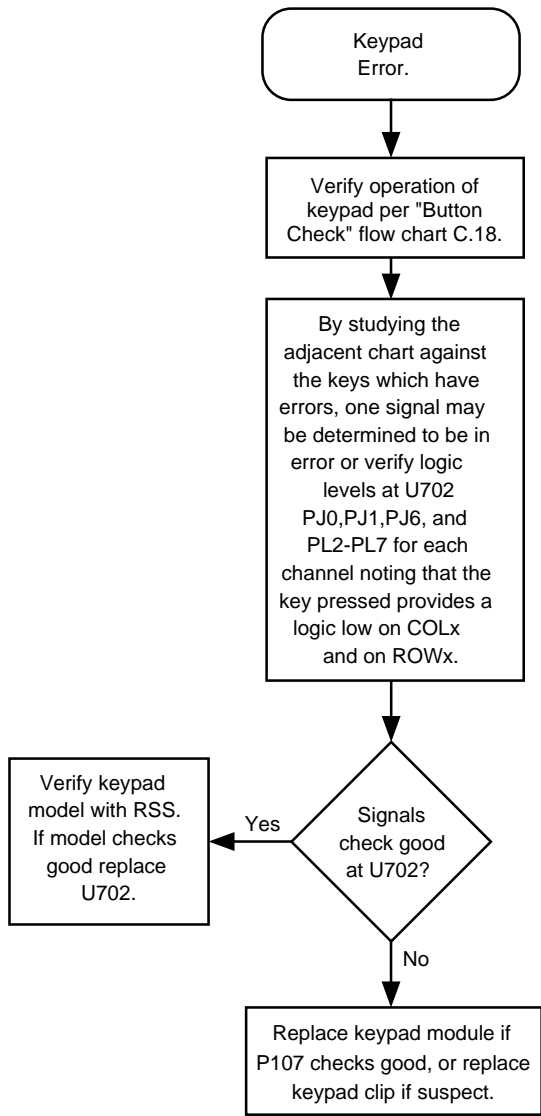
- 1) Failure in control top/ptt or keypad flex assembly.
- 2) Bad connection.
- 3) Defective switches or pads.
- 4) Defective A/D port in host  $\mu$ C.

Button Table		
<u>Button</u>	<u>Code</u>	<u>Chart</u>
PTT	1/ 0-1	C.22
Top Button (Emergency)	3/ 0-1	C.22
Top Side Button (Monitor)	96/ 0-1	C.22
Side Button 1 (RAT 1)	97/ 0-1	C.22
Side Button 2 (RAT 2)	98/ 0-1	C.22
Secure/Clear Switch	65/ 0-1	C.22
Zone/Channel Select (Frequency)	4/ 0-15	C.21
Volume Control Knob	2/ 0-255	C.20
Toggle Switch	67/ A=0, B=1, C=2	



MAEPF-26032-O

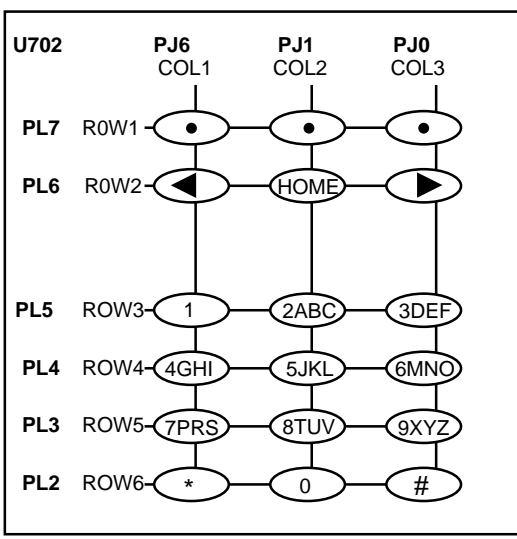
Chart 18. Button Test



**Synopsis**

This chart relates to a failure in reading the keypad. Basic Failure modes are as follows:

- 1) Failure in flex circuit.
- 2) Bad connection.
- 3) Defective keypad.
- 4) Defective port in SLIC.



MAEPF-26033-O

Chart 19. Keypad Error

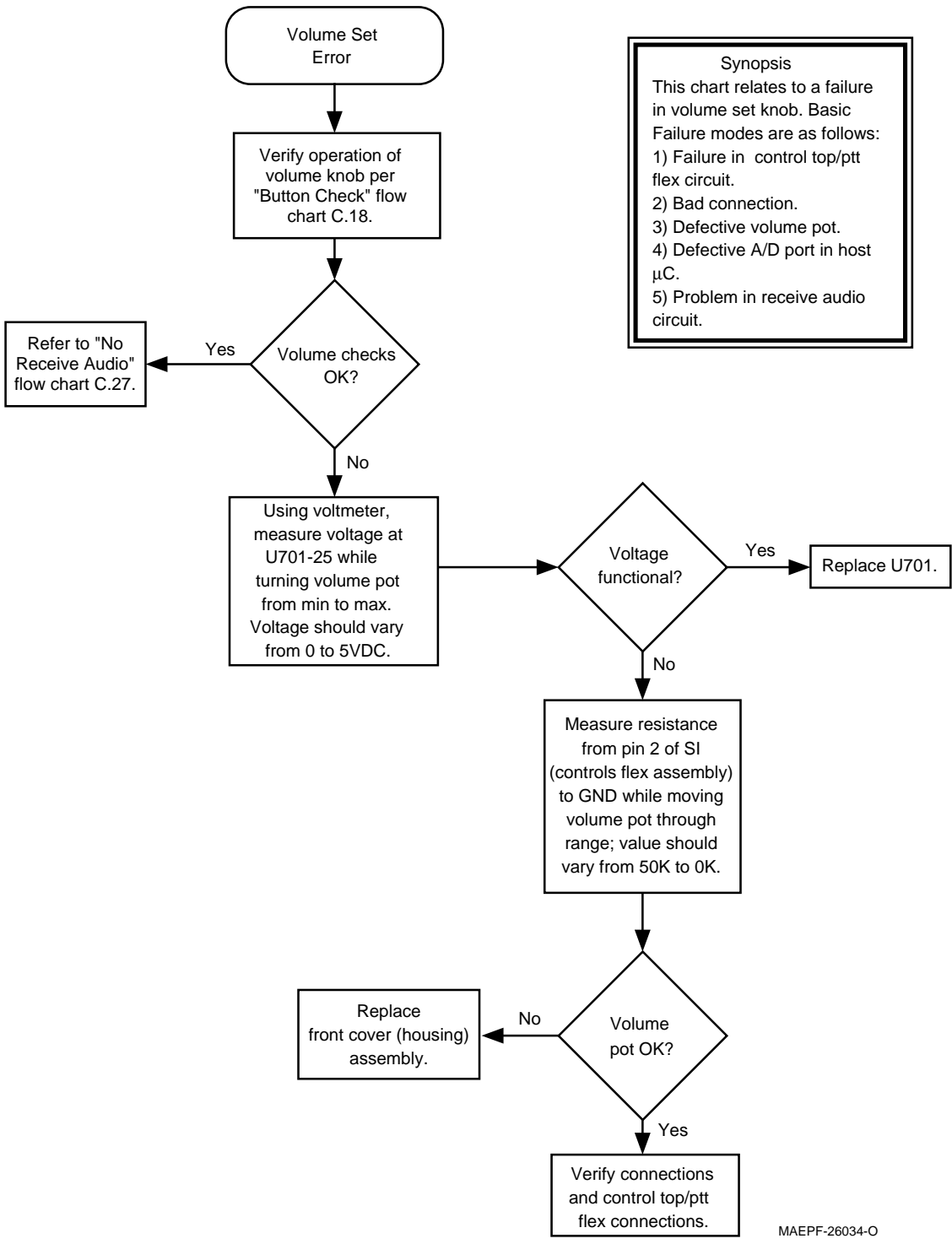
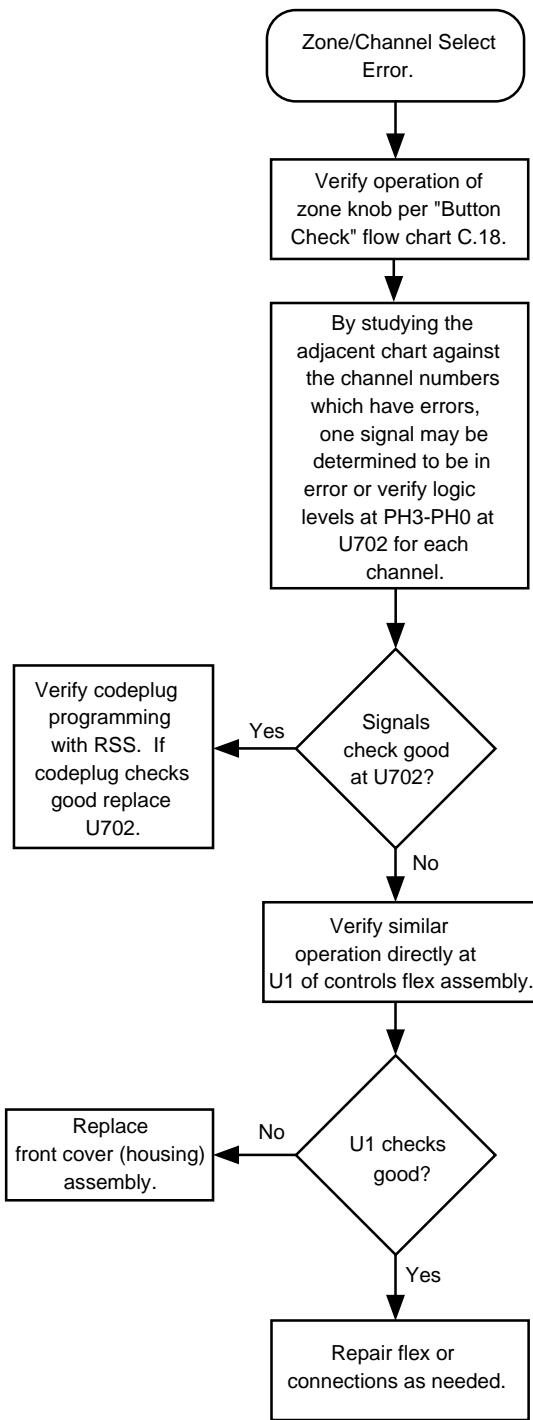


Chart 20. Volume Set Error



**Synopsis**

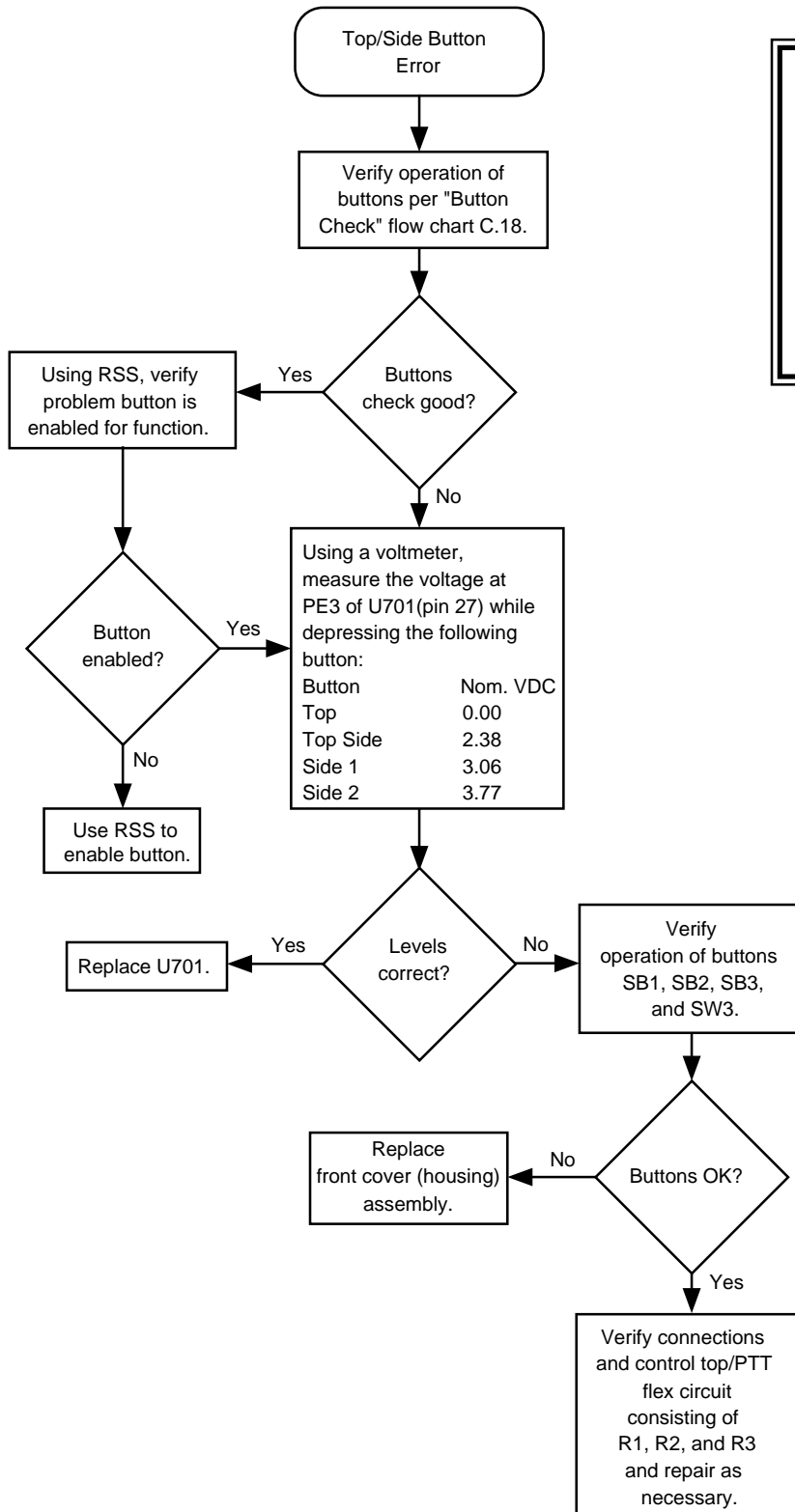
This chart relates to a failure in reading the zone/channel select knob. Basic Failure modes are as follows:

- 1) Failure in flex circuit.
- 2) Bad connection.
- 3) Defective switch.
- 4) Defective port in SLIC.

Channel	RTA3	RTA2	RTA1	RTA0
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

MAEPF-26035-O

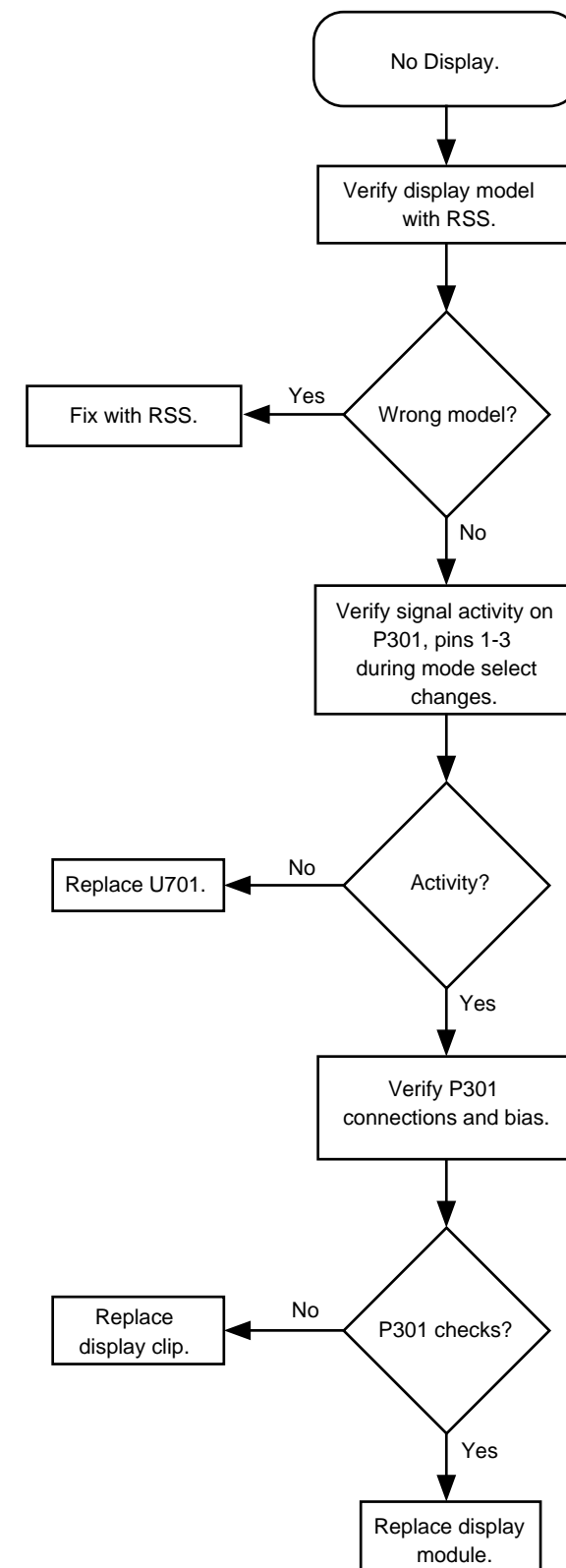
Chart 21. Zone/Channel select Error



**Synopsis**  
 This chart relates to a failure in reading the buttons: Top, Top Side, Side Button 1, or Side Button 2. Basic Failure modes are as follows:  
 1) Failure in controls flex circuit.  
 2) Bad connection.  
 3) Defective switch.  
 4) Defective A/D port in host  $\mu$ C.

Chart 22. Top/Side Button Error

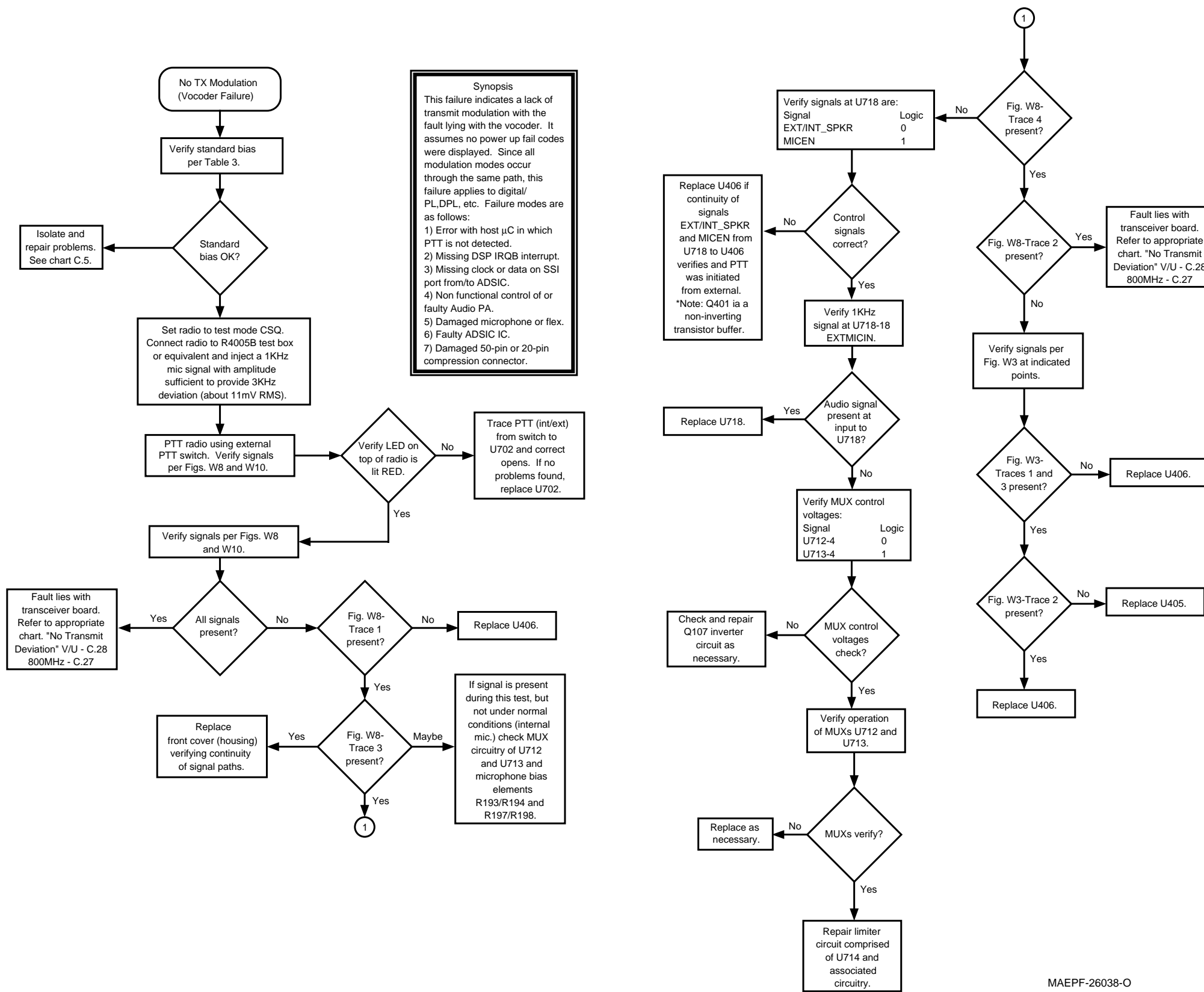




Synopsis  
 This chart relates to a failure in the display. The display is considered not field repairable and must be replaced as a unit. Basic Failure modes are as follows:  
 1) Non-display model radio.  
 2) Bad connection.  
 3) Defective  $\mu$ C.

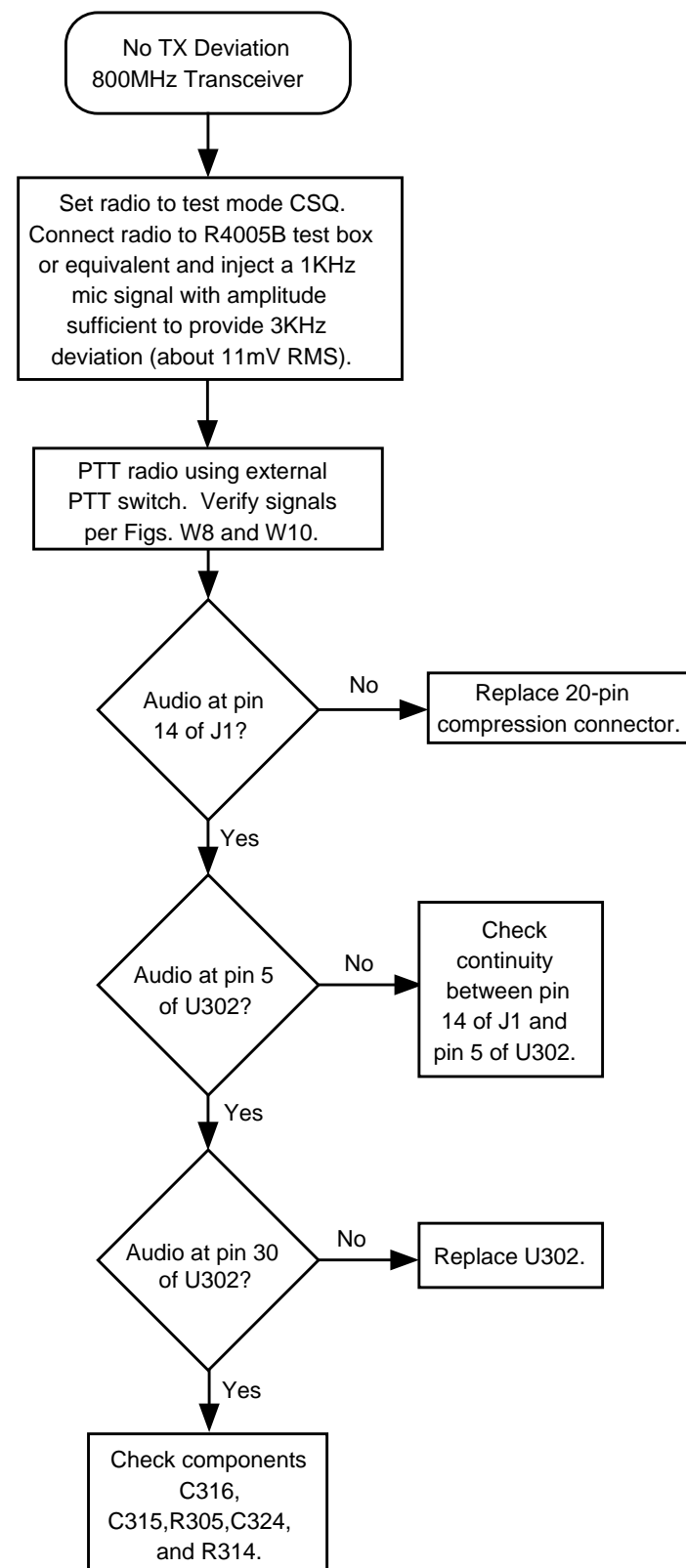
MAEPF-26037-O

Chart 23. Radio Power-up Fail



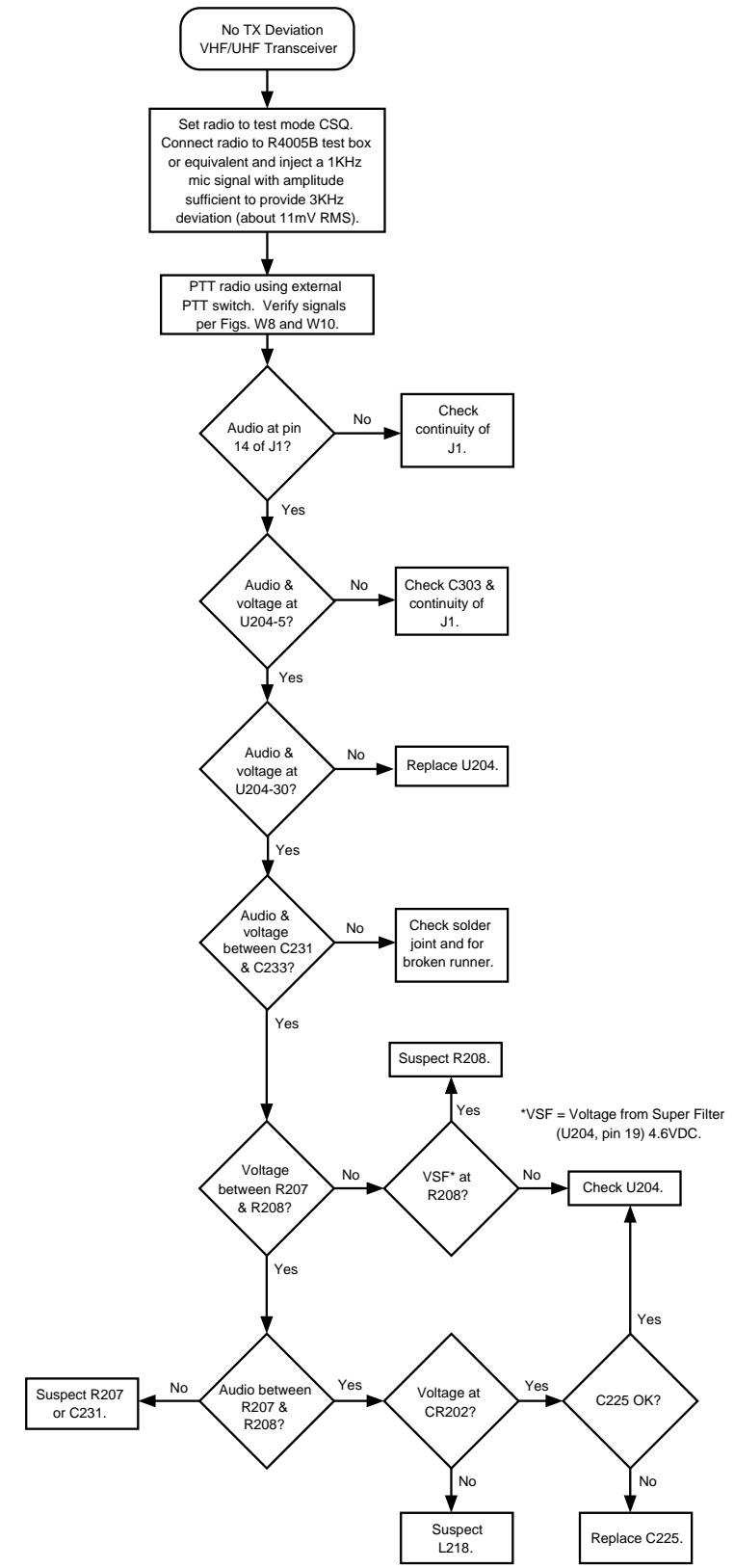
MAEPF-26038-O

Chart 24. Bootstrap Fail



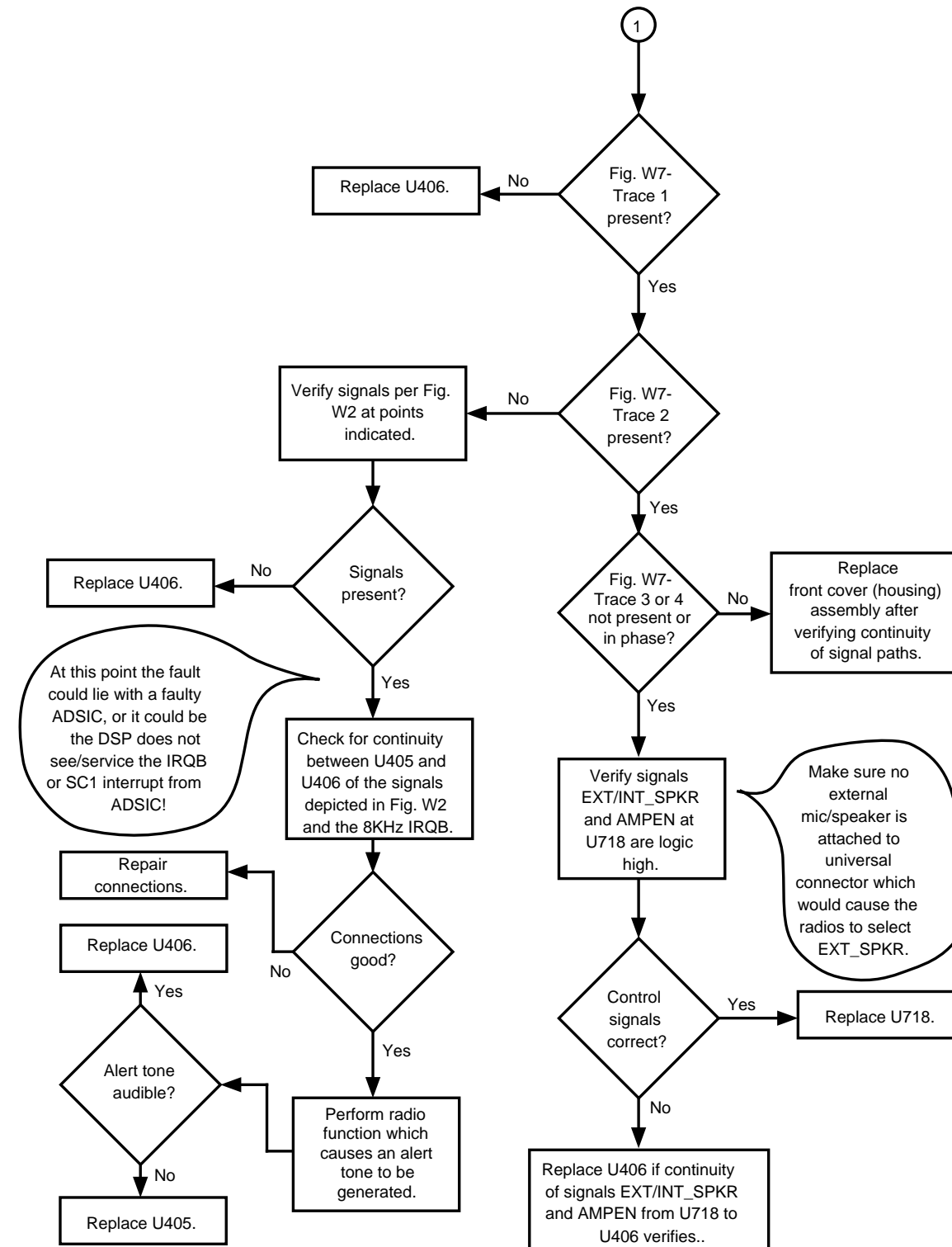
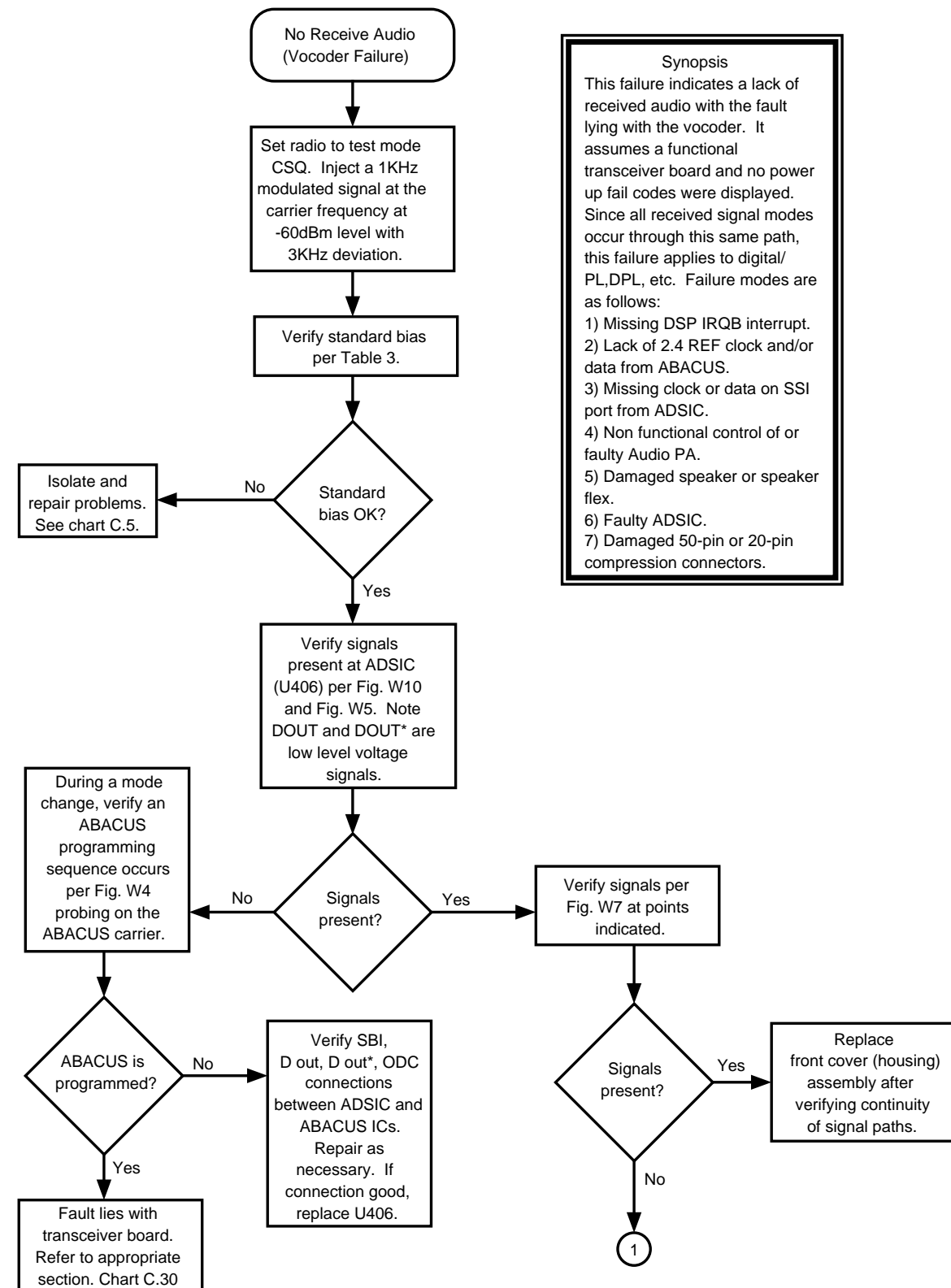
MAEPF-26039-O

Chart 25. 800 MHz No TX Deviation



MAEPF-26040-O

Chart 26. VHF/UHF No TX Deviation



MAEPF-26041-O

Chart 27. No RX Audio

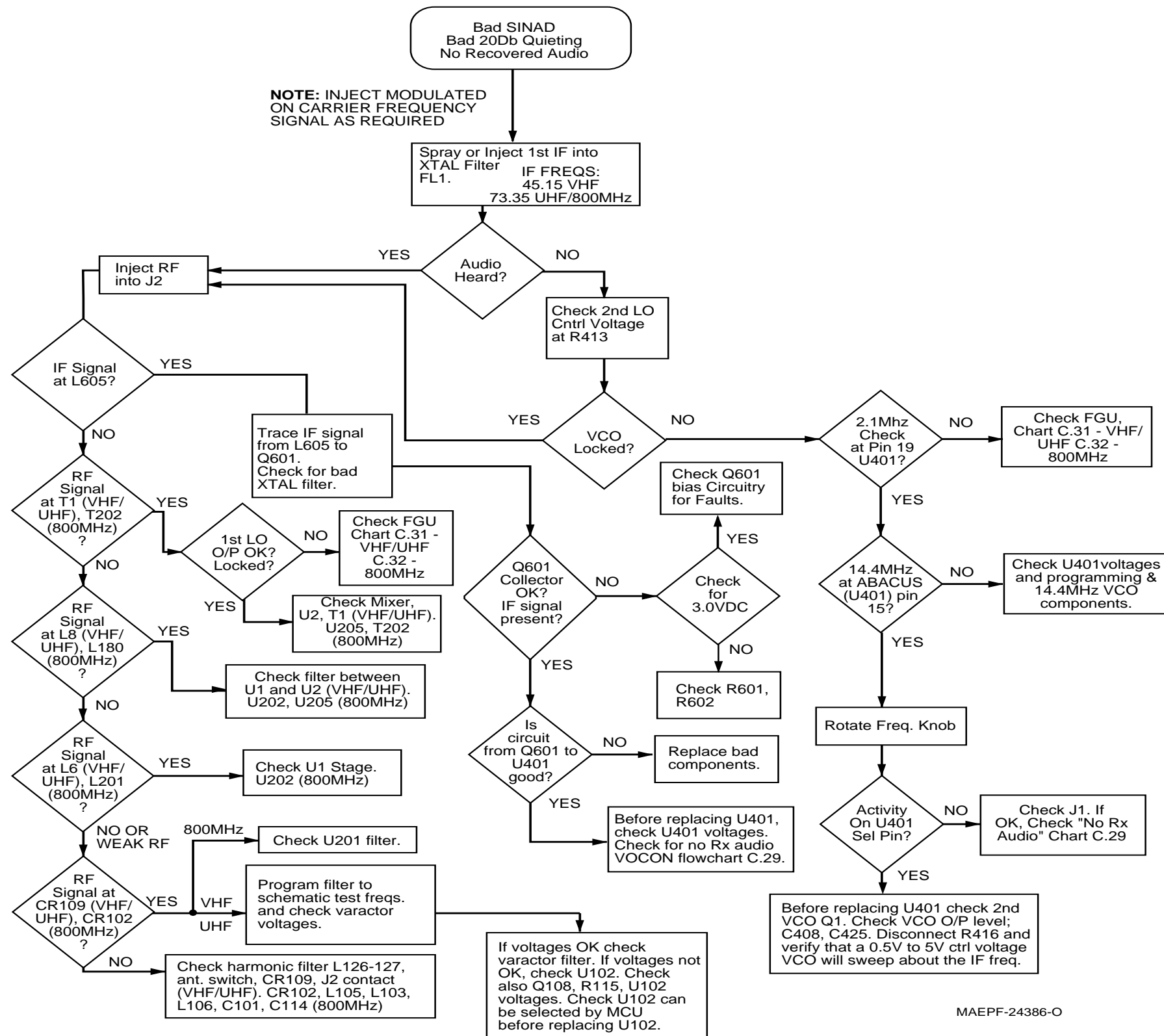


Chart 28. VHF/UHF/800 MHz Receiver RF

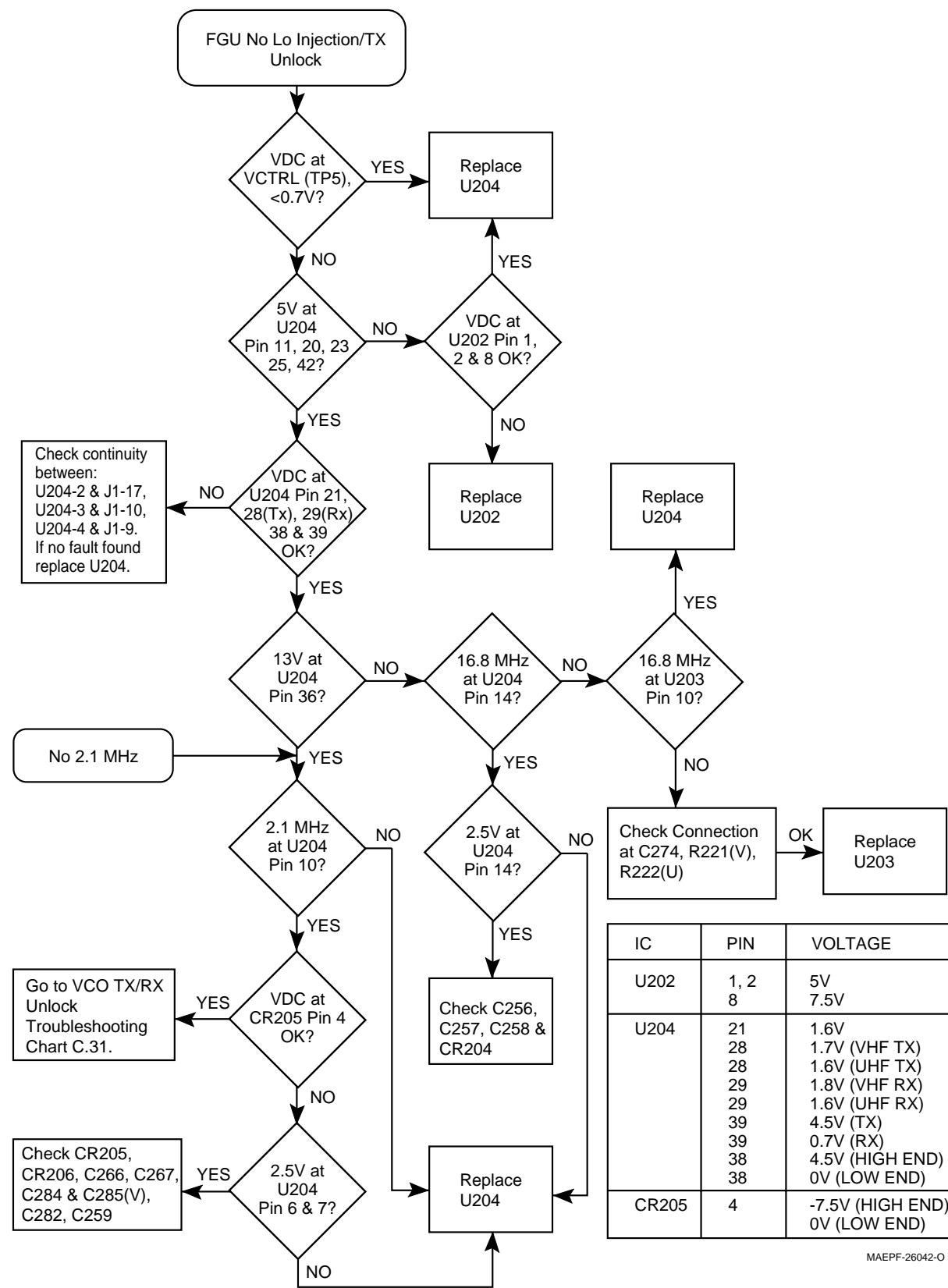


Chart 29. VHF/UHF Frequency Generation Unit (FGU)

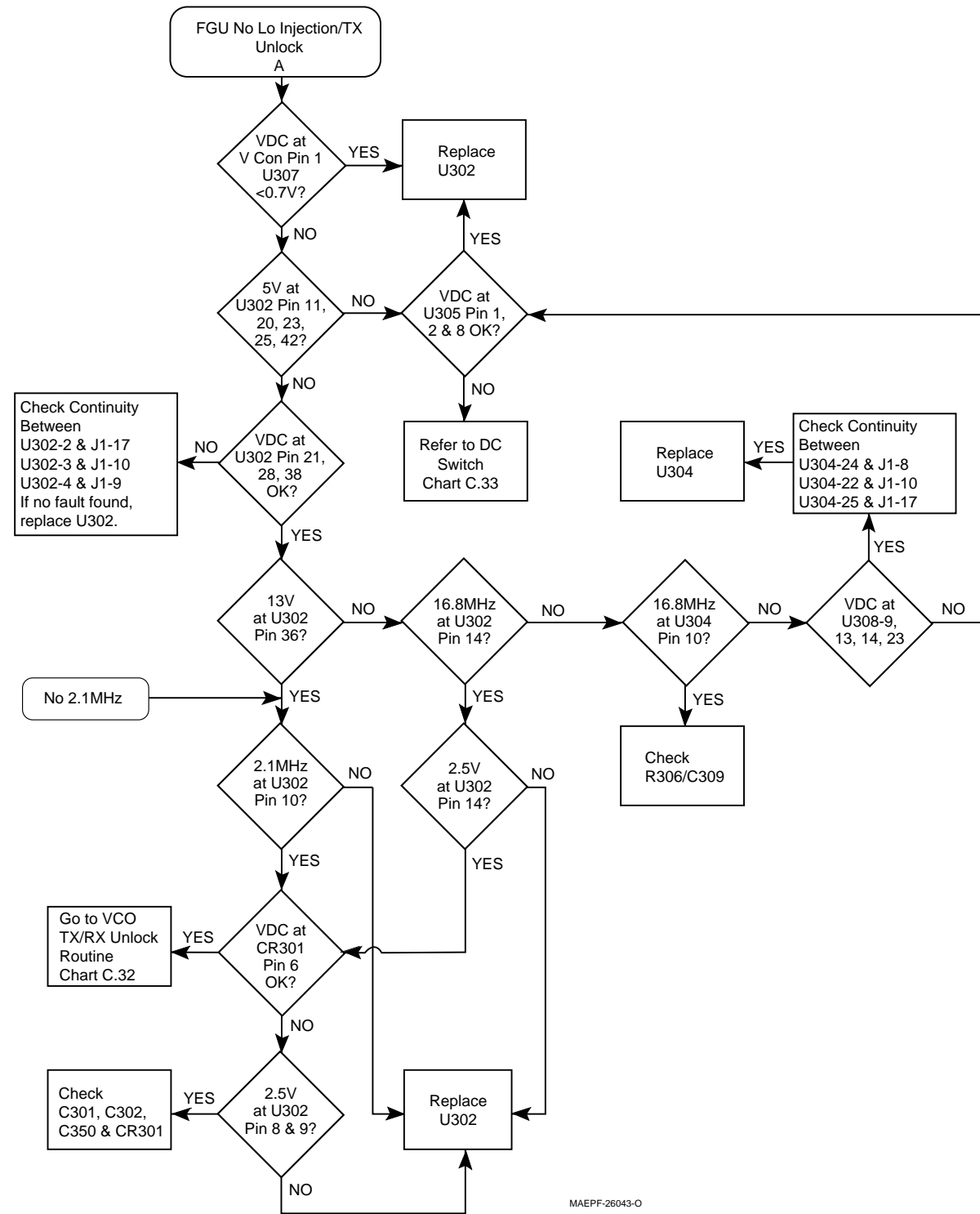
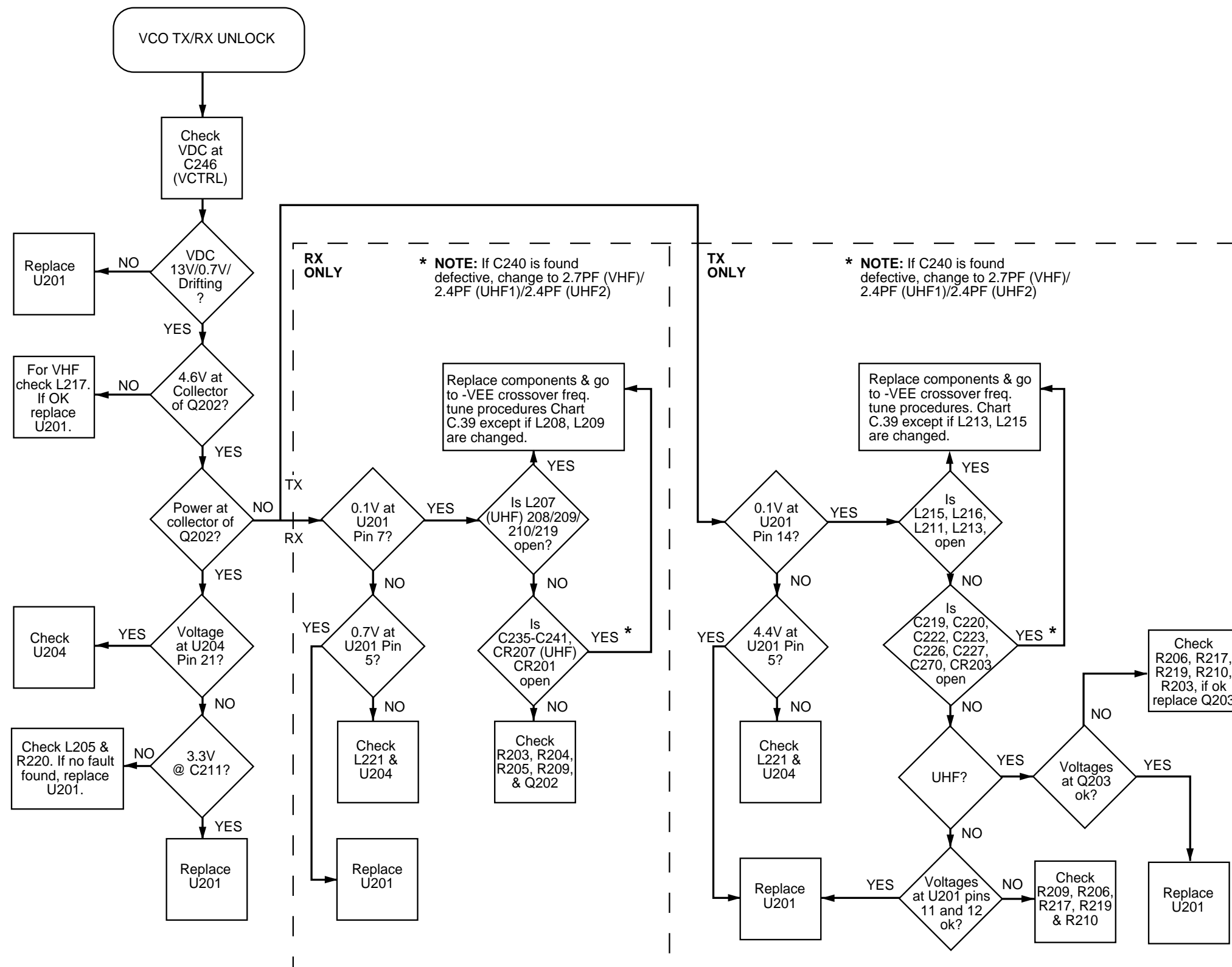
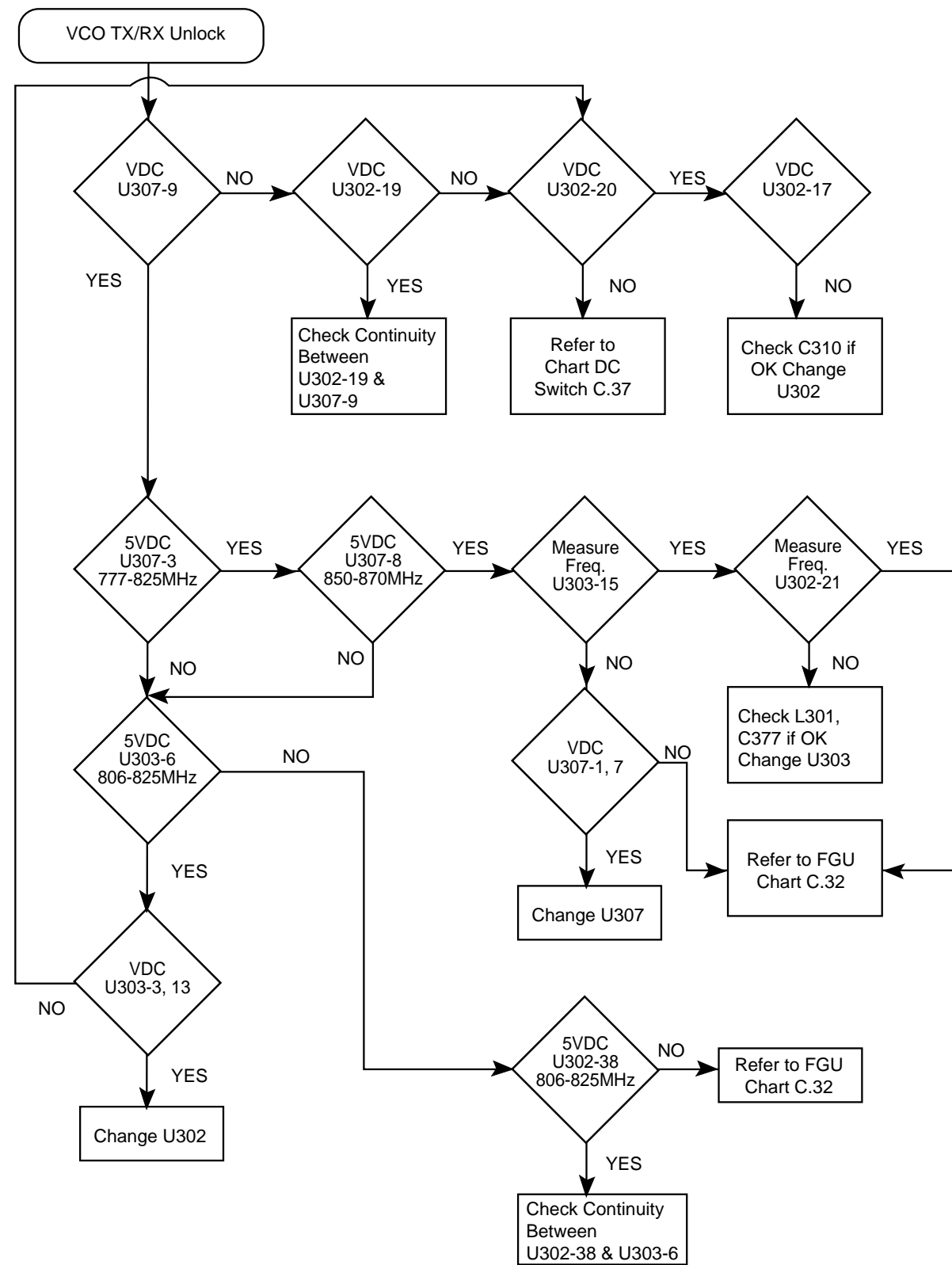


Chart 30. 800 MHz Frequency Generation Unit (FGU)



MAEPF-24387-O

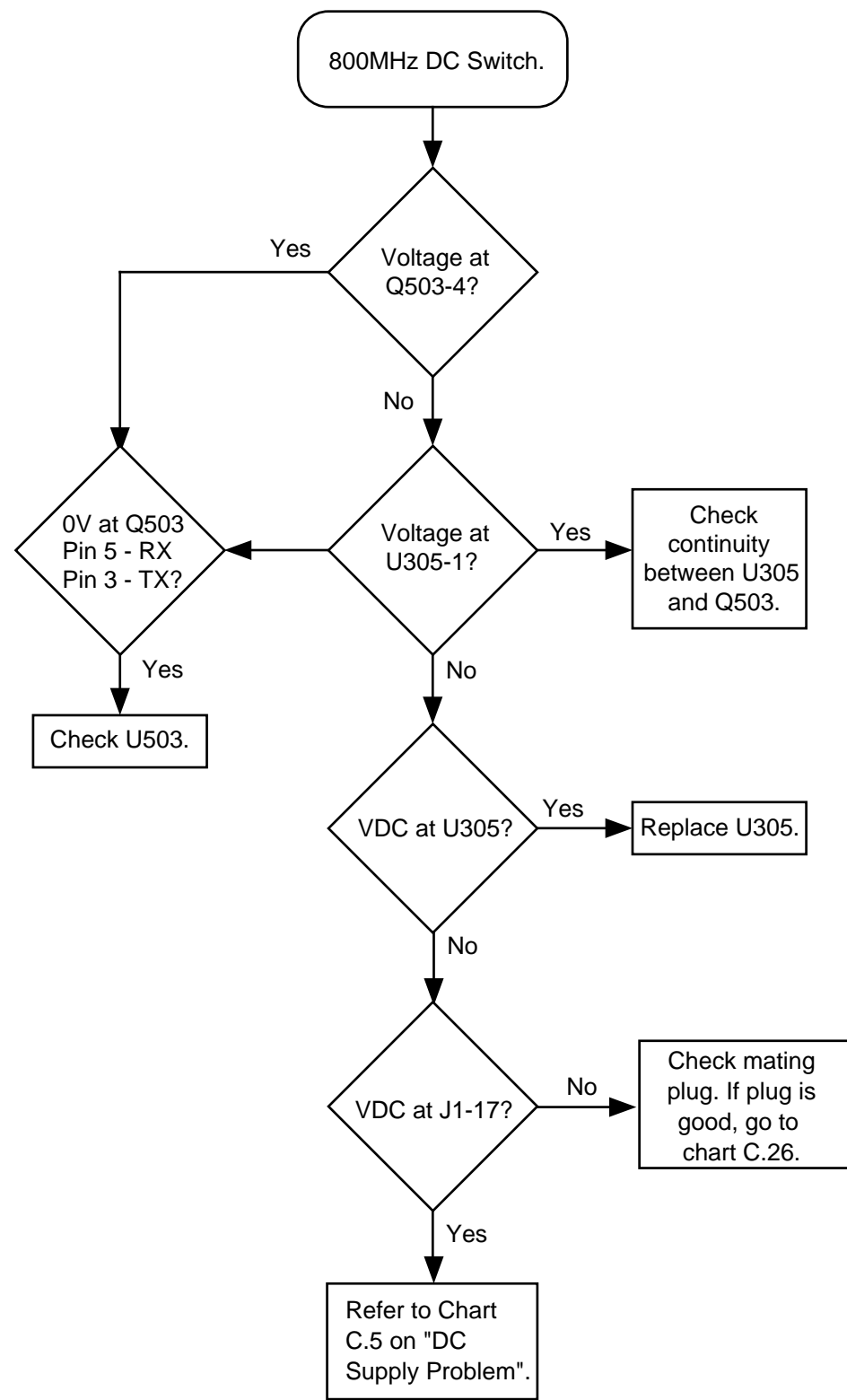
Chart 31. VHF/UHF Voltage Controlled Oscillator (VCO)



MAEPF-24388-O

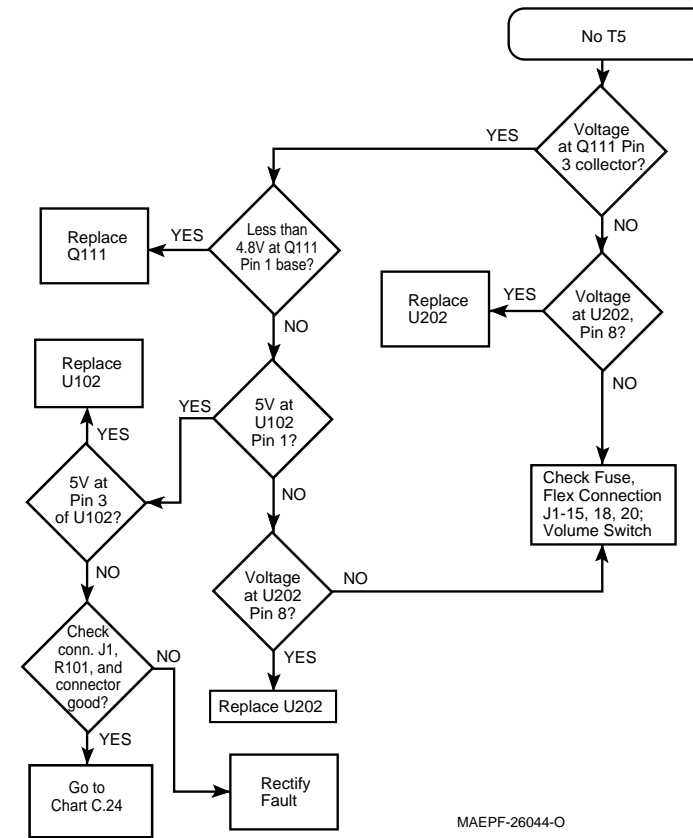
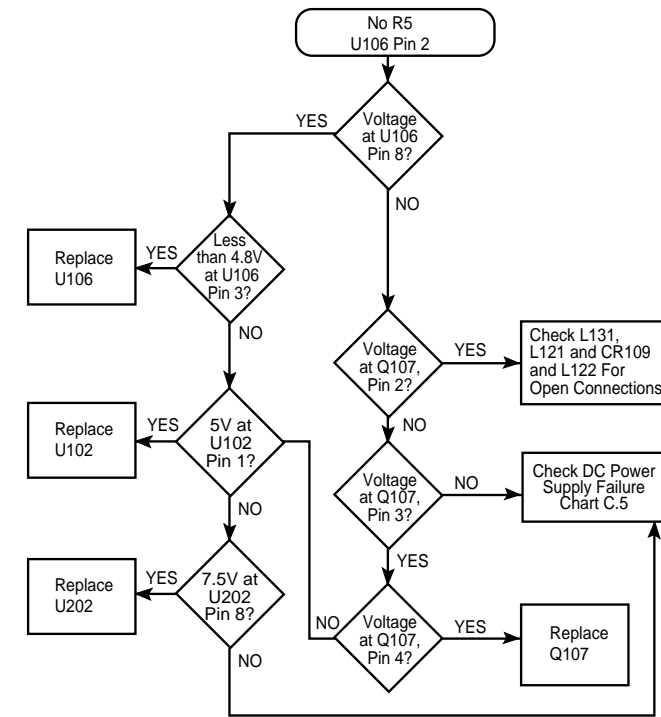
Chart 32. 800 MHz Voltage Controlled Oscillator (VCO)





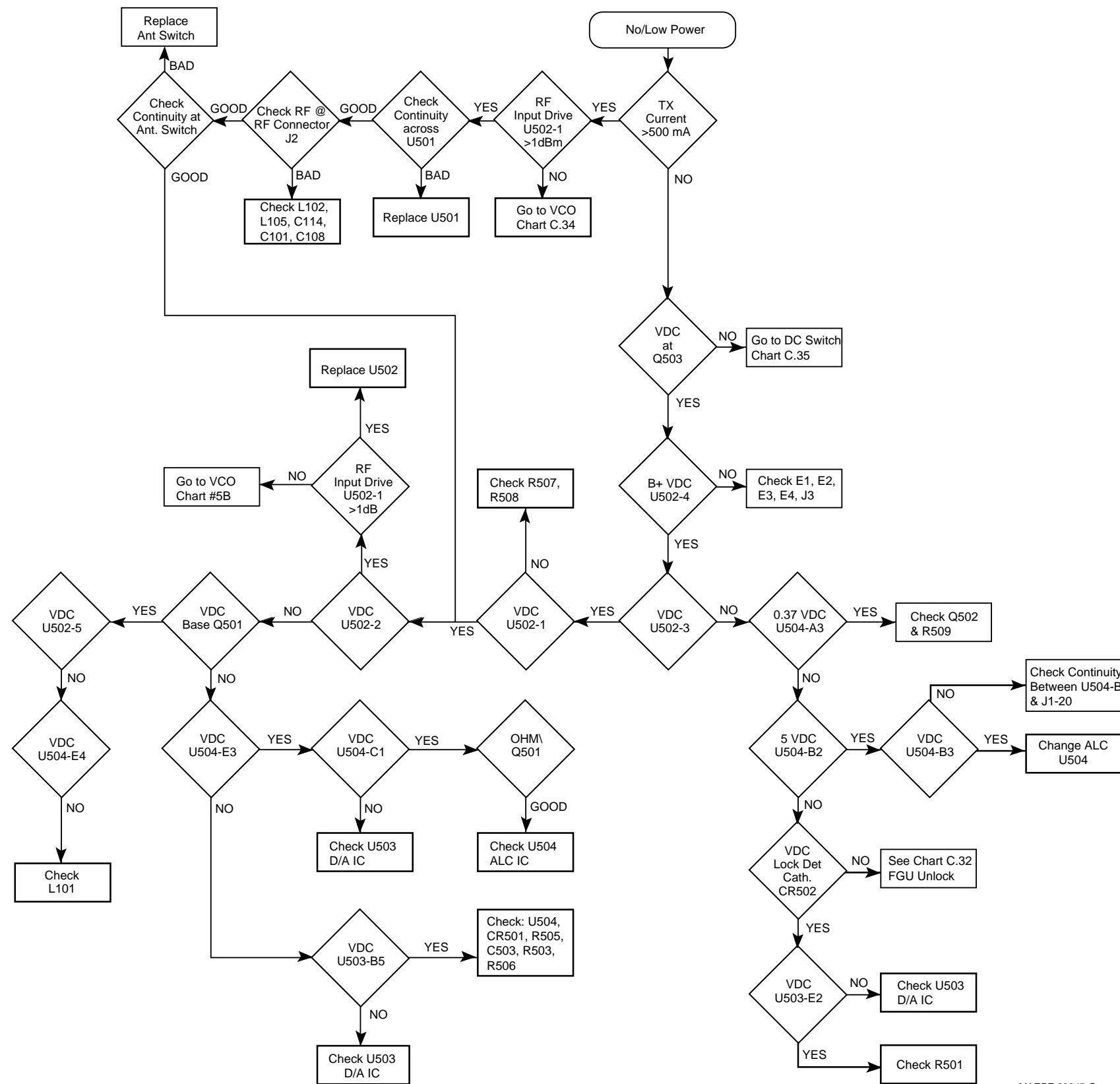
MAEPF-24392-O

Chart 33. 800 MHz DC Switch



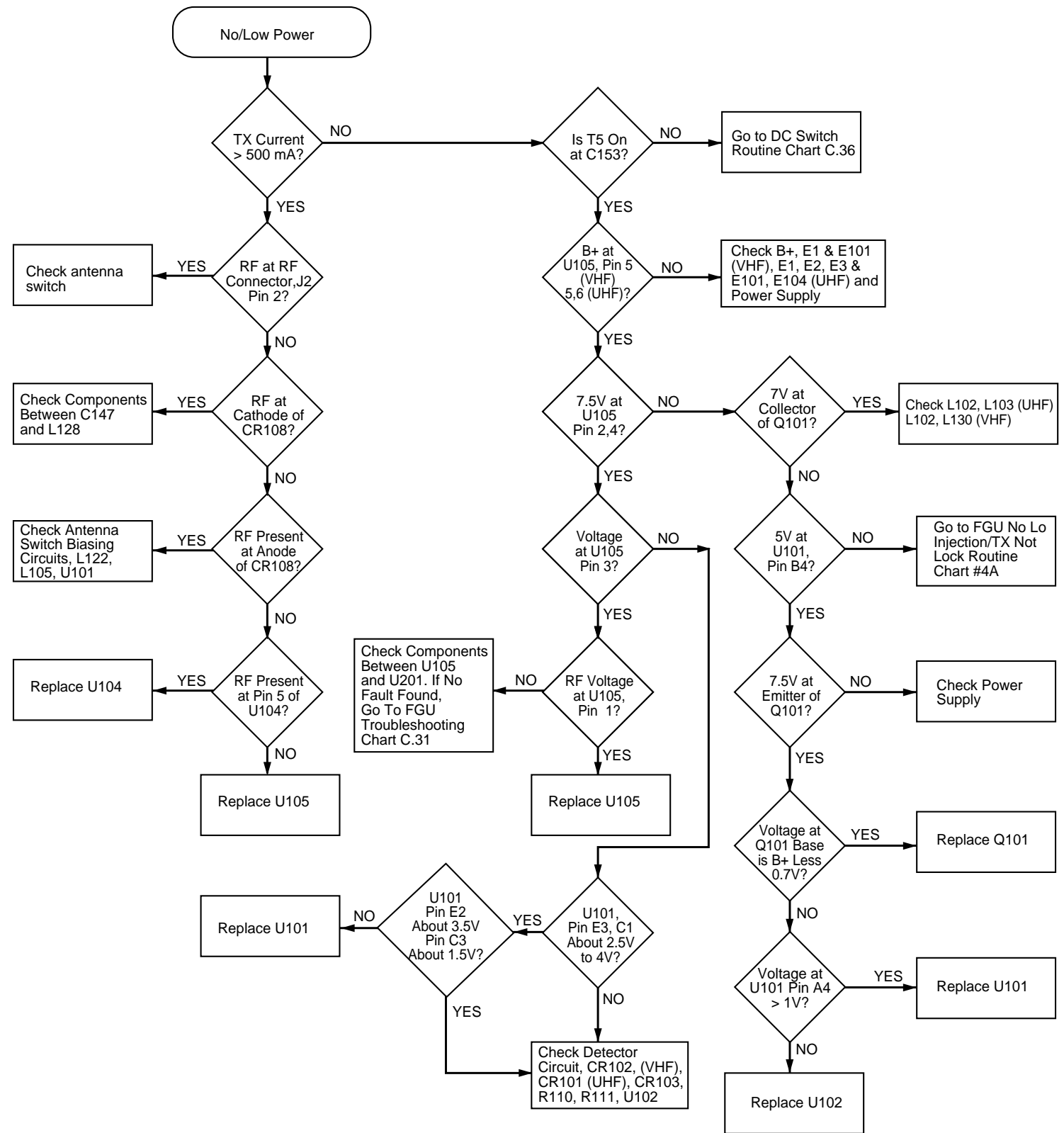
MAEPF-26044-O

Chart 34. VHF/UHF DC Switch



MAEPF-26045-0

Chart 35. 800 MHz Transmitter RF



MAEPF-26046-O

Chart 36. VHF/UHF Transmitter RF

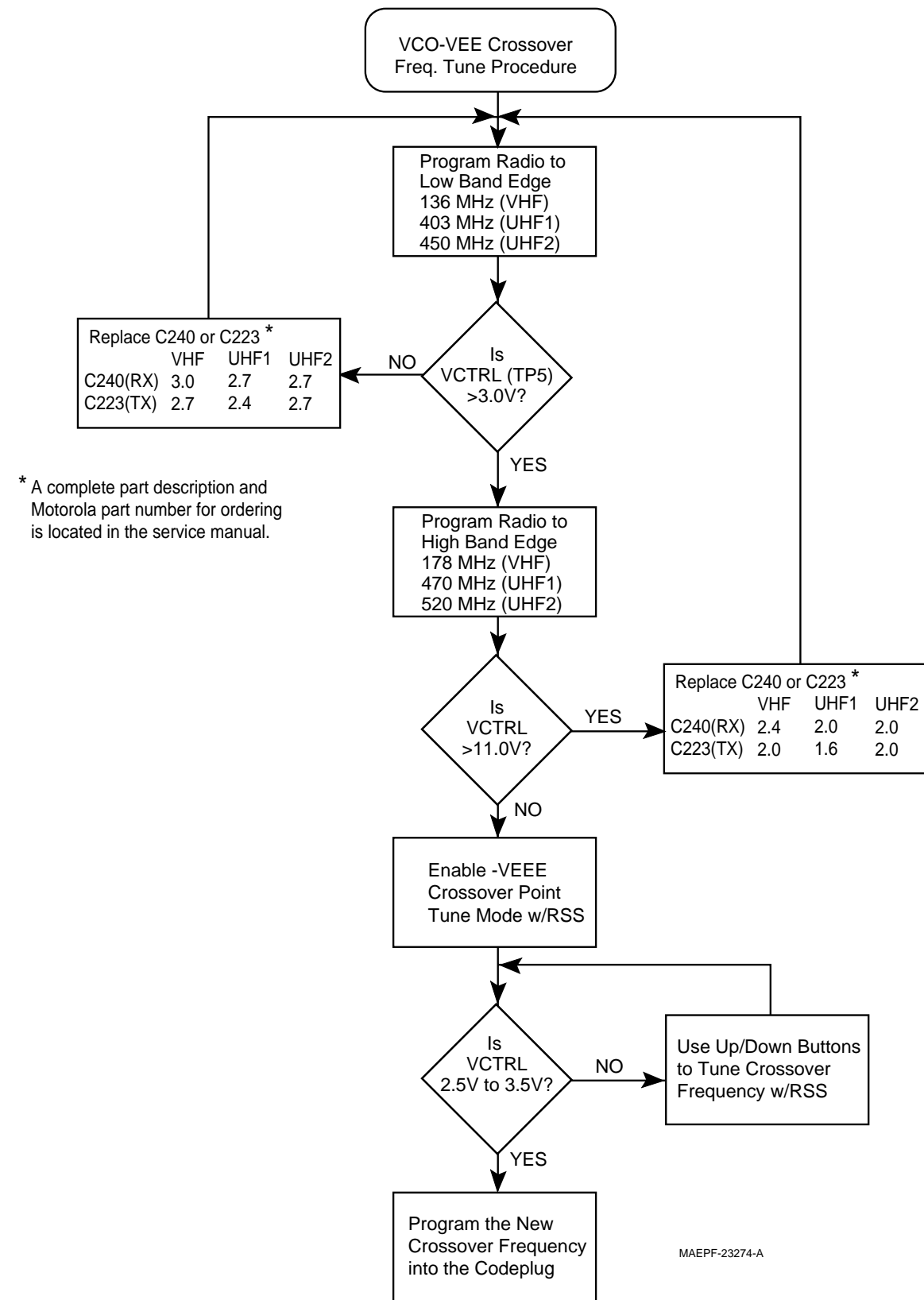
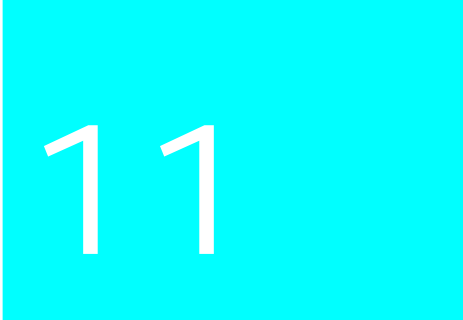


Chart 37. VHF/UHF Only, VCO Crossover Frequency Tune

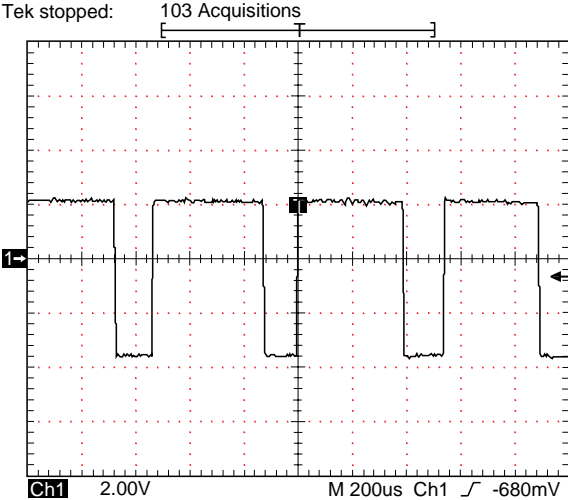
# Troubleshooting Waveforms



## Introduction to This Section

This section contains images of waveforms which may be useful in verifying operation of certain parts of the circuitry. These waveforms are for reference only; the actual data depicted will vary depending upon operating conditions.

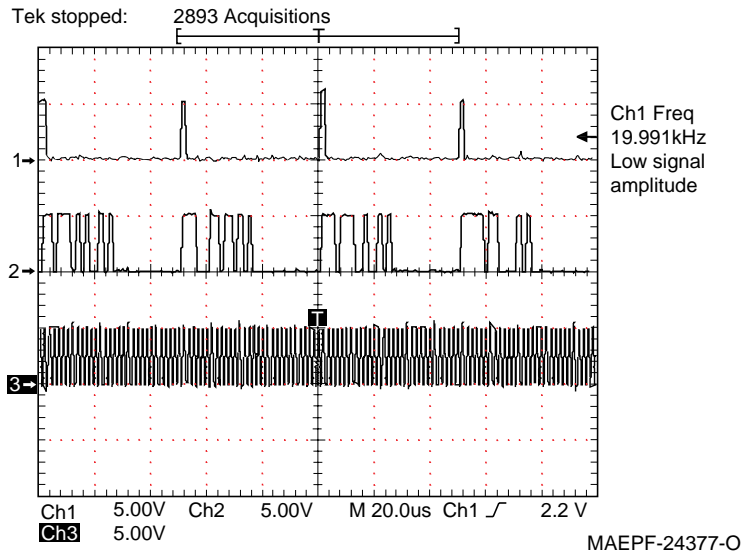
## Waveforms



W1: Switched Regulator Clock Out  
Trace 1 - (U709)LX measured with radio in standby mode with UNSW\_B+ at 7.5VDC.

MAEPF-26008-O

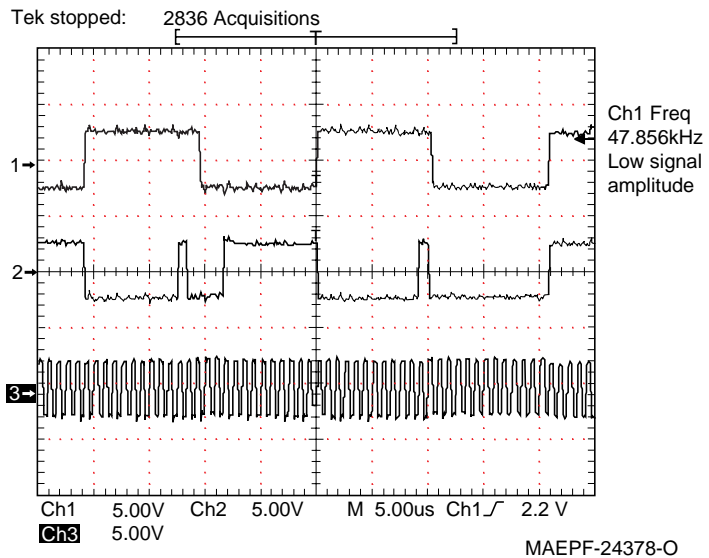
### Waveform W1



W2: DSP SSI Port RX mode.  
Receiving  
1KHz tone @ 3KHz deviation, -60dBm.  
Trace 1 - RFS  
Trace 2 - RXD  
Trace 3 - SCKR<sub>1</sub> (2.4/0.600MHz)

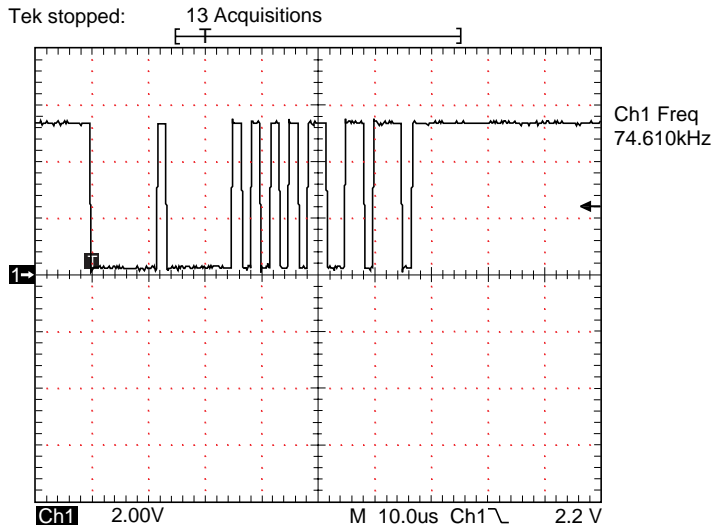
Note 1: Typically SCKR is a 2.4 MHz clock. In low power modes, as shown here, SCKR is 600KHz.

### Waveform W2



W3: DSP SSI Port TX mode CSQ.  
Trace 1 - SC2  
Trace 2 - STD  
Trace 3 - SCK (1.2MHz)

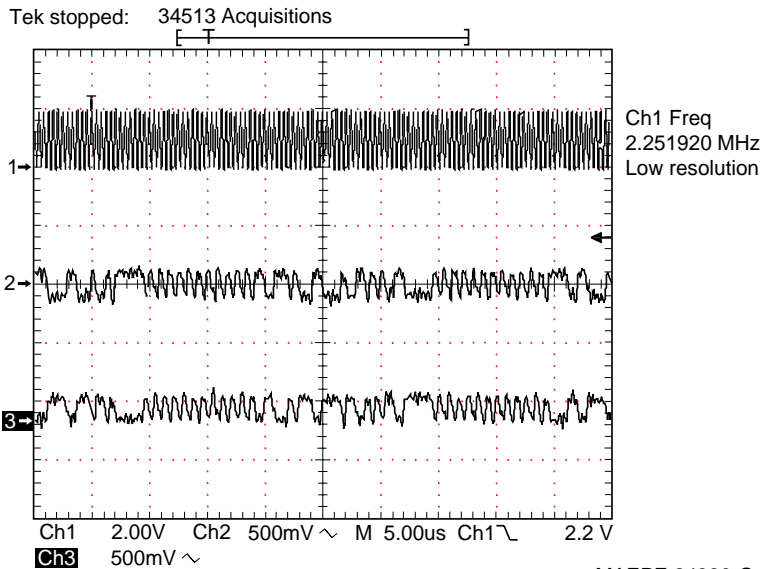
### Waveform W3



W4: ABACUS programming  
captured during mode change.  
Trace 1 - (ADSIC) SBI

MAEPF-24379-O

**Waveform W4**

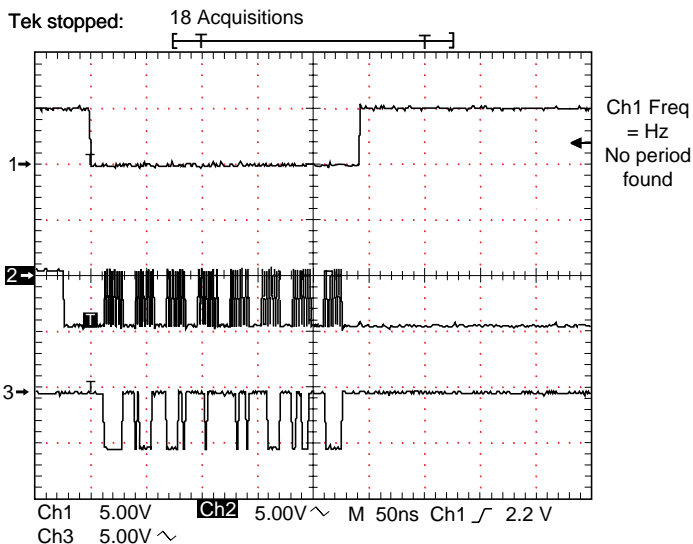


W5: ABACUS/ADSIC Interface.  
Receiving 1KHz tone @ 3KHz deviation,  
-60dbm.  
Trace 1 - IDC (2.4MHz)  
Trace 2 - DOUT<sup>2</sup>  
TRACE 3 - DOUT<sup>+</sup>

MAEPF-24380-O

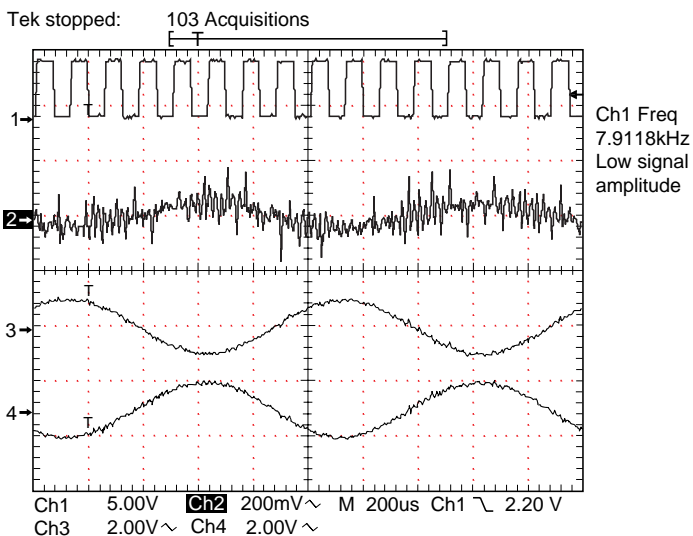
Note 2: Since these signals are a differential  
current loop these voltages are very low.

**Waveform W5**



W6: SPI Bus Programming ADSIC. MAEPF-24381-O  
 Trace 1 - ADSIC\_SEL\*  
 Trace 2 - SPI\_SCK  
 Trace 3 - MOSI  
 Note: These waveforms are typical to any device on the SPI bus.

**Waveform W6**



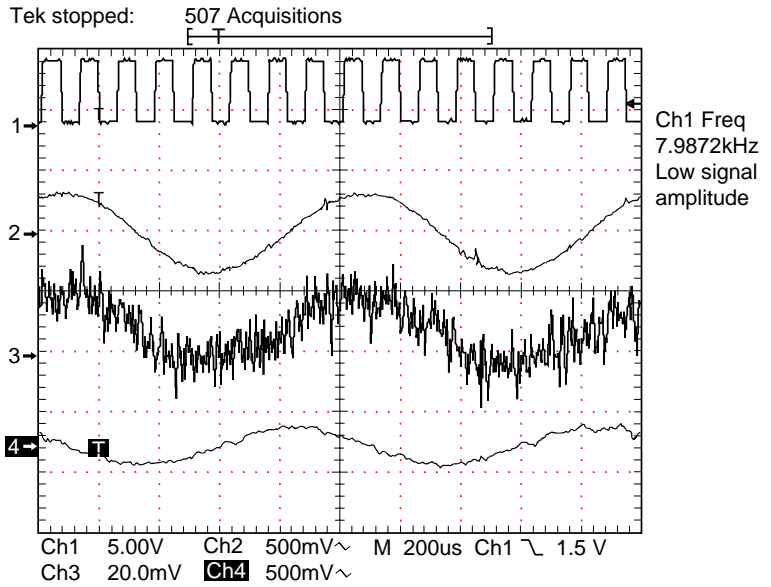
W7: Receive audio: Receiving  
 1KHz tone @ 3KHz deviation, -60dBm.  
 Trace 1 - IRQB @ DSP (8KHz)  
 Trace 2 - SD0 @ C219  
 Trace 3 - SPKR\_COMMON  
 Trace 4 - INT\_SPKR<sup>3</sup>

Note 3: Actual level is dependent upon volume setting.

**Waveform W7**

MAEPF-26009-O

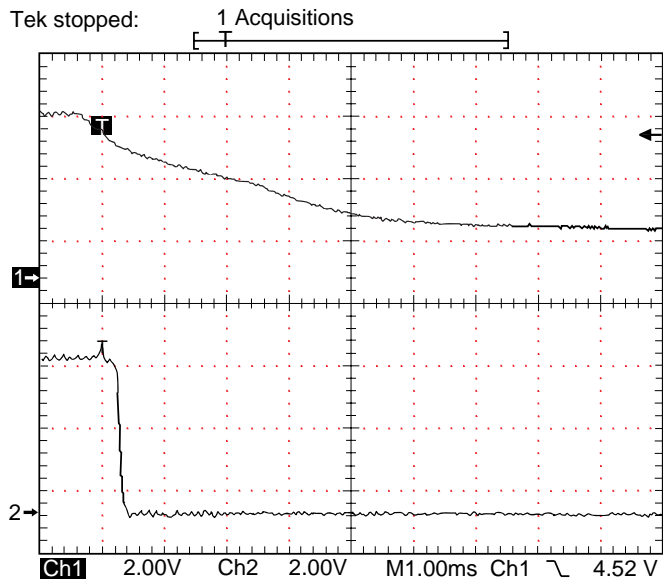




W8: Transmit Audio. 1KHz Tone  
which provides 3KHz deviation.  
Trace 1 - IRQB @ DSP (8KHz)  
Trace 2 - MODIN  
Trace 3 - EXT MIC @ node C189/R198  
Trace 4 - MAI @ node R207/U718  
MICAMPOUT

MAEPF-26010-O

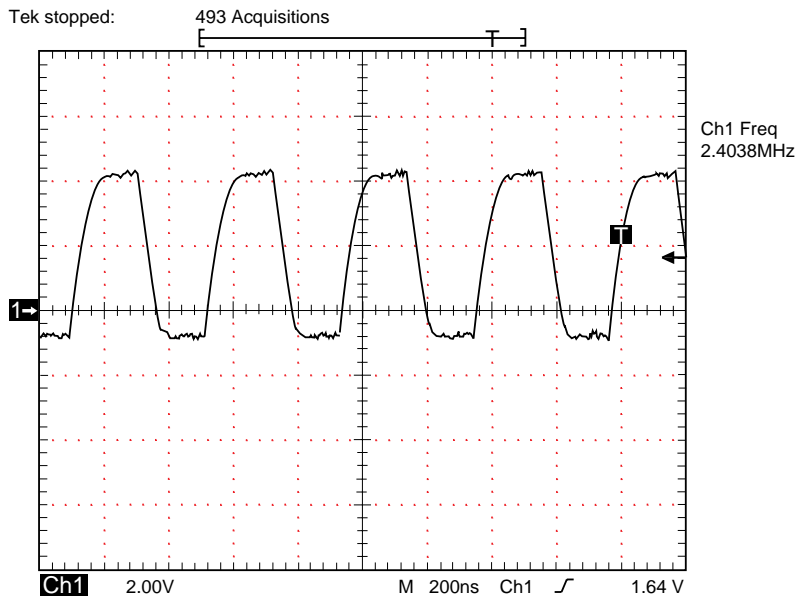
**Waveform W8**



W9: Power Down Reset.  
Trace 1 - +5V @ U726 (VDD)  
Trace 2 - Reset @ U726 (OUT)

MAEPF-26011-O

**Waveform W9**



W10 ADSIC 2.4 MHz Reference  
Trace 1 - IDC @ U406

MAEPF-24385-O

*Waveform W10*

# Troubleshooting Diagrams

# 12

## Introduction to This Section

This section contains troubleshooting diagrams necessary to isolate a problem to the component level. Use these diagrams in conjunction with the theory of operation, troubleshooting procedures, charts, and waveforms.

J101  
Controller Board to Controls Flex Assembly

J101 Pin #	Description	To/From	Side Conn Pin #
1	CTSOUT*	U702-B6	10
2	LHDATA/BOOT_DOUT/KEYFAIL	U717-1	13
3	GROUND	N/C	8
4	RS232IN	U702-B2/G3	12
5	SPKR_COMMON	U718-27	6
6	RS232_DOUT/BOOT_DIN	U702-A5	11
7	OPT_SEL_2	U702-C6	5
8	SB9600_BUSY	U701-74	9
9	EXT_SPEAKER	U718-31	2
10	RTSIN*	U702-J8	7
11	OPT_SEL_1	U702-A6	1
12	OPT_B+/BOOT_SEL/VPP	VR119/D100	4
13	EXT_MIC	U714-6	3
15-18	GROUND	N/C	
19	BL_HOME	Q111-2	
20	BL_FREQ	Q111-1	
21	RED_LED	Q112-2	
22	GREEN_LED	Q112-1	
23	TG2	U701-24	
24	RTA1	U702-F4	
25	RTA3	U702-H1	
26	RTA2	U702-F2	
27	RTA0	U702-F3	
28-30	GROUND	N/C	
31	VOL	U701-25	
32	B+_SENSE	VR101	
33	UNSW_B+	P201-15/20	
34	TG1	U701-19	
35	+5V	U709-9	
36	INT_MIC	U714-2	
37	SPKR_COMMON	U718-27	
38	INT_PTT	U702-H2	
39	GROUND	N/C	
40	INT_SPKR	U718-23	
14, 41	EMERG	U701-27	

J401  
Controller Board to Vocoder Board

J401 Pin #	Description	To/From
1	R/W*	U701-35
2	HEN*	U702-J7
3	A0	U701-17
4	A2	U701-15
5	VPP	Q110
6	DSP_RST*	U701-58
7	EMC_RXD	J601-5
8	+5V	U709-9
9	+5V	U709-9
10	+5VA	U710-3
11	MICEN	U718-14
12	INTMICEN	U718-16
13	GROUND	N/C
14	HREQ*	U701-75
15	GROUND	N/C
16	A1	U701-16
17	VPP	Q110
18	BOOT_MODE	U701-76
19	EMC_TXD	J601-3
20	MOSI	U701-66
21	SPI_SCK	U701-67
22	SBI	P201-4
23	+5VA	U710-3
24	EXT_INT_SPKR*	U718-20
25	SPKEN	U718-19
26	D7	U701-49
27	D5	U701-47
28	D3	U701-45
29	D1	U701-43
30	+5V	U709-9
31	GROUND	N/C
32	GROUND	N/C
33	DOUT*	P201-1
34	SDO	U718-6
35	MODIN	P201-14
36	MAI	U718-15
37	ADSIC_RST*	701-56
38	GROUND	N/C
39	D6	U701-48
40	D4	U701-46
41	D2	U701-44
42	D0	U701-40
43	ODC-2.4MHZ	P201-11
44	GROUND	N/C
45	DOUT	P201-2
46-49	GROUND	N/C
50	ADSIC_SEL*	U701-57

J601  
Controller Board to Encryption Module

J601 Pin #	Description	To/From
1	SW_B+	Q106-5
2	SW_B+	Q106-5
3	EMC_TXD	J401-19
4		N/C
5	EMC_RXD	J401-7
6		N/C
7	MISO	U701-65
8		N/C
9	SPI_SCK	U701-67
10		N/C
11	EMC_REQ	U702-H3
12		N/C
13	TAMPER	GROUND
14	UNSW_B+	P201-15, 20
15	KEYFAIL	U717-2
16		N/C
17	MOSI	U701-66
18		N/C
19	EMC_EN	U702-D6
20		N/C
21	TAMPER	GROUND
22		N/C
23		N/C
24	TAMPER	GROUND
25	EMC_WAKEUP	U702-K7

P107  
Controller Board to Keypad Module

P107 Pin #	Description	To/From
1	COL1	U702-A7
2	COL2	U702-D5
3	COL3	U702-B4
4	BL_EN	U702-E7
5	ROW1	U702-J3
6	ROW2	U702-G4
7	ROW3	U702-K8
8	ROW4	U702-G9
9	ROW5	U702-F8
10	ROW6	U702-G7
11	+5V	U709-9
12	GROUND	N/C

P201  
Controller Board to RF Board

P201 Pin #	Description	To/From
1	DOUT*	J401-33
2	DOUT	J401-45
3	LOCK_DET*	U702-K2
4	SBI	J401-22
5	BAT_STATUS	U701-28
6	GROUND	N/C
7	DA_SEL*	U701-68
8	ROSC/PSC_CE*	U701-59
9	SYN_SEL*	U701-62
10	SPL_SCK	U701-67
11	OD - 24MHZ	U701-43
12	POR*	U726-1
13	GROUND	N/C
14	MODIN	J401-35
15	UNSW_B+	Q1-2, 3
16	GROUND	N/C
17	MOSI	U701-66
18	SW_B+	Q106-5
19	GROUND	N/C
20	UNSW_B+	Q106-2, 3

P301  
Controller Board to Display Module

P301 Pin #	Description	To/From
1	SPI_SCK	U701-67
2	MOSI	U701-66
3	DISP_EN*	U702-G8
4	BL_EN	U702-E7
5	GROUND	N/C
6	GROUND	N/C
7	+5V	U709-9

