Exhibit 8A
FCC ID: QKGRDX-U3

CARRIER FREQUENCY GENERATION AND STABLIZATION

Circuit Description:

The carrier frequency is generated using a fractional-N frequency synthesizer. This consists of a phase-locked loop circuit with a voltage controlled oscillator (VCO) whose output is fed back to a programmable divider chain. The divide ratios are determined from information stored in the memory ICs and bussed to - the synthesizer via a microcomputer. The microcomputer extracts the data for the division ratios as determined by the system select switch or by loading data stored in the memory [Cs. Using a time averaged algorithm a combination of divide ratios are used so that the reference frequency can be a much higher value than the value of the frequency resolution. Modulation occurs by a combination of directly coupling the modulation signal to the low pass filter in the loop and by processing the digitized analog modulation signal to alter the divider values, A temperature compensated crystal oscillator, a 16.8 MHz and stable to 1.5 parts per million over temperature extremes is used for the frequency reference. The 16.8 MHz reference is further divided into one of three reference frequencies which is compared to the divided down VCO output in a phase detector which in turn provides a DC steering voltage back to the VCO.

A Block diagram of the VCO/Synthesizer system is attached.