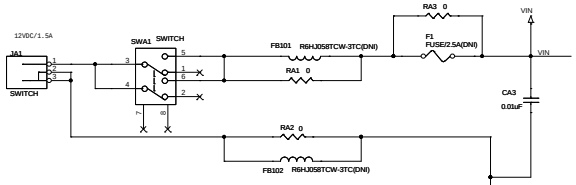
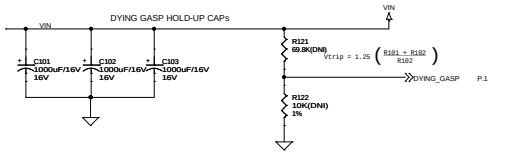
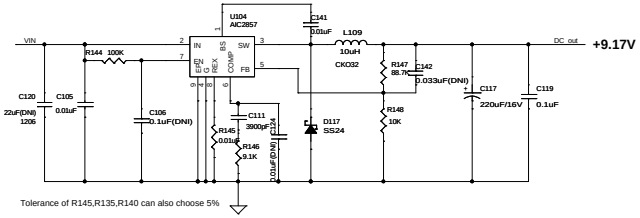
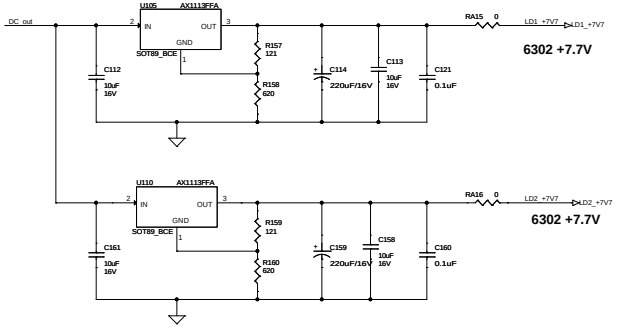
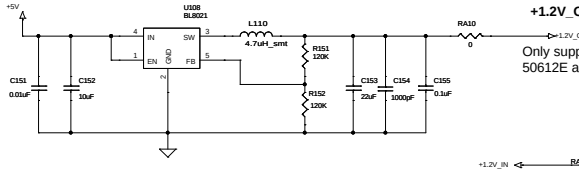
+12VDC Regulated Input

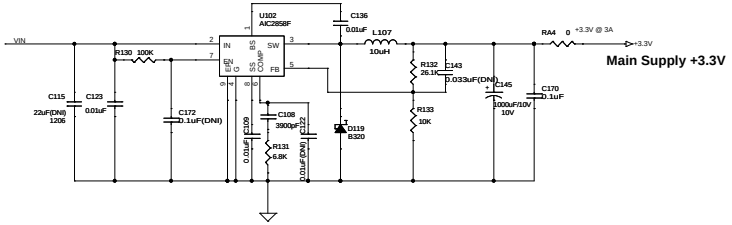


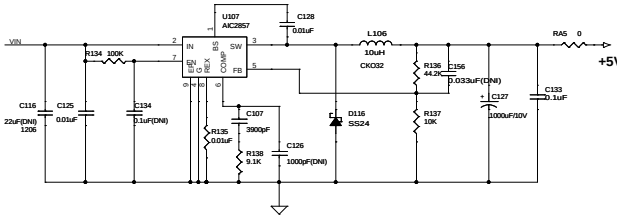


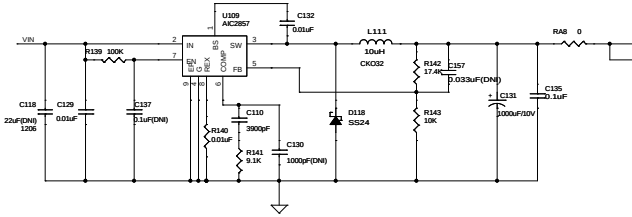


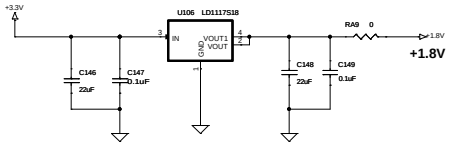


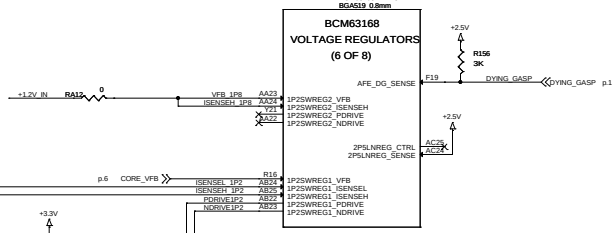




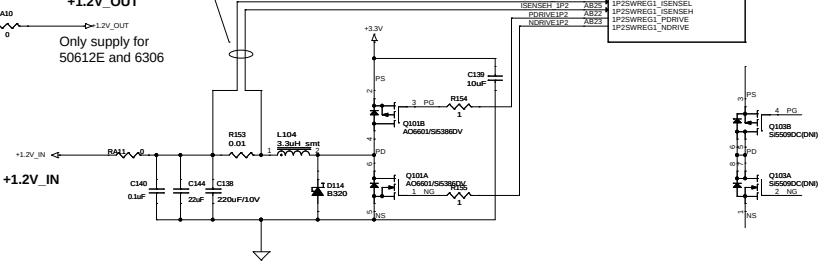




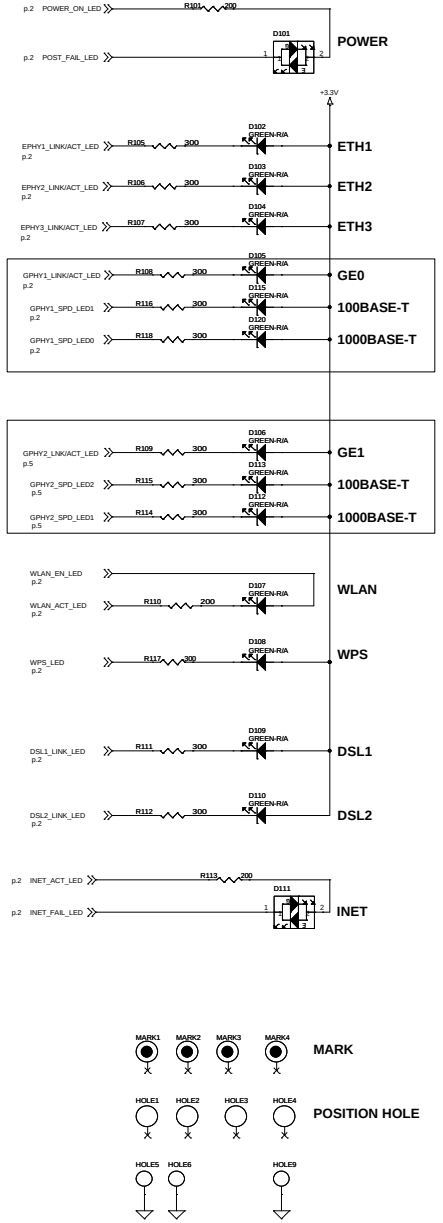




Route these as a diff pair. Do not connect ISENSEL ball directly to the 1.2V power plane.



FRONT PANEL LEDs



BEC 8920NE		
Title	POWER and LEDS	
Size: Custom	Document Number	Rev: 1.0
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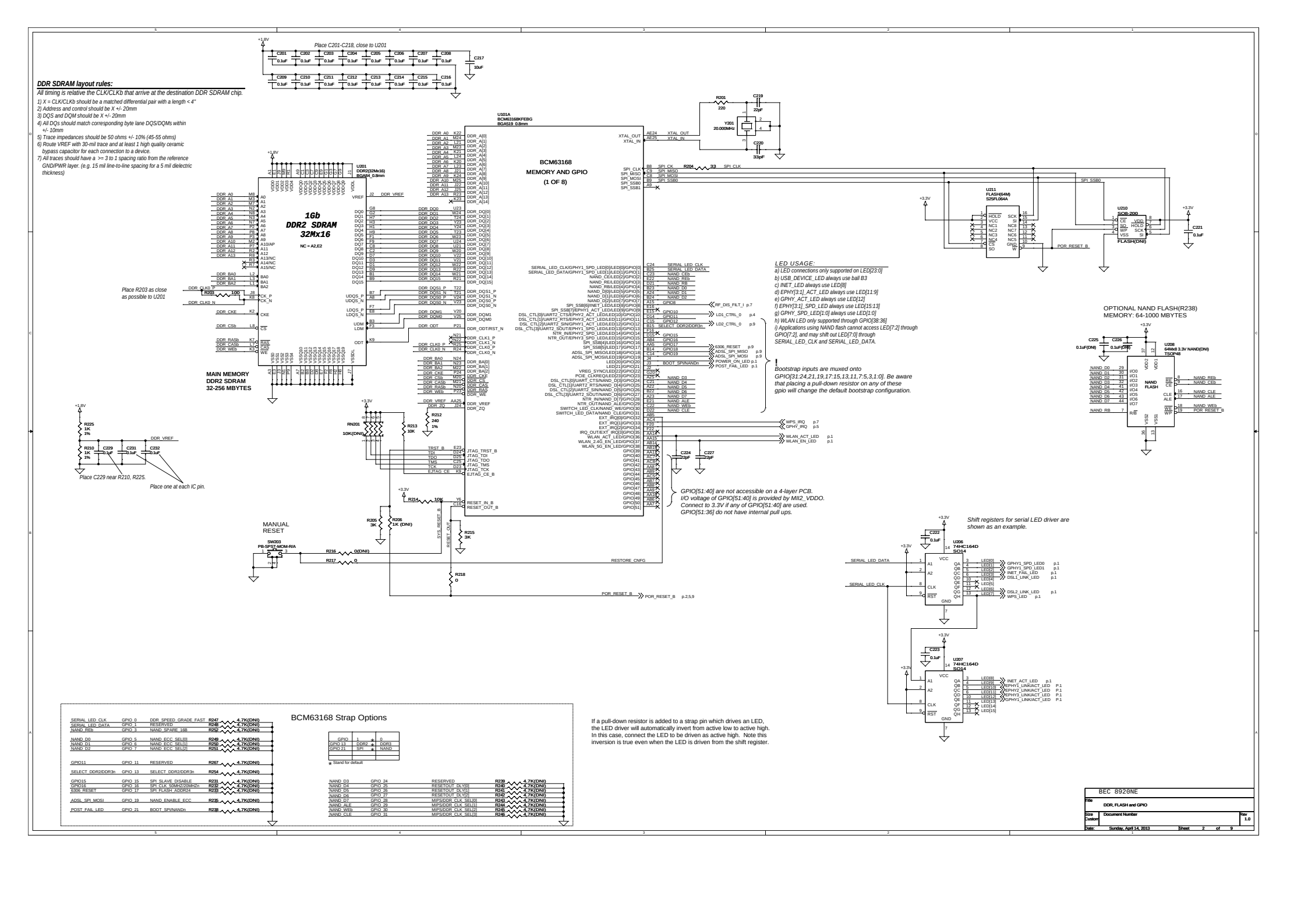
DDR SDRAM layout rules:
All timing is relative the CLK/CLKb that arrive at the destination DDR SDRAM chip.
1) X = CLK/CLKb should be a matched differential pair with a length < 4"
2) Address and control should be X +/- 20mm
3) DQS and DQM should be X +/- 20mm
4) All DQs should match corresponding byte lane DQS/DQMs within +/- 10mm
5) Trace impedances should be 50 ohms +/- 10% (45-55 ohms)
6) Route VREF with 30-mil trace and at least 1 high quality ceramic bypass capacitor for each connection to a device.
7) All traces should have a >= 3 to 1 spacing ratio from the reference GND/PWR layer. (e.g. 15 mil line-to-line spacing for a 5 mil dielectric thickness)
Place C201-C218, close to U201
C201 C202 C203 C204 C205 C206 C207 C208 C209 C210 C211 C212 C213 C214 C215 C216 0.1uF
C217 10uF
+1.8V
U201
DDR2(32Mx16)
BGA84 0.8mm
16Gb
DDR2 SDRAM
32Mx16
NC = A2,E2
MAIN MEMORY
DDR2 SDRAM
32-256 MBYTES
Place R203 as close as possible to U201
R203 100
DDR_CLK0_P
DDR_CLK0_N
U101A
BCM63168KFEBG
BGA519 0.8mm
BCM63168
MEMORY AND GPIO
(1 OF 8)
R204 33
SPI_CLK
SPI_MISO
SPI_MOSI
SPI_SSB0
SPI_SSB1
R201 220
Y201
20.000MHz
C219 22pF
C220 33pF
XTAL_OUT
XTAL_IN
U211
FLASH(64M)
S25FL064A
U210
SOB-200
FLASH(DNI)
C221 0.1uF
POR_RESET_B
LED USAGE:
a) LED connections only supported on LED[23:0]
b) USB_DEVICE_LED always use ball B3
c) INET_LED always use LED[8]
d) EPHY[3:1]_ACT_LED always use LED[11:9]
e) GPHY_ACT_LED always use LED[12]
f) EPHY[3:1]_SPD_LED always use LED[15:13]
g) GPHY_SPD_LED[1:0] always use LED[1:0]
h) WLAN LED only supported through GPIO[38:36]
i) Applications using NAND flash cannot access LED[7:2] through GPIO[7:2], and may shift out LED[7:0] through SERIAL_LED_CLK and SERIAL_LED_DATA.
Bootstrap inputs are muxed onto GPIO[31:24,21,19,17:15,13,11,7:5,3,1:0]. Be aware that placing a pull-down resistor on any of these gpio will change the default bootstrap configuration.
OPTIONAL NAND FLASH(R238)
MEMORY: 64-1000 MBYTES
U208
64Mx8 3.3V NAND(DNI)
TSOP48
NAND FLASH
C225 0.1uF(DNI)
C226 0.1uF(DNI)
NAND_REb
NAND_CEb
NAND_CLE
NAND_ALE
NAND_WEb
POR_RESET_B
Place C229 near R210, R225.
Place one at each IC pin.
R225 1K 1%
R210 1K 1%
C229 0.1uF
C231 0.1uF
C232 0.1uF
DDR_VREF
RN201 10K(DNI)
R212 240 1%
R213 10K
R214 10K
R205 3K
R206 1K (DNI)
R215 3K
R216 0(DNI)
R217 0
R218 0
MANUAL RESET
SW203
PB-SPST-MOM-R/A
SYS_RESET_B
RESET_OUT
RESTORE_CNFG
POR_RESET_B p.2,5,9
JTAG_TRST_B
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
EJTAG_CE_B
RESET_IN_B
RESET_OUT_B
C224 2pF
C227 2pF
GPIO[51:40] are not accessible on a 4-layer PCB.
I/O voltage of GPIO[51:40] is provided by MII2_VDDO.
Connect to 3.3V if any of GPIO[51:40] are used.
GPIO[51:36] do not have internal pull ups.
WPS_IRQ p.7
GPHY_IRQ p.5
WLAN_ACT_LED p.1
WLAN_EN_LED p.1
RF_DIS_FILT_I p.7
LD1_CTRL_0 p.4
LD2_CTRL_0 p.9
6306_RESET p.9
ADSL_SPI_MISO p.9
ADSL_SPI_MOSI p.9
POWER_ON_LED p.1
POST_FAIL_LED p.1
Shift registers for serial LED driver are shown as an example.
U206
74HC164D
SO14
U207
74HC164D
SO14
SERIAL_LED_DATA
SERIAL_LED_CLK
GPHY1_SPD_LED0 p.1
GPHY1_SPD_LED1 p.1
INET_FAIL_LED p.1
DSL1_LINK_LED p.1
DSL2_LINK_LED p.1
WPS_LED p.1
INET_ACT_LED p.1
EPHY1_LINK/ACT_LED P.1
EPHY2_LINK/ACT_LED P.1
EPHY3_LINK/ACT_LED P.1
GPHY1_LINK/ACT_LED P.1
BCM63168 Strap Options
SERIAL_LED_CLK GPIO_0 DDR_SPEED_GRADE_FAST R247 4.7K(DNI)
SERIAL_LED_DATA GPIO_1 RESERVED R248 4.7K(DNI)
NAND_REb GPIO_3 NAND_SPARE_16B R252 4.7K(DNI)
NAND_D0 GPIO_5 NAND_ECC_SEL[0] R249 4.7K(DNI)
NAND_D1 GPIO_6 NAND_ECC_SEL[1] R250 4.7K(DNI)
NAND_D2 GPIO_7 NAND_ECC_SEL[2] R251 4.7K(DNI)
GPIO11 GPIO_11 RESERVED R267 4.7K(DNI)
SELECT_DDR2/DDR3n GPIO_13 SELECT_DDR2/DDR3n R254 4.7K(DNI)
GPIO15 GPIO_15 SPI_SLAVE_DISABLE R231 4.7K(DNI)
GPIO16 GPIO_16 SPI_CLK_50MHZ/20MHZn R232 4.7K(DNI)
6306_RESET GPIO_17 SPI_FLASH_ADDR24 R233 4.7K(DNI)
ADSL_SPI_MOSI GPIO_19 NAND_ENABLE_ECC R235 4.7K(DNI)
POST_FAIL_LED GPIO_21 BOOT_SPI/NANDn R238 4.7K(DNI)
GPIO 1 * 0
GPIO 13 DDR2 * DDR3
GPIO 21 SPI * NAND
* Stand for default
NAND_D3 GPIO_24 RESERVED R239 4.7K(DNI)
NAND_D4 GPIO_25 RESETOUT_DLY[0] R240 4.7K(DNI)
NAND_D5 GPIO_26 RESETOUT_DLY[1] R241 4.7K(DNI)
NAND_D6 GPIO_27 RESETOUT_DLY[2] R242 4.7K(DNI)
NAND_D7 GPIO_28 MIPS/DDR_CLK_SEL[0] R243 4.7K(DNI)
NAND_ALE GPIO_29 MIPS/DDR_CLK_SEL[1] R244 4.7K(DNI)
NAND_WEb GPIO_30 MIPS/DDR_CLK_SEL[2] R245 4.7K(DNI)
NAND_CLE GPIO_31 MIPS/DDR_CLK_SEL[3] R246 4.7K(DNI)
If a pull-down resistor is added to a strap pin which drives an LED, the LED driver will automatically invert from active low to active high. In this case, connect the LED to be driven as active high. Note this inversion is true even when the LED is driven from the shift register.
BEC 8920NE
DDR, FLASH and GPIO
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Document Number
Rev: 1.0
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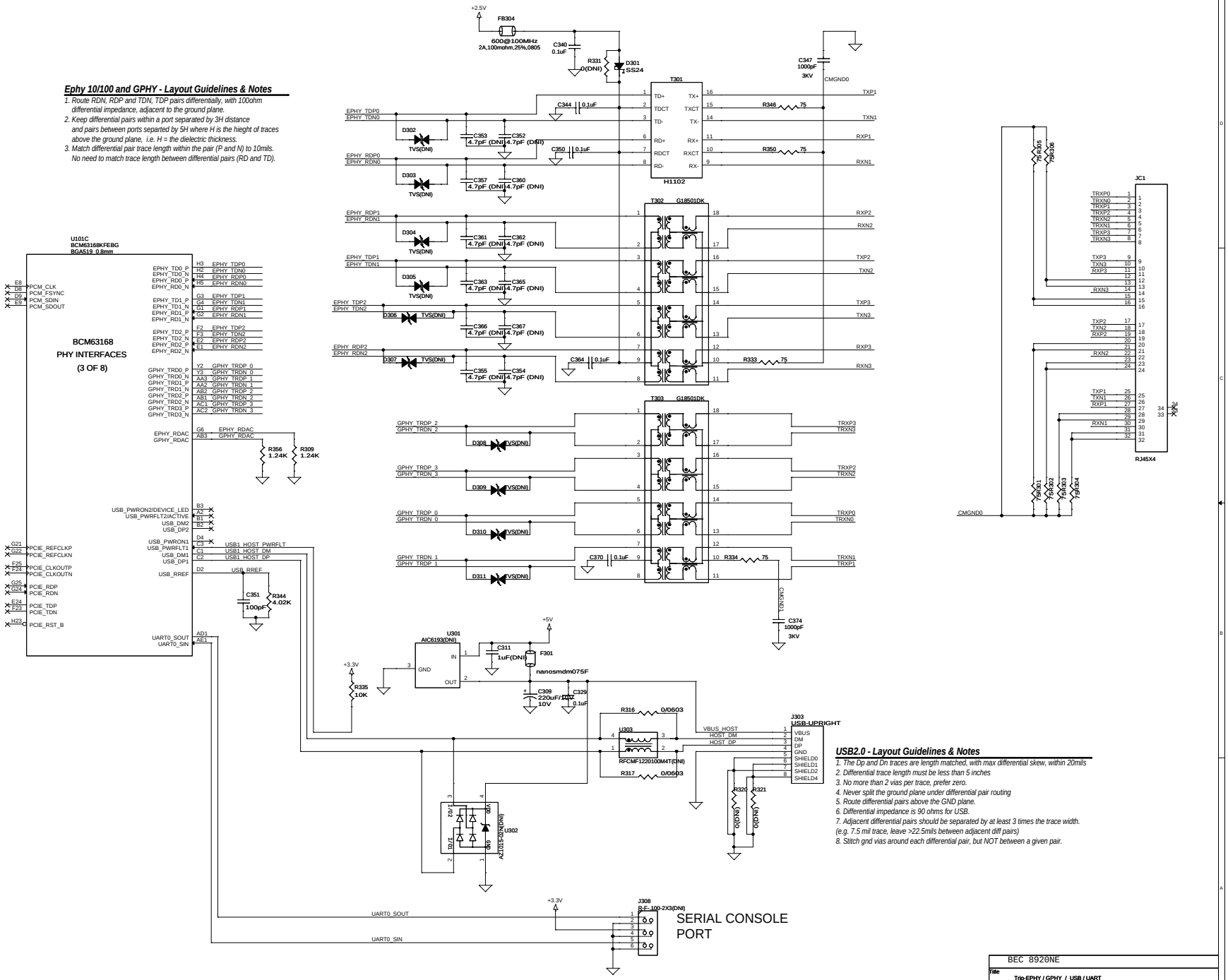
Ephy 10/100 and GPHY - Layout Guidelines & Notes
1. Route RDN, RDP and TDN, TDP pairs differentially, with 100ohm differential impedance, adjacent to the ground plane.
2. Keep differential pairs within a port separated by 3H distance and pairs between ports separted by 5H where H is the hieght of traces above the ground plane, i.e. H = the dielectric thickness.
3. Match differential pair trace length within the pair (P and N) to 10mils. No need to match trace length between differential pairs (RD and TD).
U101C
BCM63168KFEBG
BGA519_0.8mm
BCM63168
PHY INTERFACES
(3 OF 8)
PCM_CLK
PCM_FSYNC
PCM_SDIN
PCM_SDOUT
EPHY_TD0_P
EPHY_TD0_N
EPHY_RD0_P
EPHY_RD0_N
EPHY_TD1_P
EPHY_TD1_N
EPHY_RD1_P
EPHY_RD1_N
EPHY_TD2_P
EPHY_TD2_N
EPHY_RD2_P
EPHY_RD2_N
GPHY_TRD0_P
GPHY_TRD0_N
GPHY_TRD1_P
GPHY_TRD1_N
GPHY_TRD2_P
GPHY_TRD2_N
GPHY_TRD3_P
GPHY_TRD3_N
EPHY_RDAC
GPHY_RDAC
R356 1.24K
R309 1.24K
USB_PWRON2/DEVICE_LED
USB_PWRFLT2/ACTIVE
USB_DM2
USB_DP2
USB_PWRON1
USB_PWRFLT1
USB_DM1
USB_DP1
USB_RREF
C351 100pF
R344 4.02K
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CLKOUTP
PCIE_CLKOUTN
PCIE_RDP
PCIE_RDN
PCIE_TDP
PCIE_TDN
PCIE_RST_B
UART0_SOUT
UART0_SIN
+2.5V
FB304
600@100MHz
2A,100mohm,25%,0805
C340 0.1uF
R331 0(DNI)
D301 1SS24
C347 1000pF 3KV
CMGND0
T301
H1102
C344 0.1uF
C350 0.1uF
R346 75
R350 75
D302 TVS(DNI)
D303 TVS(DNI)
C353 4.7pF (DNI)
C352 4.7pF (DNI)
C357 4.7pF (DNI)
C360 4.7pF (DNI)
T302 G18501DK
D304 TVS(DNI)
D305 TVS(DNI)
D306 TVS(DNI)
C361 4.7pF (DNI)
C362 4.7pF (DNI)
C363 4.7pF (DNI)
C365 4.7pF (DNI)
C366 4.7pF (DNI)
C367 4.7pF (DNI)
T303 G18501DK
D307 TVS(DNI)
C364 0.1uF
R333 75
C355 4.7pF (DNI)
C354 4.7pF (DNI)
D308 TVS(DNI)
D309 TVS(DNI)
D310 TVS(DNI)
D311 TVS(DNI)
C370 0.1uF
R334 75
C374 1000pF 3KV
U301
AIC6193(DNI)
C311 1uF(DNI)
F301 nanosmdm075F
C309 220uF/10V
C329 0.1uF
+5V
+3.3V
R335 10K
R316 0/0603
R317 0/0603
U303
RFCMF1220100M4T(DNI)
J303
USB-UPRIGHT
VBUS_HOST
HOST_DM
HOST_DP
R320 (DNI)
R321 (DNI)
U302
AZ1015-04D(DNI)
J308
R-F-100-2X3(DNI)
SERIAL CONSOLE PORT
JC1
RJ45X4
R305 75R306
R311 75R312 75R303 75R304
USB2.0 - Layout Guidelines & Notes
1. The Dp and Dn traces are length matched, with max differential skew, within 20mils
2. Differential trace length must be less than 5 inches
3. No more than 2 vias per trace, prefer zero.
4. Never split the ground plane under differential pair routing
5. Route differential pairs above the GND plane.
6. Differential impedance is 90 ohms for USB.
7. Adjacent differential pairs should be separated by at least 3 times the trace width. (e.g. 7.5 mil trace, leave >22.5mils between adjacent diff pairs)
8. Stitch gnd vias around each differential pair, but NOT between a given pair.
BEC 8920NE
Title
Trio-EPHY / GPHY / USB / UART
Size Custom
Document Number
Rev 1.0
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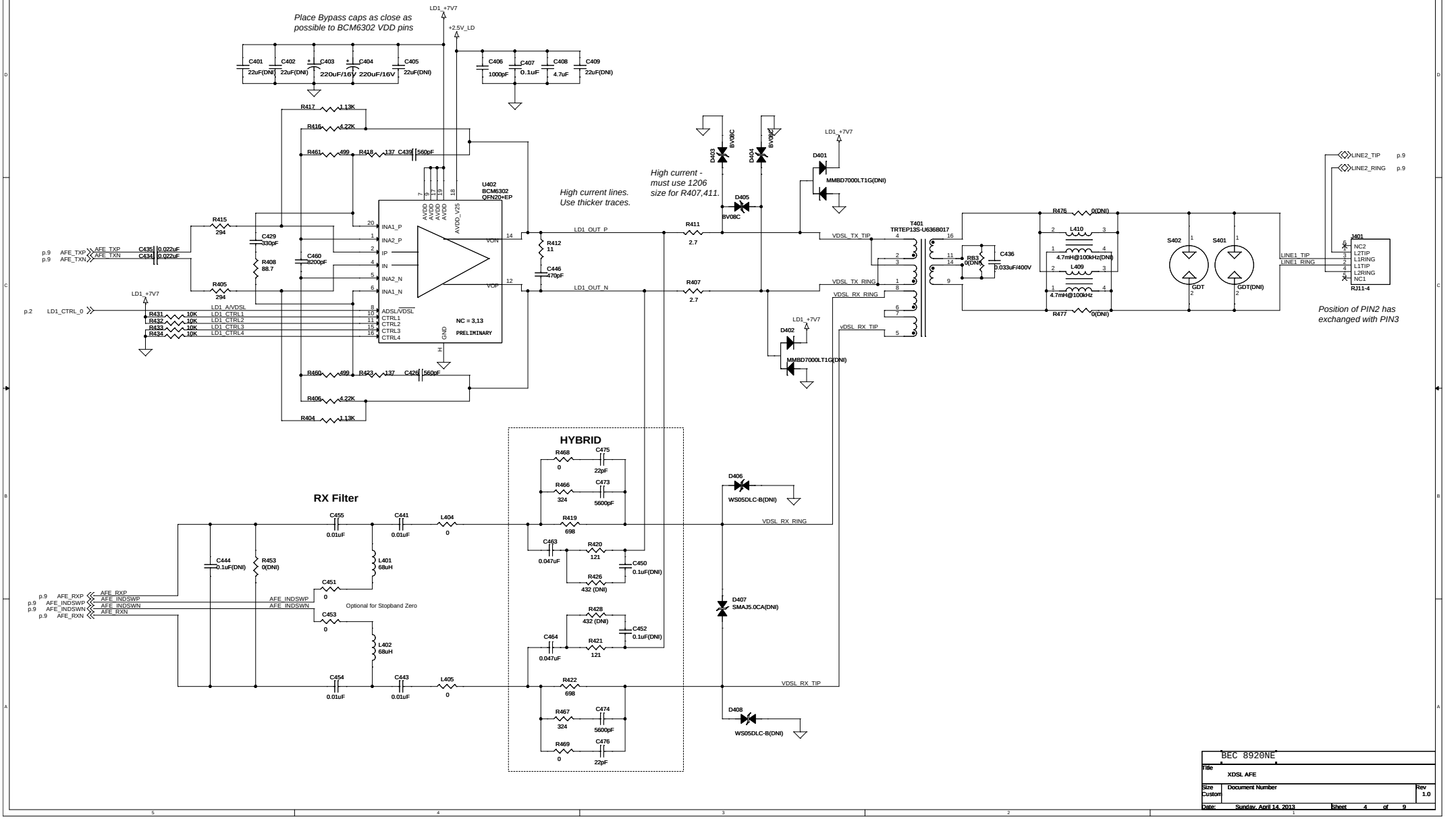


	BEC 8920NE	
Title	XDSL AFE	
Size: Custom	Document Number	Rev: 1.0
Date: Sunday, April 14, 2013	Sheet 4 of 9	

MII/TMII/RGMII - Layout Guidelines & Notes

1. Route traces with 50ohm characteristic impedance.
2. Match trace lengths to a tolerance of 385 mil within TX and RX separately.
3. Keep the receive and transmit signals kept away from each other and other analog and clock signals.
4. Place capacitors and ferrite beads close to VDD traces and routes short.

When programmed for LOM LED Mode.
Then SPEED LED behavior is as below:

Status	LED[2]	LED[1]	Speed
1000BASE-T	1	0	Green
100BASE-T	0	1	Yellow
10BASE-T	1	1	off
No Link	1	1	off

CONNECT MIIx_VDDO_1 & _2 TO 3.3V WHEN USED IN MII, RvMII, TMII MODE, OR WHEN NOT USED
CONNECT MIIx_VDDO_1 & _2 TO 2.5V WHEN USED IN RGMII MODE, OR WHEN NOT USED

! MII2_VDDO_1 & _2 PROVIDE THE I/O VOLTAGE FOR GPIO[51:40]. THEREFORE, MII2_VDDO_1 & _2 MUST BE CONNECTED TO 3.3V WHEN ANY OF GPIO[51:40] ARE USED.

VOLTAGE ON 63168 MII_VDDO AND 50612E OVDD_RGMII PINS MUST BE THE SAME AND MUST MATCH THE MII MODE SELECTED. THE BCM63268 DOES NOT SUPPORT 3.3V RGMII.

No decoupling cap necessary when MII port not used.

Place R511-516 close to 63168. MII outputs have 50 driver impedance. Use value to match trace impedance. Rtrace = Rterm + Rdriver. Increase value to reduce EMC.

Place R523-528 close to 54610. MII outputs have 50 driver impedance. Use value to match trace impedance. Rtrace = Rterm + Rdriver. Increase value to reduce EMC.

Place C503, C504, FB506 physically close to OVDD_RGMII pins, and keep traces very short. Place C505 physically close to OVDD pin.

Route TRD+/- pairs with 100-ohms differential trace immpedance

Place C506 physically close to center-tap pins of T501.

Place C511 physically close to U501 pin 3.
Place C512-C513 physically close to DVDD pins.
Place C515-C517 physically close to AVDDL pins.

Place C522-C523 physically close to U501 AVDD pins.

Board installed capacitors C510 and C511 values are based on a crystal specificed load capacitor.
CL value of 18 pF. C514 = C518 = 2x(CL - CS)
CS = C Stray = Combined trace and pin capacitance
Place Y501, C514 and C518 physically close to pins 7 and 8.

PHY ADDR: 0x18

TEST[3:2] = 11 for PHYA mode in which addr = 0x18 + PHYA0

To support EEE sleep/wake power surges, set C504 to 10uF, C514, C517 to 22uF and C524 to 33uF. Also install R510

B50612E PHY Address

PHY Addr	TEST[3:2]	PHYA0
0x00	00	0
0x01	00	1
0x18	11	0
0x19	11	1

Strap the B50612E to RGMII 3.3V mode to preserve LED configuration and allow LED4 to be compatible with IRQ (open-drain with pull-up). Software configures the B50612E to the correct RGMII mode (2.5V RGMII).

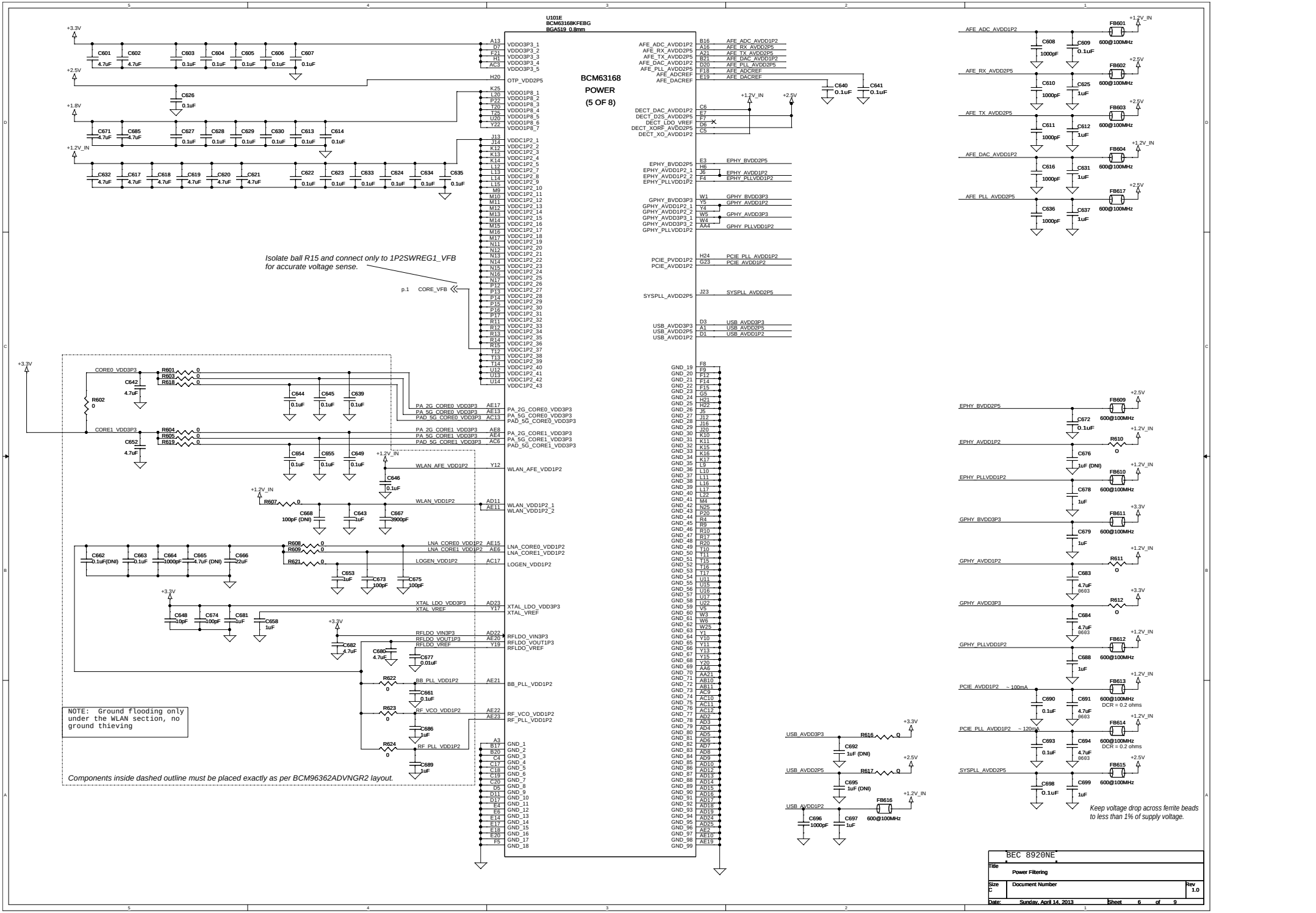
B50612E RGMII MODE SELECTION TABLE

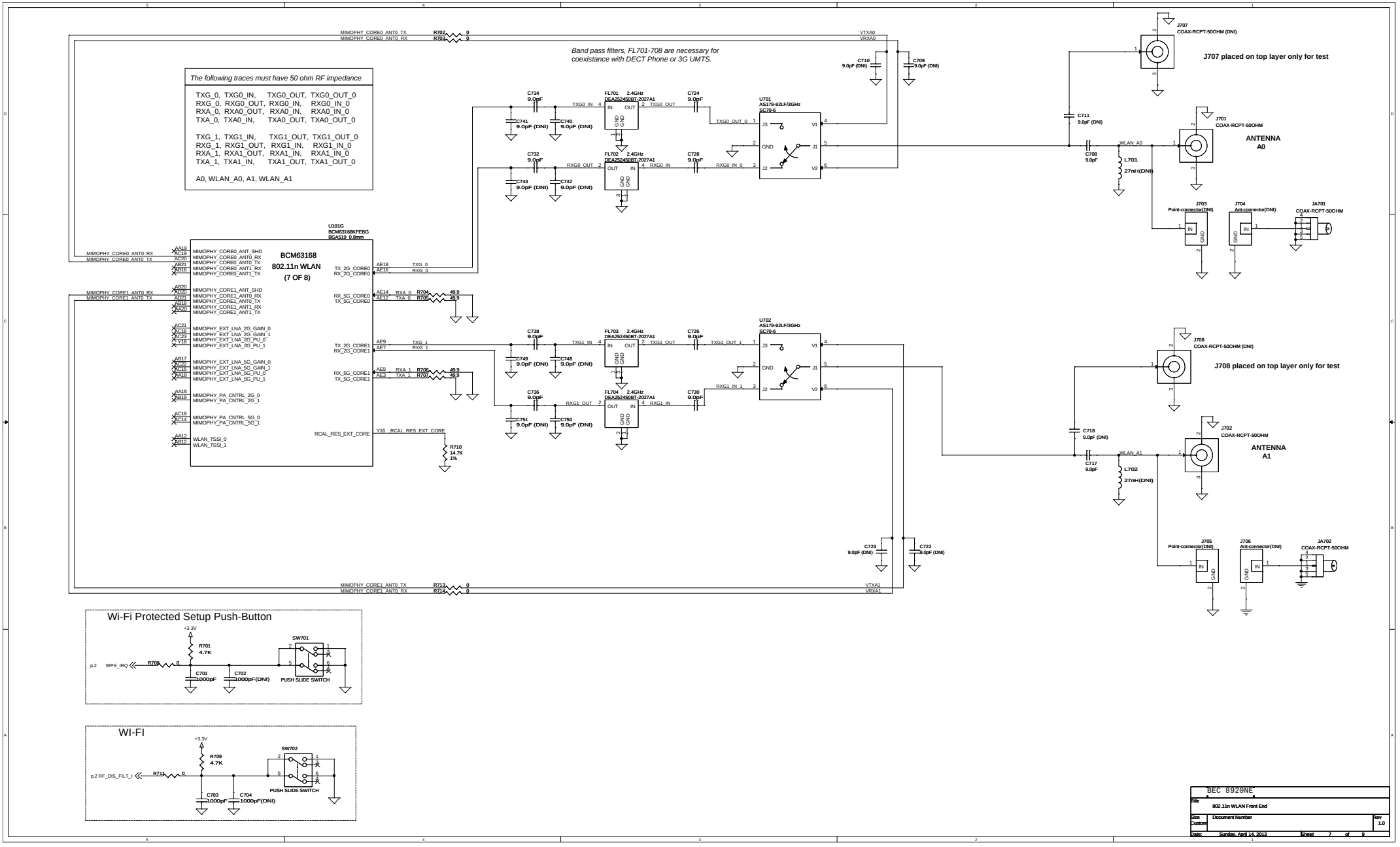
RGMII Mode	MODE_SEL[1:0]	Pin Configuration
RGMII 3.3V	00	TEST[3:2] = 00 or 11, LED[3]=0 LED[2]=0 LED[4]=0
-> RGMII 2.5V	01	TEST[3:2] = 00 or 11, LED[3]=0 LED[2]=1 LED[4]=0
RGMII HSTL	10	TEST[3:2] = 00 or 11, LED[3]=1 LED[2]=0 LED[4]=0
Reserved	11	TEST[3:2] = 00 or 11, LED[3]=1 LED[2]=1 LED[4]=0
RGMII 3.3V	00	TEST[3:2] = 00 or 11, LED[3]=0 LED[2]=X LED[4]=1
RGMII HSTL	10	TEST[3:2] = 00 or 11, LED[3]=1 LED[2]=X LED[4]=1

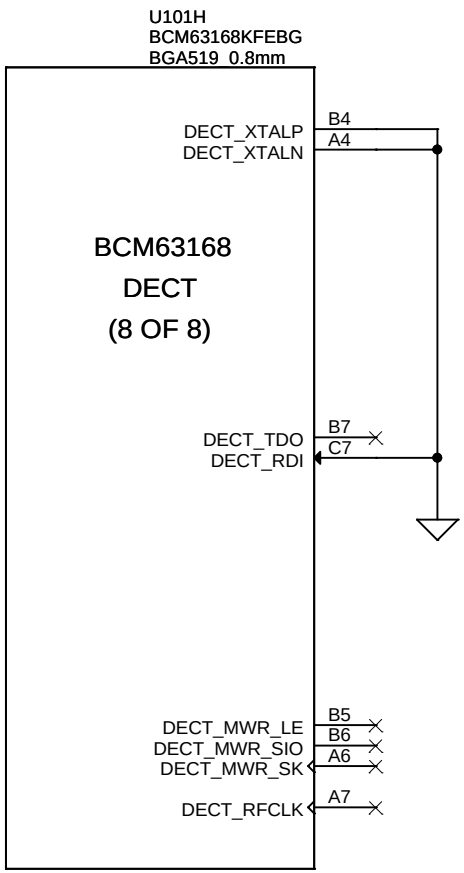
X = Don't Care

MODE_SEL[1] =LED[3]
MODE_SEL[0] =LED[2]

BEC 8920NE	
Title	GPHY2 on MII1 and MII Ports 3
Size C	Document Number — Rev 1.0
Date: Sunday, April 14, 2013	Sheet 5 of 9


U101E
BCM63168KFEBG
BGA519_0.8mm
BCM63168
POWER
(5 OF 8)
Isolate ball R15 and connect only to 1P2SWREG1_VFB for accurate voltage sense.
p.1 CORE_VFB
NOTE: Ground flooding only under the WLAN section, no ground thieving
Components inside dashed outline must be placed exactly as per BCM96362ADVNGR2 layout.
Keep voltage drop across ferrite beads to less than 1% of supply voltage.
BEC 8920NE
Power Filtering
Size C
Document Number
Rev 1.0
Date: Sunday, April 14, 2013
Sheet 6 of 9


The following traces must have 50 ohm RF impedance
TXG_0, TXG0_IN, TXG0_OUT, TXG0_OUT_0
RXG_0, RXG0_OUT, RXG0_IN, RXG0_IN_0
RXA_0, RXA0_OUT, RXA0_IN, RXA0_IN_0
TXA_0, TXA0_IN, TXA0_OUT, TXA0_OUT_0
TXG_1, TXG1_IN, TXG1_OUT, TXG1_OUT_0
RXG_1, RXG1_OUT, RXG1_IN, RXG1_IN_0
RXA_1, RXA1_OUT, RXA1_IN, RXA1_IN_0
TXA_1, TXA1_IN, TXA1_OUT, TXA1_OUT_0
A0, WLAN_A0, A1, WLAN_A1
Band pass filters, FL701-708 are necessary for coexistance with DECT Phone or 3G UMTS.
BCM63168
802.11n WLAN
(7 OF 8)
U101G
BCM63168KFEBG
BGA519 0.8mm
J707 placed on top layer only for test
J708 placed on top layer only for test
ANTENNA A0
ANTENNA A1
Wi-Fi Protected Setup Push-Button
WI-FI
PUSH SLIDE SWITCH
BEC 8920NE
802.11n WLAN Front End



BEC 8920NE			
Title: DECT			
Size: A	Document Number		Rev: 1.0
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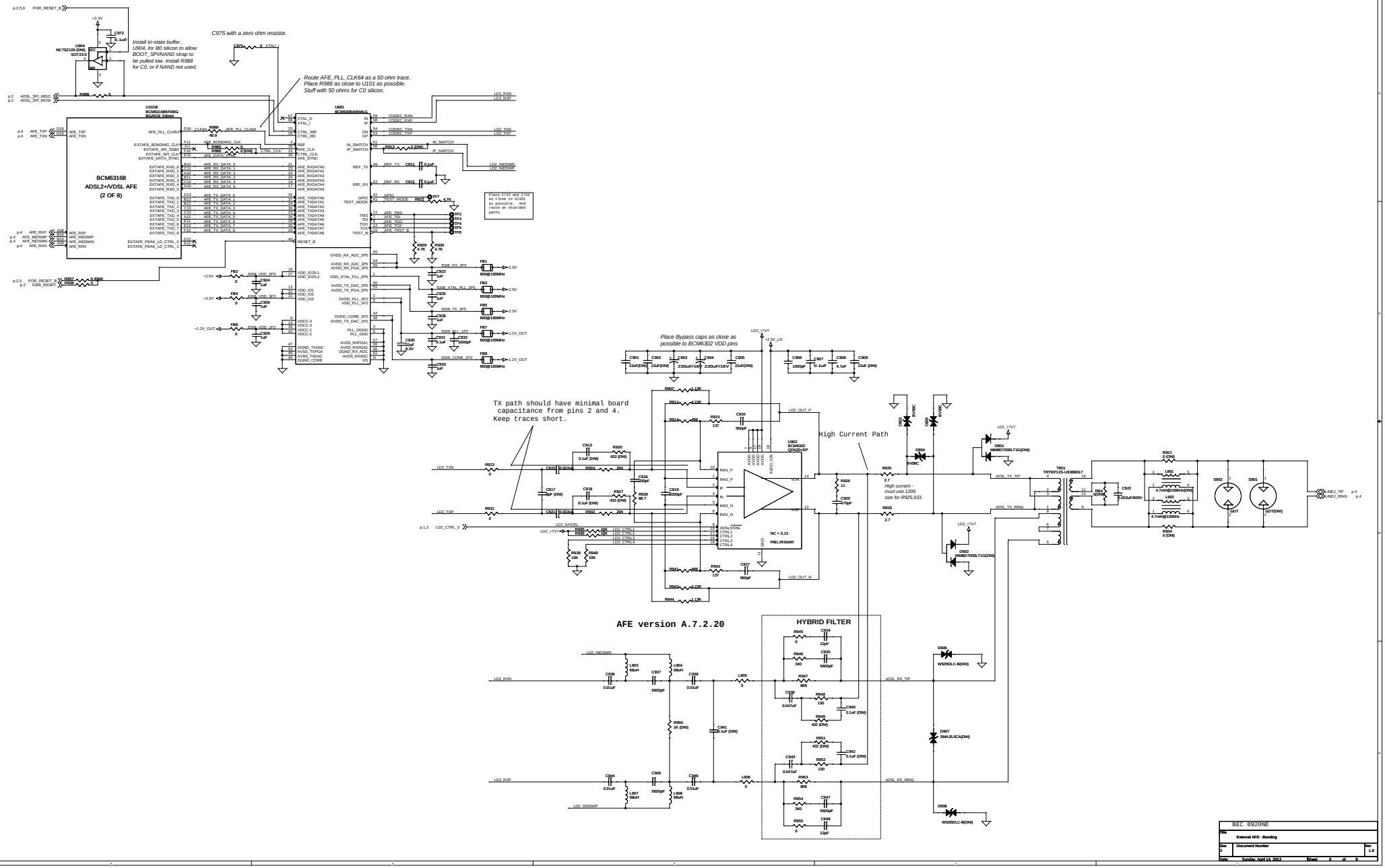
C975 with a zero ohm resistor.
Install tri-state buffer , U904, for B0 silicon to allow BOOT_SPI/NAND strap to be pulled low. Install R988 for C0, or if NAND not used.
Route AFE_PLL_CLK64 as a 50 ohm trace. Place R989 as close to U101 as possible. Stuff with 50 ohms for C0 silicon.
BCM63168
ADSL2+/VDSL AFE
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Place Bypass caps as close as possible to BCM6302 VDD pins
TX path should have minimal board capacitance from pins 2 and 4. Keep traces short.
High Current Path
AFE version A.7.2.20
HYBRID FILTER
BEC 8920NE
External AFE - Bonding
Sunday, April 14, 2013