Transmitter Description

The ISL3873B transmitter is designed as a Direct Sequence Spread Spectrum Phase Shift Keying (DSSS PSK) modulator which is capable of handling data rates of up to 11Mbps (refer to AC and DC specifications). The various modes of the modulator are Differential Binary Phase Shift Keying (DBPSK) for 1Mbps, Differential Quaternary Phase Shift Keying (DQPSK) for 2Mbps, and Complementary Code Keying (CCK) for 5.5Mbps and 11Mbps.

CCK is essentially a quadra-phase form of M-ARY Keying. A description of that modulation can be found in Chapter 5 of: "Telecommunications System Engineering", by Lindsey and Simon, Prentiss Hall publishing. The formula for CCK can be found later in this datasheet.

The implemented data rates using a clock rate of 44MHz are shown in Table 6 and the modulation schemes are indicated in Figure 13. The major functional blocks of the transmitter include a Processor Interface, Modulator, Data Scrambler, Preamble/Header Generator, TX Filter, AGC Control, and ADC and DAC circuits.

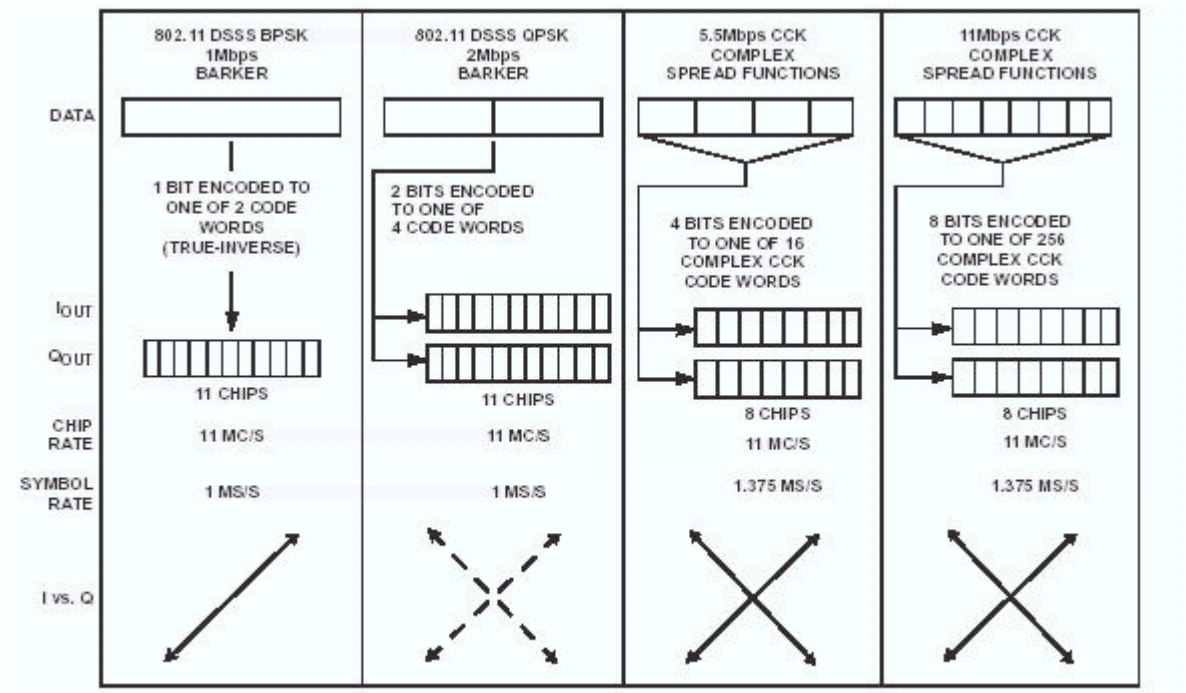

FIGURE 13. MODULATION MODES

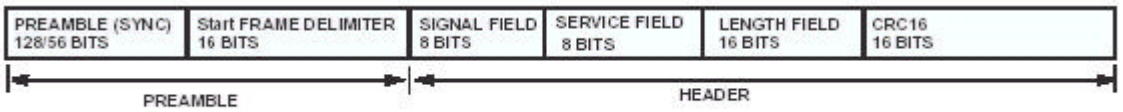

FIGURE 14. 802.11 PREAMBLE/HEADER

The preamble is always transmitted as the DBPSK waveform while the header can be configured to be either DBPSK, or DQPSK,and data packetscan be configured forDBPSK, DQPSK, or CCK. The preamble is used by the receiver to achieve initial Pseudo Noise (PN) synchronization while the header includes the necessary data fields of the communications protocol to establish the physical layer link. The transmitter generates the synchronization preamble and header and knows when to make the DBPSK to DQPSK or CCK switchover, as required.

For the 1 and 2Mbps modes, the transmitter accepts data from the external source, scrambles it, differentially encodes it as either DBPSK or DQPSK, and spreads it with the BPSK PN sequence. The baseband digital signals are then output to the external IF modulator.

For the CCK modes, the transmitter inputs the data and partitions it into nibbles (4 bits) or bytes (8 bits). At 5.5Mbps, it uses four of those bits to select one of 16 complex spread sequences from a table of CCK sequences. Thus, there are 16 possible spread sequences to send, but only one is sent. This sequence is then modulated on the I and Q outputs. The initial phase reference for the data portion of the packet is the phase of the last bit of the header. At 11Mbps, one byte is used as above where 8 bits are used to select one of 256 spread sequences for a symbol.

Bit rates for the ISL3873B are defined in Table 6. This table provides information on bit rates, data rates and symbol rates for an MCLK of 44MHz clock. Figure 13 shows the modulation schemes for the different bits rates. The modulator is completely independent from the demodulator, allowing the PRISM baseband processor to be used in full duplex operation.

Header/Packet Description

The ISL3873B is designed to handle packetized Direct Sequence Spread Spectrum (DSSS) data transmissions. The ISL3873B generates its own preamble and header information. It uses two packet preamble and header configurations. The first is backwards compatible with the existing IEEE 802.11-1997 1 and 2Mbps modes and the second is the optional shortened mode which maximizes throughput at the expense of compatibility with legacy equipment.

In the long preamble mode, the device uses a synchronization preamble of 128 symbols along with a header that includes four fields. The preamble is all 1's (before entering the scrambler) plus a Start Frame Delimiter (SFD). The actual transmitted pattern of the preamble is randomized by the scrambler. The preamble is always transmitted as a DBPSK waveform (1Mbps). The duration of the long preamble and header is 192s.

In the short preamble mode, the modem uses a synchronization field of 56 zero symbols along with an SFD transmitted at 1Mbps. The short header is transmitted at the 2Mbps rate. The synchronization preamble is all 0's to distinguish it from the long header mode and the short preamble SFD is the time reverse of the long preamble SFD. The duration of the short preamble and header is 96s.

Start Frame Delimiter (SFD) Field (16 Bits)

This field is used to establish the link frame timing. The ISL3873B will not declare a valid data packet, even if it PN acquires, unless it detects the SFD. The ISL3873B receiver auto-detects if the packet is long or short preamble and sets SFD time-out. The timer starts counting after initialization of the de-scrambler is complete.

Header Field

The header field is defined by four fields which are shown in Figure 14. These fields are Signal Field, Service Field, Length Field and CITT-CRC16 Field. They are further defined by the following:

Signal Field (8 Bits) - This field indicates what data rate the data packet that follows the header will be. The ISL3873B receiver looks at the signal field to determine whether it needs to switch from DBPSK demodulation into DQPSK, or CCK demodulation at the end of the preamble and header fields.

Service Field (8 Bits) - The MSBofthisfield is used to indicate the correct length when the length field value is ambiguous at 11Mbps. See IEEE STD 802.11 for definition of the other bits. Bit 2 is used by the ISL3873B to indicate that the carrier reference and the bit timing references are derived from the same oscillator (locked oscillators).

Length Field (16 Bits) - This field indicates the number of microseconds it will take to transmit the payload data (PSDU). The external controller (MAC) will check the length field in determining when it needs to de-assert RX_PE.

CCITT - CRC 16 Field (16 Bits) - This field includes the 16-bit CCITT - CRC 16 calculation of the three header fields. This value is compared with the CCITT - CRC 16 code calculated at the receiver. The ISL3873B receiver will indicate a CCITT - CRC 16 error via CR24 bit 2 and will lower MD_RDY and reset the receiver to the acquisition mode if there is an error.

The CRC or cyclic Redundancy Check is a CCITT CRC-16 FCS (Frame Check Sequence). It is the ones complement of the remainder generated by the modulo 2 division of the protected bits by the polynomial:

$x^{16} + x^{12} + x^5 + 1$

The protected bits are processed in transmit order. All CRC calculations are made ahead of data scrambling. A shift register with two taps is used for the calculation. It is preset to all ones and then the protected fields are shifted through the register. The output is then complemented and the residual shifted out MSB first.

The following Configuration Registers (CR) are used to program the preamble/header functions, more programming details about these registers can be found in the Control Registers section of this document:

CR 3 - Defines the short preamble length minus the SFD in symbols. The 802.11 protocol requires a setting of 56d = 38h for the optional short preamble.

CR 4 - Defines the long preamble length minus the SFD in symbols. The 802.11 protocol requires a setting of 128d = 80h for the mandatory long preamble.

CR 5 Bits 0, 1 - These bits of the register set the Signal field to indicate what modulation is to be used for the data portion of the packet.

CR 6 - The value to be used in the Service field.

CR 7 and 8 - Defines the value of the transmit data length field. This value includes all symbols following the last header field symbol and is in microseconds required to transmit the data at the chosen data rate.

The packet consists of the preamble, header and MAC Protocol Data Unit (MPDU). The data is transmitted exactly as received from the control processor. Some dummy bits will be appended to the end of the packet to ensure an orderly shutdown of the transmitter. This prevents spectrum splatter. At the end of a packet, the external controller is expected to de-assert the TX_PE line to shut the transmitter down.

Scrambler and Data Encoder Description

The modulator has a data scrambler that implements the scrambling algorithm specified in the IEEE 802.11 standard. This scrambler is used for the preamble, header, and data in all modes. The data scrambler is a self synchronizing circuit. It consists of a 7-bit shift register with feedback from specified taps of the register. Both transmitter and receiver use the same scrambling algorithm. The scrambler can be disabled by setting CR32 bit 2 to 1.

NOTE: Be advised that the IEEE 802.11 compliant scrambler in the ISL3873B has the property that it can lock up (stop scrambling) on random data followed by repetitive bit patterns. The probability of this happening is 1/128. The patterns that have been identified are all zeros, all ones, repeated 10s, repeated 1100s, and repeated 111000s. Any break in the repetitive pattern will restart the scrambler. To ensure that this does not cause any problem, the CCK waveform uses a ping pong differential coding scheme that breaks up repetitive 0' s patterns.

Scrambling is done by division with a prescribed polynomial as shown in Figure 15. A shift register holds the last quotient and the output is the exclusive or of the data and the sum of taps in the shift register. The transmit scrambler seed for the long preamble or for the short preamble can be set with CR48 or CR49.

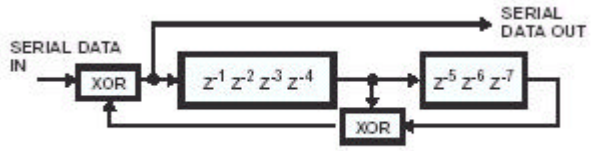

FIGURE 15. SCRAMBLING PROCESS

For the 1Mbps DBPSK data rates and for the header in all rates using the long preamble, the data coder implements the desired DBPSK coding by differential encoding the serial data from the scrambler and driving both the I and Q output channels together. For the 2Mbps DQPSK data rate and for the header in the short preamble mode, the data coder implements the desired coding as shown in the DQPSK Data Encoder Table 7. This coding scheme results from differential coding of dibits (2 bits). Vector rotation is counterclockwise although bits 6 and 7 of configuration register CR 1 can be used to reverse the rotation sense of the TX or RX signal if desired.

Spread Spectrum Modulator Description

The modulator is designed to generate DBPSK, DQPSK, and CCK spread spectrum signals. The modulator is capable of automatically switching its rate where the preamble is DBPSK modulated, and the data and/or header are modulated differently. The modulator can support date rates of 1, 2, 5.5 and 11Mbps. Quadraphase (I/Q) modulation is used at the baseband for all modulation modes. Further information on the programming details required to set up the modulator can be obtained by contacting the factory.

TABLE 7. DQPSK DATA ENCODER

PHASE SHIFT	DIBIT PATTERN (d0, d1) d0 IS FIRST IN TIME
0	00
+90	01
+180	11
-90	10

In the 1Mbps DBPSK mode, the I and Q Channels are connected together and driven with the output of the scrambler and differential encoder. The I and Q Channels are then both multiplied with the 11-bit Barker word at the spread rate. The I and Q signals go to the Quadrature upconverter (HFA3724) to be modulated onto a carrier. Thus, the spreading and data modulation are BPSK modulated onto the carrier.

For the 2Mbps DQPSK mode, the serial data is formed into dibits or bit pairs in the differential encoder as detailed above. One of the bits from the differential encoder goes to the I Channel and the other to the Q Channel. The I and Q Channels are then both multiplied with the 11-bit Barker word at the spread rate. This forms QPSK modulation at the symbol rate with BPSK modulation at the spread rate.

CCK Modulation

For the CCK modes, the spreading code length is 8 complex chips and based on complementary codes. The chipping rate is 11Mchip/s. The following formula is used to derive the CCK code words that are used for spreading both 5.5 and 11Mbps:

$$c = \left\{ e^{j(\varphi_1+\varphi_2+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_4)}, -e^{j(\varphi_1+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_3)}, e^{j(\varphi_1+\varphi_3)}, -e^{j(\varphi_1+\varphi_2)}, e^{j\varphi_1} \right\}$$

(LSB to MSB), where c is the code word.

The terms: $\phi 1$, $\phi 2$, $\phi 3$, and $\phi 4$ are defined below for 5.5Mbps and 11Mbps.

This formula creates 8 complex chips (LSB to MSB) that are transmitted LSB first. The coding is a form of the generalized Hadamard transform encoding where the phase $\phi 1$ is added to all code chips, $\phi 2$ is added to all odd code chips, $\phi 3$ is added to all odd pairs of code chips and $\phi 4$ is added to all odd quads of code chips.

The phase $\phi 1$ modifies the phase of all code chips of the sequence and is DQPSK encoded for 5.5 and 11Mbps. This will take the form of rotating the whole symbol by the appropriate amount relative to the phase of the preceding symbol. Note that the last chip of the symbol defined above is the chip that indicates the symbol' s reference phase.

For the 5.5Mbps CCK mode, the output of the scrambler is partitioned into nibbles. The first two bits are encoded as differential symbol phase modulation in accordance with Table 8. All odd numbered symbols of the MPDU are given an extra 180 degree (π) rotation in addition to the standard DQPSK modulation as shown in the table. The symbols of the MPDU shall be numbered starting with "0" for the first symbol for the purposes of determining odd and even symbols. That is, the MPDU starts on an even numbered symbol. The last data dibit (d2 and d3) CCK encodes the chips as specified in Table 9. This table is derived from the CCK formula above by setting $\phi 2$ =(d2*pi)+pi/2, $\phi 3$ = 0, and $\phi 4$ = d3*pi. In Table 9 d2 and d3 are in the order shown and the complex chips are shown LSB to MSB (left to right) with LSB transmitted first.

TABLE 8. DQPSK ENCODING TABLE

DIBIT PATTERN (d(0), d(1)) d(0) IS FIRST IN TIME	EVEN SYMBOLS PHASE CHANGE (+jω)	ODD SYMBOLS PHASE CHANGE (+jω)
00	0	π
01	π/2	3π/2 (-π/2)
11	π	0
10	3π/2 (-π/2)	π/2

TABLE 9. 5.5Mbps CCK ENCODING TABLE

d2, d3	CHIPS							
00	1*j*	1	1*j*	-1	1*j*	1	-1*j*	1
01	-1*j*	-1	-1*j*	1	1*j*	1	-1*j*	1
10	-1*j*	1	-1*j*	-1	-1*j*	1	1*j*	1
11	1*j*	-1	1*j*	1	-1*j*	1	1*j*	1

At 11Mbps, 8 bits (d0 to d7; d0 first in time) are transmitted per symbol.

The first dibit (d0, d1) encodes the phase $\phi 1$ based on DQPSK. The DQPSK encoder is specified in Table 8 above. The phase change for $\phi 1$ is relative to the phase $\phi 1$ of the preceding symbol. In the case of rate change, the phase change for $\phi 1$ is relative to the phase $\phi 1$ of the preceding CCK symbol. All odd numbered symbols of the MPDU are given an extra 180 degree (π) rotation in accordance with the DQPSK modulation as shown in Table 8. Symbol numbering starts with "0" for the first symbol of the MPDU.

The data dibits: (d2, d3), (d4, d5), (d6, d7) encode $\phi 2$, $\phi 3$, and $\phi 4$ respectively based on QPSK as specified in Table 10. Note that this table is binary, not Grey, coded.

TABLE 10. QPSK ENCODING TABLE

DIBIT PATTERN (d(i), d(i+1)) d(i) IS FIRST IN TIME	PHASE
00	0
01	π/2
10	π
11	3π/2 (-π/2)