Ivy Bridge Processor (DMI,PEG,FDI)

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

[4,6,7,8,10,33,34,38,43] +1.05V_PCH
[4,10,12,13,33,34,37,43] +1.5V_SUS
[6,7,8,9,10,27,31,34] +3V_S5
[4,33] +1.5V_CPU

02

U36A

DMI
- [6] DMI_TXN0 → B27 DMI_RX#[0]
- [6] DMI_TXN1 → B25 DMI_RX#[1]
- [6] DMI_TXN2 → A25 DMI_RX#[2]
- [6] DMI_TXN3 → B24 DMI_RX#[3]
- [6] DMI_TXP0 → B28 DMI_RX[0]
- [6] DMI_TXP1 → B26 DMI_RX[1]
- [6] DMI_TXP2 → A24 DMI_RX[2]
- [6] DMI_TXP3 → B23 DMI_RX[3]
- G21 DMI_TX#[0] → [6] DMI_RXN0
- E22 DMI_TX#[1] → [6] DMI_RXN1
- F21 DMI_TX#[2] → [6] DMI_RXN2
- D21 DMI_TX#[3] → [6] DMI_RXN3
- G22 DMI_TX[0] → [6] DMI_RXP0
- D22 DMI_TX[1] → [6] DMI_RXP1
- F20 DMI_TX[2] → [6] DMI_RXP2
- C21 DMI_TX[3] → [6] DMI_RXP3

Intel(R) FDI
- [6] FDI_TXN0 → A21 FDI0_TX#[0]
- [6] FDI_TXN1 → H19 FDI0_TX#[1]
- [6] FDI_TXN2 → E19 FDI0_TX#[2]
- [6] FDI_TXN3 → F18 FDI0_TX#[3]
- [6] FDI_TXN4 → B21 FDI1_TX#[0]
- [6] FDI_TXN5 → C20 FDI1_TX#[1]
- [6] FDI_TXN6 → D18 FDI1_TX#[2]
- [6] FDI_TXN7 → E17 FDI1_TX#[3]
- [6] FDI_TXP0 → A22 FDI0_TX[0]
- [6] FDI_TXP1 → G19 FDI0_TX[1]
- [6] FDI_TXP2 → E20 FDI0_TX[2]
- [6] FDI_TXP3 → G18 FDI0_TX[3]
- [6] FDI_TXP4 → B20 FDI1_TX[0]
- [6] FDI_TXP5 → C19 FDI1_TX[1]
- [6] FDI_TXP6 → D19 FDI1_TX[2]
- [6] FDI_TXP7 → F17 FDI1_TX[3]
- [6] FDI_FSYNC0 → J18 FDI0_FSYNC
- [6] FDI_FSYNC1 → J17 FDI1_FSYNC
- [6] FDI_INT → H20 FDI_INT
- [6] FDI_LSYNC0 → J19 FDI0_LSYNC
- [6] FDI_LSYNC1 → H17 FDI1_LSYNC

eDP
- eDP_COMP → A18 eDP_COMPIO
- INT_eDP_HPD_Q → B16 eDP_ICOMPO
- A17 eDP_HPD
- C15 eDP_AUX
- D15 eDP_AUX#
- C17 eDP_TX[0]
- E16 eDP_TX[1]
- C16 eDP_TX[2]
- G15 eDP_TX[3]
- C18 eDP_TX#[0]
- E16 eDP_TX#[1]
- D16 eDP_TX#[2]
- F15 eDP_TX#[3]

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils. eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22 → PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_RXN[0..15] [14]
- PEG_RX#[0] K33 PEG_RXN0
- PEG_RX#[1] M35 PEG_RXN1
- PEG_RX#[2] L34 PEG_RXN2
- PEG_RX#[3] J35 PEG_RXN3
- PEG_RX#[4] J32 PEG_RXN4
- PEG_RX#[5] H34 PEG_RXN5
- PEG_RX#[6] H31 PEG_RXN6
- PEG_RX#[7] G33 PEG_RXN7
- PEG_RX#[8] G30 PEG_RXN8
- PEG_RX#[9] F35 PEG_RXN9
- PEG_RX#[10] E34 PEG_RXN10
- PEG_RX#[11] E32 PEG_RXN11
- PEG_RX#[12] D33 PEG_RXN12
- PEG_RX#[13] D31 PEG_RXN13
- PEG_RX#[14] B33 PEG_RXN14
- PEG_RX#[15] C32 PEG_RXN15

PEG_RXP[0..15] [14]
- PEG_RX[0] J33 PEG_RXP0
- PEG_RX[1] L35 PEG_RXP1
- PEG_RX[2] K34 PEG_RXP2
- PEG_RX[3] H35 PEG_RXP3
- PEG_RX[4] H32 PEG_RXP4
- PEG_RX[5] G34 PEG_RXP5
- PEG_RX[6] G31 PEG_RXP6
- PEG_RX[7] F33 PEG_RXP7
- PEG_RX[8] F30 PEG_RXP8
- PEG_RX[9] E35 PEG_RXP9
- PEG_RX[10] E33 PEG_RXP10
- PEG_RX[11] E32 PEG_RXP11
- PEG_RX[12] D34 PEG_RXP12
- PEG_RX[13] E31 PEG_RXP13
- PEG_RX[14] C33 PEG_RXP14
- PEG_RX[15] B32 PEG_RXP15

PEG_TX[0..15]
- PEG_TX#[0] M29 PEG_TXN0_C
- PEG_TX#[1] M32 PEG_TXN1_C
- PEG_TX#[2] M31 PEG_TXN2_C
- PEG_TX#[3] L32 PEG_TXN3_C
- PEG_TX#[4] L29 PEG_TXN4_C
- PEG_TX#[5] K31 PEG_TXN5_C
- PEG_TX#[6] K28 PEG_TXN6_C
- PEG_TX#[7] J30 PEG_TXN7_C
- PEG_TX#[8] J28 PEG_TXN8_C
- PEG_TX#[9] H29 PEG_TXN9_C
- PEG_TX#[10] G27 PEG_TXN10_C
- PEG_TX#[11] E29 PEG_TXN11_C
- PEG_TX#[12] E27 PEG_TXN12_C
- PEG_TX#[13] D28 PEG_TXN13_C
- PEG_TX#[14] E26 PEG_TXN14_C
- PEG_TX#[15] E25 PEG_TXN15_C
- PEG_TX[0] M28 PEG_TXP0_C
- PEG_TX[1] M33 PEG_TXP1_C
- PEG_TX[2] M30 PEG_TXP2_C
- PEG_TX[3] L31 PEG_TXP3_C
- PEG_TX[4] L28 PEG_TXP4_C
- PEG_TX[5] K30 PEG_TXP5_C
- PEG_TX[6] K27 PEG_TXP6_C
- PEG_TX[7] J29 PEG_TXP7_C
- PEG_TX[8] J27 PEG_TXP8_C
- PEG_TX[9] H28 PEG_TXP9_C
- PEG_TX[10] G28 PEG_TXP10_C
- PEG_TX[11] E28 PEG_TXP11_C
- PEG_TX[12] F28 PEG_TXP12_C
- PEG_TX[13] D27 PEG_TXP13_C
- PEG_TX[14] E26 PEG_TXP14_C
- PEG_TX[15] D25 PEG_TXP15_C

Ivy Bridge_rPGA_2DPC_Rev0p61

Ivy Bridge Processor (CLK,MISC,JTAG)

U36B

MISC
- [7] H_SNB_IVB# → C26 PROC_SELECT#
- TP12 → SKTOCC# AN34 SKTOCC#

THERMAL
- TP9 → TP_CATERR# AL33 CATERR#
- [32] EC_PECI → AN33 PECI
- [32,41] H_PROCHOT# → R168 56_4 H_PROCHOT#_R → AL32 PROCHOT#
- [9] PM_THRMTRIP# → AN32 THERMTRIP#

PWR MANAGEMENT
- [6] PM_SYNC → R448 *0_4_S PM_SYNC_R → AM34 PM_SYNC
- [9] H_PWRGOOD → R450 *0_4_S H_PWRGOOD_R → AP33 UNCOREPWRGOOD
- R461 10K_4, C524 0.1U/10V_4, PM_DRAM_PWRGD_R → V8 SM_DRAMPWROK
- +1.05V_PCH → R421 *75_4 → CPU_PLTRST#
- CPU_PLTRST# → R444 *43_4 CPU_PLTRST#_R → AR33 RESET#
- R160 750/F_4, RV11 *EGA-0402, For ESD

CLOCKS
- BCLK A28 → CLK_CPU_BCLKP [8]
- BCLK# A27 → CLK_CPU_BCLKN [8]
- DPLL_REF_CLK A16 ← R533 1K/F_4
- DPLL_REF_CLK# A15 ← R536 1K/F_4 ← +1.05V_PCH
- DPLL_SSCLKP_R R534 *0_4 → CLK_DPLL_SSCLKP [8]
- DPLL_SSCLKN_R R537 *0_4 → CLK_DPLL_SSCLKN [8]

DDR3 MISC
- SM_DRAMRST# → R8 CPU_DRAMRST#
- SM_RCOMP[0] AK1 SM_RCOMP_0 R565 140/F_4
- SM_RCOMP[1] AS SM_RCOMP_1 R559 25.5/F_4
- SM_RCOMP[2] A4 SM_RCOMP_2 R560 200/F_4

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

JTAG & BPM
- PRDY# AP29 XDP_PRDY# → TP19
- PREQ# AP27 XDP_PREQ# → TP17
- TCK AR26 XDP_TCLK → TP47
- TMS AR27 XDP_TMS → TP41
- TRST# AP30 XDP_TRST# → TP38
- TDI AR28 XDP_TDI_R → TP43
- TDO AP26 XDP_TDO → TP56
- DBR# AL35 XDP_DBRST# → XDP_DBRST# [6]
- BPM#[0] AT28
- BPM#[1] AR29
- BPM#[2] AR30
- BPM#[3] AT30
- BPM#[4] AP32
- BPM#[5] AR31
- BPM#[6] AT31
- BPM#[7] AR32

Ivy Bridge_rPGA_2DPC_Rev0p61

+1.5V_SUS
- R278 1K/F_4
- [12,13] DDR3_DRAMRST# → R280 1K/F_4 CPU_DRAMRST#_R
- For ESD: SC52 *0.1U/10V_4
- R275 *0_4, Q31 ME2N7002E → CPU_DRAMRST#
- [8] DRAMRST_CNTRL_PCH → R613 0_4
- FOR DEEP S3 [32] EC_DRAMRST_GATE → R614 *0_4
- C289 0.047U/10V_4, R271 4.99K/F_4
- [12,13] DRAMRST_CNTRL_DDR

CPU_PLTRST#_R
- R147 1.5K/F_4
- +3V_S5 → C500 *0.1U/10V_4
- U32 *74LVC1G07GW: NC, VCC, IN, GND, OUT
- [8,14,24,27] PLTRST# → CPU_PLTRST#

+3V_S5
- C290 *0.1U/10V_4
- U15 *74AHC1G09GW
- [6] SYS_PWROK
- [6] PM_DRAM_PWRGD → R268 *0_4 → PM_DRAM_PWRGD_Q
- R270 *0_4_S
- PM_DRAM_PWRGD_Q → R272 *3K/F_4

+1.5V_CPU
- R274 200/F_4
- PM_DRAM_PWRGD_Q → R269 130/F_4 → PM_DRAM_PWRGD_R
- R273 39_4, Q30 ME2N7002E → MAINON# [4,34]

PEG x16 (UMA Non-stuff)

0.1uF AC coupling Caps for PCIE GEN2
0.22uF AC coupling Caps for PCIE GEN3

PEG_TXP[0..15] [14]
- PEG_TXP0_C C499 DIS@0.1U/10V/X5R_4 PEG_TXP0
- PEG_TXP1_C C475 DIS@0.1U/10V/X5R_4 PEG_TXP1
- PEG_TXP2_C C513 DIS@0.1U/10V/X5R_4 PEG_TXP2
- PEG_TXP3_C C493 DIS@0.1U/10V/X5R_4 PEG_TXP3
- PEG_TXP4_C C487 DIS@0.1U/10V/X5R_4 PEG_TXP4
- PEG_TXP5_C C508 DIS@0.1U/10V/X5R_4 PEG_TXP5
- PEG_TXP6_C C477 DIS@0.1U/10V/X5R_4 PEG_TXP6
- PEG_TXP7_C C504 DIS@0.1U/10V/X5R_4 PEG_TXP7
- PEG_TXP8_C C478 DIS@0.1U/10V/X5R_4 PEG_TXP8
- PEG_TXP9_C C502 DIS@0.1U/10V/X5R_4 PEG_TXP9
- PEG_TXP10_C C481 DIS@0.1U/10V/X5R_4 PEG_TXP10
- PEG_TXP11_C C494 DIS@0.1U/10V/X5R_4 PEG_TXP11
- PEG_TXP12_C C483 DIS@0.1U/10V/X5R_4 PEG_TXP12
- PEG_TXP13_C C491 DIS@0.1U/10V/X5R_4 PEG_TXP13
- PEG_TXP14_C C484 DIS@0.1U/10V/X5R_4 PEG_TXP14
- PEG_TXP15_C C497 DIS@0.1U/10V/X5R_4 PEG_TXP15

0.1uF AC coupling Caps for PCIE GEN2
0.22uF AC coupling Caps for PCIE GEN3

PEG_TXN[0..15] [14]
- PEG_TXN0_C C498 DIS@0.1U/10V/X5R_4 PEG_TXN0
- PEG_TXN1_C C474 DIS@0.1U/10V/X5R_4 PEG_TXN1
- PEG_TXN2_C C514 DIS@0.1U/10V/X5R_4 PEG_TXN2
- PEG_TXN3_C C492 DIS@0.1U/10V/X5R_4 PEG_TXN3
- PEG_TXN4_C C486 DIS@0.1U/10V/X5R_4 PEG_TXN4
- PEG_TXN5_C C509 DIS@0.1U/10V/X5R_4 PEG_TXN5
- PEG_TXN6_C C476 DIS@0.1U/10V/X5R_4 PEG_TXN6
- PEG_TXN7_C C503 DIS@0.1U/10V/X5R_4 PEG_TXN7
- PEG_TXN8_C C479 DIS@0.1U/10V/X5R_4 PEG_TXN8
- PEG_TXN9_C C501 DIS@0.1U/10V/X5R_4 PEG_TXN9
- PEG_TXN10_C C480 DIS@0.1U/10V/X5R_4 PEG_TXN10
- PEG_TXN11_C C495 DIS@0.1U/10V/X5R_4 PEG_TXN11
- PEG_TXN12_C C482 DIS@0.1U/10V/X5R_4 PEG_TXN12
- PEG_TXN13_C C490 DIS@0.1U/10V/X5R_4 PEG_TXN13
- PEG_TXN14_C C485 DIS@0.1U/10V/X5R_4 PEG_TXN14
- PEG_TXN15_C C496 DIS@0.1U/10V/X5R_4 PEG_TXN15

DP & PEG Compensation

+1.05V_PCH → R527 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

+1.05V_PCH → R532 *10K_4 INT_eDP_HPD_Q

+1.05V_PCH → R528 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)

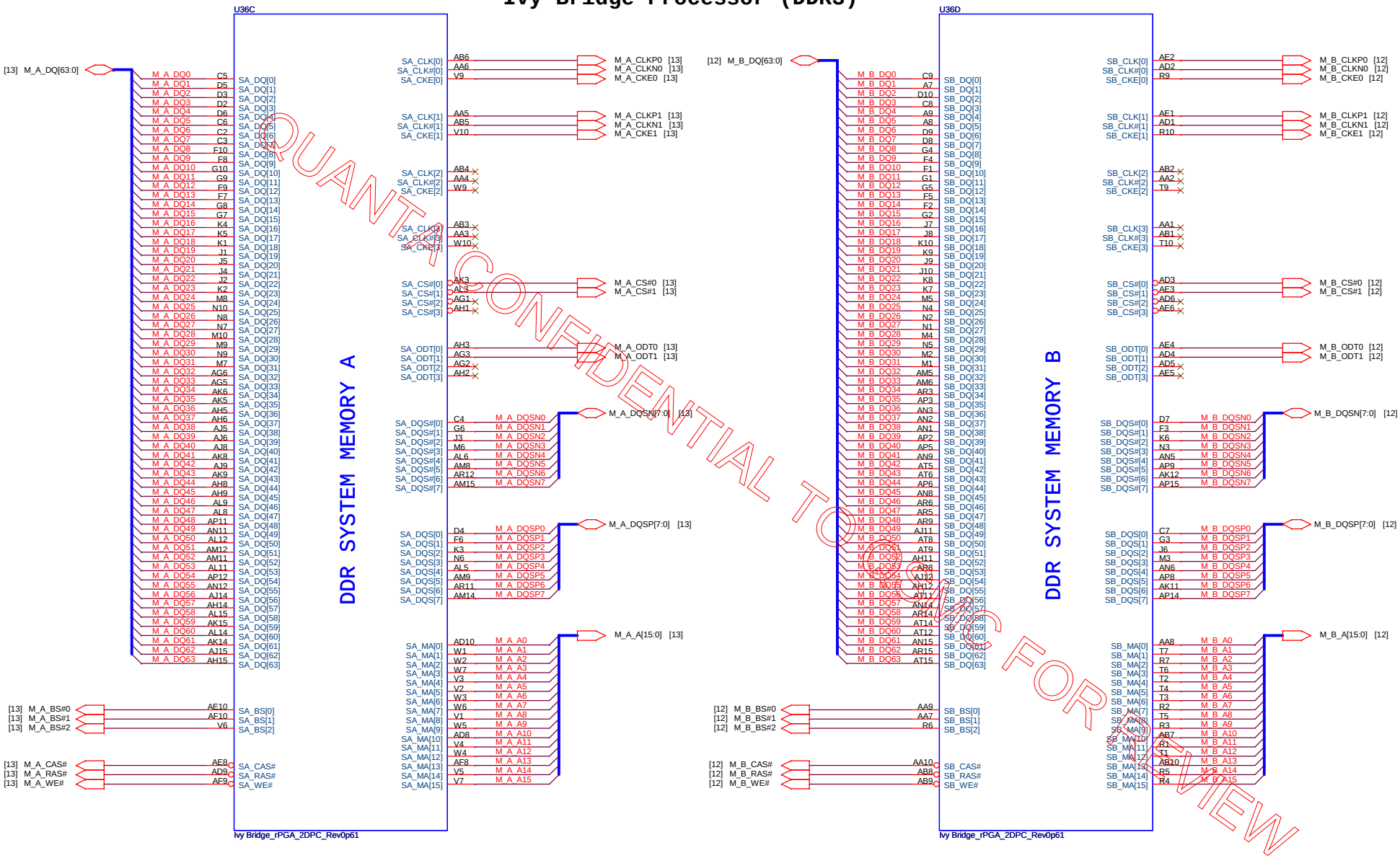
+1.05V_PCH
- H_PROCHOT# R164 62_4
- XDP_TDO R178 51_4
- XDP_TMS R480 51_4
- XDP_TDI_R R477 51_4
- XDP_PREQ# R172 *51_4
- XDP_TCLK R487 51_4
- XDP_TRST# R470 51_4

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	IVY Bridge 1/4	1A

Date: Wednesday, December 07, 2011 Sheet 2 of 45

Ivy Bridge Processor (DDR3)



PROJECT : LZ2A			
Quanta Computer Inc.			
Size	Document Number: IVY Bridge 2/4		Rev: 1A
Date: Wednesday, December 07, 2011	Sheet 3 of 45		

Ivy Bridge Processor (GRAPHIC POWER)

04

POWER

POWER

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

U36F

U36G

Ivy Bridge_rPGA_2DPC_Rev0p61

QUANTA CONFIDENTIAL TO QSMC FOR REVIEW

+VCC_CORE

SNB: 55A
IVY: 55A

22uF_8 x8 Socket TOP cavity

10uF_8 x10 Socket BOT cavity

+VCC_CORE:
22uF_8 x8 TOP Socket cavity
22uF_8 x8 TOP Socket edge
10uF_8 x10 BOT Socket cavity

+1.05V_PCH

SNB: 8.5A
IVY: 8.5A

22uF_8 x7 TOP Socket cavity
22uF_8 x5 BOT Socket cavity

22uF (Reserved)

+1.05V_PCH_40

R526 *0_4_S

+VCC_GFX

SNB: 21.5A
IVY: 33A

+VCC_GFX:
22uF_8 x2 TOP Socket cavity
22uF_8 x4 TOP Socket edge
22uF_8 x2 BOT Socket cavity
22uF_8 x4 BOT Socket edge

+1.8V

CPU VCCPL
SNB 45W:1.5A
330uF/7mohm x 1
10uF x 1
1uF x 2

VIDALERT# A29 H_CPU_SVIDALRT#
VIDSCLK A30 H_CPU_SVIDCLK
VIDSOUT A28 H_CPU_SVIDDAT

VCC_SENSE A35 R455 100_4 +VCC_CORE
VSS_SENSE A34 R454 100_4

VCCIO_SENSE B10 VTT_SENSE
VSS_SENSE_VCCIO A10 VSSP_SENSE

VTT_SENSE R550 10/F_4 +1.05V_PCH
VSSP_SENSE R556 10/F_4

VAXG_SENSE AK35 R423 100/F_4 +VCC_GFX
VSSAXG_SENSE AK34 R425 100/F_4

TP34
TP36

VCC_AXG_SENSE [41]
VSS_AXG_SENSE [41]

SM_VREF AL1 +VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1

SMDDR_VREF_DQ0_M3 [13]
SMDDR_VREF_DQ1_M3 [12]

R561 *1K_4
R564 *1K_4

SNB: 5A
IVY: 5A

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

+1.5V_CPU

330uF x1, 10uF_8 x6 Socket BOT edge.

SNB: 6A
IVY: 6A

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

+0.85V

330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

VCCSA_SENSE H23 R610 *0_4_S VCCSUSA_SENSE [39]

VCCSA_VID[0] C22 R241 1K_4
VCCSA_VID[1] C24 R235 1K_4

VCCSA_SEL0 [39]
VCCSA_SEL [39]

VCCIO_SEL A19 R521 *0_4 H_VTTVID1 [38]

Ivy Bridge_rPGA_2DPC_Rev0p61

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Close to VR

+1.05V_PCH R484 54.9/F_4

H_CPU_SVIDCLK R169 *0_4_S VR_SVID_CLK [41]

Place PU resistor close to CPU

+1.05V_PCH R158 130/F_4

SVID DATA

Close to VR

+1.05V_PCH R469 130/F_4

H_CPU_SVIDDAT R171 *0_4_S VR_SVID_DATA [41]

Place PU resistor close to CPU

+1.05V_PCH R157 75_4

SVID ALERT

H_CPU_SVIDALRT# R170 43_4 R156 *0_4_S VR_SVID_ALERT# [41]

+VDDR_REF_CPU

[12,13,37] SMDDR_VREF R566 *0_8

Q51 ME2N7002E

[34] MAINON_15V R563 100K_4

+1.5V_CPU +1.5V

R276 *0_8_S

40mile routing

+1.5V_SUS

5A

Q35 AON7406

[34] MAINON_15V

C288 *470P/50V/X7R_4

R277 220_8

[2,34] MAINON#

Q36 ME2N7002E

C293 0.1U/10V_4
C294 0.1U/10V_4
C291 0.1U/10V_4
C292 0.1U/10V_4

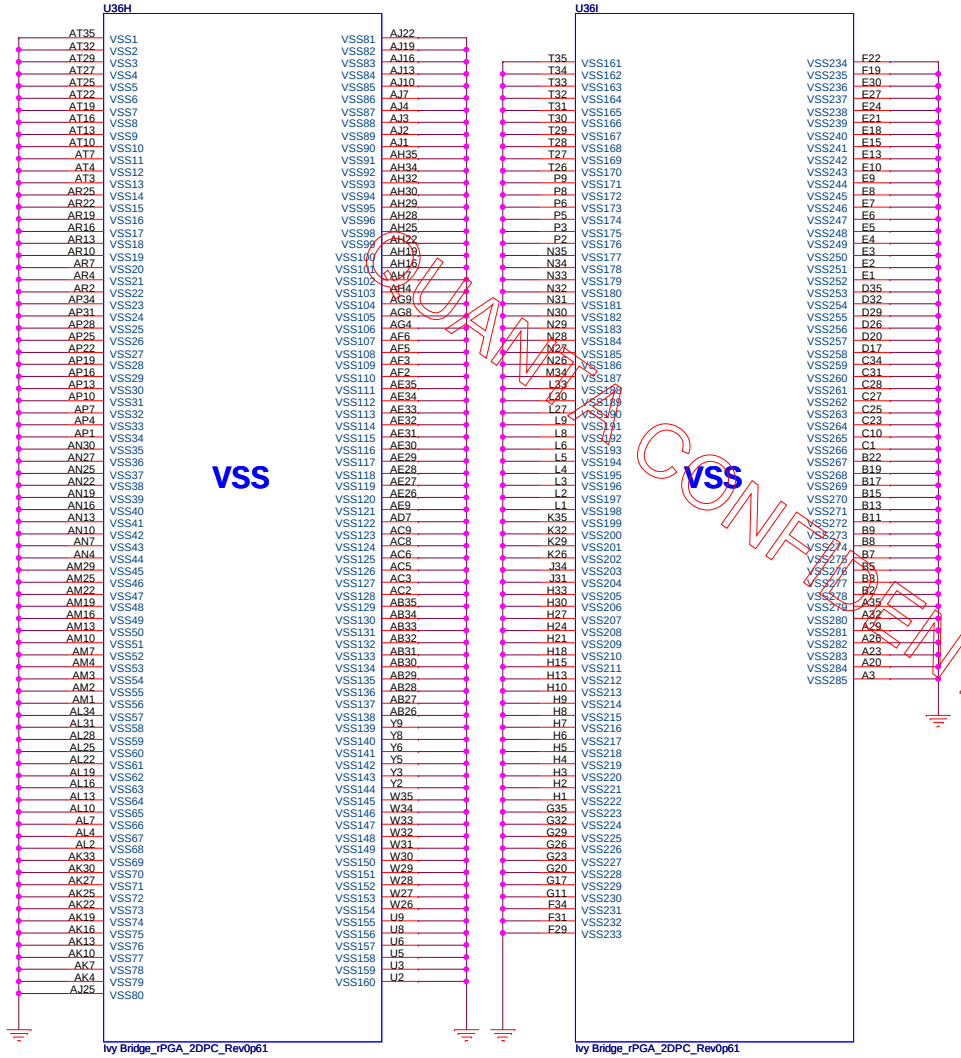
Placement close to CPU.

PROJECT : LZ2A
Quanta Computer Inc.

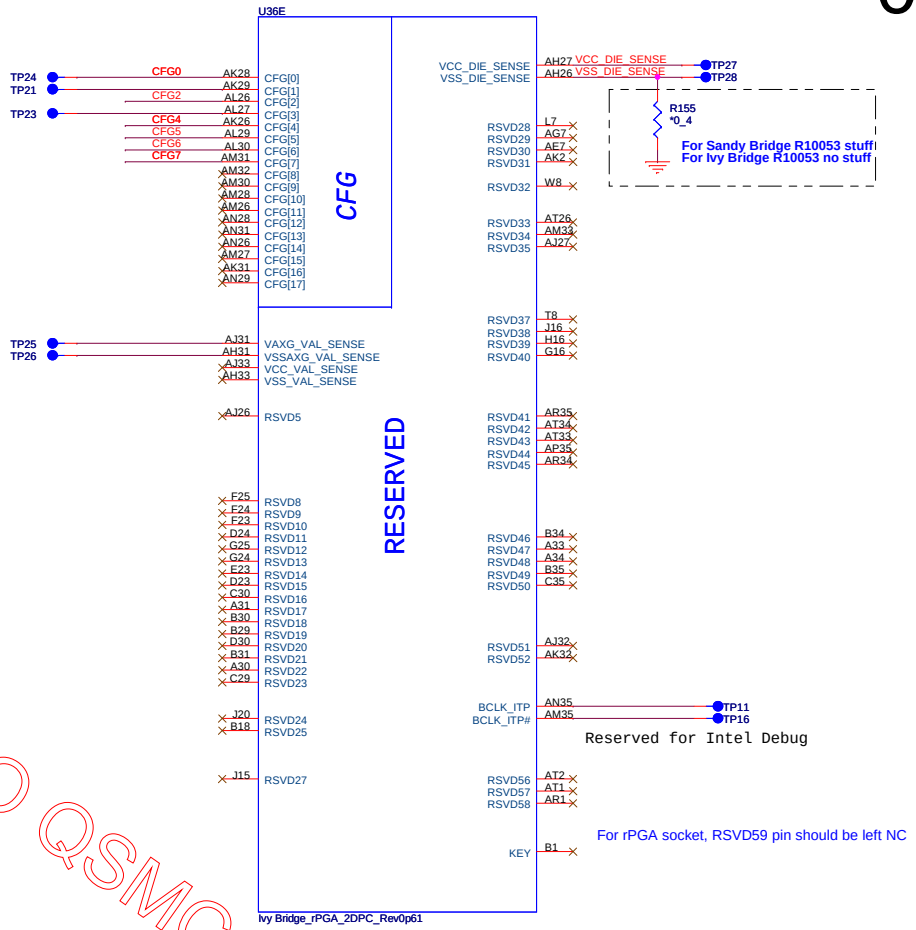
Size	Document Number	Rev
	IVY Bridge 3/4	1A

Date: Wednesday, December 07, 2011 Sheet 4 of 45

Ivy Bridge Processor (GND)



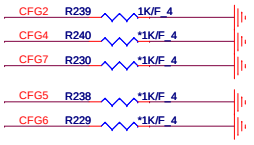
Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	IVY Bridge 4/4	1A

Date: Wednesday, December 07, 2011 Sheet 5 of 45

[2,4,7,8,10,33,34,38,43] +1.05V_PCH
[7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,7,8,9,10,27,31,34] +3V_S5
[7,10,32] +3V_RTC

Cougar Point/Panther Point (DMI,FDI,PM)

U13C

DMI
FDI
System Power Management

DMI0RXN BC24 ← [2] DMI_RXN0
DMI1RXN BE20 ← [2] DMI_RXN1
DMI2RXN BG18 ← [2] DMI_RXN2
DMI3RXN BG20 ← [2] DMI_RXN3
DMI0RXP BE24 ← [2] DMI_RXP0
DMI1RXP BC20 ← [2] DMI_RXP1
DMI2RXP BJ18 ← [2] DMI_RXP2
DMI3RXP BJ20 ← [2] DMI_RXP3
DMI0TXN AW24 → [2] DMI_TXN0
DMI1TXN AW20 → [2] DMI_TXN1
DMI2TXN BB18 → [2] DMI_TXN2
DMI3TXN AV18 → [2] DMI_TXN3
DMI0TXP AY24 → [2] DMI_TXP0
DMI1TXP AY20 → [2] DMI_TXP1
DMI2TXP AY18 → [2] DMI_TXP2
DMI3TXP AU18 → [2] DMI_TXP3
DMI_ZCOMP BJ24 — +1.05V_PCH — R543 49.9/F_4
DMI_IRCOMP BG25 — R260 750/F_4
DMI2RBIAS BH21 — DMI_RBIAS

FDI_RXN0 BJ14 ← FDI_TXN0 [2]
FDI_RXN1 AY14 ← FDI_TXN1 [2]
FDI_RXN2 BE14 ← FDI_TXN2 [2]
FDI_RXN3 BH13 ← FDI_TXN3 [2]
FDI_RXN4 BC12 ← FDI_TXN4 [2]
FDI_RXN5 BJ12 ← FDI_TXN5 [2]
FDI_RXN6 BG10 ← FDI_TXN6 [2]
FDI_RXN7 BG9 ← FDI_TXN7 [2]
FDI_TXP0 BG14 → FDI_TXP0 [2]
FDI_TXP1 BB14 → FDI_TXP1 [2]
FDI_TXP2 BF14 → FDI_TXP2 [2]
FDI_TXP3 BG13 → FDI_TXP3 [2]
FDI_TXP4 BE12 → FDI_TXP4 [2]
FDI_TXP5 BG12 → FDI_TXP5 [2]
FDI_TXP6 BJ10 → FDI_TXP6 [2]
FDI_TXP7 BH9 → FDI_TXP7 [2]
FDI_INT AW16 → FDI_INT [2]
FDI_FSYNC0 AV12 → FDI_FSYNC0 [2]
FDI_FSYNC1 BC10 → FDI_FSYNC1 [2]
FDI_LSYNC0 AV14 → FDI_LSYNC0 [2]
FDI_LSYNC1 BB10 → FDI_LSYNC1 [2]

FOR DEEP S3
[32] SUSACK# — SUSACK# R620 0_4 — C12 SUSACK#
SUSWARN#_R R436 *0_4 — K16 SUSWARN#/SUSPWRDNACK/GPIO30
[2] XDP_DBRST# — XDP_DBRST# — K3 SYS_RESET#
SYS_PWROK — C522 *1U/6.3V_4, R451 *0_4_S — SYS_PWROK_R — P12 SYS_PWROK
[32] EC_PWROK — R426 *0_4, R460 *0_4_S — EC_PWROK_R — L22 PWROK
EC_PWROK_R — R428 *0_4_S — APWROK_R — L10 APWROK
[2] PM_DRAM_PWRGD — PM_DRAM_PWRGD — B13 DRAMPWROK
[32] RSMRST# — RSMRST# — C21 RSMRST#
FOR DEEP S3
[32] SUSWARN# — R410 0_4 — SUSWARN#_R
[32] SIO_PWRBTN# — E20 PWRBTN#
[17,32] AC_PRESENT — R459 *0_4_S — AC_PRESENT_R — H20 ACPRESENT / GPIO31
PM_BATLOW# — E10 BATLOW# / GPIO72
PM_RI# — A10 RI#

+3V_S5
+3V_S5
+3V_S5
+3V_S5
+3V_S5
DSW

DSWVRMEN A18 ← DSWVREN
DPWROK E22 ← R615 *0_4 DPWROK, R124 0_4 RSMRST# ← RSMRST# [32]
WAKE# B9 ← PCIE_WAKE# [24,27,32]
CLKRUN# / GPIO32 N3 ↔ CLKRUN# [32]
SUS_STAT# / GPIO61 G8 → LPC_PD# → T18
SUSCLK / GPIO62 N14 → PCH_SUSCLK → T21
SLP_S5# / GPIO63 D10 → SLP_S5# → T17
SLP_S4# H4 → PM_SLP_S4# [32]
SLP_S3# F4 → SIO_SLP_S3# [32]
SLP_A# G10 → SLP_A# → T16
SLP_SUS# G16 → SLP_SUS# [10,32]
PMSYNCH AP14 → PM_SYNC [2]
SLP_LAN# / GPIO29 K14 ← WLAN_AOAC_ON [27]

FOR DEEP S3
FOR DEEP S3
FOR DEEP S3

CPT_PPT_Rev_0p5

Cougar Point/Panther Point (LVDS,DDI)

U13D

LVDS
CRT
Digital Display Interface

[23] INT_LVDS_BLON → J47 L_BKLTEN
[23] INT_LVDS_VDDEN → M45 L_VDD_EN
[23] PCH_BRIGHT_PWM → P45 L_BKLTCTL
[23] INT_EDIDCLK → T40 L_DDC_CLK
[23] INT_EDIDDAT → K47 L_DDC_DATA
+3V — R496 2.2K_4, R489 2.2K_4 → T45 L_CTRL_CLK, P39 L_CTRL_DATA
R511 2.37K/F_4 — LVD_IBG — T22 — AF37 LVD_IBG, AF36 LVD_VBG
AE48 LVD_VREFH
AE47 LVD_VREFL

[23] INT_TXLCLKOUTN → AK39 LVDSA_CLK#
[23] INT_TXLCLKOUTP → AK40 LVDSA_CLK
[23] INT_TXLOUTN0 → AN48 LVDSA_DATA#0
[23] INT_TXLOUTN1 → AM47 LVDSA_DATA#1
[23] INT_TXLOUTN2 → AK47 LVDSA_DATA#2
AJ48 LVDSA_DATA#3
[23] INT_TXLOUTP0 → AN47 LVDSA_DATA0
[23] INT_TXLOUTP1 → AM49 LVDSA_DATA1
[23] INT_TXLOUTP2 → AK49 LVDSA_DATA2
AJ47 LVDSA_DATA3
AE40 LVDSB_CLK#
AE39 LVDSB_CLK
AH45 LVDSB_DATA#0
AH47 LVDSB_DATA#1
AF49 LVDSB_DATA#2
AF45 LVDSB_DATA#3
AH43 LVDSB_DATA0
AH49 LVDSB_DATA1
AF47 LVDSB_DATA2
AF43 LVDSB_DATA3

R place close to PCH
R183 150/F_4 — INT_CRT_BLU
R193 150/F_4 — INT_CRT_GRE
R192 150/F_4 — INT_CRT_RED

[22] INT_CRT_BLU → N48 CRT_BLUE
[22] INT_CRT_GRE → P49 CRT_GREEN
[22] INT_CRT_RED → T49 CRT_RED
[22] INT_DDCCLK → T39 CRT_DDC_CLK
[22] INT_DDCDAT → M40 CRT_DDC_DATA
[22] INT_CRT_HSYNC — R176 33_4 — INT_CRT_HSYNC_R → M47 CRT_HSYNC
[22] INT_CRT_VSYNC — R182 33_4 — INT_CRT_VSYNC_R → M49 CRT_VSYNC
DAC_IREF → T43 DAC_IREF
R506 1K/F_4 — T42 CRT_IRTN

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 ↔ INT_HDMI_SCL [21]
SDVO_CTRLDATA M39 ↔ INT_HDMI_SDA [21]
DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 ← INT_HDMI_HPD_Q
DDPB_0N AV42 → INT_HDMI_TXDN2 [21]
DDPB_0P AV40 → INT_HDMI_TXDP2 [21]
DDPB_1N AV45 → INT_HDMI_TXDN1 [21]
DDPB_1P AV46 → INT_HDMI_TXDP1 [21]
DDPB_2N AU48 → INT_HDMI_TXDN0 [21]
DDPB_2P AU47 → INT_HDMI_TXDP0 [21]
DDPB_3N AV47 → INT_HDMI_TXCN [21]
DDPB_3P AV49 → INT_HDMI_TXCP [21]
DDPC_CTRLCLK P46
DDPC_CTRLDATA P42
DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT38 ← DDPC_HPD_PU R548 10K_4 ← +3V
DDPC_0N AV47 → Follow PDG eDP disable guide
DDPC_0P AV49
DDPC_1N AV43
DDPC_1P AV45
DDPC_2N BA47
DDPC_2P BA48
DDPC_3N BB47
DDPC_3P BB49
DDPD_CTRLCLK M43
DDPD_CTRLDATA M36
DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH41 ← DDPD_HPD_PU R547 10K_4 ← +3V
DDPD_0N BB43 → Follow PDG eDP disable guide
DDPD_0P BB45
DDPD_1N BF44
DDPD_1P BE44
DDPD_2N BF42
DDPD_2P BE42
DDPD_3N BJ42
DDPD_3P BG42

INT. HDMI
INT. DP

CPT_PPT_Rev_0p5

INT_HDMI_HPD_Q — R535 *0_4_S — INT_HDMI_HPD [21]
R523 *100K_4
R540 100K_4

DPWROK FOR DSW (DEEP S3)

FOR DEEP S3
+3V_DSW, +3VPCU, +3VPCU
+3V_S5 — D28 *RB500V-40 — R616 *10K_4
+3VPCU — D29 *RB500V-40 — R617 *10K_4
Q55 *LTC044EUBFS8TL
Q56 *2N7002
DPWROK — C665 *0.1U/10V/X5R_4 add cap to timing tune

System PWR_OK(CLG)

+3V_S5
U7 TC7SH08FU
C171 0.1U/10V_4
[2] SYS_PWROK → SYS_PWROK
DELAY_VR_PWRGOOD [41]
EC_PWROK
R117 *0_4
R112 100K_4

+3V_RTC
R127 330K_4
DSWVREN
R140 *330K_4

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

PCH Pull-high/low(CLG)

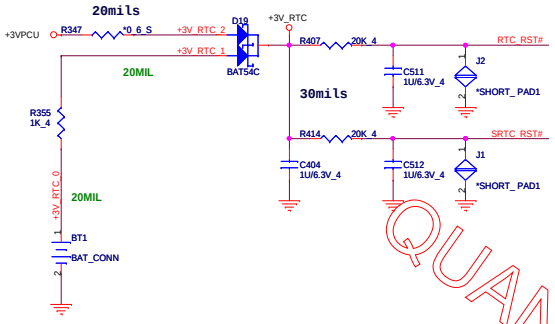
+3V, +3V_S5
CLKRUN# R198 8.2K_4
XDP_DBRST# R180 1K_4
R173 *1K_4
RSMRST# R139 10K_4
SYS_PWROK R457 100K_4
PM_RI# R142 10K_4
PM_BATLOW# R445 8.2K_4
PCIE_WAKE# R146 10K_4
WLAN_AOAC_ON R418 10K_4
SUSWARN# R409 10K_4
AC_PRESENT R442 10K_4
PM_DRAM_PWRGD R435 *200/F_4
For AOAC

PROJECT : LZ2A
Quanta Computer Inc.

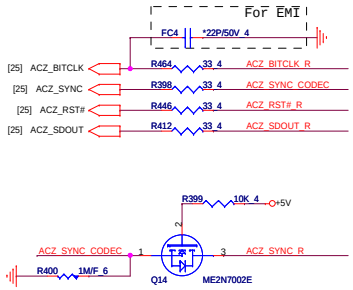
Size	Document Number	Rev
	Panther Point 1/6	1A

Date: Wednesday, December 07, 2011 Sheet 6 of 45

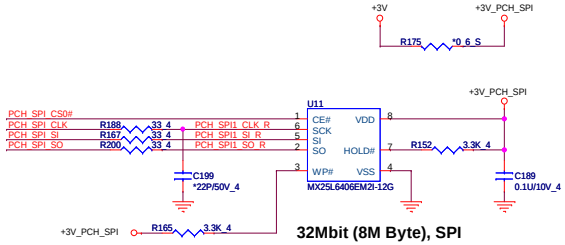
RTC Circuitry(RTC)



HDA Bus(CLG)

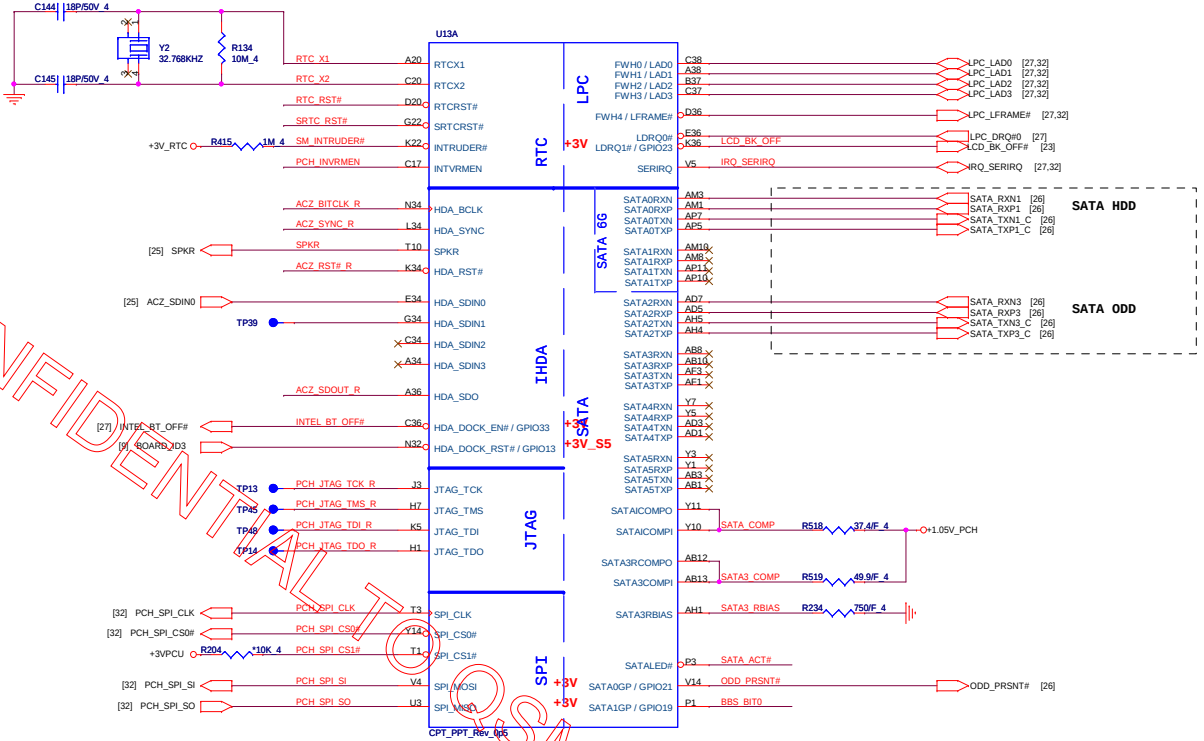


PCH Dual SPI (CLG)



32Mbit (8M Byte), SPI

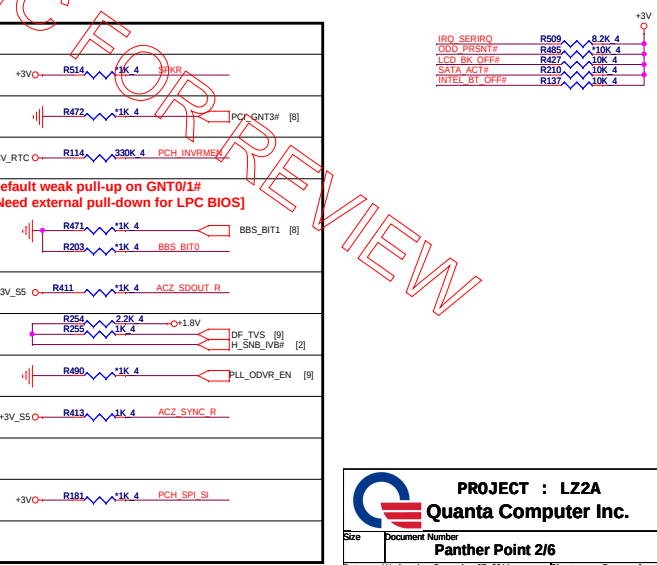
Cougar Point/Panther Point (HDA,JTAG,SATA)



PCH Strap Table

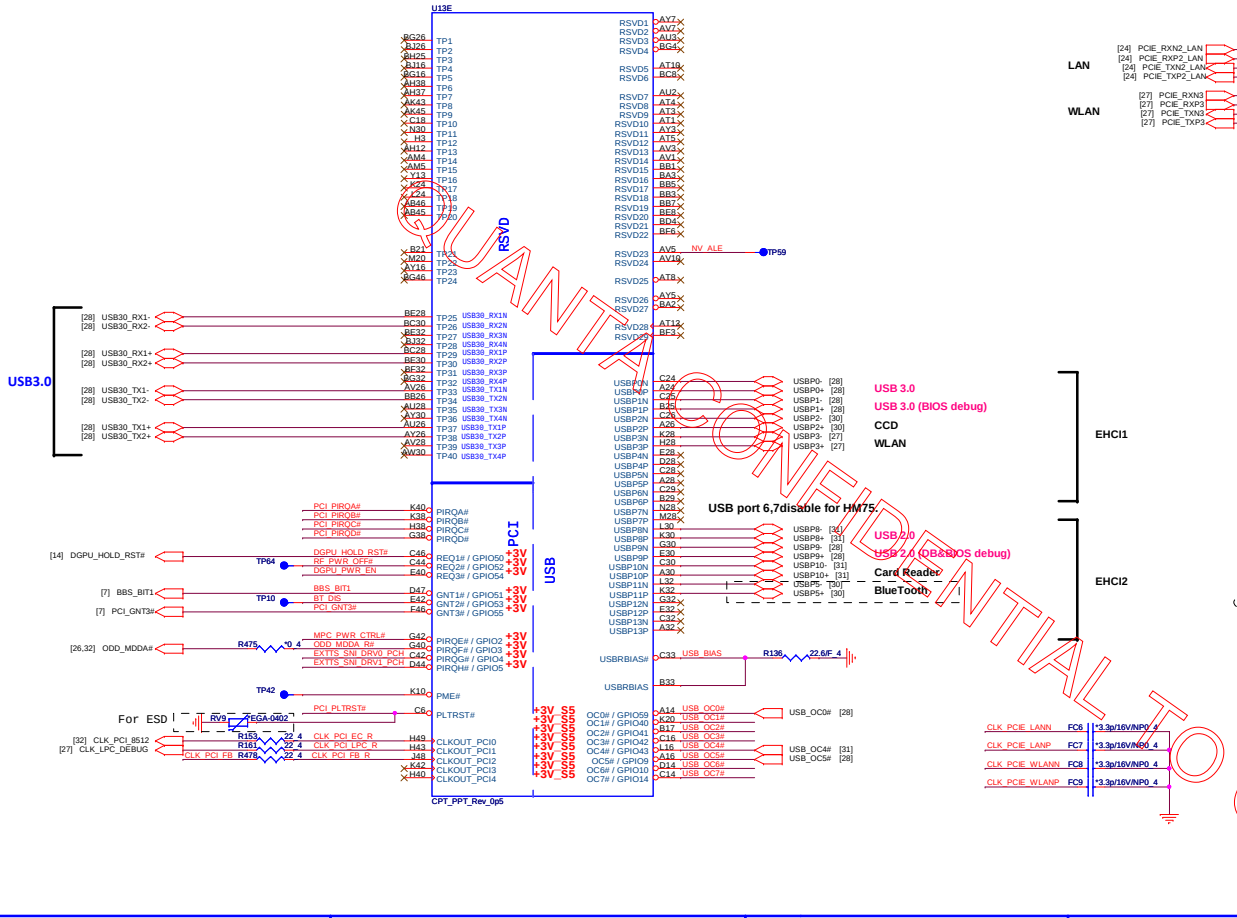
Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)

GNT1#	GNT0#	Boot Location
1	1	SPI *
0	0	LPC

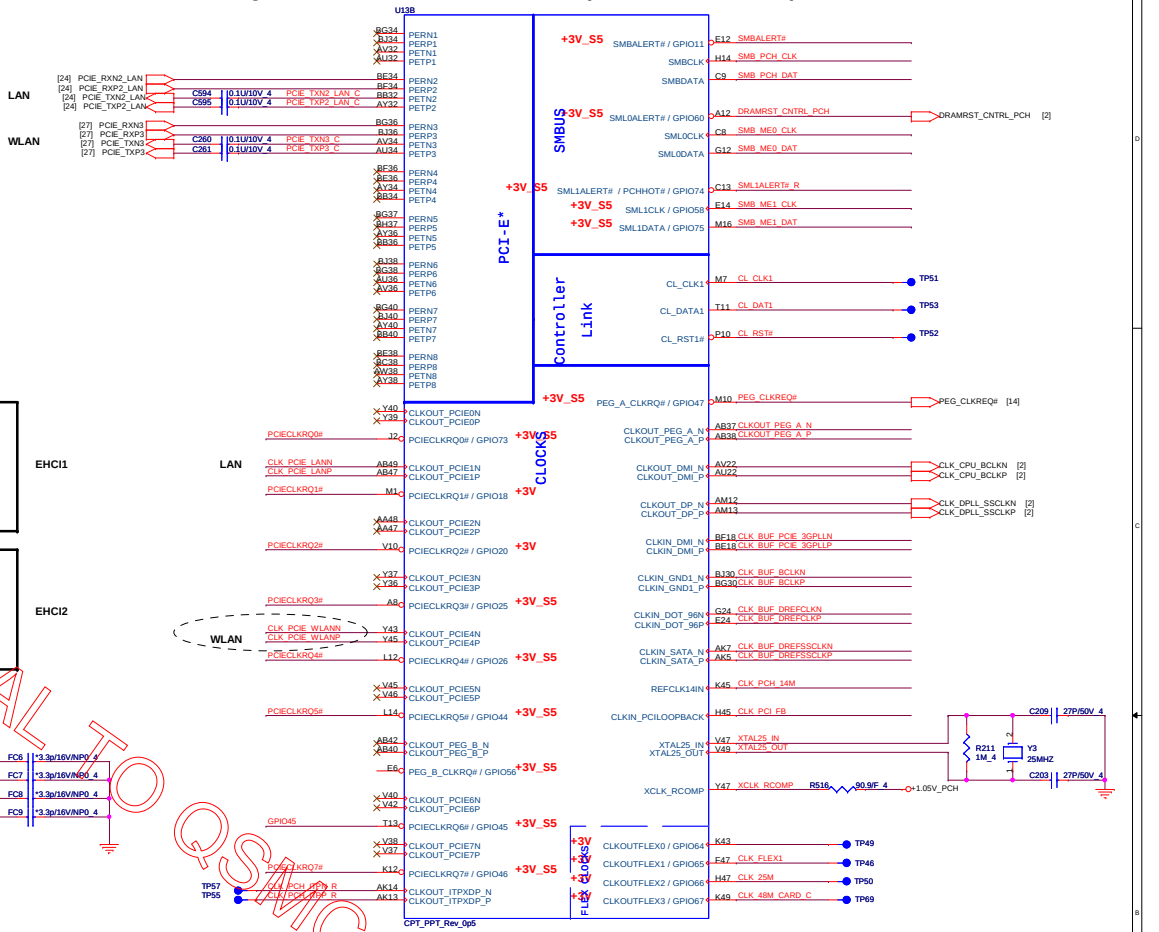


PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Document Number: Panther Point 2/6	Rev: 1A
Date: Wednesday, December 07, 2011	Sheet 7 of 45	

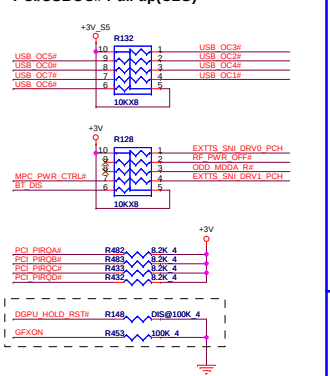
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



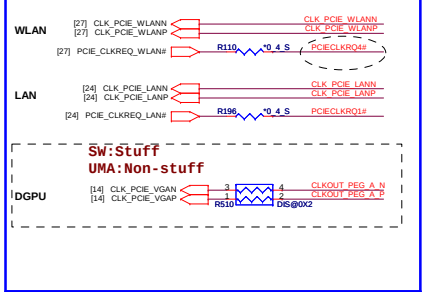
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



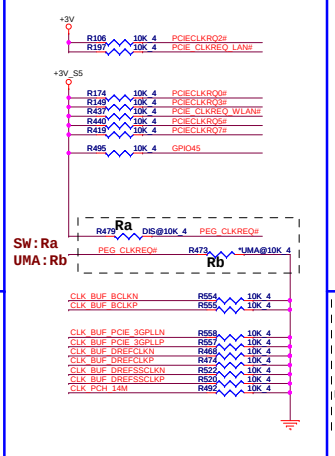
PCI/USBOC# Pull-up(CLG)



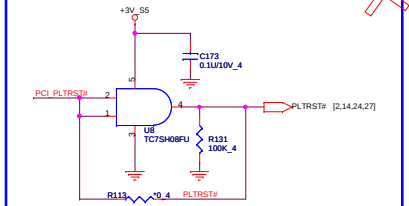
PCIE CLOCK



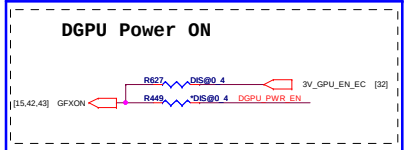
CLK_REQ/Strap Pin(CLG)



PLTRST#(CLG)



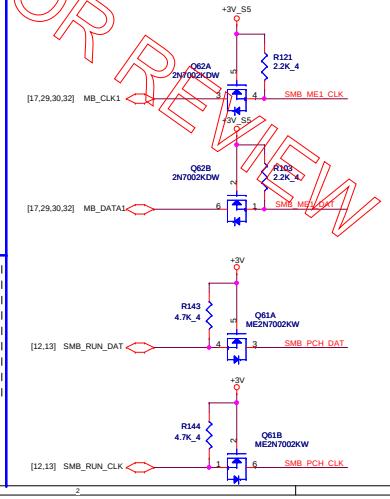
DGPU Power ON



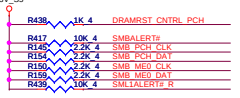
MPC Switch Control

MPC_PWR_CTRL#	LOw = MPC ON High = MPC OFF (Default)

SMBus(CLK)



SMBus/Pull-up(CLG)



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Panther Point 3/6	1A

Date: Wednesday, December 07, 2011 Sheet 8 of 45

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

[2,6,7,8,10,27,31,34] +3V_S5
[6,7,8,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V

09

U13F

S_GPIO R507 100_4 T7 BMBUSY# / GPIO0 +3V
[32] EC_EXT_SMI# A42 TACH1 / GPIO1 +3V
BOARD_ID1 H36 TACH2 / GPIO6 +3V
[32] EC_EXT_SCI# E38 TACH3 / GPIO7 +3V
TP8 ICC_EN# C10 GPIO8 +3V_S5
[27] LAN_DISABLE# C4 LAN_PHY_PWR_CTRL / GPIO12 +3V_S5
HOST_ALERT#1_R G2 GPIO15 +3V_S5
BOARD_ID2 U2 SATA4GP / GPIO16 +3V
[14,43] GFXPG R100 *0_4_S GFXPG_R D40 TACH0 / GPIO17 +3V
BIOS_REC T5 SCLOCK / GPIO22 +3V
SYSTEM_ID1 E8 GPIO24 / MEM_LED +3V_S5
GPIO27 E16 GPIO27 DSW
[7] PLL_ODVR_EN R494 *0_4_S PLL_ODVR_EN_R P6 GPIO28 +3V_S5
SYSTEM_ID0 K1 STP_PCI# / GPIO34 +3V
[30] BT_ON# BT_ON# K4 GPIO35 +3V
[30] CCD_ON# CCD_ON# V8 SATA2GP / GPIO36 +3V
FDI_OVRVLTG M5 SATA3GP / GPIO37 +3V
MFG_MODE N2 SLOAD / GPIO38 +3V
DGPU_PRSNT# M3 SDATAOUT0 / GPIO39 +3V
TEST_SET_UP V13 SDATAOUT1 / GPIO48 +3V
[29,32] TEMP_ALERT# V3 SATA5GP / GPIO49 +3V
SV_DET D6 GPIO57 +3V_S5

GPIO

TACH4 / GPIO68 C40 FB_CLAMP_PCH
TACH5 / GPIO69 B41 R122 1.5K/F_4
TACH6 / GPIO70 C41 GPU_EVENT_PCH#
TACH7 / GPIO71 A40 PCB_LAYER_ID

R25 10K/F_4
R118 *GS@0_4 FB_CLAMP [15]
R462 *GS@0_4 GPU_EVENT# [17]
R634 10K/F_4@GS@NC +3V

NVidia N13P-GS
NVidia N13P-GS

CPU/MISC

A20GATE P4 EC_A20GATE [32]
PECI AU16 TP58
RCIN# P5 EC_RCIN# [32]
PROCPWRGD AY11 H_PWRGOOD [2]
THRMTRIP# AY10 PCH_THRMTRIP# R539 390_4 PM_THRMTRIP# [2]
INIT3_3V# T14
DF_TVS AY1 DF_TVS [7]

TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37

NCTF

VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BF1
VSS_NCTF_14 BF49
VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
VSS_NCTF_21 BJ45
VSS_NCTF_22 BJ46
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49

CPT_PPT_Rev_0p5

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			

Board ID use below GPIO:
BOARD_ID1
BOARD_ID2
BOARD_ID3

PCB_LAYER_ID:
0-->6 layer
1-->8 layer

System ID[0],ID[1]:
-->LZ1 [0,0]
-->LZ2 [0,1]
-->LZ3 [1,0]

+3V
R209 *10K_4 BOARD_ID2 R213 10K_4
R429 10K_4 BOARD_ID1 R430 *10K_4
R129 *10K_4 PCB_LAYER_ID R138 10K_4
R187 10K_4 SYSTEM_ID0 R179 *10K_4
+3V_S5
R476 *10K_4 SYSTEM_ID1 R467 10K_4
R503 10K_4 BOARD_ID3 R443 *10K_4
BOARD_ID3 [7]

GPIO Pull-up/Pull-down(CLG)

+3V_S5
LAN_DISABLE# R162 10K_4
+3V
EC_EXT_SMI# R130 10K_4
EC_EXT_SCI# R431 10K_4
EC_A20GATE R498 10K_4
EC_RCIN# R500 10K_4
TEMP_ALERT# R223 10K_4
BT_ON# R481 10K_4
GPIO27 R441 10K_4

SATA2GP/GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.

+3V
CCD_ON# R515 *200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V
R491 100K_4 FDI_OVRVLTG R486 *1K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

SGPIO

+3V
S_GPIO R508 10K_4
R505 *0_4

+3V
BIOS_REC R499 10K_4
R501 *0_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP
High = Strong (Default)

+3V
TEST_SET_UP R194 10K_4
R185 *0_4

+3V_S5
R456 *10K_4 SV_DET R458 100K_4

+3V_S5
HOST_ALERT#1_R R466 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

MFG-TEST

+3V
MFG_MODE R199 10K_4
R202 *0_4

	SWITCHABLE	UMA
Stuff	R186	R195
No Stuff	R195	R186

+3V
R195 *UMA@10K_4 DGPU_PRSNT# R186 DIS@100K_4

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Panther Point 4/6	1A

Date: Wednesday, December 07, 2011 Sheet 9 of 45

Cougar Point/Panther Point (POWER)

[2,4,6,7,8,33,34,38,43] +1.05V_PCH
[6,7,8,9,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[6,7,32] +3V_RTC
[2,6,7,8,9,27,31,34] +3V_S5
[23,26,28,31,33,34] +5V_S5
[7,21,22,25,26,29,30,33,34] +5V

Cougar Point/Panther Point (POWER)

U13G — POWER

VccCORE =1.3 A(60mils)
VccIO =2.925 A(140mils)
VccADAC =1mA(8mils)
VccALVDS=1mA(8mils)
VccTX_LVDS=60mA(10mils)
VCCDMI = 42mA(10mils)
VCCCLKDMI = 20mA(8mils)
VCCPNAND = 190 mA(25mils)
VCCSPI = 20mA(8mils)
VCCVRM: 1.8V (Destop) 1.5V (Mobile)
160mA (15mils)

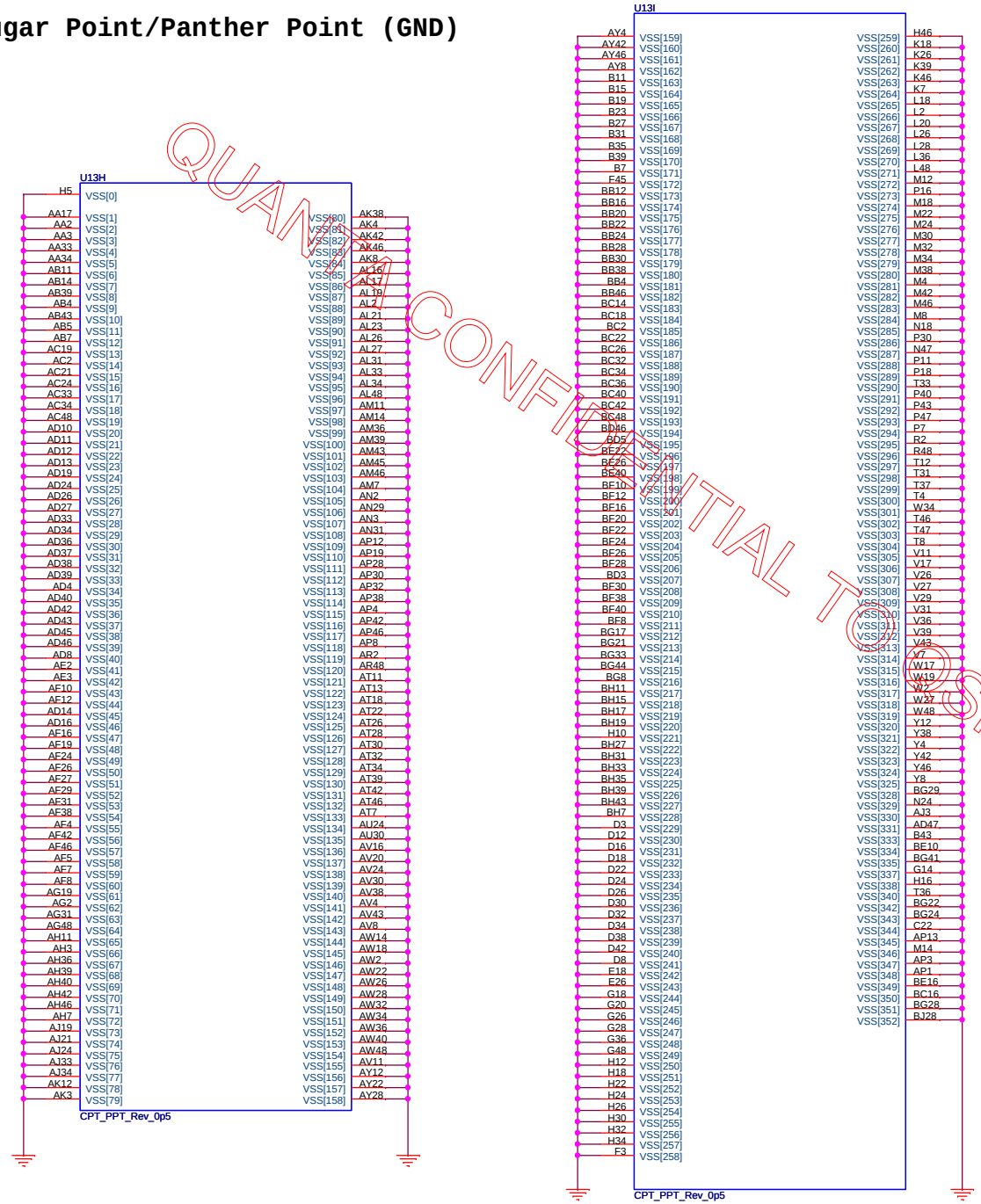
U13J — POWER

FOR DEEP S3
VCCDSW3_3= 3mA
VccASW =1.01 A(60mils)
65mA(10mils)
8mA(8mils)
VCCDIFFCLKN= 55mA(10mils)
VCCSSC= 95mA(10mils)
VCCRTC=1mA(8mils)
VCCSUS3_3 = 119mA(15mils)
VCCSUS3_3 = 119mA(15mils)
VCCPCORE = 28mA(10mils)
VCCVRM= 114mA(15mils)
VCCME = 1.01A(60mils)
VCCSUSHDA= 10mA(8mils)
VCCSREFSUS=1mA
V5REF= 1mA

FOR DEEP S3

PROJECT : LZ2A
Quanta Computer Inc.
Size | Document Number: Panther Point 5/6 | Rev: 1A
Date: Wednesday, December 07, 2011 | Sheet 10 of 45

Cougar Point/Panther Point (GND)



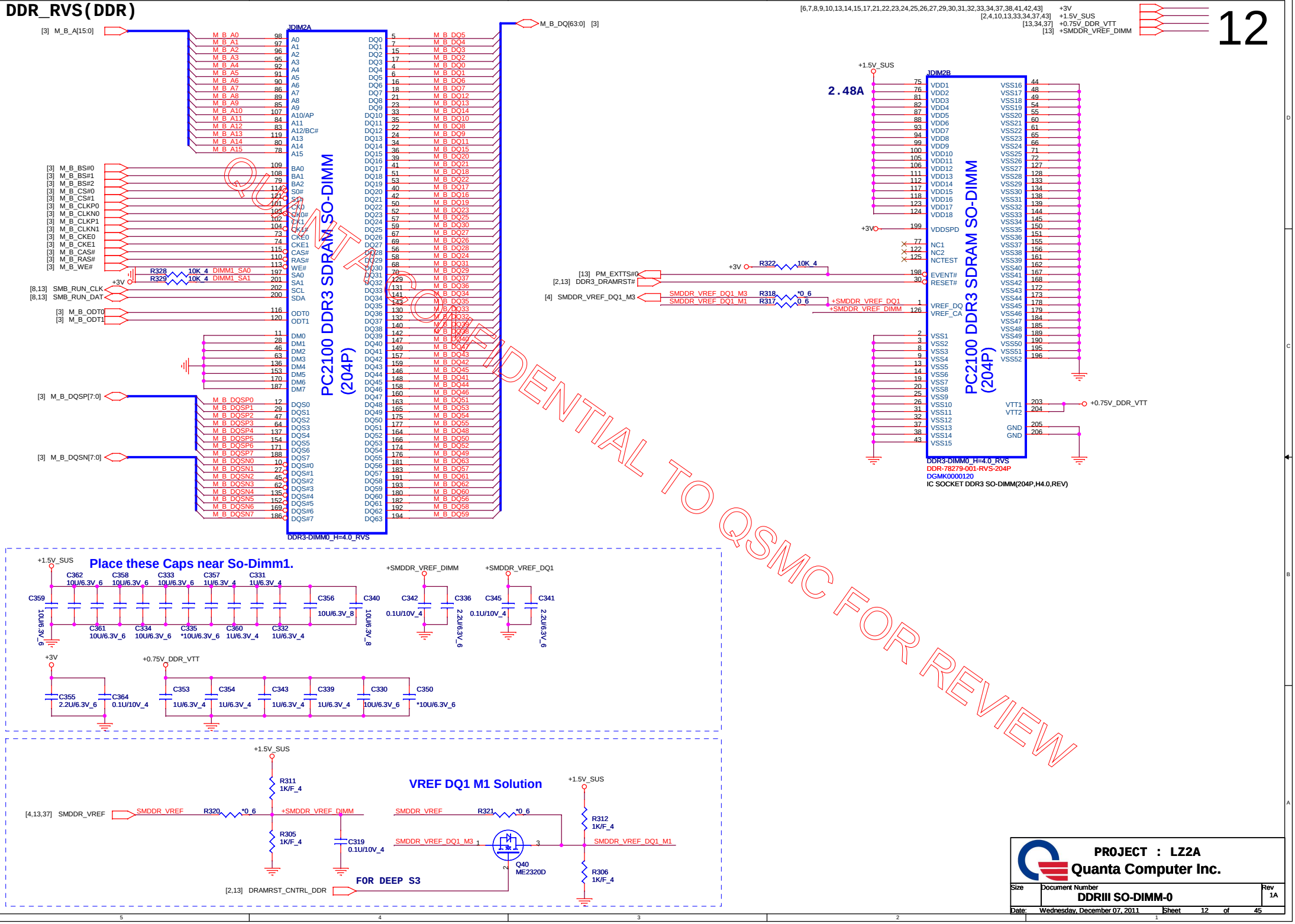
PROJECT : LZ2A

Quanta Computer Inc.

Size	Document Number	Rev
	Panther Point 6/6	1A

Date: Wednesday, December 07, 2011 Sheet 11 of 45

DDR_RVS(DDR)



DDR_RVS(DDR)

[6,7,8,9,10,12,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,4,10,12,33,34,37,43] +1.5V_SUS
[12,34,37] +0.75V_DDR_VTT
[12] +SMDDR_VREF_DIMM

JDIM1A — PC2100 DDR3 SDRAM SO-DIMM (204P)

[3] M_A_A[15:0]
M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

[3] M_A_BS#0 109 BA0
[3] M_A_BS#1 108 BA1
[3] M_A_BS#2 79 BA2
[3] M_A_CS#0 114 S0#
[3] M_A_CS#1 121 S1#
[3] M_A_CLKP0 101 CK0
[3] M_A_CLKN0 103 CK0#
[3] M_A_CLKP1 102 CK1
[3] M_A_CLKN1 104 CK1#
[3] M_A_CKE0 73 CKE0
[3] M_A_CKE1 74 CKE1
[3] M_A_CAS# 115 CAS#
[3] M_A_RAS# 110 RAS#
[3] M_A_WE# 113 WE#

R308 10K_4 DIMM0_SA0
R307 10K_4 DIMM0_SA1
[8,12] SMB_RUN_CLK 197 SA0
[8,12] SMB_RUN_DAT 201 SA1
202 SCL
200 SDA

[3] M_A_ODT0 116 ODT0
[3] M_A_ODT1 120 ODT1

11 DM0
28 DM1
46 DM2
63 DM3
136 DM4
153 DM5
170 DM6
187 DM7

[3] M_A_DQSP[7:0]
M_A_DQSP0 12 DQS0
M_A_DQSP1 29 DQS1
M_A_DQSP2 47 DQS2
M_A_DQSP3 64 DQS3
M_A_DQSP4 137 DQS4
M_A_DQSP5 154 DQS5
M_A_DQSP6 171 DQS6
M_A_DQSP7 188 DQS7

[3] M_A_DQSN[7:0]
M_A_DQSN0 10 DQS#0
M_A_DQSN1 27 DQS#1
M_A_DQSN2 45 DQS#2
M_A_DQSN3 62 DQS#3
M_A_DQSN4 135 DQS#4
M_A_DQSN5 152 DQS#5
M_A_DQSN6 169 DQS#6
M_A_DQSN7 186 DQS#7

DQ0 5 M_A_DQ4
DQ1 7 M_A_DQ5
DQ2 15 M_A_DQ6
DQ3 17 M_A_DQ7
DQ4 4 M_A_DQ0
DQ5 6 M_A_DQ1
DQ6 16 M_A_DQ3
DQ7 18 M_A_DQ2
DQ8 21 M_A_DQ13
DQ9 23 M_A_DQ9
DQ10 33 M_A_DQ15
DQ11 35 M_A_DQ14
DQ12 22 M_A_DQ12
DQ13 24 M_A_DQ8
DQ14 34 M_A_DQ10
DQ15 36 M_A_DQ11
DQ16 39 M_A_DQ22
DQ17 41 M_A_DQ19
DQ18 51 M_A_DQ16
DQ19 53 M_A_DQ21
DQ20 40 M_A_DQ18
DQ21 42 M_A_DQ23
DQ22 50 M_A_DQ17
DQ23 52 M_A_DQ20
DQ24 57 M_A_DQ31
DQ25 59 M_A_DQ27
DQ26 67 M_A_DQ30
DQ27 69 M_A_DQ29
DQ28 56 M_A_DQ24
DQ29 58 M_A_DQ26
DQ30 68 M_A_DQ25
DQ31 70 M_A_DQ28
DQ32 129 M_A_DQ37
DQ33 131 M_A_DQ33
DQ34 141 M_A_DQ38
DQ35 143 M_A_DQ34
DQ36 130 M_A_DQ32
DQ37 132 M_A_DQ36
DQ38 140 M_A_DQ35
DQ39 142 M_A_DQ39
DQ40 147 M_A_DQ44
DQ41 149 M_A_DQ47
DQ42 157 M_A_DQ46
DQ43 159 M_A_DQ45
DQ44 146 M_A_DQ41
DQ45 148 M_A_DQ40
DQ46 158 M_A_DQ42
DQ47 160 M_A_DQ43
DQ48 163 M_A_DQ54
DQ49 165 M_A_DQ55
DQ50 175 M_A_DQ51
DQ51 177 M_A_DQ50
DQ52 164 M_A_DQ48
DQ53 166 M_A_DQ49
DQ54 174 M_A_DQ53
DQ55 176 M_A_DQ52
DQ56 181 M_A_DQ61
DQ57 183 M_A_DQ58
DQ58 191 M_A_DQ57
DQ59 193 M_A_DQ63
DQ60 180 M_A_DQ56
DQ61 182 M_A_DQ60
DQ62 192 M_A_DQ59
DQ63 194 M_A_DQ62

DDR3-DIMM1_H=8.0_RVS

M_A_DQ[63:0] [3]

JDIM1B — PC2100 DDR3 SDRAM SO-DIMM (204P)

2.48A
+1.5V_SUS
VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V 199 VDDSPD

NC1 77
NC2 122
NCTEST 125

+3V R286 10K_4
[12] PM_EXTTS#0 198 EVENT#
[2,12] DDR3_DRAMRST# 30 RESET#

SMDDR_VREF_DQ0_M1 R303 0_6 +SMDDR_VREF_DQ0
SMDDR_VREF_DQ0_M3 R314 *0_6 +SMDDR_VREF_DIMM
[4] SMDDR_VREF_DQ0_M3 1 VREF_DQ
126 VREF_CA

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203 +0.75V_DDR_VTT
VTT2 204

GND 205
GND 206

DDR3-DIMM1_H=8.0_RVS

Place these Caps near So-Dimm0.

+1.5V_SUS
C303 10U/6.3V_6
C324 10U/6.3V_6
C306 10U/6.3V_6
C301 1U/6.3V_4
C326 1U/6.3V_4
C300 10U/6.3V_6
C307 10U/6.3V_6
C325 10U/6.3V_6
C322 *10U/6.3V_6
C305 1U/6.3V_4
C327 1U/6.3V_4
C296 *330U/2V/ESR9_7343
C297 10U/6.3V_8
C323 10U/6.3V_8

+SMDDR_VREF_DIMM
+SMDDR_VREF_DQ0
C299 0.1U/10V_4
C304 2.2U/6.3V_6
C317 0.1U/10V_4
C318 2.2U/6.3V_6

+3V
C316 2.2U/6.3V_6
C321 0.1U/10V_4

+0.75V_DDR_VTT
C298 1U/6.3V_4
C302 1U/6.3V_4
C328 1U/6.3V_4
C320 1U/6.3V_4
C308 10U/6.3V_6
C311 *10U/6.3V_6

VREF DQ0 M3 Solution

+1.5V_SUS
R325 1K/F_4
[4,12,37] SMDDR_VREF
R323 *0_6
SMDDR_VREF_DQ0_M1
R324 1K/F_4
SMDDR_VREF_DQ0_M3 1
3
Q41 ME2320D
FOR DEEP S3
[2,12] DRAMRST_CNTRL_DDR

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

Date: Wednesday, December 07, 2011 Sheet 13 of 45

[15,16,33,43] +1.05V_GFX_PCIE
[16,17,18,43] +3V_GPU
[15,19,20,33,43] +1.5V_GPU
[6,7,8,9,10,12,13,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[18,33,42] GFX_CORE

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >3.45A

U30A

N13P-GS

To be placed no further from the GPU than bewteen the PS and GPU

PLACE UNDER BGA

PLACE NEAR BALLS

+1.05V_GFX_PCIE

C94 C149 C108 C150 C105 C116 C117

DIS@22U/6.3V_8 DIS@22U/6.3V_8 DIS@10U/6.3V_8 DIS@10U/6.3V_8 DIS@4.7U/6.3V_6 DIS@1U/6.3V_4 DIS@1U/6.3V_4

AG19 AG21 AG22 AG24 AH21 AH25 PEX_IOVDD

C106 C130 C107 C138 C104 C120 C123

DIS@22U/6.3V_8 DIS@22U/6.3V_8 DIS@10U/6.3V_8 DIS@10U/6.3V_8 DIS@4.7U/6.3V_6 DIS@1U/6.3V_4 DIS@1U/6.3V_4

AG13 AG15 AG16 AG18 AG25 AH15 AH18 AH26 AH27 AJ27 AK27 AL27 AM28 AN28 PEX_IOVDDQ

CAP CLOSE TO BGA

12~16 mils width 210mA

+3V_GPU PLACE NEAR BGA

+PEX_SVDD_3V3 R86 *GS@0_4 AH12 PEX_PLL_HVDD

C467 DIS@0.1U/10V_4
C77 DIS@4.7U/6.3V_6
C118 DIS@4.7U/6.3V_6

AG12 PEX_SVDD_3V3

0ohm (R86)	
N13P-GS (GK107)	Stuff
N13P-GL (GF108) N13M-GE1 (GF119)	unstuff

1/19 PCI_EXPRESS

[42] GPU_VCCSENSE L4 VDD_SENSE

[42] GPU_VSSSENSE L5 GND_SENSE

16 mils width for 110mA

P8 3V3AUX_NC

R90 *DIS@200/F_4 PEX_TSTCLK AJ26 PEX_TSTCLK_OUT
PEX_TSTCLK# AK26 PEX_TSTCLK_OUT*

150mA

+1.05V_GFX_PCIE L5 DIS@0_6 PLACE UNDER GPU

C112 DIS@0.1U/10V_4

C127 DIS@1U/6.3V_4

C129 DIS@1U/6.3V_4
C136 DIS@4.7U/6.3V_6

PLACE NEAR BGA

+PEX_PLLVDD AG26 PEX_PLLVDD

TESTMODE AK11 TESTMODE

R94 DIS@10K_4

PEX_TERMP AP29 PEX_TERMP

R98 DIS@2.49K/F_4

bga908-nvidia-n13p-gs-a1

N13P-GS

PEX_WAKE AJ11

PEX_RST AJ12 GPU_RST#

PEX_CLKREQ AK12 R405 DIS@10K_4 +3V_GPU
PEX_CLKREQ#

PEX_REFCLK AL13 CLK_PCIE_VGAP [8]
PEX_REFCLK# AK13 CLK_PCIE_VGAN [8]

PEX_TX15	AK14	PEG_RXP15_C	C143	DIS@0.1U/10V_4	PEG_RXP15 [2]
PEX_TX15#	AJ14	PEG_RXN15_C	C141	DIS@0.1U/10V_4	PEG_RXN15 [2]
PEX_RX15	AN12				PEG_TXP15 [2]
PEX_RX15#	AM12				PEG_TXN15 [2]
PEX_TX14	AH14	PEG_RXP14_C	C195	DIS@0.1U/10V_4	PEG_RXP14 [2]
PEX_TX14#	AG14	PEG_RXN14_C	C196	DIS@0.1U/10V_4	PEG_RXN14 [2]
PEX_RX14	AN14				PEG_TXP14 [2]
PEX_RX14#	AM14				PEG_TXN14 [2]
PEX_TX13	AK15	PEG_RXP13_C	C166	DIS@0.1U/10V_4	PEG_RXP13 [2]
PEX_TX13#	AJ15	PEG_RXN13_C	C167	DIS@0.1U/10V_4	PEG_RXN13 [2]
PEX_RX13	AP14				PEG_TXP13 [2]
PEX_RX13#	AP15				PEG_TXN13 [2]
PEX_TX12	AL16	PEG_RXP12_C	C186	DIS@0.1U/10V_4	PEG_RXP12 [2]
PEX_TX12#	AK16	PEG_RXN12_C	C187	DIS@0.1U/10V_4	PEG_RXN12 [2]
PEX_RX12	AN15				PEG_TXP12 [2]
PEX_RX12#	AM15				PEG_TXN12 [2]
PEX_TX11	AK17	PEG_RXP11_C	C152	DIS@0.1U/10V_4	PEG_RXP11 [2]
PEX_TX11#	AJ17	PEG_RXN11_C	C153	DIS@0.1U/10V_4	PEG_RXN11 [2]
PEX_RX11	AN17				PEG_TXP11 [2]
PEX_RX11#	AM17				PEG_TXN11 [2]
PEX_TX10	AH17	PEG_RXP10_C	C164	DIS@0.1U/10V_4	PEG_RXP10 [2]
PEX_TX10#	AG17	PEG_RXN10_C	C165	DIS@0.1U/10V_4	PEG_RXN10 [2]
PEX_RX10	AP17				PEG_TXP10 [2]
PEX_RX10#	AP18				PEG_TXN10 [2]
PEX_TX9	AK18	PEG_RXP9_C	C184	DIS@0.1U/10V_4	PEG_RXP9 [2]
PEX_TX9#	AJ18	PEG_RXN9_C	C185	DIS@0.1U/10V_4	PEG_RXN9 [2]
PEX_RX9	AN18				PEG_TXP9 [2]
PEX_RX9#	AM18				PEG_TXN9 [2]
PEX_TX8	AL19	PEG_RXP8_C	C163	DIS@0.1U/10V_4	PEG_RXP8 [2]
PEX_TX8#	AK19	PEG_RXN8_C	C162	DIS@0.1U/10V_4	PEG_RXN8 [2]
PEX_RX8	AN20				PEG_TXP8 [2]
PEX_RX8#	AM20				PEG_TXN8 [2]
PEX_TX7	AK20	PEG_RXP7_C	C183	DIS@0.1U/10V_4	PEG_RXP7 [2]
PEX_TX7#	AJ20	PEG_RXN7_C	C182	DIS@0.1U/10V_4	PEG_RXN7 [2]
PEX_RX7	AP20				PEG_TXP7 [2]
PEX_RX7#	AP21				PEG_TXN7 [2]
PEX_TX6	AH20	PEG_RXP6_C	C161	DIS@0.1U/10V_4	PEG_RXP6 [2]
PEX_TX6#	AG20	PEG_RXN6_C	C160	DIS@0.1U/10V_4	PEG_RXN6 [2]
PEX_RX6	AN21				PEG_TXP6 [2]
PEX_RX6#	AM21				PEG_TXN6 [2]
PEX_TX5	AK21	PEG_RXP5_C	C180	DIS@0.1U/10V_4	PEG_RXP5 [2]
PEX_TX5#	AJ21	PEG_RXN5_C	C181	DIS@0.1U/10V_4	PEG_RXN5 [2]
PEX_RX5	AN23				PEG_TXP5 [2]
PEX_RX5#	AM23				PEG_TXN5 [2]
PEX_TX4	AL22	PEG_RXP4_C	C158	DIS@0.1U/10V_4	PEG_RXP4 [2]
PEX_TX4#	AK22	PEG_RXN4_C	C159	DIS@0.1U/10V_4	PEG_RXN4 [2]
PEX_RX4	AP23				PEG_TXP4 [2]
PEX_RX4#	AP24				PEG_TXN4 [2]
PEX_TX3	AK23	PEG_RXP3_C	C157	DIS@0.1U/10V_4	PEG_RXP3 [2]
PEX_TX3#	AJ23	PEG_RXN3_C	C156	DIS@0.1U/10V_4	PEG_RXN3 [2]
PEX_RX3	AN24				PEG_TXP3 [2]
PEX_RX3#	AM24				PEG_TXN3 [2]
PEX_TX2	AH23	PEG_RXP2_C	C179	DIS@0.1U/10V_4	PEG_RXP2 [2]
PEX_TX2#	AG23	PEG_RXN2_C	C178	DIS@0.1U/10V_4	PEG_RXN2 [2]
PEX_RX2	AN26				PEG_TXP2 [2]
PEX_RX2#	AM26				PEG_TXN2 [2]
PEX_TX1	AK24	PEG_RXP1_C	C155	DIS@0.1U/10V_4	PEG_RXP1 [2]
PEX_TX1#	AJ24	PEG_RXN1_C	C154	DIS@0.1U/10V_4	PEG_RXN1 [2]
PEX_RX1	AP26				PEG_TXP1 [2]
PEX_RX1#	AP27				PEG_TXN1 [2]
PEX_TX0	AL25	PEG_RXP0_C	C176	DIS@0.1U/10V_4	PEG_RXP0 [2]
PEX_TX0#	AK25	PEG_RXN0_C	C177	DIS@0.1U/10V_4	PEG_RXN0 [2]
PEX_RX0	AN27				PEG_TXP0 [2]
PEX_RX0#	AM27				PEG_TXN0 [2]

PEG Capacitance	
N13P-GS (GK107)	CH4222K9B04: CAP CHIP 0.22U 10V(+-10%,X5R,0402)
N13P-GL (GF108) N13M-GE1 (GF119)	CH41002KB93: CAP CHIP 0.1U 10V(+-10%,X5R,0402)

GPU RST#(CLG)

+3V C510 DIS@0.1U/10V_4

[2,8,24,27] PLTRST#

[8] DGPU_HOLD_RST#

GPU_RST#

U9 DIS@TC7SH08FU

All GPU power rails must ramp up after VDD33. The following conditions must be met:

- tNVVDD > 0
- tFBVDDQ > 0
- tPEX_VDD > 0
- tIFPx_IOVDD ≥ 0
- tIFPy_IOVDD ≥ 0
- The ramp time for any rail must be more than 40 us.

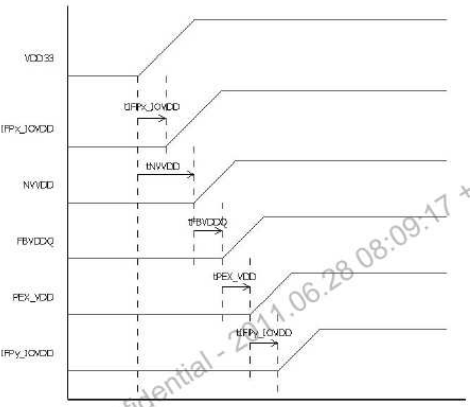


Figure 17. Recommended Power On Sequencing Order

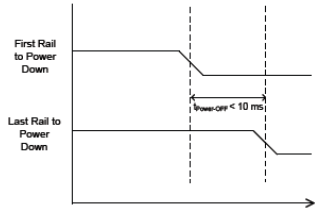


Figure 18. Recommended Power Off Sequencing Order

For power-down sequency

+3V_GPU +1.5V_GPU +3V_GPU GFX_CORE +3V_GPU +1.05V_GFX_PCIE

D1 DIS@RB500V-40 D2 DIS@RB500V-40 D25 DIS@RB500V-40

PEG CLK detect

GFXPG [9,43]

[8] PEG_CLKREQ# PEX_CLKREQ#

Q15 DIS@ME2N7002E

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Nvidia-N13P GB4-128(PCIe)	1A

Date: Wednesday, December 07, 2011 Sheet 14 of 45

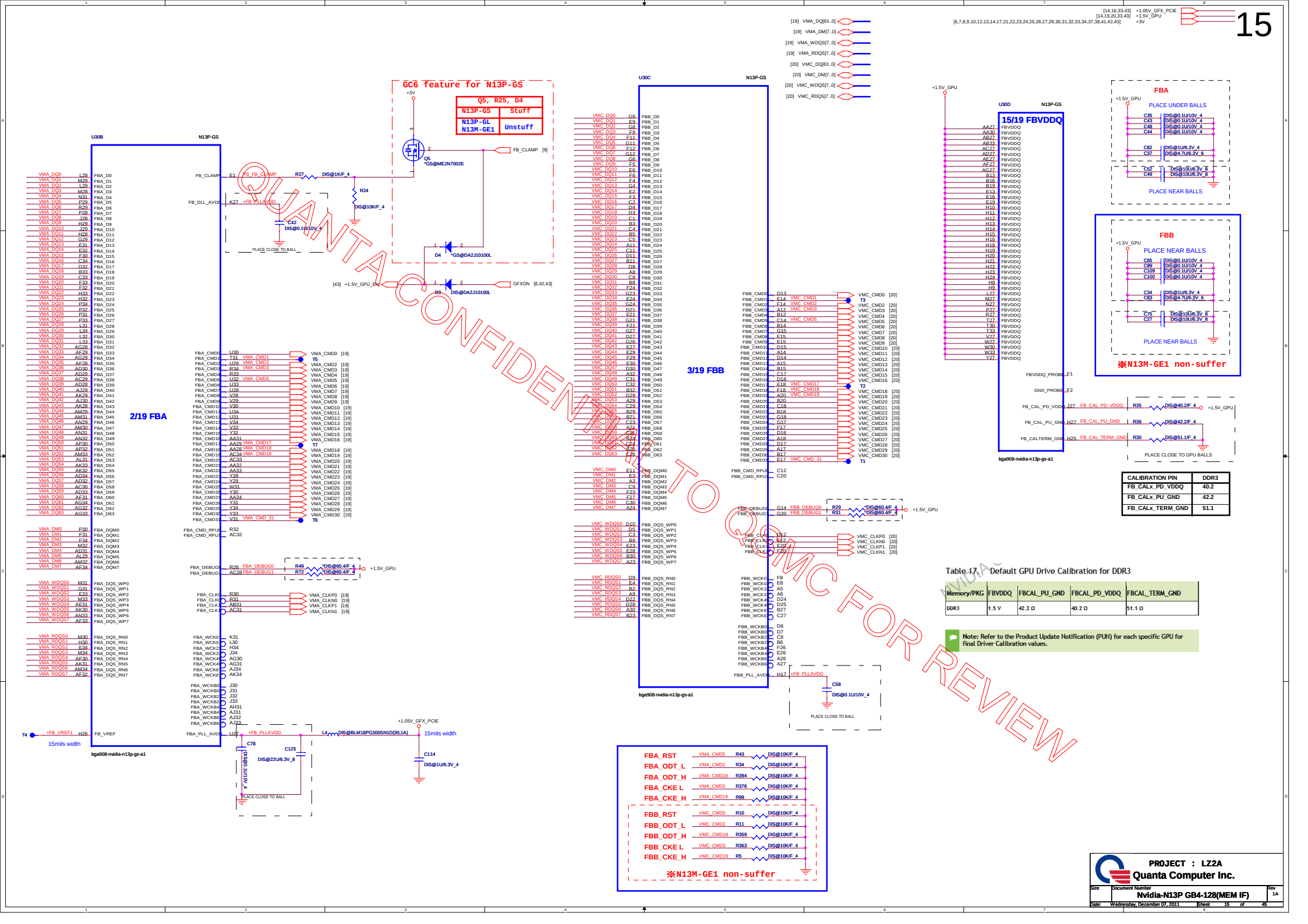


Table 17. Default GPU Drive Calibration for DDR3

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR3	1.5 V	42.2 Ω	40.2 Ω	51.1 Ω

Note: Refer to the Product Update Notification (PUN) for each specific GPU for final Driver Calibration values.

CALIBRATION PIN	DDR3
FB_CALx_PD_VDDQ	40.2
FB_CALx_PU_GND	42.2
FB_CALx_TERM_GND	51.1

PROJECT : LZ2A
Quanta Computer Inc.
Size | Document Number: Nvidia-N13P GB4-128(MEM IF) | Rev: 1A
Date: Wednesday, December 07, 2011 | Sheet 15 of 45

[14,15,33,43] +1.05V_GFX_PCIE

50 mA

160 mA+160 mA

200 mA

U30J N13P-GS

6/19 IFPAB

ALL PINS NC FOR GF117

IFPAB_RSET AJ8

+IFPAB_PLLVDD AH8 IFPAB_PLLVDD

R91 DIS@10K/F_4

+IFPAB_IOVDD AG8 IFPA_IOVDD AG9 IFPB_IOVDD

R83 DIS@10K/F_4

IFPA_TXC AN6 IFPA_TXC AM6

IFPA_TXD0 AN3 IFPA_TXD0 AP3

IFPA_TXD1 AM5 IFPA_TXD1 AN5

IFPA_TXD2 AK6 IFPA_TXD2 AL6

IFPA_TXD3 AH6 IFPA_TXD3 AJ6

IFPB_TXC AH9 IFPB_TXC AJ9

IFPB_TXD0 AP5 IFPB_TXD0 AP6

IFPB_TXD1 AL7 IFPB_TXD1 AM7

IFPB_TXD2 AM8 IFPB_TXD2 AN8

IFPB_TXD3 AL8 IFPB_TXD3 AK8

GPIO16 N4

IFPAB

bga908-nvidia-n13p-gs-a1

U30K N13P-GS

7/19 IFPC

ALL PINS NC FOR GF117

IFPC_RSET AF8

+IFPCD_PLLVDD AF7 IFPC_PLLVDD

R79 DIS@10K/F_4

+IFPCD_IOVDD AF6 IFPC_IOVDD

R84 DIS@10K/F_4

DVI/HDMI DP

I2CW_SDA I2CW_SCL

TXC TXC

TXD0 TXD0

TXD1 TXD1

TXD2 TXD2

IFPC_AUX AG2 IFPC_AUX AG3

IFPC_L3 AG4 IFPC_L3 AG5

IFPC_L2 AH4 IFPC_L2 AH3

IFPC_L1 AJ2 IFPC_L1 AJ3

IFPC_L0 AJ1 IFPC_L0 AK1

GPIO15 P2

IFPC

bga908-nvidia-n13p-gs-a1

U30L N13P-GS

8/19 IFPD

ALL PINS NC FOR GF117

IFPD_RSET AN2

+IFPCD_PLLVDD AG7 IFPD_PLLVDD

+IFPCD_IOVDD AG6 IFPD_IOVDD

DVI/HDMI DP

I2CX_SDA I2CX_SCL

TXC TXC

TXD0 TXD0

TXD1 TXD1

TXD2 TXD2

IFPD_AUX AK2 IFPD_AUX AK3

IFPD_L3 AK5 IFPD_L3 AK4

IFPD_L2 AL4 IFPD_L2 AL3

IFPD_L1 AM4 IFPD_L1 AM3

IFPD_L0 AM2 IFPD_L0 AM1

GPIO17 M6

IFPD

bga908-nvidia-n13p-gs-a1

U30M N13P-GS

9/19 IFPEF

ALL PINS NC FOR GF117

R60 DIS@10K_4 +IFPEF_PLLVDD AB8 IFPEF_PLLVDD

AD6 IFPEF_RSET

R61 DIS@10K_4 +IFPEF_IOVDD AC7 IFPE_IOVDD AC8 IFPF_IOVDD

DVI-DL DVI-SL/HDMI DP

I2CY_SDA I2CY_SCL

TXC TXC

TXD0 TXD0

TXD1 TXD1

TXD2 TXD2

HPD_E

IFPE_AUX AB4 IFPE_AUX AB3

IFPE_L3 AC5 IFPE_L3 AC4

IFPE_L2 AC3 IFPE_L2 AC2

IFPE_L1 AC1 IFPE_L1 AD1

IFPE_L0 AD3 IFPE_L0 AD2

GPIO18 R1

IFPE

I2CZ_SDA I2CZ_SCL

TXC TXC

TXD3 TXD3

TXD4 TXD4

TXD5 TXD5

HPD_F

IFPF_AUX AF2 IFPF_AUX AF3

IFPF_L3 AF1 IFPF_L3 AG1

IFPF_L2 AD5 IFPF_L2 AD4

IFPF_L1 AF5 IFPF_L1 AF4

IFPF_L0 AE4 IFPF_L0 AE3

GPIO19 P3

IFPF

bga908-nvidia-n13p-gs-a1

U30N N13P-GS

4/19 DACA

GF108/GKx GF117

R78 DIS@10K_4

TP29

TP31

DACA_VDD AG10

DACA_VREF AP9

DACA_RSET AP8

TSEN_VREF

GF117 GF108/GKx

I2CA_SCL R4 EV_CRTDCLK R630 DIS@2.2K_4 +3V_GPU

I2CA_SDA R5 EV_CRTDDAT R631 DIS@2.2K_4 +3V_GPU

DACA_HSYNC AM9 TP6

DACA_VSYNC AN9 TP30

DACA_RED AK9 TP4

DACA_GREEN AL10 TP3

DACA_BLUE AL9 TP5

bga908-nvidia-n13p-gs-a1

60mA 12~16 mil

+1.05V_GFX_PCIE

L2 DIS@BLM18PG300SN1D(30,1A)

PLACE CLOSE TO BGA

C122 DIS@22U/6.3V_8

C96 DIS@0.1U/10V_4

PLACE UNDER BGA

+PLLVDD

+1.05V_GFX_PCIE

L3 DIS@HCB1608KF(180,1.5A)_6

+NV_PLLVDD

90mA 12~16 mil

C126 DIS@1U/6.3V_4

C111 DIS@22U/6.3V_8

C101 DIS@4.7U/6.3V_6

C98 DIS@0.1U/10V_4

C97 DIS@0.1U/10V_4

C99 DIS@0.1U/10V_4

U30O N13P-GS

12/19 XTAL_PLL

PLLVDD AD8

SP_PLLVDD AE8

VID_PLLVDD AD7

NC

GF108/GKx GF117

XTALSSIN H1

XTALIN H3

XTALOUTBUFF J4

XTALOUT H2

BXTALOUT

XTAL_SSIN R33 DIS@10K_4

R38 DIS@10K_4

XTALI_27M Y1 XTALO_27M

C39 DIS@27P/50V_4

DIS@27MHZ

C41 DIS@33P/50V/NPO_4

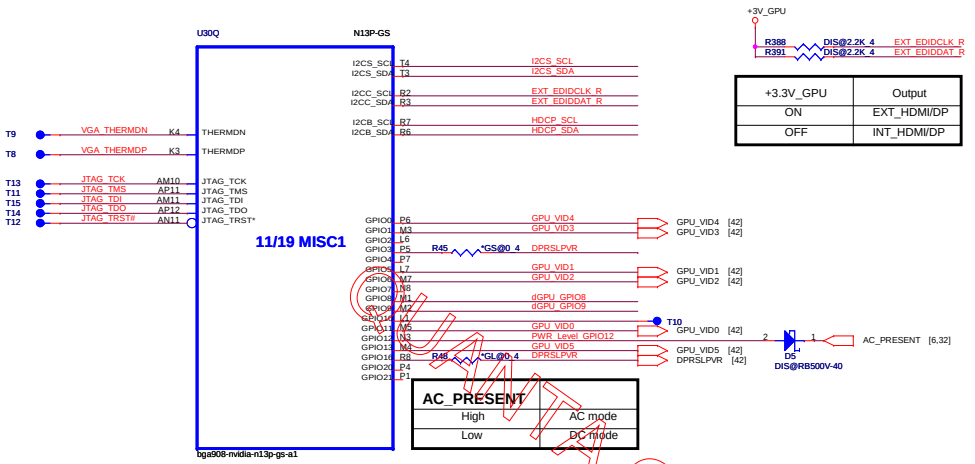
bga908-nvidia-n13p-gs-a1

PROJECT : LZ2A

Quanta Computer Inc.

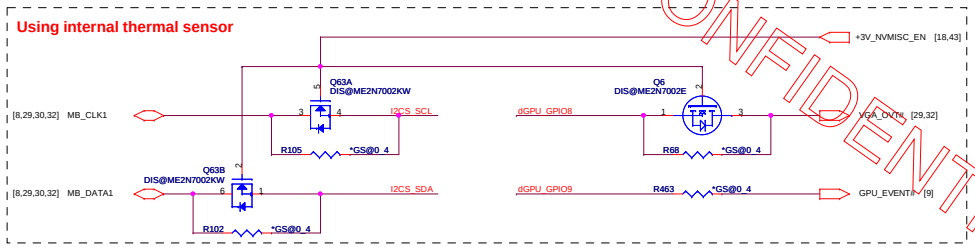
Size Document Number Nvidia-N13P GB4-128(Display) Rev 1A

Date: Wednesday, December 07, 2011 Sheet 16 of 45



+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP

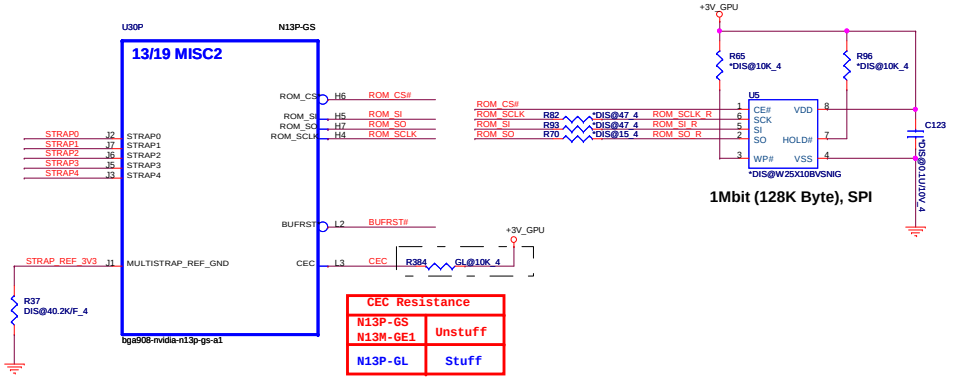
AC_PRESENT	
High	AC mode
Low	DC mode



	Q6,Q63, R81,R104	R68,R102, R105,R463
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor



CEC Resistance	
N13P-GS N13M-GE1	Unstuff
N13P-GL	Stuff

Table 2. GB4-128 Ballout Compatibility

Ball Number	N13P-PES/-GL/-NS1 Signal Names	N13M-GE1 Signal Names	N13P-GV / N13M-GS Signal Names	N13P-GT/-GS/-LP and N14P-Q1/-Q3 Signal Names	Comment
L3	CEC	NC	NC	NC	Place a 10k pull-up to 3V3 on N13P-PES/-GL/-NS1.

[14,16,18,43] +3V_GPU
[6,7,8,9,10,12,13,14,15,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[18] +3V_NVMISC

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	XXXX

Resistance	Quanta PN	DESCRIPTION
4.99K/F_4	CS24992FB26	RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4	CS31002FB26	RES CHIP 10K 1/16W +1% (0402)
15K/F_4	CS31502FB24	RES CHIP 15K 1/16W +1% (0402)
20K/F_4	CS32002FB29	RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4	CS32492FB16	RES CHIP 24.9K 1/16W +-1%(0402)
30K/F_4	CS33002FB13	RES CHIP 30K 1/16W +-1%(0402)]
34.8K/F_4	CS33482FB22	RES CHIP 34.8K 1/16W +-1%(0402)
45.3K/F_4	CS34532FB18	RES CHIP 45.3K 1/16W +-1% (0402)

VRAM Configuration Table

※ROM_SI Strap Bit for RAM Mapping

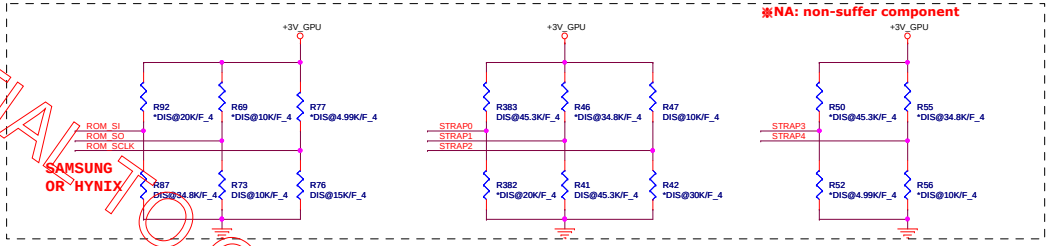
VRAM Configure	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN	RAMCFG [3:0]	ROM_SI
900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11	0x7(0111)	R87 (45.3K ohm)
900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C	0x6(0110)	R87 (34.8K ohm)
900MHz 1GB(64M*16) Samsung	AKD5EGGT500		K4W1G1646G-BC11	0x3(0011)	R87 (20K ohm)
900MHz 1GB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C	0x2(0010)	R87 (15K ohm)

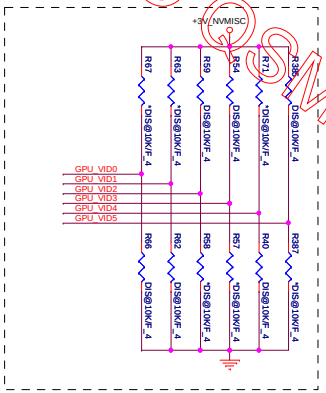
Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU Model Strap Table

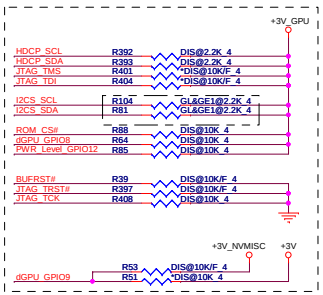
GPU Model	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1-A1 (GF119)	R73 (30K ohm) PD	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R47 (4.99K ohm) PU	R52 (4.99K ohm) PD	R56 (10K ohm) PD
N13P-GL-A1 (GF108)	R73 (10K ohm) PD	R76 (15K ohm) PD	R383 (45.3K ohm) PU	R41 (45.3K ohm) PD	R47 (10K ohm) PU	NA	NA
N13P-GS-A2 (GK107)	R69 (10K ohm) PU	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R42 (15K ohm) PD	R52 (4.99K ohm) PD	R56 (10K ohm) PD

※NA: non-suffer component





NVVDD Table	N13M-GE1-A1 (GF119)	N13P-GL-A1 (GF108)	N13P-GS-A1 (GK107)
	NVVDD (0.9V)	NVVDD (0.95V)	NVVDD (0.9V)
GPU_VID0	0 (R66)	0 (R66)	0 (R66)
GPU_VID1	0 (R62)	0 (R62)	0 (R62)
GPU_VID2	0 (R58)	1 (R59)	0 (R58)
GPU_VID3	0 (R57)	1 (R54)	0 (R57)
GPU_VID4	1 (R71)	0 (R40)	1 (R71)
GPU_VID5	1 (R385)	1 (R385)	1 (R385)



GPIO ASSIGNMENTS

GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding
GPIO4	LCD_BLEN	O	Panel Backlight Enable
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		

PROJECT : LZ2A
Quanta Computer Inc.
Size: Document Number: Nvidia-N13P GB4-128(GPIO/STRAP) Rev: 1A
Date: Wednesday, December 07, 2011 Sheet 17 of 45

U30E N13P-GS

14/19 NVVDD

GFX_CORE

VDD AA12, AA14, AA16, AA19, AA21, AA23, AB13, AB15, AB17, AB18, AB20, AB22, AC12, AC14, AC16, AC19, AC21, AC23, M12, M14, M16, M19, M21, M23, N13, N15, N17, N18, N20, N22, P12, P14, P16, P19, P21, P23, R13, R15, R17, R18, R20, R22, T12, T14, T16, T19, T21, T23, U13, U15, U17, U18, U20, U22, V13, V15, V17, V18, V20, V22, W12, W14, W16, W19, W21, W23, Y13, Y15, Y17, Y18, Y20, Y22

bga908-nvidia-n13p-gs-a1

GFX_CORE — PLACE UNDER BALLS

C85	DIS@0.1U/10V_4
C54	DIS@0.1U/10V_4
C46	DIS@0.1U/10V_4
C47	DIS@0.1U/10V_4
C59	DIS@4.7U/6.3V_6
C68	DIS@4.7U/6.3V_6
C79	DIS@4.7U/6.3V_6
C72	DIS@4.7U/6.3V_6
C80	DIS@4.7U/6.3V_6
C71	DIS@4.7U/6.3V_6
C63	DIS@4.7U/6.3V_6
C67	DIS@4.7U/6.3V_6
C50	DIS@4.7U/6.3V_6
C88	DIS@4.7U/6.3V_6

GFX_CORE — PLACE NEAR BALLS

C93	DIS@22U/6.3V_8
C66	DIS@47U/6.3V_8
C61	DIS@4.7U/6.3V_6
C73	DIS@4.7U/6.3V_6
C74	DIS@4.7U/6.3V_6
C90	DIS@4.7U/6.3V_6
C87	DIS@4.7U/6.3V_6
C76	*DIS@330U/2V/ESR9_7343

U30G N13P-GS

16/19 GND_1/2

GND A2, AA17, AA18, AA20, AA22, AB12, AB14, AB16, AB19, AB2, AB21, A33, AB23, AB28, AB30, AB32, AB5, AB7, AC13, AC15, AC17, AC18, AA13, AC20, AC22, AE2, AE28, AE30, AE32, AE33, AE5, AE7, AH10, AA15, AH13, AH16, AH19, AH2, AH22, AH24, AH28, AH29, AH30, AH32, AH33, AH5, AH7, AJ7, AK10, AK7, AL12, AL14, AL15, AL17, AL18, AL2, AL20, AL21, AL23, AL24, AL26, AL28, AL30, AL32, AL33, AL5, AM13, AM16, AM19, AM22, AM25, AN1, AN10, AN13, AN16, AN19, AN22, AN25, AN30, AN34, AN4, AN7, AP2, AP33, B1, B10, B22, B25, B28, B31, B34, B4, B7, C10, C13, C19, C22, C25, C28, C7, D2, D31, D33, E10, E22, E25, E5, E7, F28, F7, G10, G13, G16, G19, G2, G22, G25, G28, G3, G30, G32, G33, G5, G7, K2, K28, K30, K32, K33, K5, K7, M13, M15, M17, M18, M20, M22, N12, N14, N16

bga908-nvidia-n13p-gs-a1

U30I N13P-GS

17/19 GND_2/2

GND N19, N2, N21, N23, N28, N30, N32, N33, N5, N7, P13, P15, P17, P18, P20, P22, R12, R14, R16, R19, R21, R23, T13, T15, T17, T18, T2, T20, T22, AG11, T28, T32, T5, T7, U12, U14, U16, U19, U21, U23, V12, V14, V16, V19, V21, V23, W13, W15, W17, W18, W20, W22, W28, Y12, Y14, Y16, Y19, Y21, Y23, AH11

Optional CMD GNDs (2) NC for 4-Lyr cards

GND_OPT C16, GND_OPT W32

bga908-nvidia-n13p-gs-a1

To be configured as needed on the PCB

U30H N13P-GS

CONFIGURABLE POWER CHANNELS

10/19 XVDD

XVDD U1, U2, U3, U4, U5, U6, U7, U8, V1, V2, V3, V4, V5, V6, V7, V8, W2, W3, W4, W5, W7, W8, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, AA1, AA2, AA3, AA4, AA5, AA6, AA7, AA8

bga908-nvidia-n13p-gs-a1

U30F N13P-GS

18/19 NC/VDD33

NC AC6, AJ28, AJ4, AJ5, AL11, C15, D19, D20, D23, D26, H32, T9, V32

N13P-GT, N13P-GS, N13P-LP, N14P-Q1, N14P-Q3 — Other N13M N13P

3V3MISC — VDD33 J8, K8

3V3MISC — VDD33 L8, M8

bga908-nvidia-n13p-gs-a1

+3V_NVMISC

PLACE NEAR BALLS

C55 DIS@0.1U/10V_4, C53 DIS@0.1U/10V_4

+3V_NVMISC_EN [17,43]

Q12 *CS@AO3404(30V 5.8A)

R74 DIS@0_6

C64 DIS@0.1U/10V_4, C69 DIS@0.1U/10V_4

C84 DIS@1U/6.3V_4, C56 DIS@4.7U/6.3V_6

+3V_GPU

PLACE NEAR BALLS

PLACE NEAR BGA

	R74	Q12
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Nvidia-N13P GB4-128(POWER)	1A

Date: Wednesday, December 07, 2011 Sheet 18 of 45

[14,15,20,33,43] +1.5V_GPU

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

CHANNEL A: 512MB/1024MB DDR3

U4 — 96-BALL SDRAM DDR3 DIS@K4W1G1646E-HC11

U29 — 96-BALL SDRAM DDR3 DIS@K4W1G1646E-HC11

U6 — 96-BALL SDRAM DDR3 DIS@K4W1G1646E-HC11

U31 — 96-BALL SDRAM DDR3 DIS@K4W1G1646E-HC11

Should be 240 Ohms +-1%

R44 DIS@240/F_4

R377 DIS@240/F_4

R97 DIS@240/F_4

R390 DIS@240/F_4

+1.5V_GPU

R379 DIS@1.33K/F_4
R378 DIS@1.33K/F_4
C452 DIS@0.01U/16V_4
VREFC_VMA1

R32 DIS@1.33K/F_4
R28 DIS@1.33K/F_4
C38 DIS@0.01U/16V_4
VREFD_VMA1

C461 *DIS@10U/6.3V_6

R75 DIS@1.33K/F_4
R80 DIS@1.33K/F_4
C115 DIS@0.01U/16V_4
VREFC_VMA3

R396 DIS@1.33K/F_4
R395 DIS@1.33K/F_4
C472 DIS@0.01U/16V_4
VREFD_VMA3

Placement has to be close to VRAM

VMA_CLKP0 — R26 DIS@162/F_4
VMA_CLKN0
VMA_CLKP1 — R95 DIS@162/F_4
VMA_CLKN1

C142	DIS@1U/6.3V_4	C507	DIS@1U/6.3V_4
C45	DIS@1U/6.3V_4	C458	DIS@1U/6.3V_4
C119	DIS@1U/6.3V_4	C468	DIS@1U/6.3V_4
C459	DIS@1U/6.3V_4	C471	DIS@1U/6.3V_4
C86	DIS@1U/6.3V_4	C463	DIS@1U/6.3V_4
C81	DIS@1U/6.3V_4	C102	DIS@1U/6.3V_4
C51	DIS@1U/6.3V_4	C465	DIS@1U/6.3V_4
C91	DIS@1U/6.3V_4	C57	DIS@1U/6.3V_4
C168	DIS@0.1U/10V_4	C505	DIS@0.1U/10V_4
C169	DIS@0.1U/10V_4	C506	DIS@0.1U/10V_4
C456	DIS@0.1U/10V_4	C170	DIS@0.1U/10V_4
C473	DIS@0.1U/10V_4	C60	DIS@0.1U/10V_4

C23	DIS@1U/6.3V_4	C442	DIS@1U/6.3V_4
C32	DIS@1U/6.3V_4	C5	DIS@1U/6.3V_4
C33	DIS@1U/6.3V_4	C446	DIS@1U/6.3V_4
C36	DIS@1U/6.3V_4	C447	DIS@1U/6.3V_4
C443	DIS@1U/6.3V_4	C439	DIS@1U/6.3V_4
C62	DIS@1U/6.3V_4	C6	DIS@1U/6.3V_4
C464	DIS@1U/6.3V_4	C70	DIS@1U/6.3V_4
C40	DIS@1U/6.3V_4	C448	DIS@1U/6.3V_4
C451	DIS@0.1U/10V_4	C121	DIS@0.1U/10V_4
C470	DIS@0.1U/10V_4	C457	DIS@0.1U/10V_4
C137	DIS@0.1U/10V_4	C128	DIS@0.1U/10V_4
C124	DIS@0.1U/10V_4	C466	DIS@0.1U/10V_4

PROJECT : LZ2A
Quanta Computer Inc.

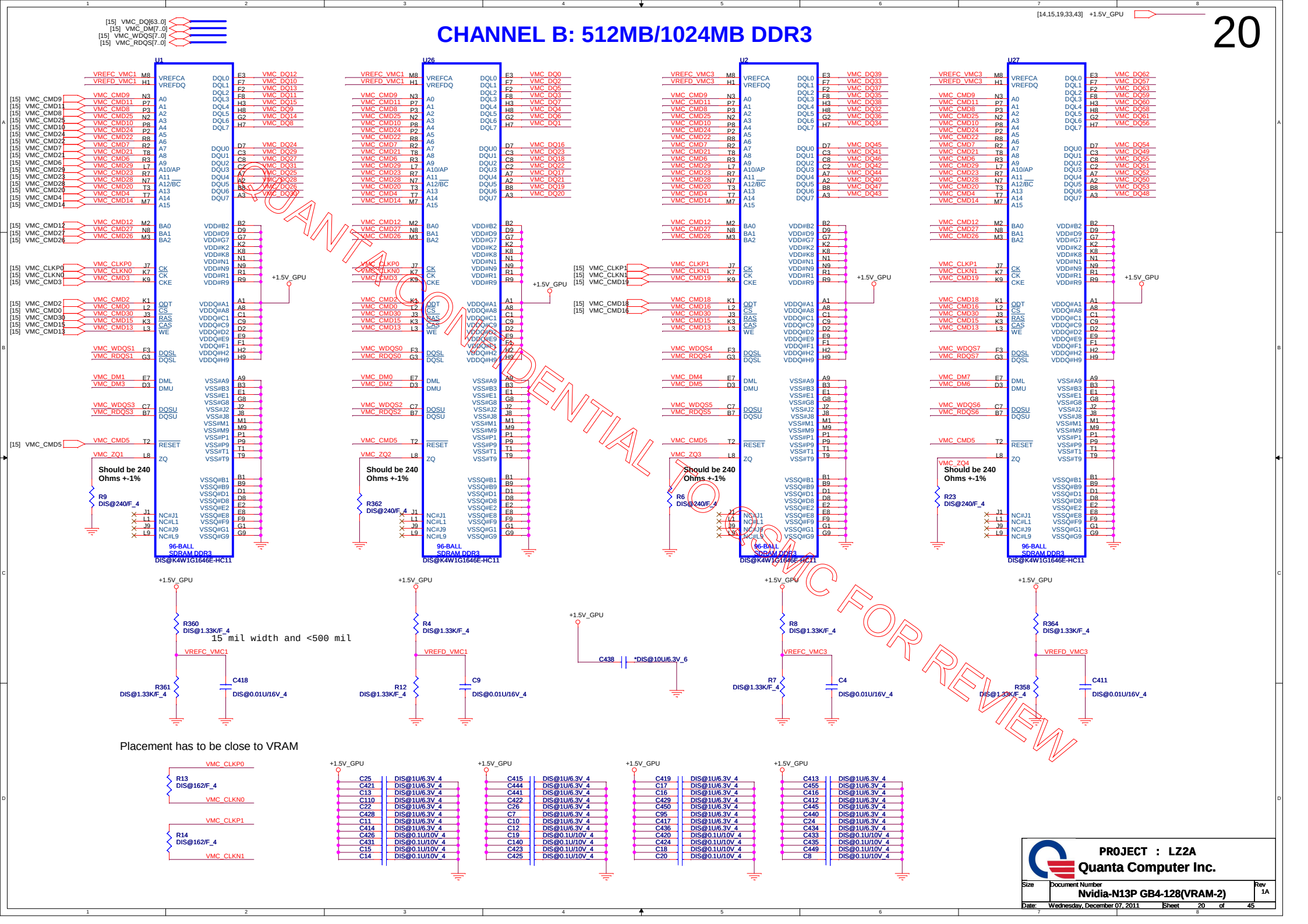
Size	Document Number	Rev
	Nvidia-N13P GB4-128(VRAM-1)	1A

Date: Wednesday, December 07, 2011 Sheet 19 of 45

CHANNEL B: 512MB/1024MB DDR3

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

[14,15,19,33,43] +1.5V_GPU



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Nvidia-N13P GB4-128(VRAM-2)	1A

Date: Wednesday, December 07, 2011 Sheet 20 of 45

[6,7,8,9,10,12,13,14,15,17,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[7,10,22,25,26,29,30,33,34] +5V

Change to KL6/BC HDMI CONN

[6] INT_HDMI_TXDP2 — C620 0.1U/10V_4 — HDMI_TX2+
[6] INT_HDMI_TXDN2 — C619 0.1U/10V_4 — HDMI_TX2-
[6] INT_HDMI_TXDP1 — C618 0.1U/10V_4 — HDMI_TX1+
[6] INT_HDMI_TXDN1 — C617 0.1U/10V_4 — HDMI_TX1-
[6] INT_HDMI_TXDP0 — C616 0.1U/10V_4 — HDMI_TX0+
[6] INT_HDMI_TXDN0 — C615 0.1U/10V_4 — HDMI_TX0-
[6] INT_HDMI_TXCP — C613 0.1U/10V_4 — HDMI_CLK+
[6] INT_HDMI_TXCN — C611 0.1U/10V_4 — HDMI_CLK-

[6] INT_HDMI_SCL — INT_HDMI_SCL
[6] INT_HDMI_SDA — INT_HDMI_SDA
[6] INT_HDMI_HPD — INT_HDMI_HPD

R316 2.2K_4, R297 2.2K_4 — Q43 DMN5L06K-7 — Q39 DMN5L06K-7
R313 2.2K_4, R568 2.2K_4
C668 *68p/50V_4, C669 *68p/50V_4
F2 FUSE_1.1A_8V_POLY
C667 0.1U/10V_4

CN16 — CONN_HDMI
HDMI_TX2+ / HDMI_TX2- / HDMI_TX1+ / HDMI_TX1- / HDMI_TX0+ / HDMI_TX0- / HDMI_CLK+ / HDMI_CLK-
HDMI_DDC_CLK / HDMI_DDC_DAT / HDMIC_5V / HP_DET
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL1 SHELL2 SHELL3 SHELL4

R315 590/F_4 — HDMI_TX2+
R310 590/F_4 — HDMI_TX2-
R304 590/F_4 — HDMI_TX1+
R302 590/F_4 — HDMI_TX1-
R300 590/F_4 — HDMI_TX0+
R298 590/F_4 — HDMI_TX0-
R294 590/F_4 — HDMI_CLK+
R291 590/F_4 — HDMI_CLK-
SC51 *0.1U/10V_4
3HDMI_LF
Q42 2N7002K

R551 10K_4, R553 10K_4
Q69A ME2N7002DKW-G
Q69B ME2N7002DKW-G
R549 20K_4
Place close to PCH

For ESD

U39 *CM1225
U38 *CM1225
U37 *CM1225
NC CH4 NC CH3 GND GND NC CH2 NC CH1
HDMI_TX2+ / HDMI_TX2- / HDMI_TX1+ / HDMI_TX1-
HDMI_TX0+ / HDMI_TX0- / HDMI_CLK+ / HDMI_CLK-
HDMI_DDC_DAT / HDMI_DDC_CLK / HDMIC_5V / HP_DET

For EMI

R574 130/F_4 — HDMI_TX2+ / HDMI_TX2-
R573 130/F_4 — HDMI_TX1+ / HDMI_TX1-
R572 130/F_4 — HDMI_TX0+ / HDMI_TX0-
R569 130/F_4 — HDMI_CLK+ / HDMI_CLK-

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

Date: Wednesday, December 07, 2011 Sheet 21 of 45

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

[6] INT_CRT_RED
[6] INT_CRT_GRE
[6] INT_CRT_BLU
[6] INT_CRT_VSYNC
[6] INT_CRT_HSYNC
[6] INT_DDCCLK
[6] INT_DDCDAT

D22 RB500V-40
CRT_VCC
C526 0.1U/10V_4
+5V
F1 FUSE_1.1A_8V_POLY
CRT_VCC_R
C527 0.1U/10V_4

L7 BLM15BA470SS1D
L8 BLM15BA470SS1D
L9 BLM15BA470SS1D
CRT_R1
CRT_G1
CRT_B1

R231 150/F_4
R232 150/F_4
R228 150/F_4
C212 5.6P/50V/COG_4
C214 5.6P/50V/COG_4
C225 5.6P/50V/COG_4
C215 5.6P/50V/COG_4
C213 5.6P/50V/COG_4
C211 5.6P/50V/COG_4

TP15

CN12
CRT_CONN

ESD PROTECTION
U35
CRT_R1
CRT_G1
IO1 GND IO2 IO4 REF IO3
CRT_B1
CRT_VCC_R
CRT_VCC
*IP4220CZ6
U12
CRTVSYNC
CRTHSYNC
DDCCLK
DDCDAT
CRT_VCC
*IP4220CZ6

+5V
U33 AHCT1G125DCH
U34 AHCT1G125DCH
C554 0.1U/10V_4
VGAVSYNC_R
VGAHSYNC_R
R493 10_4
R502 10_4
CRTVSYNC1
CRTHSYNC1

Place near
U37,U38 < 200 mil

C538 *10P/50V/COG_4
C529 *10P/50V/COG_4

L25 BK1608HS121-T
L26 BK1608HS121-T
CRTVSYNC
CRTHSYNC
C539 10P/50V/COG_4
C528 10P/50V/COG_4

Place near CN5002 connector
< 200 mil

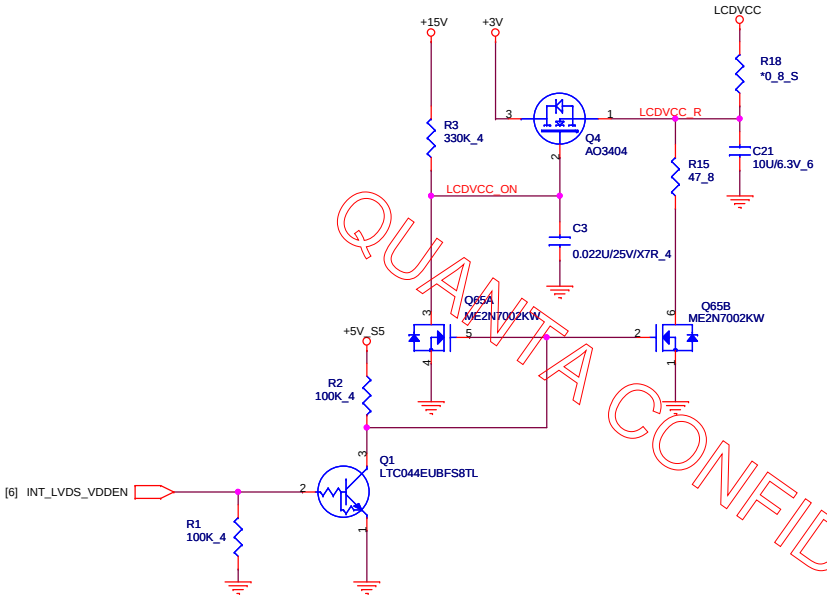
+3V
R201 2.2K_4
R163 2.2K_4
CRT_VCC
R191 4.7K_4
R177 4.7K_4
Q64A ME2N7002DKW-G
Q64B ME2N7002DKW-G
DDCCLK
DDCDAT

C201 *10P/50V/COG_4
C194 *10P/50V/COG_4
For EMI

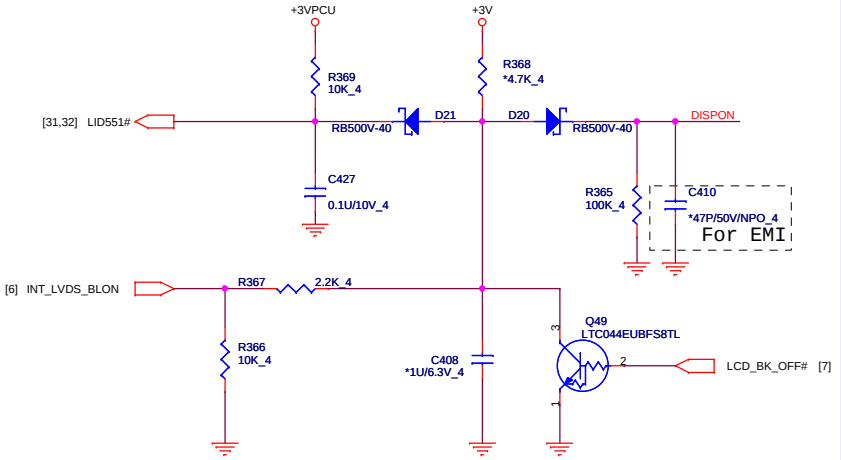
PROJECT : LZ2A
Quanta Computer Inc.
Size Custom
Document Number CRT CONN
Rev 1A
Date: Wednesday, December 07, 2011
Sheet 22 of 45

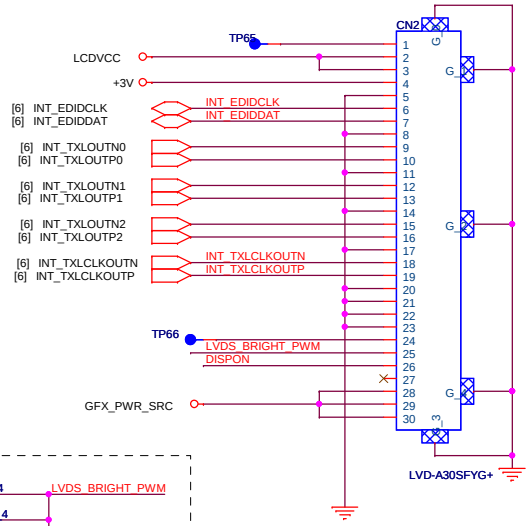
[26,30,34,36,43] +15V
[6,7,8,9,10,12,13,14,15,17,21,22,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,26,28,31,33,34] +5V_S5
[6,7,24,26,27,31,32,34,35,36,40] +3VPCU
[33,35,36,37,38,39,41,42] VIN

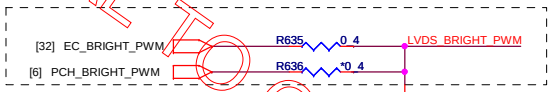
LCDVCC

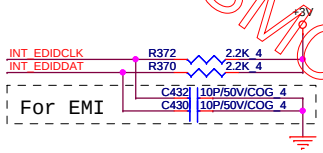


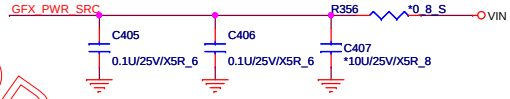
Back Light

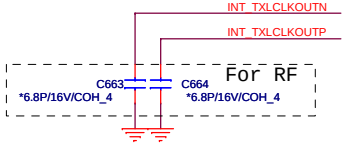












PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A

Date: Wednesday, December 07, 2011 Sheet 23 of 45

[6,7,23,26,27,31,32,34,35,36,40] +3VPCU
[33,34] LANVCC
[6,7,8,9,10,12,13,14,15,17,21,22,23,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V

LANVCC

+3VPCU, LANVCC
Q47 AO6402A
[34] LAN_ON
R341 *0_8_S
LANVCC_R
C394 *10U/6.3V_8
C393 0.1U/10V_4

* R594 open when use RTL8105E

TP60, R594 *LAN1G@10K_4, R599 1K/F_4
C650 *10P/50V/COG_4 RJ45_LINKUP#
C644 *10P/50V/COG_4 RJ45_ACTIVITY#
LED3/EEDO, EECS R606 10K_4, EEDI R603 10K_4, TP62

U45 RTL81111F/RTL8105E

CTRL12/VDD, LANVCC, CTRL12A, LAN_DVDD12, LAN_EVDD12
VDDREG, AVDD33, AVDD33(NC), DVDD33, DVDD3, REGOUT, AVDD10, AVDD10(NC), DVDD10, DVDD10(NC), EVDD10
GPO/SMBALERT, SMBCLK(NC)/SMBDATA(NC), LED1/EESK, LED0, LED3/EEDO, EECS/SCL, EEDI/SDA
MDIP0/MDIN0 MDI_0+/MDI_0-, MDIP1/MDIN1 MDI_1+/MDI_1-, MDIP2(NC)/MDIN2(NC) MDI_2+/MDI_2-, MDIP3(NC)/MDIN3(NC) MDI_3+/MDI_3-
ISOLATEB, LANWAKEB, ENSWREG
CKXTAL1 XTAL1, CKXTAL2 XTAL2
RSET R593 2.49K/F_4
PERSTB, CLKREQB, HSIP, HSIN, REFCLK_P, REFCLK_N, HSOP, HSON, GND, GND

+3V
R601 1K_4
R600 15K_4
D24 RB500V-40
LAN_ISOLATEB [32]
PCIE_WAKE# [6,27,32]
LANVCC
Y4 25MHZ
C637 33P/50V/NPO_4
C638 33P/50V/NPO_4

[2,8,14,27] PLTRST#
[8] PCIE_CLKREQ_LAN#

GPP_TX2N_LAN C649 0.1U/10V_4
GPP_TX2P_LAN C646 0.1U/10V_4
PCIE_RXN2_LAN [8]
PCIE_RXP2_LAN [8]
CLK_PCIE_LANN [8]
CLK_PCIE_LANP [8]
PCIE_TXN2_LAN [8]
PCIE_TXP2_LAN [8]

LANVCC
C656 0.1U/10V_4, C654 0.1U/10V_4, C633 0.1U/10V_4, C648 0.1U/10V_4, C639 0.1U/10V_4, R607 *0_8_S, C634 0.1U/10V_4, C653 0.1U/10V_4, C657 4.7U/6.3V_6
CTRL12/VDD

* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

Place C5113 ,C5094 closed to U5006 pins44,45.

* C476 and C472 are for U24 LAN_EVDD12 pin 21.

CTRL12A
L28 4.7uH
CTRL12A_R
C662 4.7U/6.3V_6, C661 0.1U/10V_4
R609 *0_8_S
R611 *0_8_S
LAN_EVDD12
C659 1U/6.3V_4, C642 0.1U/10V_4
C635 0.1U/10V_4, C632 0.1U/10V_4, C636 0.1U/10V_4, C655 0.1U/10V_4, C641 0.1U/10V_4, C630 0.1U/10V_4, C631 0.1U/10V_4

* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Tramsformer

U43 *CM1293A-04SO
U22 *LAN1G@CM1293A-04SO
10/100 non-stuff
Reserve for Surge
Line to GND TVS

Reserve for Surge
Line to Line TVS
U41 *UCLAMP2512T.TCT

MDI_0- R590 1/F_4, MDI_0+ R589 1/F_4, MDI_1- R584 1/F_4, MDI_1+ R583 1/F_4
MDI_2- R588 *LAN1G@1/F_4, MDI_2+ R587 *LAN1G@1/F_4, MDI_3- R586 *LAN1G@1/F_4, MDI_3+ R585 *LAN1G@1/F_4

U40 TST1284R LF
TD4-/MX4-, TD4+/MX4+, TCT4/MCT4, TD3-/MX3-, TD3+/MX3+, TCT3/MCT3, TD2-/MX2-, TD2+/MX2+, TCT2/MCT2, TD1-/MX1-, TD1+/MX1+, TCT1/MCT1
LAN_MX0-, LAN_MX0+, LAN_MCT0, LAN_MX1-, LAN_MX1+, LAN_MCT1, LAN_MX2-, LAN_MX2+, LAN_MCT2, LAN_MX3-, LAN_MX3+, LAN_MCT3

U20 *LAN1G@UCLAMP2512T.TCT
Reserve for Surge
Line to Line TVS

C623 0.01U/50V/X7R_4

Layout:All termination signal should have 30 mil trace

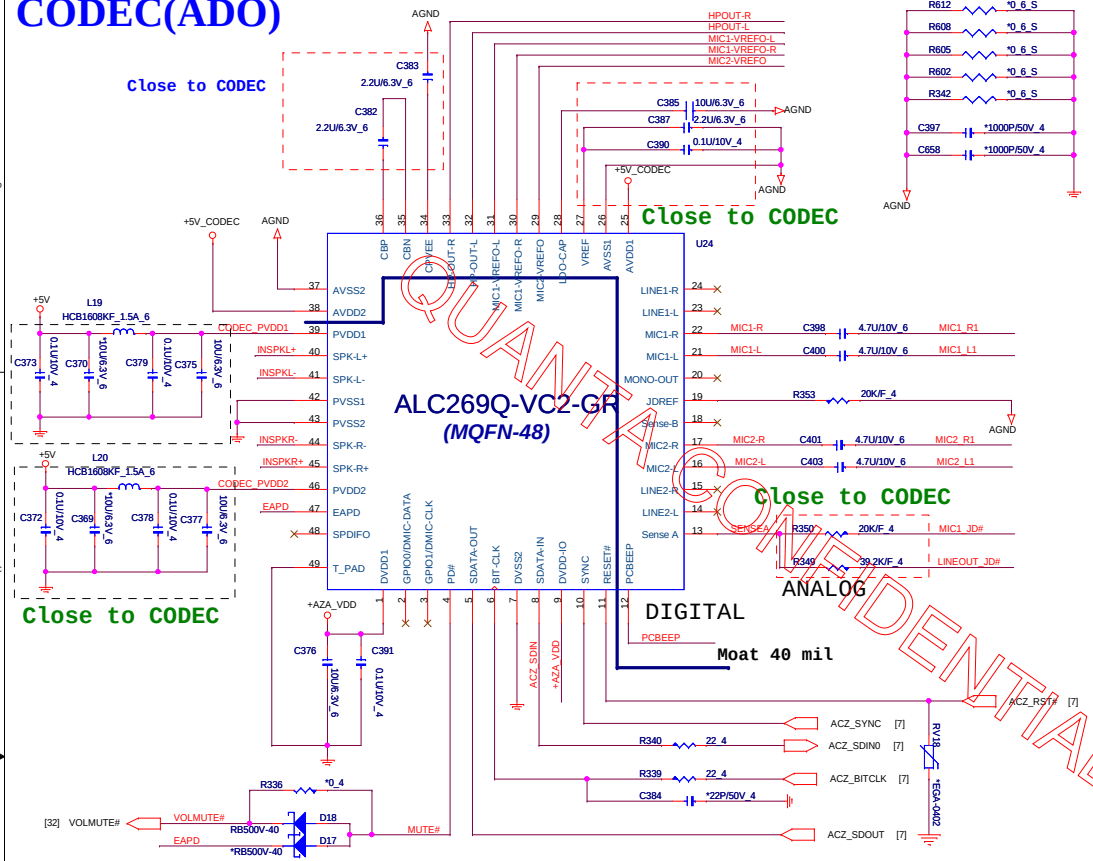
R570 75/F_8, D30 *BS201N-LV_1206, LANCT3, LANCT5
Gas Tube Discharge _ Reserve for Surge
R571 75/F_8, D31 *BS201N-LV_1206
Gas Tube Discharge _ Reserve for Surge
R296 0/F_8 For EMI, D32 *BS201N-LV_1206
Gas Tube Discharge _ Reserve for Surge
R295 0/F_8 For EMI, D33 *BS201N-LV_1206
Gas Tube Discharge _ Reserve for Surge
Reserve for Surge
Line to GND Gas Tube Discharge
C366 10P/3KV/NPO_1808
R327 1M_8
PJP18 *SHORTPAD

RJ45 Connector

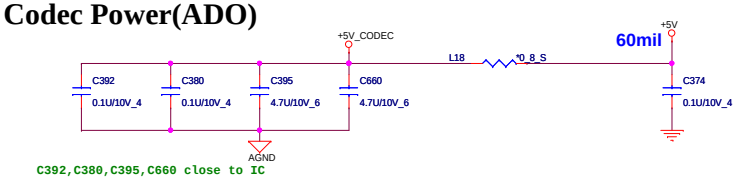
EMI:close RJ45
RV15 *AZ5123-01H, RV14 *AZ5123-01H
C270 *0.1U/10V_4
CN13
LANVCC R256 150_4
Orange LED
LAN_OLED
RJ45_LINKUP#
LAN_MX0+, LAN_MX0-, LAN_MX1+, LAN_MX1-, LAN_MX2+, LAN_MX2-, LAN_MX3+, LAN_MX3-
LANVCC R567 150_4
LAN_GLED
RJ45_ACTIVITY#
GREEN LED
RJ45
RV26 *AZ5123-01H, RV27 *AZ5123-01H
C609 *0.1U/10V_4
EMI:close RJ45

PROJECT : LZ2A			
Quanta Computer Inc.			
Size: Custom	Document Number: RTL81111F/RTL8105E		Rev: 1A
Date: Wednesday, December 07, 2011	Sheet 24 of 45		

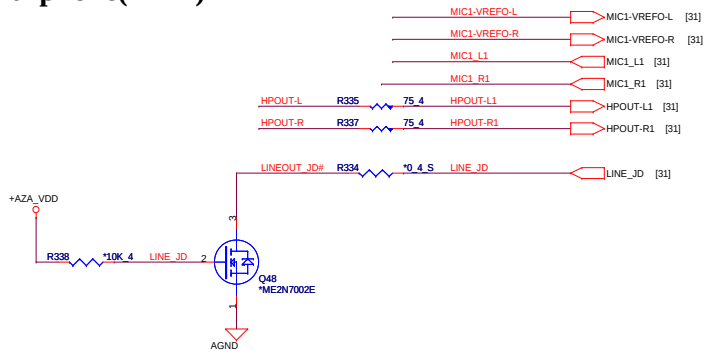
CODEC(ADO)



Codec Power(ADO)

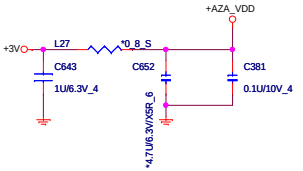


Earphone(AMP)

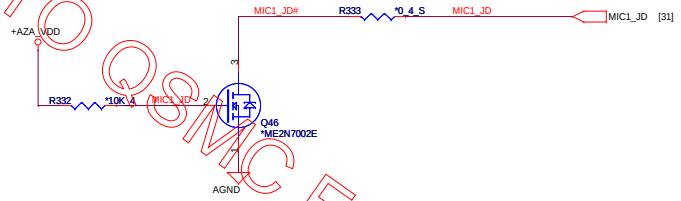


HDA Power(ADO)

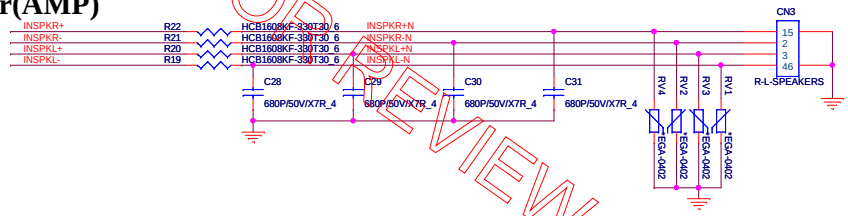
*Intel HDA Either +1.5V_S5 or +3V_S5



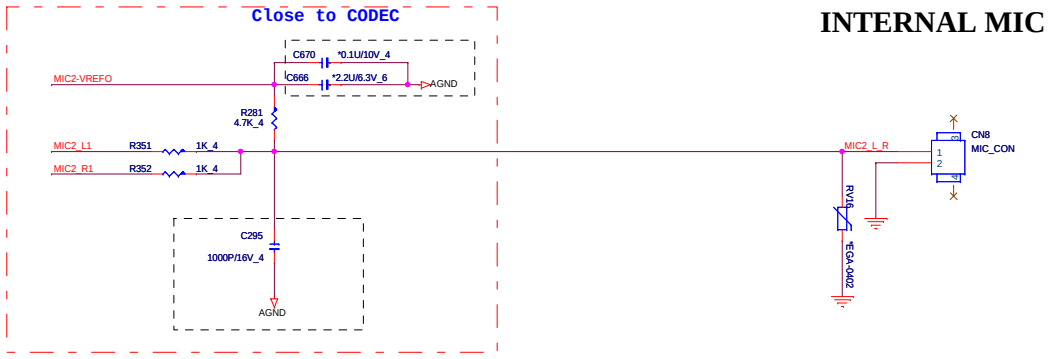
System MIC(AMP)



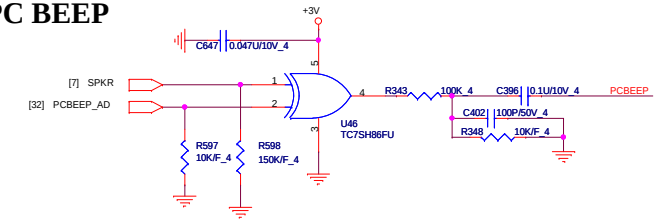
Speaker(AMP)



INTERNAL MIC

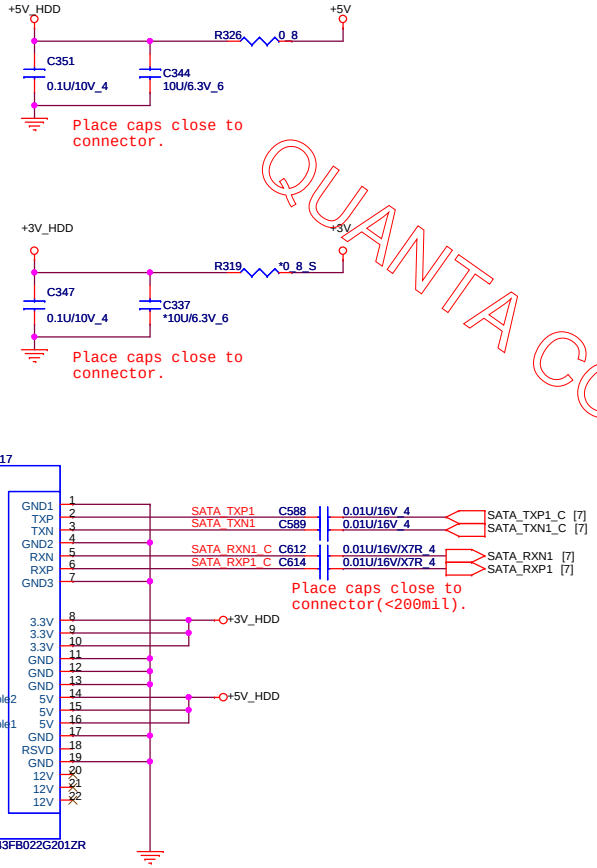


PC BEEP



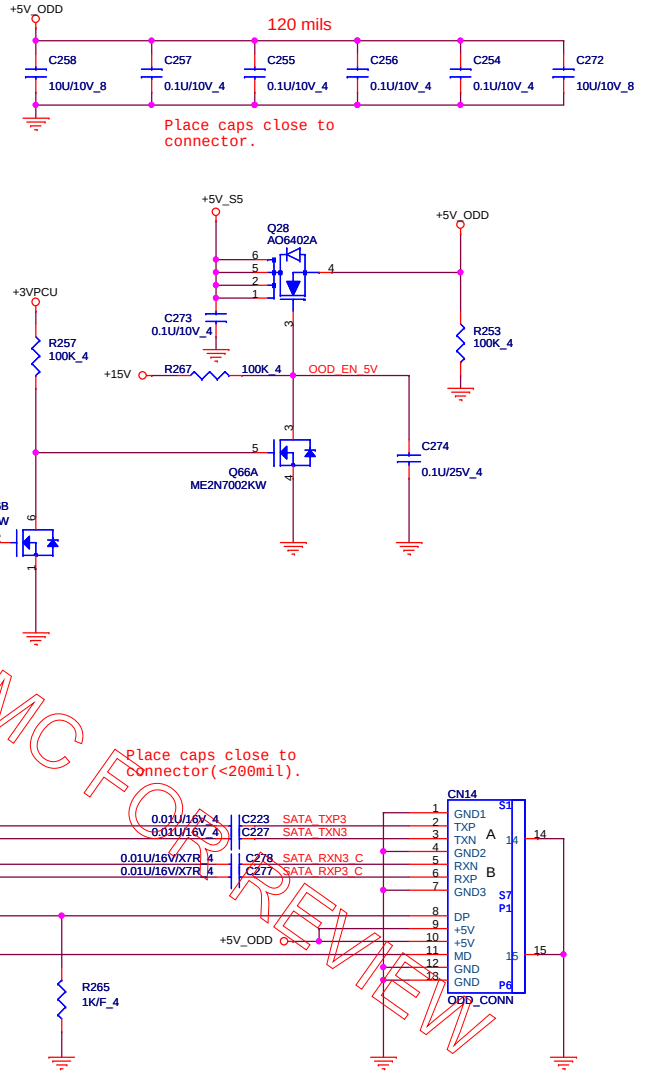
PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: ALC269/MIC/Line out	Rev: 1A
Date: Wednesday, December 07, 2011	Sheet 25 of 45	

SATA HDD Connector.



SATA ODD Connector.

[7,10,21,22,25,29,30,33,34] +5V
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,34,35,36,37,38,39,40,41,42,43] +5VPCU
[6,7,23,24,27,31,32,34,35,36,40] +3VPCU
[23,30,34,36,43] +15V



PROJECT : LZ2A

Quanta Computer Inc.

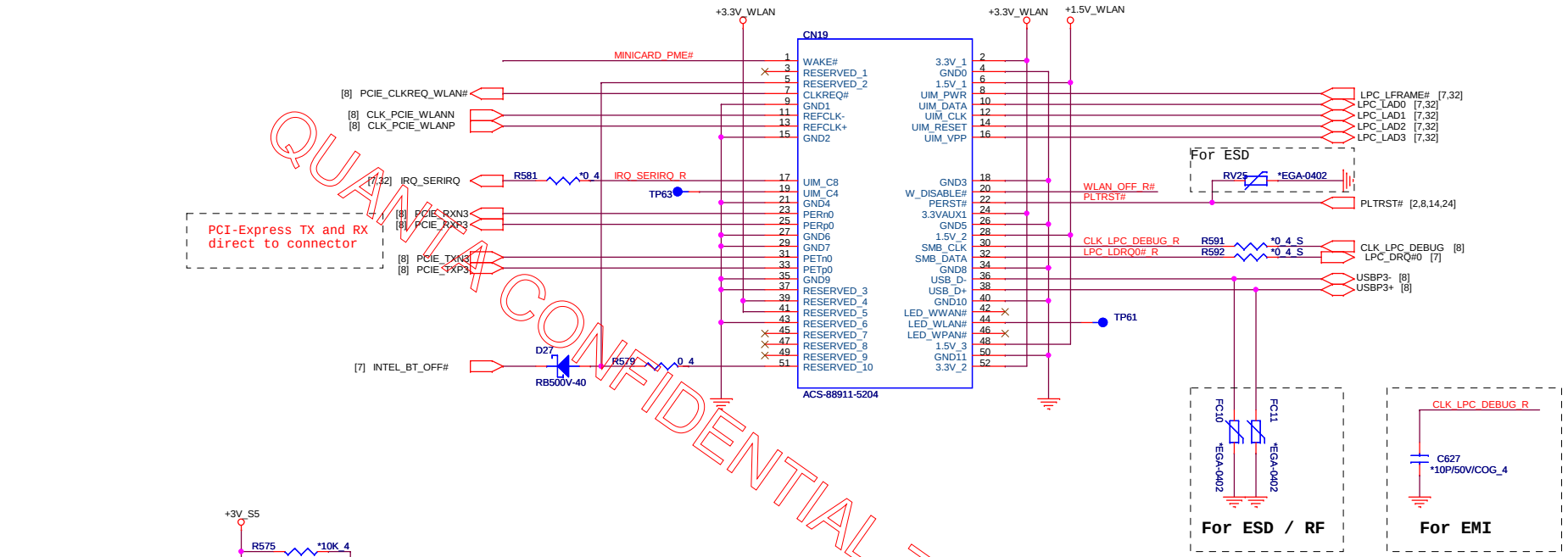
Size	Document Number	Rev
Custom	SATA HDD/CD-ROM	1A

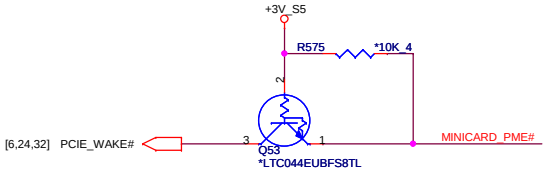
Date: Wednesday, December 07, 2011 Sheet 26 of 45

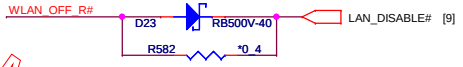
MiniCard WLAN connector

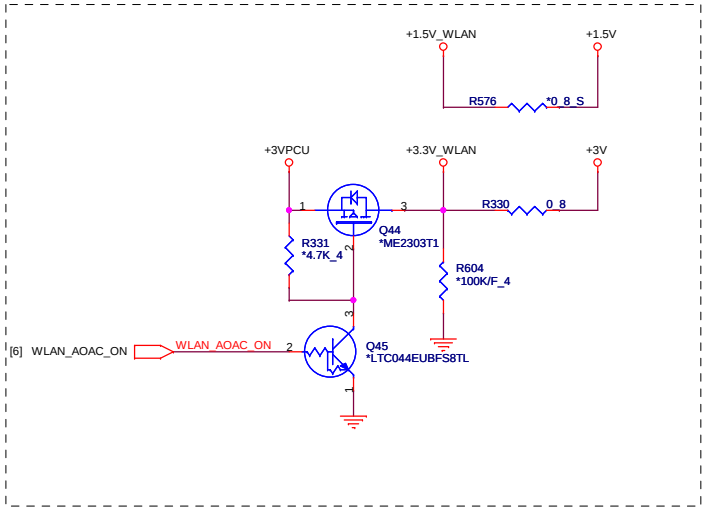
[2,6,7,8,9,10,31,34] +3V_S5
[4,10] +1.5V
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,29,30,31,32,33,34,37,38,41,42,43] +3V

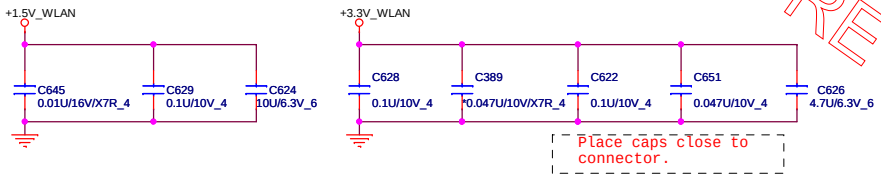
27









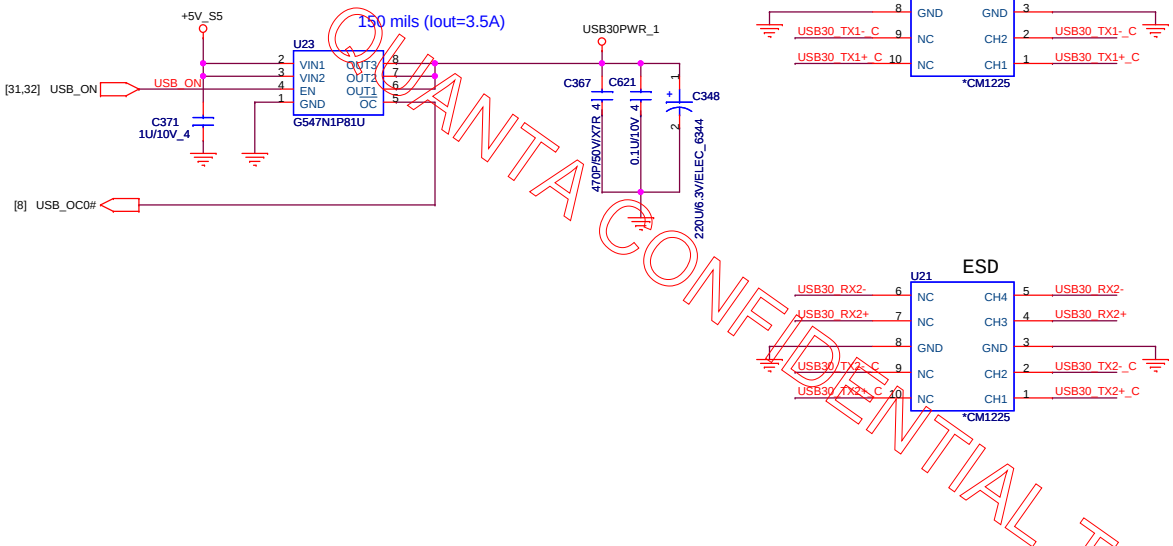


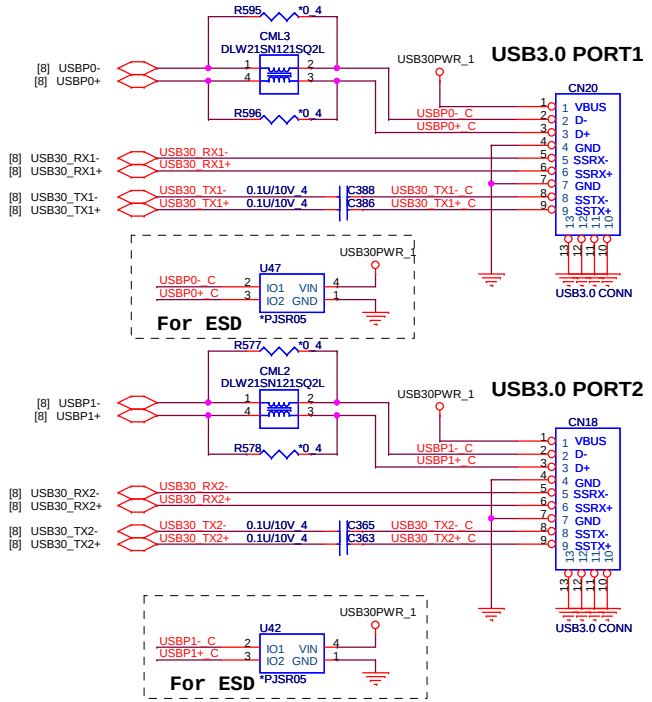
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB2.0*2/WLAN/BT	1A

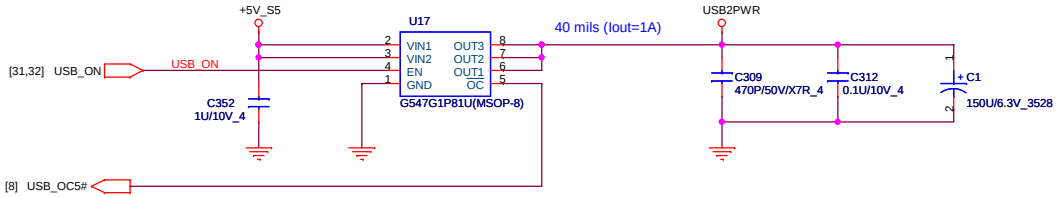
Date: Wednesday, December 07, 2011 Sheet 27 of 45

USB3.0*2

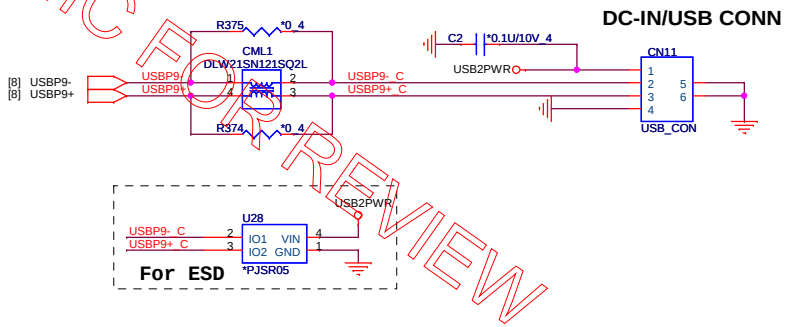




USB2.0*1



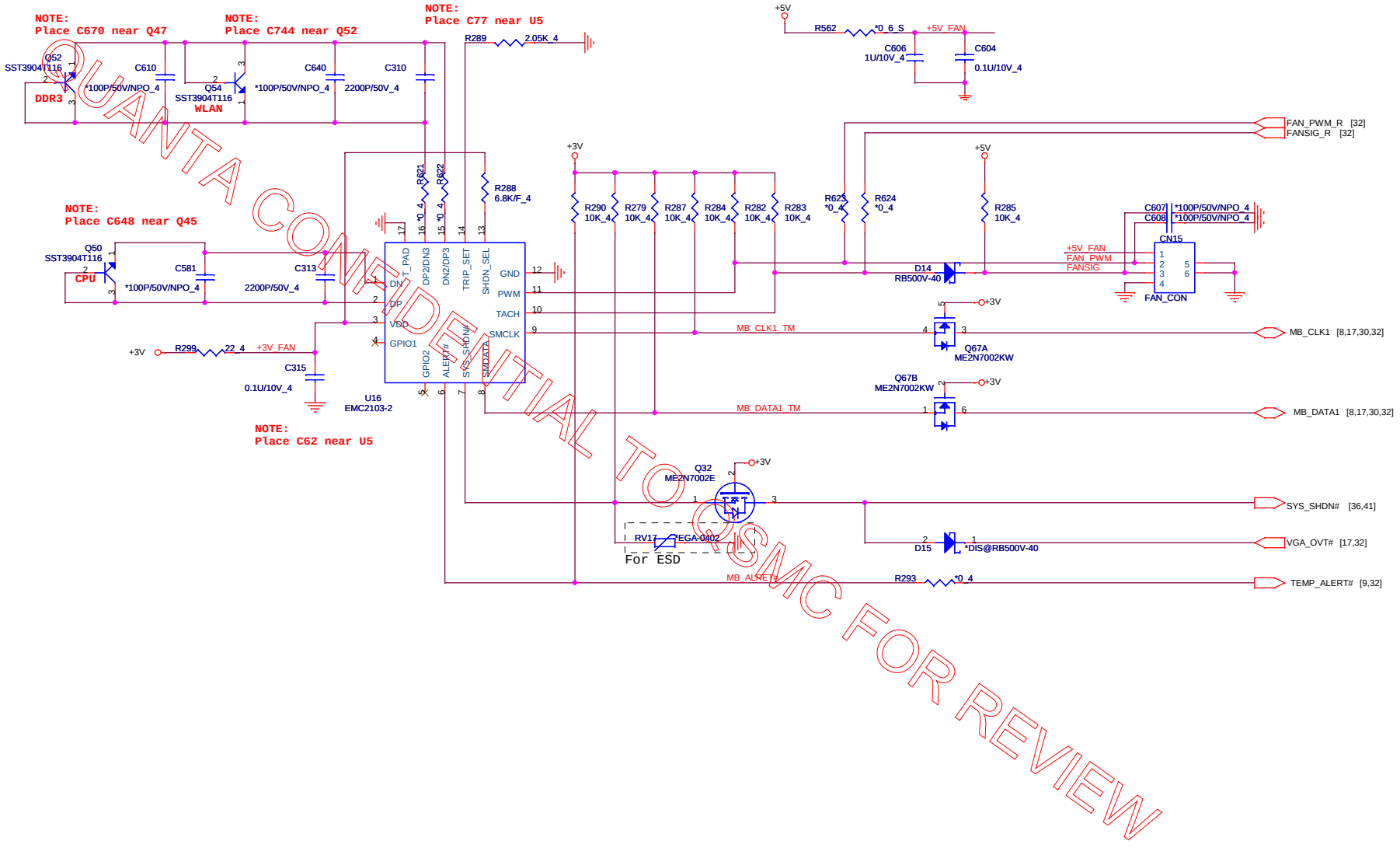
DC-IN Board



PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: USB3.0 *1	Rev: 1A
Date: Wednesday, December 07, 2011	Sheet 28 of 45	

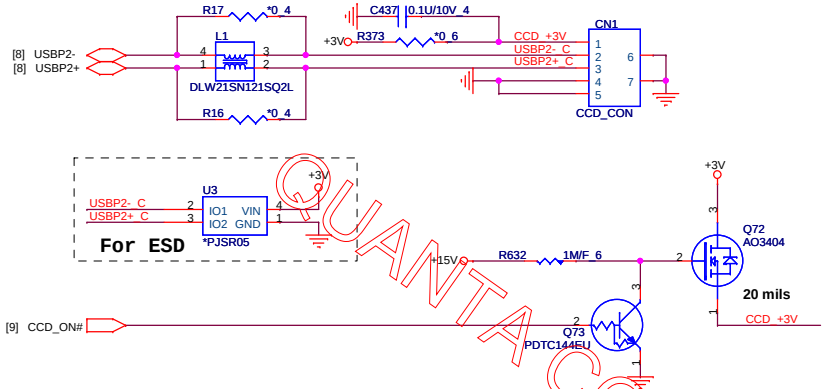
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,30,31,32,33,34,37,38,41,42,43] +3V
[7,10,21,22,25,26,30,33,34] +5V

FAN CONTROL

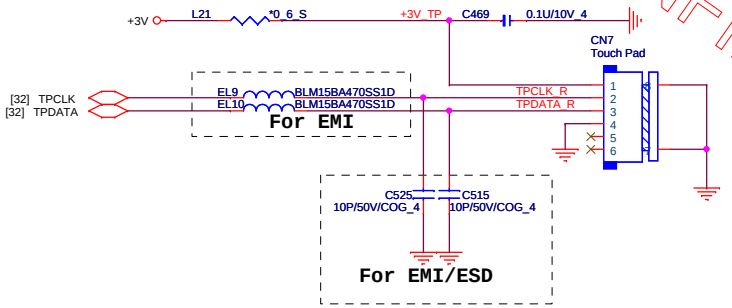


PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: FAN /THERMAL	Rev: 1A
Date: Wednesday, December 07, 2011	Sheet 29 of 45	

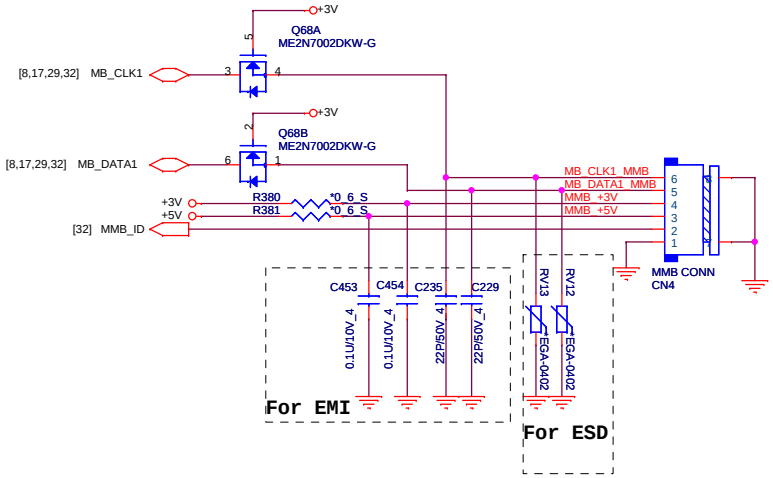
CCD BOARD



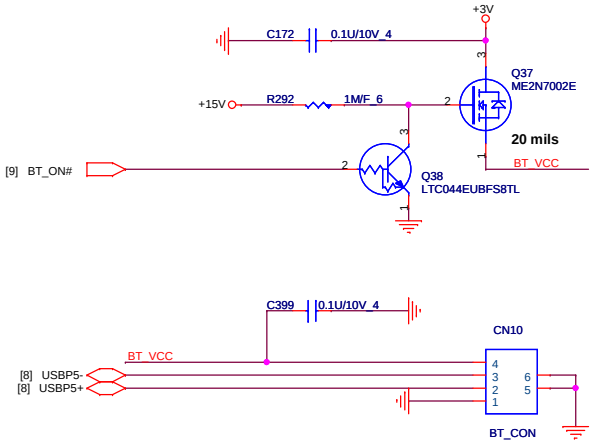
Touch pad



MMB



BLUETOOTH

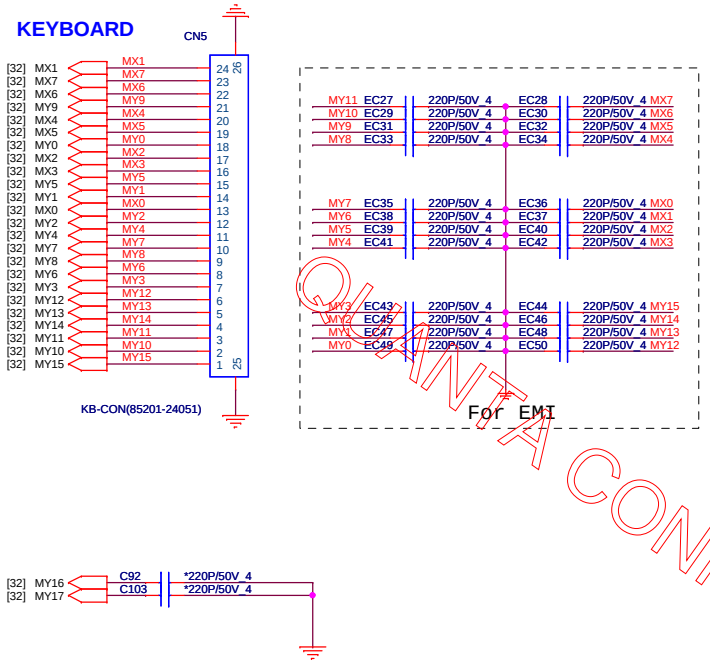


PROJECT : LZ2A
Quanta Computer Inc.

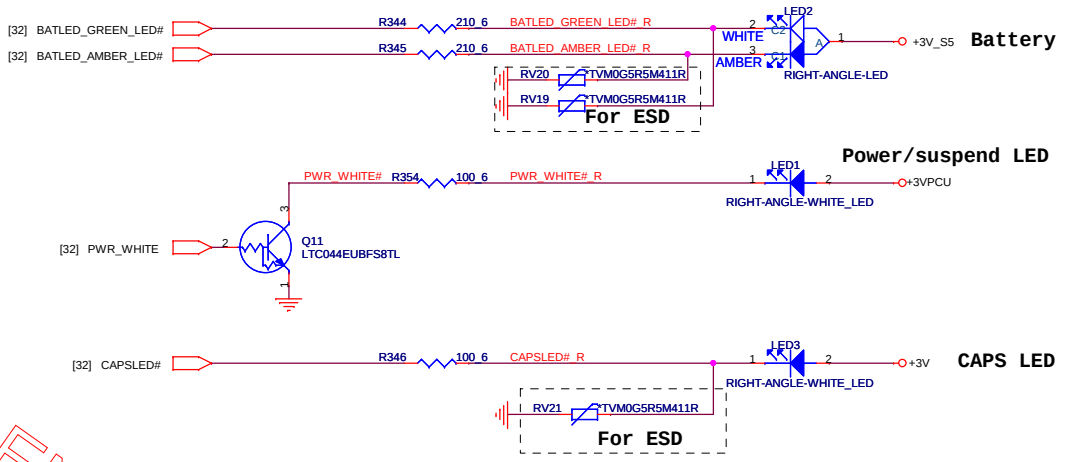
Size	Document Number	Rev
Custom	CCD/TP/BT/MMB	1A

Date: Wednesday, December 07, 2011 Sheet 30 of 45

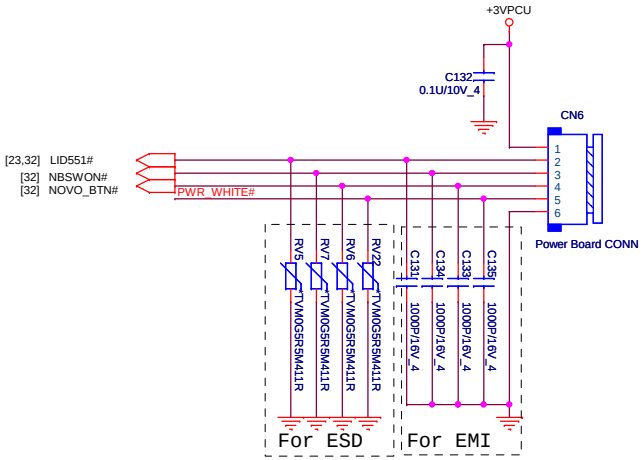
KEYBOARD



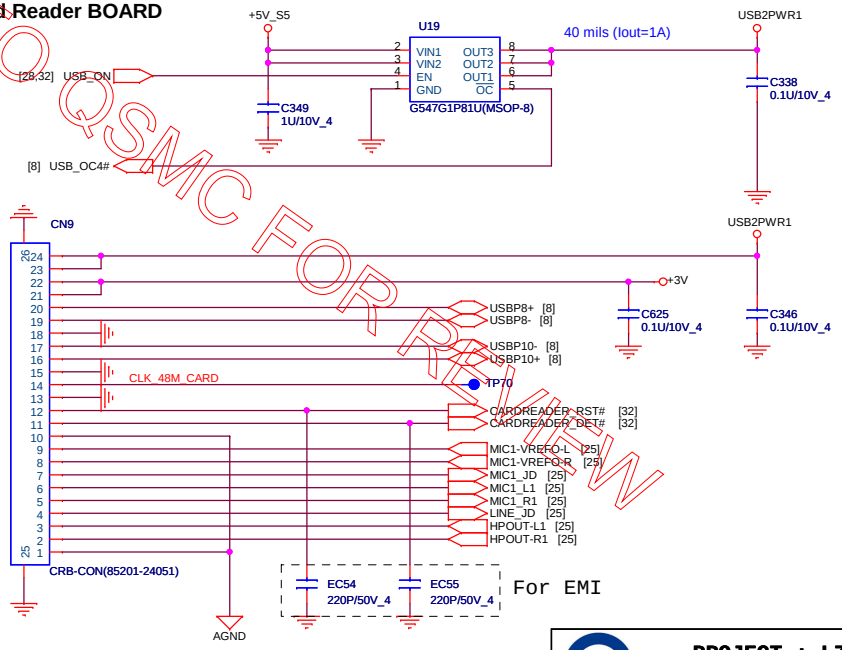
LED



POWER BOARD



Card Reader BOARD



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/PB/LED/CRB	1A

Date: Wednesday, December 07, 2011 Sheet 31 of 45

IT8518 IT8519

U10 IT8518

LPC
GPIO
PS/2
SM BUS
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK

Board ID

DIS =>R116
UMA=>R115

POWER SWITCH/ NOVO BUTTON

4Mbit (512K Byte), SPI

Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13

W25X40BVSSIG

For EMI

FOR DEEP S3

Project	PU/PD
Z380(LZ1)-INTEL	PU
Z480(LZ2)-INTEL	PU
Z485(LZ2)-AMD	PU
Z580(LZ3)-INTEL	PD
Z585(LZ3)-AMD	PD

PROJECT : LZ2A
Quanta Computer Inc.

Size: Custom | Document Number: KBC IT8518 | Rev: 1A
Date: Wednesday, December 07, 2011 | Sheet 32 of 45

Screw for ME

SPAD1 *SPAD-Z480-1
SPAD3 *SPAD-Z480-1
SPAD4 *SPAD-Z480-2
SPAD2 *SPAD-Z480-2

VGA
HOLE12 DIS@H-TC5_5BC4I3D3P2
HOLE13 H-TC5_5BC4I3D3P2

SMT NUT H=4/7mm

HOLE8 *HG-TC276BC315D106P2
HOLE10 *HG-TC276BC315D106P2
HOLE6 *HG-TC256BC315D106P2
HOLE11 *HG-TC276BC315D106P2

CPU BKT

HOLE4 *H-C86D86N
HOLE7 *C142D102N
HOLE3 *H-TC217BC256D118P2
HOLE14 *H-TC7IC3_7BC8D2_7P2
HOLE9 *H-C87D87N
HOLE5 *H-O316X276ID91P2
HOLE2 *H-O316X276ID91P2
HOLE1 *H-TC6_3IC3_7BC8D2_7P2

For ESD

+0.85V +1.8V SC23 SC24 *0.1U/10V_4
+1.05V_GFX_PCIE +1.05V_PCH SC31 SC32 *0.1U/10V_4
+0.85V +1.5V_CPU SC11 SC13 SC12 SC27 SC26 *0.1U/10V_4
+5V_S5 SC42 *0.1U/10V_4
+5V_S5 SC41 *0.1U/10V_4
+1.5V_SUS +1.5V_CPU SC29 SC28 *0.1U/10V_4
+1.5V_SUS VIN SC40 SC39 0.1U/25V_4
+3V +5V SC33 SC30 0.1U/10V_4
+VCC_CORE VIN SC9 SC46 0.1U/25V_4
+VCC_GFX SC15 SC18 *0.1U/10V_4
+5V SC38 SC25 SC37 0.1U/10V_4
+1.05V_GFX_PCIE GFX_CORE SC4 *0.1U/10V_4
+VCC_GFX SC17 SC16 SC14 SC20 SC19 SC21 SC49 SC22 SC50 SC47 SC48 SC6 SC5 *0.1U/10V_4
+1.05V_PCH
+1.05V_PCH
+1.05V_GFX_PCIE
+VCC_CORE SC8 SC10 *0.1U/10V_4
+1.5V_GPU SC2 SC43 SC3 *0.1U/10V_4
+1.5V_GPU SC7 SC45 *0.1U/10V_4
+1.5V_GPU SC44 SC1 *0.1U/10V_4
+1.5V_SUS SC35 SC34 SC36 *0.1U/10V_4

For EMI

VIN EC6 EC20 EC12 EC25 EC1 EC18 EC2 EC21 EC5 EC3 EC16 0.1U/25V_4
LANVCC EC11 0.1U/10V_4
VBATT EC22 0.1U/25V_4
+1.5V_SUS FC2 3.3p/16V/NP0_4
+1.5V_SUS FC1 3.3p/16V/NP0_4
+1.5V_WLAN FC5 47P/50V/NPO_4
+3.3V_WLAN FC3 47P/50V/NPO_4
+5V EC51 EC52 0.1U/10V_4 *0.1U/10V_4

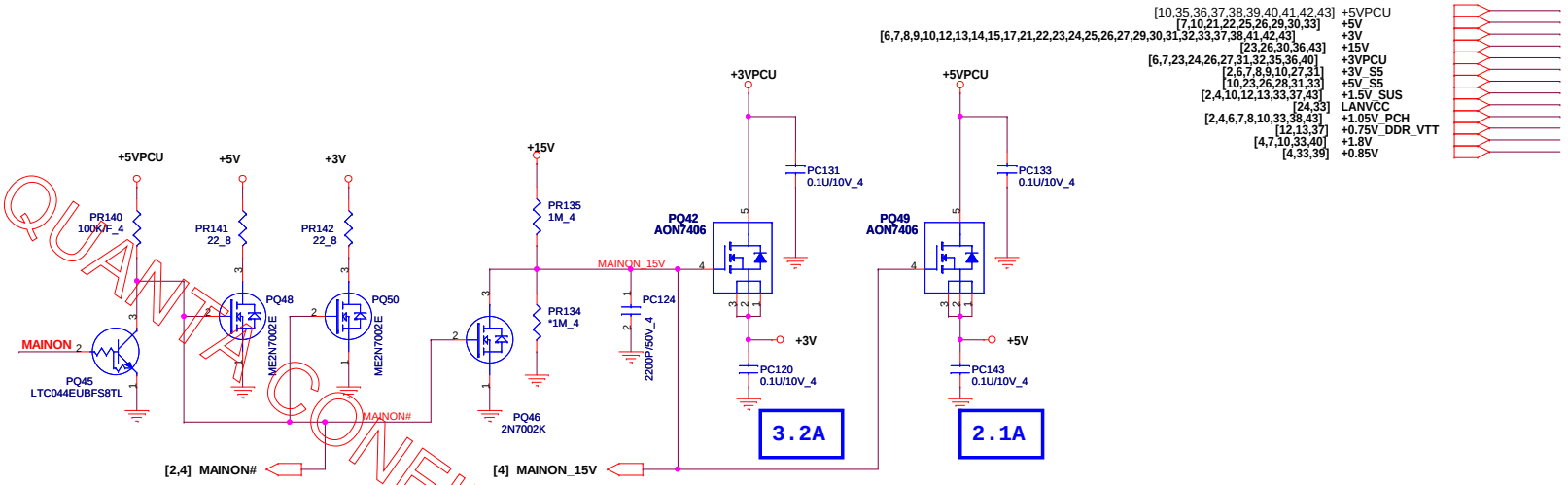
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
B	HOLD/SKEW/ESD/EMI	1A

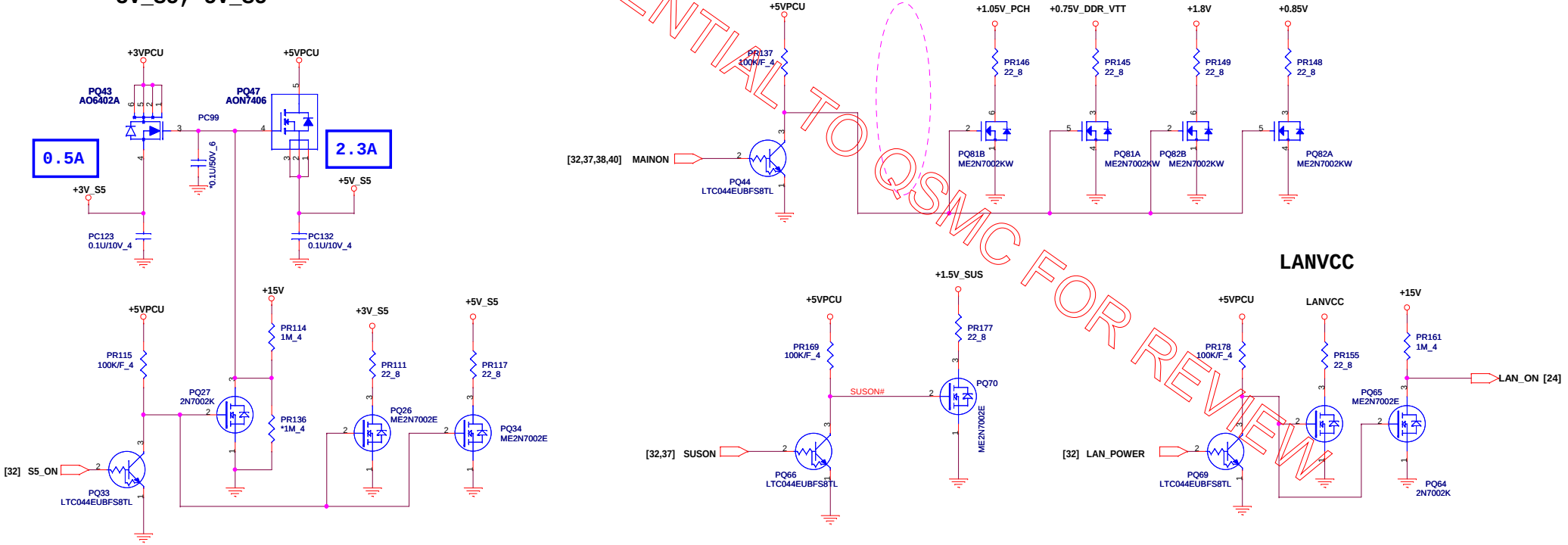
Date: Wednesday, December 07, 2011 Sheet 33 of 45

DISCHARGE

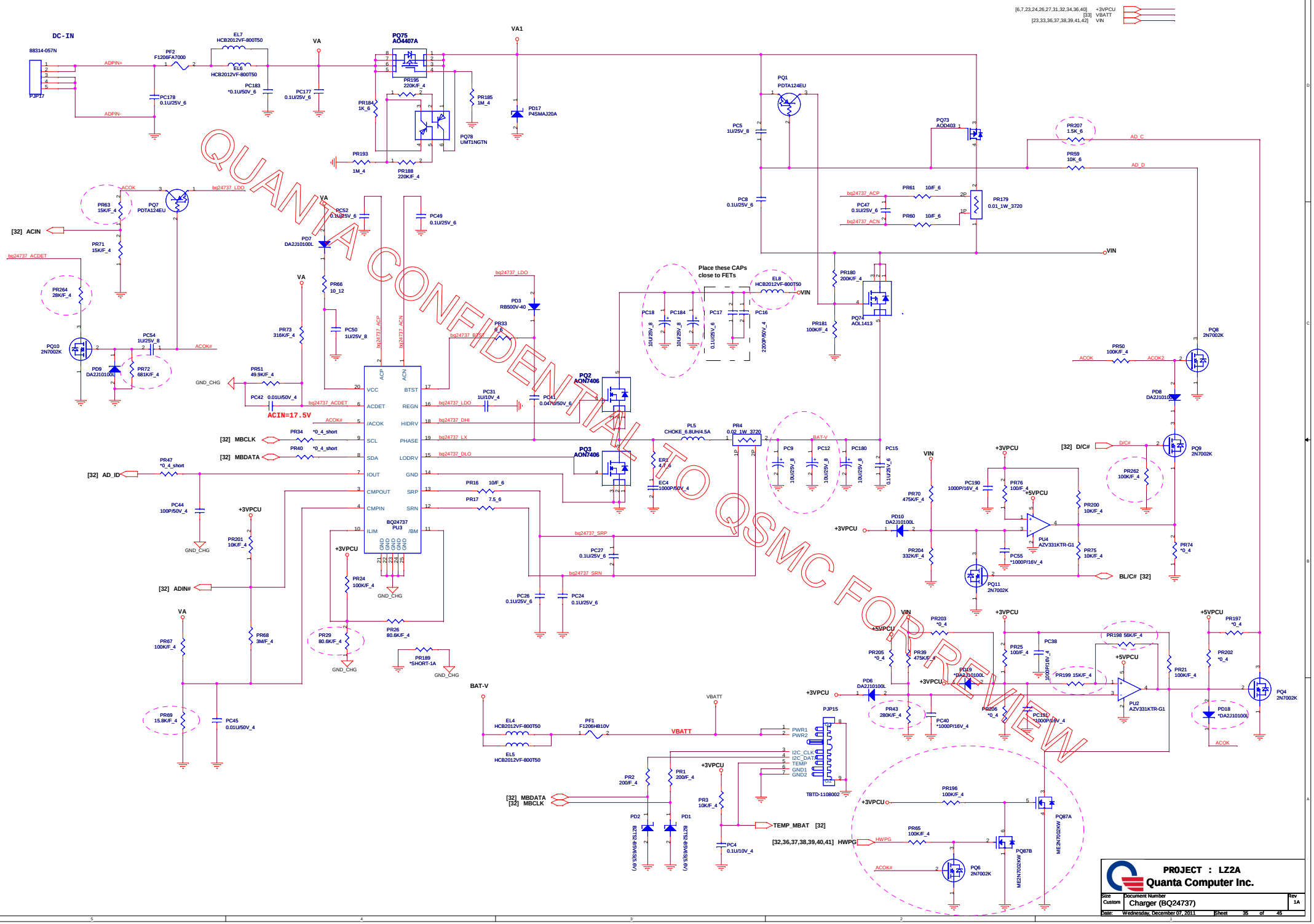
+3V, +5V



3V_S5, 5V_S5



PROJECT : LZ2A Quanta Computer Inc.		
Size	Document Number Discharge	Rev
Date: Wednesday, December 07, 2011	Sheet 34 of 45	



[23,33,35,37,38,39,41,42] VIN
5V_AL
3V_AL
REF
[10,34,35,37,38,39,40,41,42,43] +5VPCU
[23,26,30,34,43] +15V
[6,7,23,24,26,27,31,32,34,35,40] +3VPCU

+5VPCU
Fs=400K
TDC :6A
Imax :8A
OCP :10A

+3VPCU
Fs=500K
TDC :6A
Imax :8A
OCP :10A

Place these CAPs close to FETs

Place these CAPs close to FETs

PU9 TPS51123ARGER

PQ51 AON7702
PQ52 AON7406
PQ53 AON7406
PQ54 AON7702

PL11 2.2UH-PCMC063T-2R2MN
PL10 2.2UH-PCMC063T-2R2MN

PD21 BAT54S-7-F
PD20 BAT54S-7-F

[29,41] SYS_SHDN#

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	3V/5V (TPS51123ARGER)	

Date: Wednesday, December 07, 2011 Sheet 36 of 45

[12,13,34] +0.75V_DDR_VTT
[23,33,35,36,38,39,41,42] VIN
[2,4,10,12,13,33,34,43] +1.5V_SUS

+0.75V_DDR_VTT
TDC : 1A

+0.75V_DDR_VTT

PC165 *0.1U/10V_4
PC163 10U/6.3V_6
PC164 10U/6.3V_6

+1.5V_SUS

PC159 10U/6.3V_6

PR165 100K/F_4

VTTGND VTT
VTTSNS VLDOIN
GND VBST
MODE DRVH
VREF LL
DRVL
REFIN PGND
VDDQSNS
VTTREF V5IN
S3
S5
PGOOD
TRIP
GND GND GND GND GND

PU6
TPS51216

DDR_VBST
DRVH
DDR_LL
DRVL
DDR_V5IN
DDR_VREF
DDR_REFIN
DDR_VDDQS
DDR_VTTREF_R
DDR_TRIP

PR157 2.2_6
PC161 0.1U/25V_6

PQ68
SK850305KL

PQ67
SK8603020L

Place these CAPs close to FETs

VIN

PC173 0.1U/25V_6
PC162 2200P/50V_4
PC153 10U/25V_8
PC158 10U/25V_8

PL2
1.0uH/PCMC104T-1R0MN

+1.5V_SUS

ER9 *4.7_6
EC17 *1000P/50V_4

PC168 330U/2.5V/ELEC_6344
PC167 DIS@330U/2.5V/ELEC_6344
PC148 *330U/2V/ESR9_7343
PC171 10U/6.3V_6
PC172 0.1U/10V_4

+1.5V_SUS
Fs=300K
TDC :16A
Imax :19A
OCP :22A

R1
R2

PR151 10K/F_4
PR150 53.6K/F_4

PC150 0.1U/10V_4
PC149 0.01U/50V_4

Vo=1.8*R2/(R1+R2)

[4,12,13] SMDDR_VREF
PR153 0_4
PC154 0.22U/10V_4

PR152 *0_6_short
PC156 1U/10V_4
+5VPCU

PR167 10K/F_4
+3V

PR166 *0_4_short
PD15 RB500V-40
PD14 RB500V-40
HWPG [32,35,36,38,39,40,41]
DRAMPWRGD [32]

PR164 71.5K/F_4

[32] EC_SLP_S4#
[32,34,38,40] MAINON
PR143 *0_4
EC_SLP_S4#
PR163 100K_4
PD16 DA2J10100L
PC170 0.1U/10V_4

[32,34] SUSON
PR162 0_4
PR144 *0_4
EC_SLP_S4#
PC169 *0.1U/10V_4

PROJECT : LZ2A
Quanta Computer Inc.

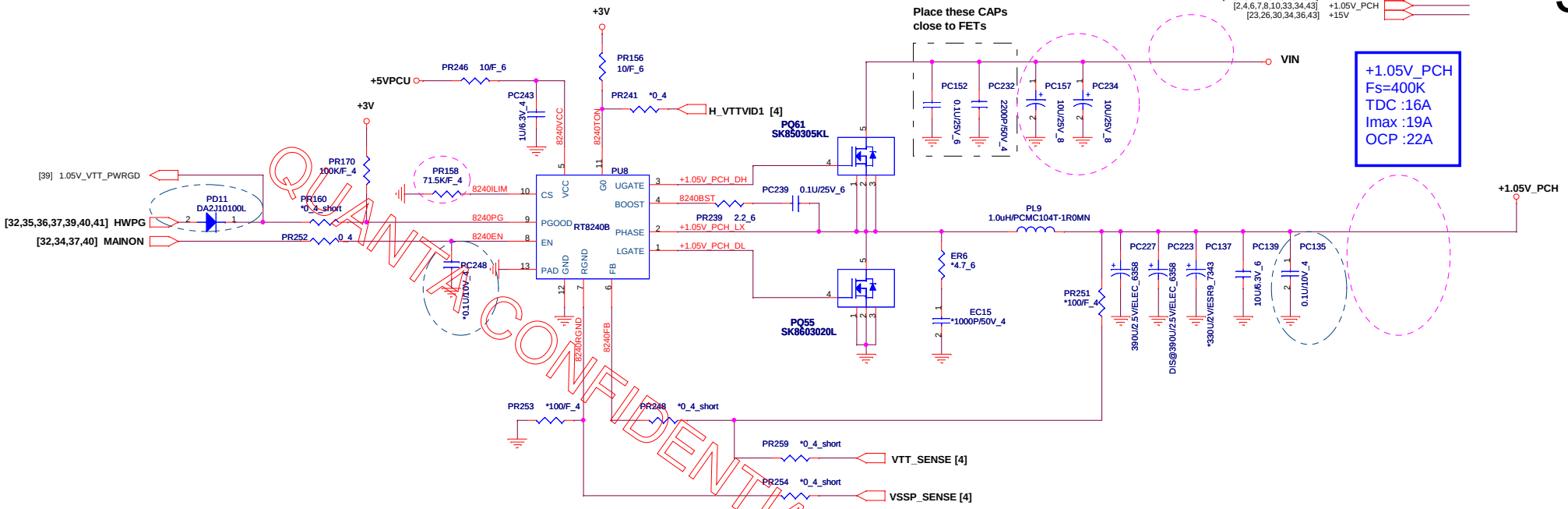
Size	Document Number	Rev
	DDR3/0.75V (TPS51216)	

Date: Wednesday, December 07, 2011 Sheet 37 of 45

[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,41,42,43] +3V
[10,34,35,36,37,39,40,41,42,43] +5VPCU
[23,33,35,36,37,39,41,42] VIN
[2,4,6,7,8,10,33,34,43] +1.05V_PCH
[23,26,30,34,36,43] +15V

+1.05V_PCH
Fs=400K
TDC :16A
Imax :19A
OCP :22A

Place these CAPs close to FETs

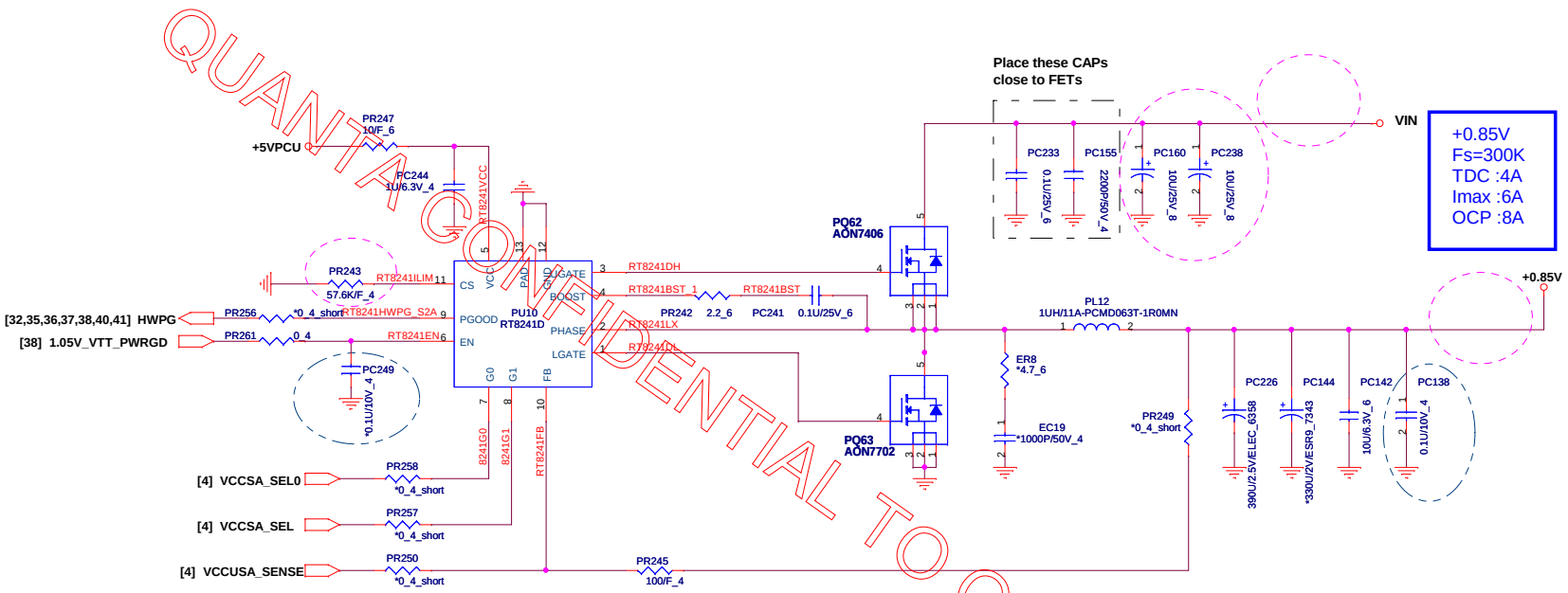


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V_PCH	

Date: Wednesday, December 07, 2011 Sheet 38 of 45

[10,34,35,36,37,38,40,41,42,43] +5VPCU
[23,33,35,36,37,38,41,42] VIN
[4,33,34] +0.85V



G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

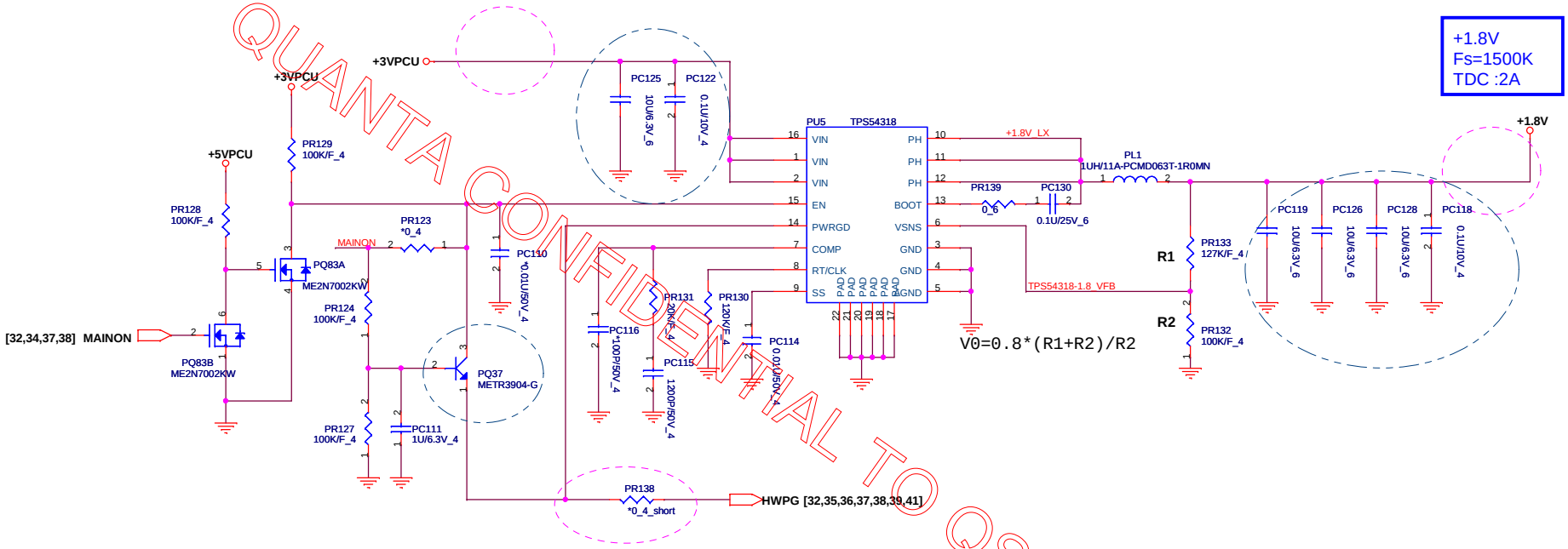
default 0.9V

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	VCCSA (RT8241A)	

Date: Wednesday, December 07, 2011 Sheet 39 of 45

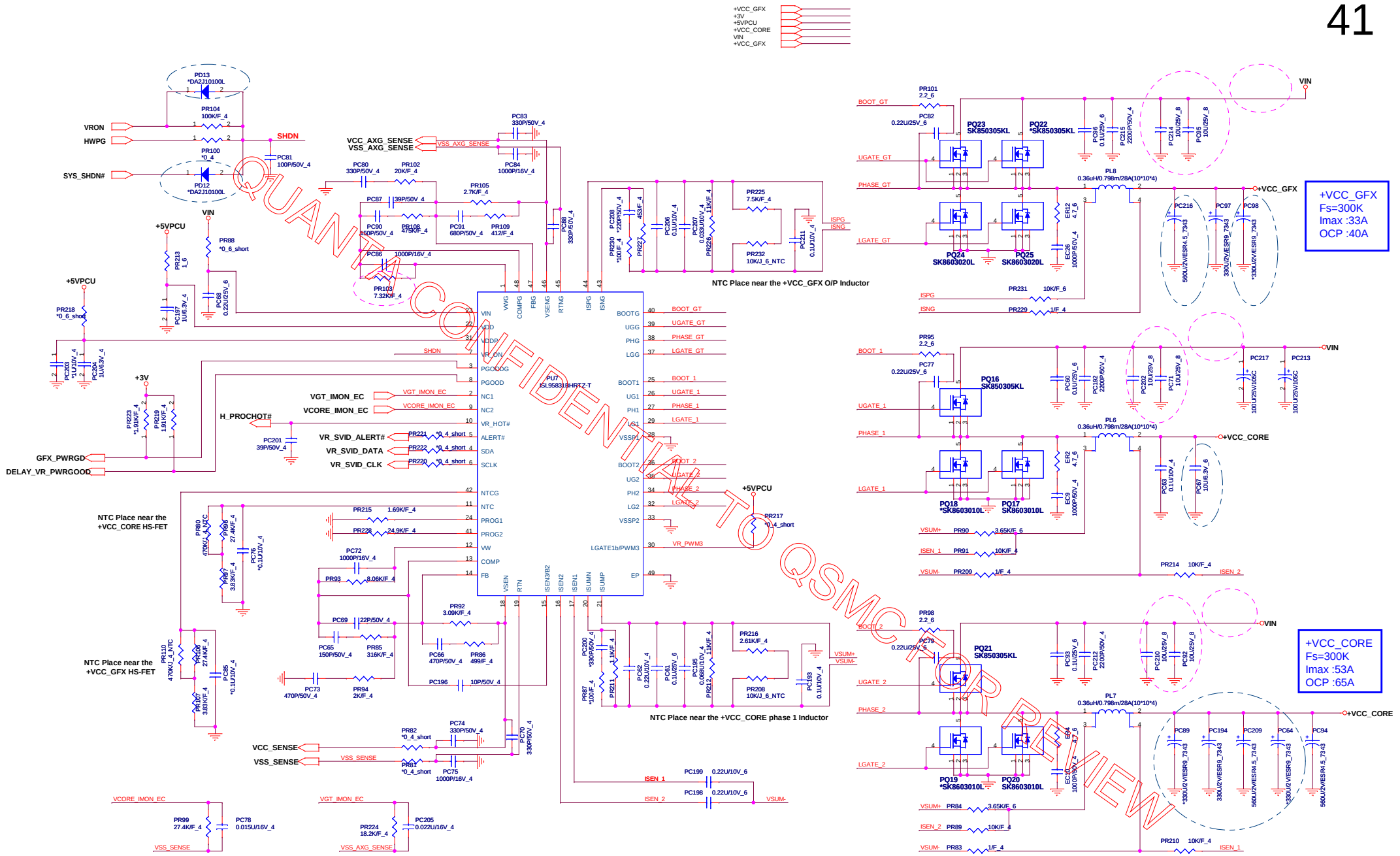
[10,34,35,36,37,38,39,41,42,43] +5VPCU
[6,7,23,24,26,27,31,32,34,35,36] +3VPCU
[4,7,10,33,34] +1.8V



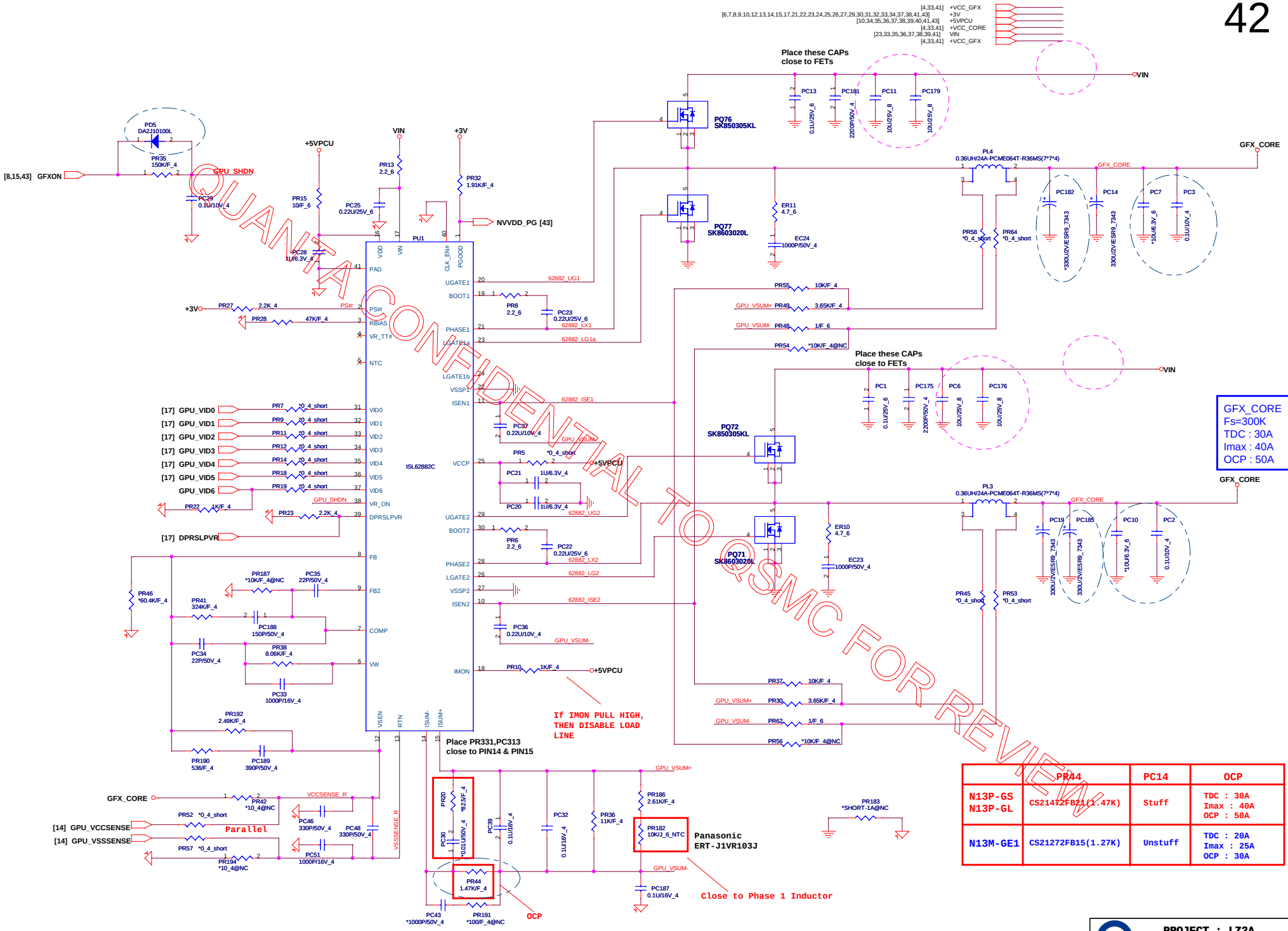
PROJECT : LZ2A
Quanta Computer Inc.

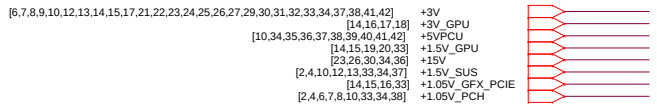
Size	Document Number	Rev
	1.8V (TPS54318)	

Date: Wednesday, December 07, 2011 Sheet 40 of 45



PROJECT : LZ2A			
Quanta Computer Inc.			
Size	Document Number		Rev
	CPU(ISL95831)IMVP2+1		
Date: Wednesday, December 07, 2011	Sheet 41 of 45		


[4,33,41] +VCC_GFX
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,43] +3V
[10,34,35,36,37,38,39,40,41,43] +5VPCU
[4,33,41] +VCC_CORE
[23,33,35,36,37,38,39,41] VIN
[4,33,41] +VCC_GFX
Place these CAPs close to FETs
VIN
GFX_CORE
PQ76 SK850305KL
PQ77 SK8603020L
PQ72 SK850305KL
PQ71 SK8603020L
PL4 0.36UH/24A-PCME064T-R36MS(7*7*4)
PL3 0.36UH/24A-PCME064T-R36MS(7*7*4)
[8,15,43] GFXON
GPU_SHDN
+5VPCU
+3V
NVVDD_PG [43]
PU1
ISL62882C
PAD
VDD
VIN
CLK_EN#
PGOOD
UGATE1
BOOT1
PHASE1
LGATE1a
LGATE1b
VSSP1
ISEN1
VCCP
UGATE2
BOOT2
PHASE2
LGATE2
VSSP2
ISEN2
IMON
PSI#
RBIAS
VR_TT#
NTC
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
FB
FB2
COMP
VW
VSEN
RTN
ISUM-
ISUM+
62882_UG1
62882_LX1
62882_LG1a
62882_ISE1
62882_UG2
62882_LX2
62882_LG2
62882_ISE2
GPU_VSUM+
GPU_VSUM-
[17] GPU_VID0
[17] GPU_VID1
[17] GPU_VID2
[17] GPU_VID3
[17] GPU_VID4
[17] GPU_VID5
GPU_VID6
[17] DPRSLPVR
If IMON PULL HIGH, THEN DISABLE LOAD LINE
Place PR331,PC313 close to PIN14 & PIN15
Parallel
[14] GPU_VCCSENSE
[14] GPU_VSSSENSE
VCCSENSE_R
VSSSENSE_R
Panasonic ERT-J1VR103J
Close to Phase 1 Inductor
OCP
GFX_CORE Fs=300K TDC : 30A Imax : 40A OCP : 50A
PR44 | PC14 | OCP
N13P-GS N13P-GL | CS21472FB21(1.47K) | Stuff | TDC : 30A Imax : 40A OCP : 50A
N13M-GE1 | CS21272FB15(1.27K) | Unstuff | TDC : 20A Imax : 25A OCP : 30A
QUANTA CONFIDENTIAL TO QSMC FOR REVIEW
PROJECT : LZ2A
Quanta Computer Inc.
Size
Document Number
DGPU (ISL62882C) 2 Phase
Rev
Date: Wednesday, December 07, 2011
Sheet 42 of 45



+3V_GPU
+3V
R109 EV@10K/F_4
R141 EV@10K/F_4
GFXPG
GFXPG [9,14]
Q16 METR3904-G
+1.5V_GPU R120 EV@10K/F_4 Q18 METR3904-G
*EV@1000P/50V_4@NC C147
+1.05V_GFX_PCIE R107 EV@10K/F_4 Q17 METR3904-G
*EV@1000P/50V_4@NC C139

5.5A
+1.5V_GPU
+1.5V_SUS
PQ40 DIS@SK8603020L
PC112 DIS@10U/6.3V_6
PC117 DIS@10U/6.3V_6
PC107 DIS@10U/6.3V_6
PC106 DIS@10U/6.3V_6
PC101 *330U/2.5V/9m_3528
PC102 *0.1U/10V_4
PR79 DIS@22_8
PR77 DIS@1M_4
+5VPCU
PQ85A ME2N7002KW
PR78 DIS@100K/F_4
PQ85B ME2N7002KW
PC100 DIS@0.022U/25V/X7R_4
[15] +1.5V_GPU_EN
PQ14 DIS@ME2N7002E
R688 100K_4

1.4A
+3V_GPU
+15V
+3V
PQ15 DIS@AO6402A
+3V_GPU
+3V_GPU [14,16,17,18]
PR113 DIS@22_8
PR125 DIS@1M_4
PC59 DIS@10U/6.3V_6
PC57 DIS@10U/6.3V_6
PC58 *0.1U/10V_4
PQ28 DIS@ME2N7002E
+5VPCU
PR118 DIS@100K/F_4
PQ84A 2N7002DW
PC56 *2200P/50V_4
[8,15,42] GFXON
GFXON
PQ84B 2N7002DW
+3V_NVMISC_EN [17,18]

3.9A
+1.05V_PCH
PQ41 DIS@AON7406
+1.05V_GFX_PCIE
PC121 DIS@10U/6.3V_6
PC127 DIS@10U/6.3V_6
PC104 DIS@10U/6.3V_6
PC105 DIS@10U/6.3V_6
PC108 *330U/2.5V/9m_3528
PC113 *DIS@0.1U/10V_4
+15V
PR116 DIS@22_8
PR265 DIS@1M_4
+5VPCU
PQ32 DIS@ME2N7002E
PR266 DIS@100K/F_4
PQ86A ME2N7002KW
PC109 *0.022U/25V_4
[42] NVVDD_PG
NVVDD_PG
PQ86B ME2N7002KW

PROJECT : LZ2A			
Quanta Computer Inc.			
Size	Document Number GPU		Rev
Date: Wednesday, December 07, 2011	Sheet 43 of 45		

LZ2 / Z480 Chief River Schematic EC Tracking Record B (for SDV --> SIV,B)OCT. 07, 2011

EC #	Page	CMVC #	Description	Date	Part Affected
B-00	15		To change D3 pin 2's connection from NVVDD_PG to GFXON for Deep_S3.	0921	
B-01	43		Add PR122 and D26 for +1.05V_GFX_PCIE discharge.	0921	
B-02	17		To change D5 pin1's connection from ACIN to AC_PRESENT for GPU Enable.	0922	
B-03	37		Change PR163 from 0R to 100K form Deep_S3	0922	
B-04	37		Add PD16 1SS355 for Deep_S3	0922	
B-05	32		Add Net EC_DRAMRST_GATE to connect U10's pin 106 and R614.	0925	
B-06	6		Add R615, Q55, Q56, D28 , D29 and Net DPWROK for Deep_S3.	0925	
B-07	10		Add Q57, Q58 and Net SLP_SUS# for Deep_S3.	0925	
B-08	32		Change U10 pin 76's net name from AB_CHARGING to SLP_SUS# for Deep_S3.	0925	
B-09	32		Change U10 pin 83's net name from RF_SW# to PCIE_WAKE#for Deep_S3.	0925	
B-10	32		Change U10 pin 100's connection from PCH to Net GFXON for Deep_S3.	1005	

LZ2 / Z480 Chief River Schematic EC Tracking Record C (for SDV --> SIV,C)Nov. 27, 2011

EC #	Page	CMVC #	Description	Date	Part Affected
C-00	24		Change LAN trandformer from dual mode to signal mode.	1126	
C-01	24		Change R295 and R296 to 0R.	1126	
C-02	24		Add D30,D31,D32,D33 for surge.	1126	
C-03	30		Net "CCD ON#" change connection from EC to PCH.	1120	
C-04	30		Change Bluetooth connection from USB PORT 5 to USB PORT 11 of PCH.	1118	
C-05	23		Add R635,636 fro brightness control.	1126	
C-06					
C-07					
C-08					
C-09					
C-10					

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	EC Tracking Record	

Date: Wednesday, December 07, 2011 Sheet 45 of 45