ITM300 GPRS Data Module
Radio Subsystem Description

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1 INTRODUCTION

This document describes the functionality of the radio subsystem of the ITM300 family of GSM/GPRS Voice/Data Modules.

1.1 System Overview

ITM300 is based upon Analog Devices' AD20msp430 baseband chipset and Silicon Labs 'Aero I' RF transceiver IC. Specifically, the devices used are:

- Analog Devices AD6527 baseband processor
- Analog Devices AD6537B mixed signal processor
- Silicon Labs Si4205 radio transceiver

ITM300 uses TTPCom's protocol stack, layer 1, DSP and data services software.

ITM300 is manufactured as a single sided assembly printed circuit board, with a 60 way base band / analogue interface connector and an RF interface connector. The PCB is electrically screened.

2 RADIO SUB SYSTEM

2.1 System Design

The radio system design has been performed to ensure compliance with 3GPP 45-005, BS EN 301-489-1, BS-EN 301-511 and FCC Parts 15b, 22, 24. The system design addresses requirements for spurious emissions.

2.2 Operating bands

The radio supports operation in the following frequency bands with channel spacing 200kHz, GMSK modulated:

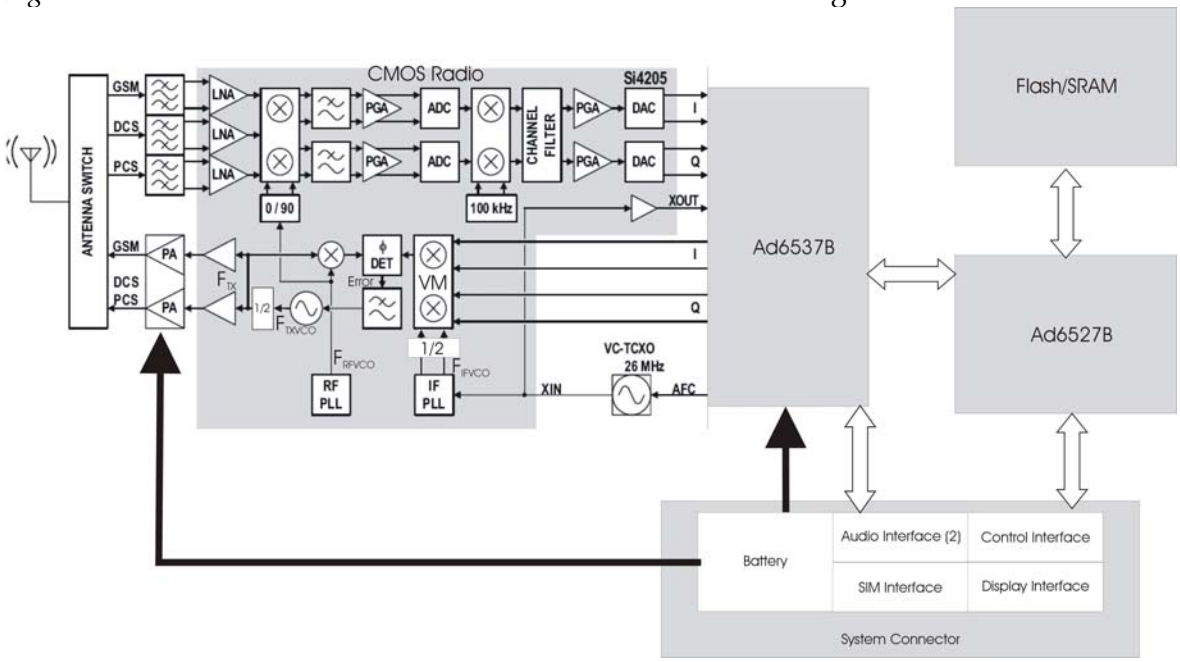
- GSM850 (uplink 824 - 849MHz, downlink 870 - 894MHz)
- E-GSM (uplink 880 - 915MHz, downlink 925 - 960MHz)
- GSM1800 (uplink 1710 - 1785MHz, downlink 1805 - 1880MHz);
- PCS1900 (uplink 1850 - 1910MHz, downlink 1930 - 1990MHz).

2.3 Transmit power levels

GSM 850 - Power class 4 with a maximum RF transmit power of 2W
E-GSM - Power class 4 with a maximum RF transmit power of 2W
GSM 1800 - Power class 1 with a maximum RF transmit power of 1W
PCS1900 - power class 1 with a maximum RF transmit power of 1W

2.4 System Architecture

Figure 1 below shows the overall architecture of the ITM300 design.



2.5 System Clock

The system clock is derived from a Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO). The frequency control loop is implemented in the baseband mixed signal processor, AD6537B, which adjusts the VCTCXO, as defined in 3GPP 45-010 Section 6.1.

2.6 Transmitter operation

Refer to Figure 1 for a block diagram of the transmitter.

The transmitter is formed using an 'Offset Phase-Locked Loop' (OPLL) architecture. It uses three Voltage Controlled Oscillators (VCO), two are inside Phase Locked Loops (PLL).

The Power Amplifier (PA) module has integral closed loop output power control.

From baseband to air interface, the following takes place:

The baseband 67kHz quadrature GMSK I & Q signals are mixed with an Intermediate Frequency (IF) in the Vector Modulator (VM). The IF is generated by the VCO in the 'IF PLL'. Its quadrature signal is divided by two to make the IF signal F_{TXIF}. The Vector Modulator uses these signals to generate the one of the comparison signals for the OPLL phase (Φ) detector.

The Φ detector error signal is output, through filtration, to the VCO 'TXVCO' tune line to make the signal F_{TXVCO}. This is followed by an optional divide-by-2 (for the GSM850 and EGSM900 bands), the output of which is identified as F_{TX}.

The signal F_{TX} goes on to the inputs of the Power amplifier.

F_{TX} is also fed back to be mixed with the signal F_{RFVCO}, generated by the VCO 'RFVCO' in the 'RF PLL'. This mixing process generates the second comparison signal for the phase detector, closing the OPLL loop.

2.7 Receiver operation

The ITM300 receiver utilises 3 balanced output RF filters, in a Superheterodyne configuration with an IF of 100kHz. It uses one VCO inside a PLL.

From air interface to Baseband, the following takes place:
The three differential receive band LNAs operate at the frequencies listed in the GSM modes, in Section 2.1. The differential outputs from the active band LNA are mixed with the quadrature signal 'F_{RFVCO}' generated at the 'RF PLL' to make an IF of 100kHz.

This quadrature signal is amplified and digitised. A 100kHz digital quadrature signal F_{RXIF} converts the IF signal to Baseband and it passes through IIR DSP filters.
The Baseband quadrature signal is amplified and converted back to analogue I & Q at the DACs.

2.8 Frequency plan

Intermediate RF frequencies are generated in the RF CMOS VLSI by the following RF blocks:

- RFVCO
- TXVCO
- IFVCO

The system clock is a Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO).

The frequency plan is shown below in tabular form.

2.8.1 System clock

Frequency (MHz)	Range (Hz)
26.0000	±390

2.8.2 RFVCO

Band & Mode	Min (MHz)	Max (MHz)
GSM850 Rx	1737.8	1787.8
EGSM900 Rx	1849.8	1919.8
DCS1800 Rx	1804.9	1879.9
PCS1900 Rx	1929.9	1989.9
GSM850 Tx	1272	1297
EGSM900 Tx	1279	1314
DCS1800 Tx	1327	1402
PCS1900 Tx	1423	1483

2.8.3 TXVCO

Band	Min (MHz)	Max (MHz)
GSM850	1648	1698
EGSM900	1760	1830
DCS1800	1710	1785
PCS1900	1850	1910

2.8.4 IFVCO

Band	Freq (MHz)
GSM850	896
EGSM900 (880-895MHz)	798
EGSM900 (895-900MHz)	790
EGSM900 (900-915MHz)	798
DCS1800	766
PCS1900	854

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