



WPS54G Operation Principal

WPS54G

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DATE	VER.	CHANGE HISTORY
03/27/03	0.1	New Draft
03/04/04	0.2	Power consumption and modify some register
03/06/03	0.3	LED modify
03/06/09	0.4	Parallel modify
03/06/09	0.5	Modify

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1. INTRODUCTION

The WPS54G project is to develop a faster printer, which with 802.11g wireless module, USB2.0 and one parallel port by mini PCI interface, with one LAN port (10/100Mbps Ethernet).

This product uses Brecis MSP2007 microcontroller, which include two 10Mbps/100Mbps Ethernet MAC controllers and one mini PCI bus.



2. FUNCTION DESCRIPTION

This project uses the Brecis MSP2007 CPU the microcontroller and it offers a memory configuration of 4M bytes Flash and 256M bytes SDRAM.

This device supports 10/100 Base-TX LAN network interfaces using Davicom DM9161 as the PHY controller. The interface to the LAN network is through an RJ45 STP port.

A parallel port is available with I/O transmission by AT7601F.

USB print port uses NEC uPD720101 host controller, which fully compliant USB specification 2.0.

WE support one USB ports.

Using WLAN module using mini PCI wireless module.

There are eight LEDs to indicate the status of the device and LAN network connection: LAN has two, WLAN has one, and Parallel has two, USB has two.

This device derives its power from a 12V DC @ 1A power adapter which needs to be converted to 2.5V, 3.3V and 5V DC.

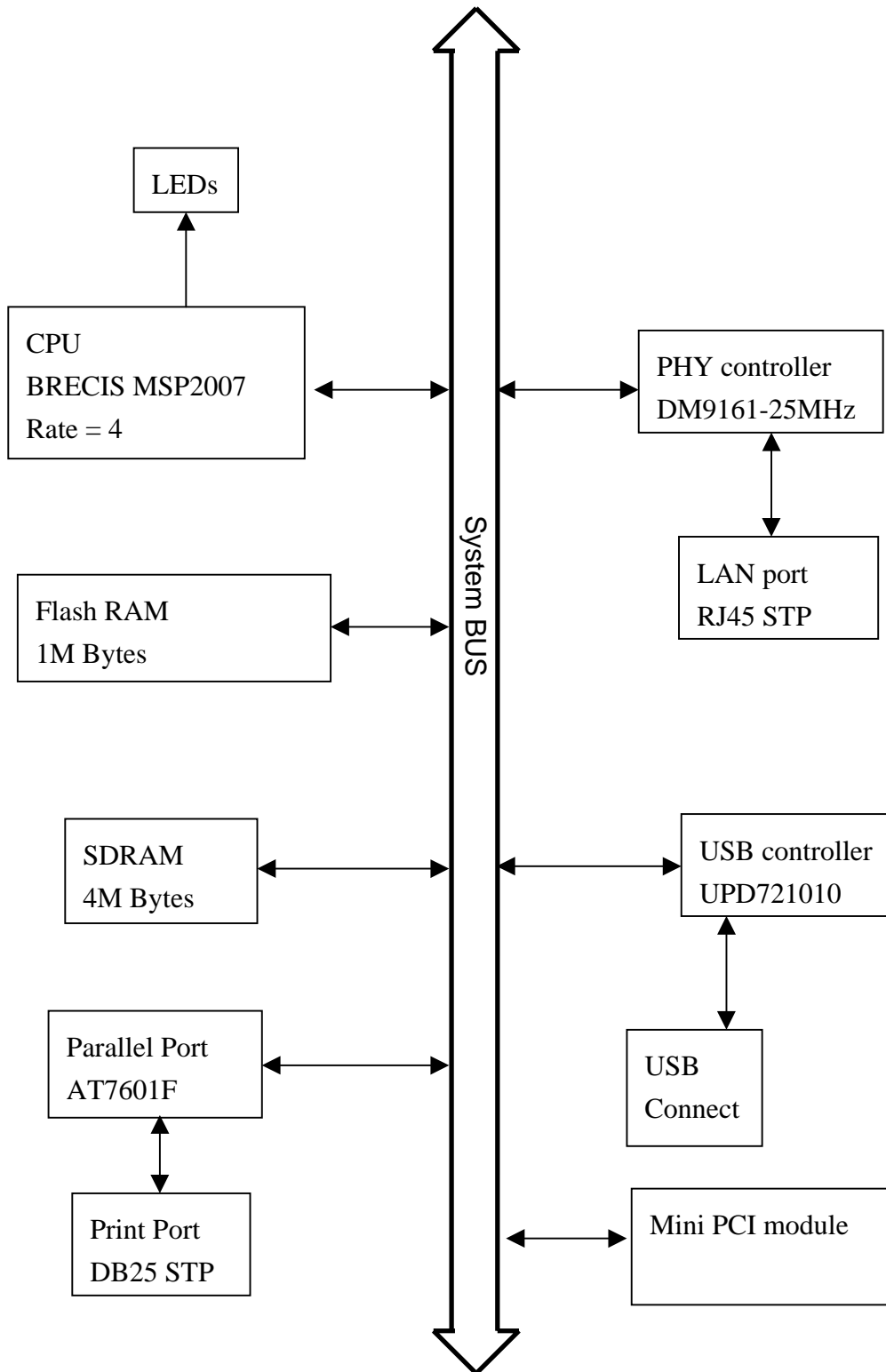
The functional requirements of the system are as follows:

1. CPU	Brecis MSP2007
2. CODE SIZE	1M bytes, HY29LV800TT-70
3. SDRAM	4M bytes, IS42S16100-7T
4. PHY	Davicom DM9161
5. USB	NEC uPD720101
6. LAN Port	One RJ45 STP Port
7. Printer Port	One parallel port
8. USB Port	One USB ports
9. Power Adapter	12V 1A
10. Debug Support	Can Connect to JTAG interface for S/W Development
11. EMC	FCC, CE , VCCI Class-B
12. PCB Spec.	105 x 135 x 30 mm, 4 layer.
13. Wireless module	Mini PCI module
14. Printer controller	AT7601F

LED:

LED	Color(s)	Activity	Desc.
Status	Orange	Blinking	Booting / System Self-Test / Firmware upgrade
		On	Error
		Off	No Ethernet Link
Ethernet	Green + Orange	Green On	Ethernet Link
		Green Blinking	Traffic
		Orange Blinking	Collision
		Off	No Wireless Link. (if wireless initiate failed)
Wireless-G	Green	Green On	802.11g module is functional.
		Green Blinking	Sending/Receiving
		Off	No printer is connected
Parallel Port	Green + Orange	Green On	Printer is connected.
		Green Blinking	Sending data
		Orange On	Problem on printer
		Off	No printer is connected
USB Port	Green + Orange	Green On	Printer is connected.
		Green Blinking	Sending data
		Orange On	Problem on printer
		Off	No printer is connected
Power	Green	On	Power on
		Off	Power Off

3. BLOCK DIAGRAM



4. MEMORY AND I/O MAPPING

4.1 Memory Mapping

There are three types of memory used in the system, Flash Memory, USB Memory and DRAM. Flash Memory is used for program, USB memory is used for USB transitions buffer and DRAM is used for system buffer.

- The address space reserved for the Flash Memory is shown in the table below:

Size	Logical address	Chip Selects	Bus Width
1M	0xBFC0_0000 ~ 0xBFCF_FFFF	-CS0	8 bits

INTEL 8-Bit Non-Muxed Mode

- The address space reserved for the USB Memory is shown in the table below:

Size	Logical address	PCI	Bus Width
			32

- The address space reserved for the Wireless module is shown in the table below:

Size	Logical address	PCI	Bus Width
			32

- The address space reserved for the Parallel port is shown in the table below:

Size	Logical address	I/O	Bus Width
4M	0xBE00_0000~0xBE3F_FFFF	-CS1	8

- The address space reserved for DRAM is shown in the table below:

Size	Logical address	SDRAM	Bus Width
4M	0x0000_0000 ~ 0x003F_FFFF	-SDR	32 bits

The access time of the SDRAM used is no slower than 7ns. F/W define range.

4.2 I/O Mapping

The I/O memory space includes printer access signals. The assigned I/O address is shown below:

COMPONENT	CHIP SELECT	BASE ADDRESS	INT	DRQ
FLASH	-ELB_CS0	0xBFC0_0000	--	--
Parallel port	-ELB_CS1	0xBF80_0000	INTD	--
Not used	-ELB_CS2	0xBF40_0000	--	--
Not used	-ELB_CS3	0xBF00_0000	--	--
Not used	-ELB_CS4	0xBEC0_0000	--	--
Not used	-ELB_CS5	0xBE80_0000	--	--
Not used	-ELB_CS6	0xBE40_0000	--	--
Not used	-ELB_CS7	0xBE00_0000	--	--

Note: 1. FLASH use -ELB_CS0

5. INTERRUPTS

The CPU provides 4 external interrupts: INT0, INT1, INT2, INT3

Source	Port	Pin	Active state
Wireless used	INT0/PCI_INTA	J17	Low active
USB used	INT1/PCI_INTB	K18	Low active
USB used	INT2/PCI_INTC	J16	Low active
Printer used	INT3/PCI_INTD	K17	Low active

6. PCI

PCI0: For Wireless Modules.

PCI1: no use.

PCI2: For USB.

PCI3: no use.

7. COMPONENT SELECT

	COMPONENT	PACKAGE
1. CPU	Brecis MSP2007	BGA-276
2. FLASH	HYNIX HY29LV800TT-70	TSOP-48
3. DRAM	ICSI IS42S16100-7T	TSOP-50
4. PHY Transceiver	DAVICOM DM9161	LQFP-48
5. USB controller	NEC uPD720101	LQFP-144
6. Wireless module	Module	Mini PCI
7. Phone Jack	RJ-45	Shielded, 90 Deg
8. Printer controller	AT7601F	PQFP-44

8. CRITICAL COMPONENT

The key components are shown below.

NAME	COMPONENT	APPROX. PRICE
CPU	Brecis MSP2007	
DRAM	ICSI IS42S16100-7T	
Flash ROM	HYNIX HY29LV800TT-70	
USB	NEC uPD720101	
PHY	DM9161	
Printer controller	AT7601F	
Wireless module	Mini PCI module	

9. DETAIL FUNCTION DESIGN

9.1 CPU

The MSP2007 belongs to a full family of Multi-Service Processors™ designed to meet the performance, QoS and security needs of communications equipment used within the customer premise. The MSP2007 is an ideal solution for wireless routers and access points. As shown below, it includes a powerful MIPS processor, two 10/100 Ethernet MACs, and a PCI interface.

The MSP2007 provides a new level of price/performance for wireless routers. Its unique systems architecture includes a 4.25 Gbps bus, 16KB Scratchpad, and intelligent context aware DMA engines. Integration of 802.11a, b, and g wireless LANs is easily facilitated through the PCI interface.

BRECIS provides a comprehensive software suite to support the MSP2007.

Reduced time-to-market is achieved through the BRECIS FastStart Program and third party relationships. Included with your FastStart Program are evaluation boards, software, application engineering support, training, and documentation that together accelerate the product development process. The FastStart program also includes support for Linux, VxWorks, or custom operating systems.

9.2 Program ROM

The code size reserved for the Flash ROM is 1Mbytes.

The address space reserved for the program ROM is shown in the table below:

Code Size	Flash	Address Range	Speed	Bus Width	CNFG
1M	HY29LV800TT-70	0xBFC0_0000 ~ 0xBFCF_FFFF	70ns	8	

Flash ROM Timing Calculation

9.3 System RAM

This device uses 1M * 16 bit SDRAMs.

The address space reserved for the system RAM is shown in the table below:

Size	SDRAM	Address Range	Speed	Bus Width
4M	IS42S16100	0x0000_0000 ~ 0x003F_FFFF	70ns	32

9.4 Detail Register Description

GPIO number	Pin number	Signal name	I/O interface	Function	Active state
-------------	------------	-------------	---------------	----------	--------------

GPIO_0	G2				
GPIO_1	H3				
GPIO_2	G1	Reserve			
GPIO_3	H2	Reserve			
GPIO_4	H1	Reserve			
GPIO_5	J3	Reserve			
GPIO_6	J2	Reserve			
GPIO_7	J1				
GPIO_8	U15				
GPIO_9	K1				
GPIO_10	K2				
GPIO_11	K3				
GPIO_12	L1				
GPIO_13	M1				
GPIO_14	L2				
GPIO_15	N3				
GPIO_16	L3				
GPIO_17	M2				
GPIO_18	N1				
GPIO_19	P1				
GPIO_20	M3				
GPIO_21	N2				
GPIO_22	T10				
GPIO_23	R9				
GPIO_24	R17				
GPIO_25	P16				
GPIO_26	R16				
GPIO_27	R11				
GPIO_28	V14				
GPIO_29	R18				
GPIO_30	N15				
GPIO_31	R15				
GPIO_32	T18				
GPIO_33	K17				
GPIO_34	J16				

GPIO_35	K18				
GPIO_36	J17				
GPIO_37	D8				
GPIO_38	D7				
GPIO_39	B7	PB_input	Input	Push bottom	Low
GPIO_40	C7	LEDSO	Output	Status LED Orange	High
GPIO_41	A5				
GPIO_42	B6	LEDWG	Output	Wireless LED Green	High
GPIO_43	A4	LEDPG	Output	Parallel LED Green	High
GPIO_44	C6	LEDPO	Output	Parallel LED Orange	High
GPIO_45	D6	LEDUG	Output	USB LED Green	High
GPIO_46	B5	LEDUO	Output	USB LED Orange	High
GPIO_47	A3	PHY_RST	Output	PHY reset	Low
GPIO_48	B4				
GPIO_49	C5	INIT_SIO	Output	ECP mode	High
GPIO_50	D5	PAL_RST	Output	Parallel port reset	High
GPIO_51	A2				
GPIO_52	B3				
GPIO_53	C4				
GPIO_54	B2				

9.5 LAN Function

The RDC R1610 microcontroller has an internal Ethernet MAC controller, which connects to an external PHY through the MII interface.

A LAN port is available using the Davicom DM9161 PHY.

COMPONENT	DESCRIPTION
Number of LAN Ports	One
Number of Uplink Port	None
Number of WAN Port	None
LAN Speed	10Base/100Base
Interface Type	10BaseT/100BaseTX

Connector Type	STP
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9.6 Printer port Control

The –CS1 (0xBE00_0000H-0xBE3F_FFFFH) of MSP2007 is used for accessing the Super I/O.

The super I/O (AT7601F) supports one 1284-compatible parallel port.

After the power on reset, the AT7601F enters the normal mode with all logical devices disabled. You must enter Configuration mode to setup AT7601F to enable the logical device. The configuration register of super I/O chip is shown below.

I/O ADDRESS	REGISTER
0xBE00_0404H	Index register
0xBE00_0405H	Data register

Super I/O Initialization

To program the configuration registers of the Super I/O chip, the following sequence must be followed:

```

; ***** *****
CLI                               ; Enter configuration mode *****
OUT  0xBE000404H,78H             ; Disable interrupts
                                   ; Write 78H data to index
                                   ; register twice
OUT  0xBE000405H,78H
STI                               ; Enable interrupts

; ***** *****
OUT  0xBE000404H,F0H             ; Configure the configuration registers *****
OUT  0xBE000405H,3FH             ; Point to CRF0
                                   ;
                                   ;
; ***** *****
OUT  0xBE000404H,AAH             ; Exit configuration mode *****
                                   ; Write AAH data to index register

```

The initialization value of configuration registers are shown below.

Register	Value	Description
CRF0	3FH	Select ECP and EPP mode
CRF1	31H	Select DRQ3 and IRQ7 for ECP

CRF2	00H	Enable DRQ and IRQ
CRF3	00H	Unlock Configuration Register

Name	AT7601F Spec.
Data	Base+000h
ECP-AFIFO	Base+000h
DSR	Base+001h
DCR	Base+002h
C-FIFO	Base+400h
ECP-DFIFO	Base+400h
T-FIFO	Base+400h
Cnfg-A	Base+400h
Cnfg-B	Base+401h
ECR	Base+402h

10. Power Consumption Estimate

	COMPONENT	TYP. CURRENT	MAX CURRENT
CPU (1.8V)	BRECIS MSP2007	566mA	833mA
CPU (3.3V)	BRECIS MSP2007	91mA	151mA
Flash (3.3V)	HY29LV800TT-70	15mA	30mA
DRAM (3.3V)	IS42S16100-7T	-	140mA
PHY (3.3V)	DM9161	-	88mA
USB (3.3V)	UPD720101	-	350mA
Parallel (3.3V)	AT7601F		300mA
Wireless module	Prims 3.0	-	350mA
Parallel (5V)	ATF16V8C-7		100mA
Printer Logic (5V)		20mA	100mA
1.8V	TOTAL CURRENT	-	833mA
3.3V	TOTAL CURRENT	-	1409mA
5V	TOTAL CURRENT	-	200mA

Calculate:

MSP2007(1.8V) typical 1.0W → 566mA, Maximum 1.5W → 833mA.

MSP2007(3.3V) typical 0.3W → 91mA, Maximum 0.5W → 151mA.

11. Power Specification

Power is derived from the power adapter with the following specifications:

Linear Power Adapter: A. 12 V DC / 1A, B. 12V DC / 800mA

A. $12 * 1 = 12W$, B. $12 * 0.8 = 9.6W$

$1.8 * 0.833 = 1.4994W$

$3.3 * 1.409 = 4.6497W$

$12 * 0.2 = 2.4W$ because 5V is use linear regular so see it like 12V

total(1.8V, 3.3V) = 6.1491W

$6.1491 / 7.2 = 85.40\%$ B will margin ($8.5491 / 9.6 = 89.05\%$)

$6.1491 / 9.6 = 64.05\%$ A method is can use ($8.5491 / 12 = 71.25\%$)

PS FP5451 Power consumption:

12V, 1.71A → $12 * 1.71 = 20.52W$

5V, 1A → $5 * 1 = 5W$

3.3V, 2.5A → $3.3 * 2.5 = 8.25W$

1.8V, 0.8A because it use Linear so see it like 3.3V, 0.8A → $3.3 * 0.8 = 2.64W$

total = 15.89W efficiency $15.89 / 20.52 \rightarrow 77.44\%$

12. PCB Specification

ITEMS	SPECIFICATION
PCB Size	114.5mm x 80.6mm
PCB Material	FR4
PCB Thickness	1.6mm
No. of Layers	4
Golden Finger Connector	No

13. Environment

	TEMPERATURE	HUMIDITY
Operating	0 ~ 40	10 ~ 80%
Storage	-10 ~ 70	5 ~ 90%

14. EMC Certification

This product will pass FCC, CE , VCCI Class-B