Tuning Up Procedure & Operational Manual

Model: A12

Version 1.0

9, Jun. 2004

ZTE CORPORATION

5.1 General description

5.1.1 Product overview:

A12 product is new model phone designed by ZTE, it works at four band, EGSM? GSM? DCS and PCS band. Its weight is only 77g, the size is 106mm × 44.4mm × 16.8mm.. It has STN screen which pixels is 96 x 64 dots and has 16 polyphonies.

A12 CPU runs a 13MHz, with 32M Flash Memory and 4M SRAM. The main IC include baseband chip (AD6537B and AD6525XCA), RF chip (AD6539? RF3146) and memory chip. A12 can dial 3 hours continuously and can be in idle mode up to 130 hours, using 710mAH battery.

3.1 Principle of Rx Circuit

3.1.1 A12 supports quad bands: GSM 850/EGSM 900/DCS 1800/PCS 1900.

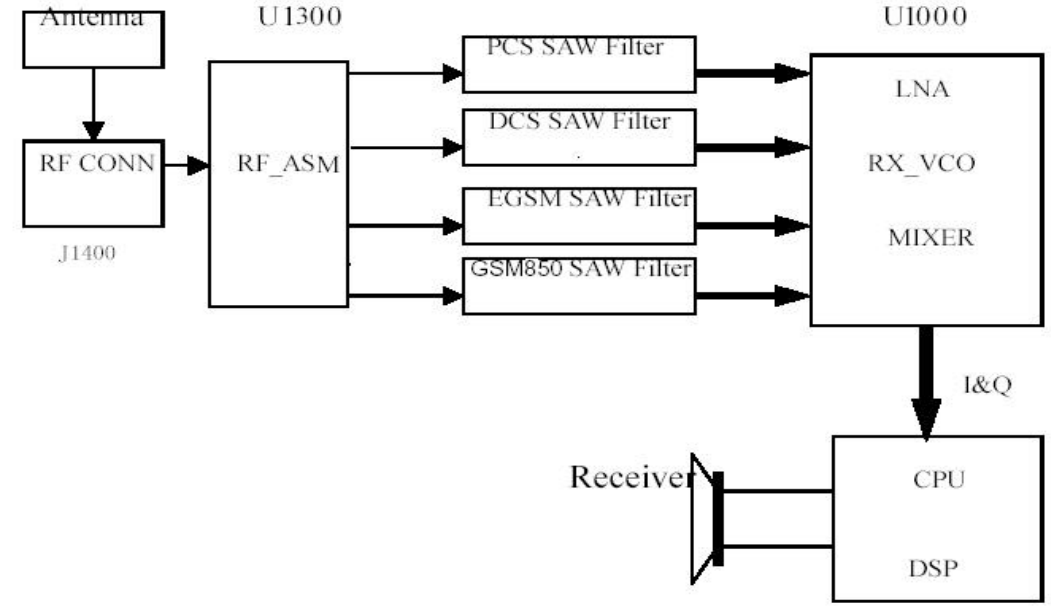
GSM 850:
Channel Range : 128-251
Downlink: 869MHZ-894MHZ
Uplink: 824MHZ-849MHZ
Duplexer: 45 MHZ
Bandwidth: 200 KHZ
Power Level Range: 5-19

PCS:
Channel Range : 512-810
Downlink: 1930MHZ-1990MHZ
Uplink: 1850MHZ-1910MHZ
Duplexer: 80 MHZ
Bandwidth: 200 KHZ
Power Level Range: 0-15

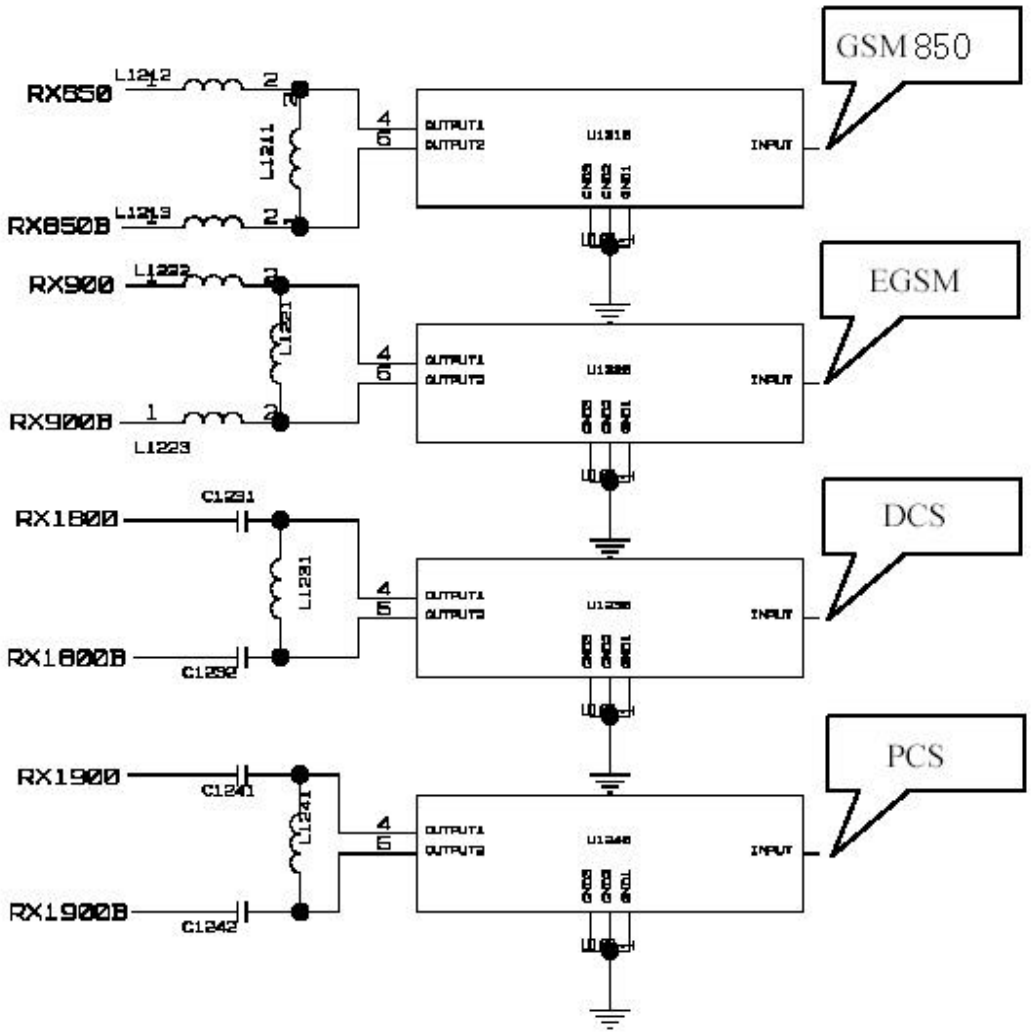
3.1.2 A12 Block Diagram for Receive Path:

3.1.3 Signal is coming from the RF Connector. RF Connector is designed for testing; with the RF cable and equipment our test engineers can analyze the Rx/Tx signal through the RF Connector. The Signal goes into RF_Switch from the RF Connector to control the working status.

After the signal comes out from RF_Switch, it goes into the related Saw Filter, and the signal turns into two signals.



Block Diagram of Rx



U1000 is the transceiver, a very important chip set. For the receive part, it mainly completes: LNAs（ Low Noise Amplifiers）？Down-Converting Mixers ？Baseband Amplifiers / Low Pass Filters and so on.

Four differential LNAs with programmable-gain drive a direct conversion demodulator that mixes down the received signal to baseband. The down converted signals then pass in quadrature to the baseband programmable-gain amplifiers and low pass filters for channel selection. The programmable-gain baseband amplifiers and the LNA gains are set via a standard 3-wire serial bus.

The baseband signals inside the Baseband Processor will be proceeded with analog to digital conversion? decoding? digital processor? digital to analog conversion, and the audio signal will be available to drive receiver.

3.1.4 Receive path circuit tuning up

We separate the failures in 3 parts: Logic failure, receiver failure and transmission failure. First we need define the failure according to the failed item then we begin the analysis in detail.

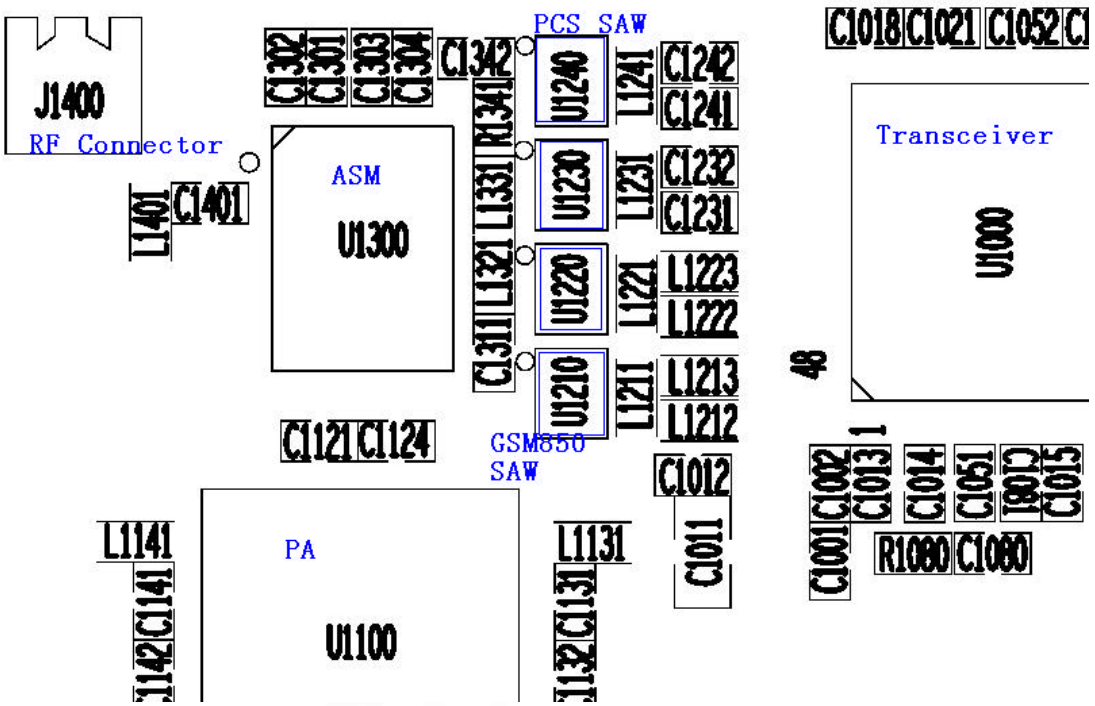
Receiver key parameters include: RX LEVEL? RX QUALITY? MOBILE CALL?

FLATNESS? TIME MASK? PHASE ERROR? FREQUENCY ERROR, etc. Here are the equipment we need to analyzer the problems（ Such as. EGSM）：

a. Set Agilent8960 to the specific channel and altitude of transmitter of the basestation .

b. Power on the mobile， the mobile is connected with Agilent8960 by the RF cable， and let the mobile be in the receive & testing mode.

c. Power meter and oscilloscope.



Step1:Measure the received signal according to signal flowing chart.

Measure the signal with spectrum analyzer on L1401 to check if the input signal is right. If wrong signal was detected it maybe J1400 cold sold or part defect. Measure the signal on pin2 of U1300 to check if the input signal is right. If wrong signal was detected it maybe C1401 cold soldering, tombstone part, part missing or screwed part.

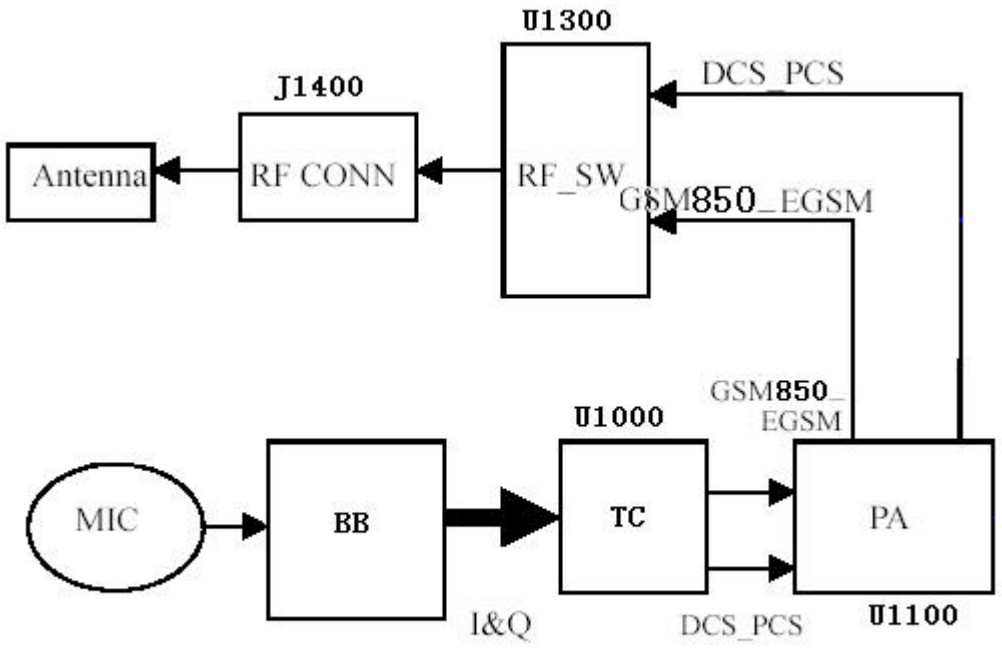
Step2: Measure the output signal from U1300 to check if the signal is right, GSM850 signal: measured from pin 10 (Measure at C1311); EGSM signal: measured from pin 11 (Measure at L1321); DCS signal: measured from pin12 (Measure at L1331), and for PCS from pin 13 at (Measure at R1341). If the signal is not right, should check if U1300 cold soldering, soldering short part, part defect or un-soldering. If no defect was found at U1300, then check if the control signal “TR_SW1_RF, TR_SW2_RF, TR_SW3_RF, TR_SW4_RF” is right. If the signal is not right please check D101 and parts around them. If no clear issue found, change U1300,D101, one by one.

Step3: Measure the input signal and output signal of SAW Filter. If the input signal is wrong, check on C1311:GSM850,L1321: EGSM ,L1331: DCS and R1341:PCS. If the output signal is wrong , check the filter U1210:GSM850, U1220:EGSM，U1230：DCS, U1240:PCS.

Step4: Measure I/Q signal output from U1000. If the signal is not good, check if there

are defects on U1000. Also need check the working voltage of U1000.

3.2.1 Transmit path circuit block diagram



Transmit signal block diagram

3.2.2 Audio signal turns into electrical signal by MIC, changes into baseband signals by A\D conversion? encoding? D\A conversion into U1000.

The transmit section of U1000 radio consists of a quadrature modulator, a high speed phase-frequency detector (PFD), with charge pump output, a Tx VCO and a feedback down converting mixer. These components implement a translation loop modulator for directly modulating baseband signals. The VCO output (divided by 2 for low band) is fed to the power amplifier (a portion of the transmitted signal is also fed back into the down-converting feedback mixer as part of the translation modulator feedback loop). An integrated power control loop is used to control the power amplifier's output level.

RF signal comes out of RF-PA(U1100) and transmits from the antenna by the RF-Connector.

3.2.3 Transmit circuit tuning up

Key parameter of Tx circuit is "Freq. error", "MAX POWER", "TX-CURRENT", "PA table", etc.

Following is normal analysis of the circuit, according to failed item to do more analysis. Confirm the instrument for analysis is good:

a. Power on the mobile, enter the key and let the mobile be in the transmit/testing mode, like EGSM: Channel 1? Power Level 15;

b. Set the spectrum analyzer to the correct center frequency 890.2MHz? bandwidth 10MHz? and suitable scan time;

c. Power meter and oscilloscope.

Step1: Measure the I/Q signal from Baseband Processor(D201) to modulation and demodulation IC (U1000). If the I/Q signal is not good, check D201.

Step2: if I/Q signal is good, Measure the output signal of U1000, If the signal is not good, check U1000, and parts around U1000.

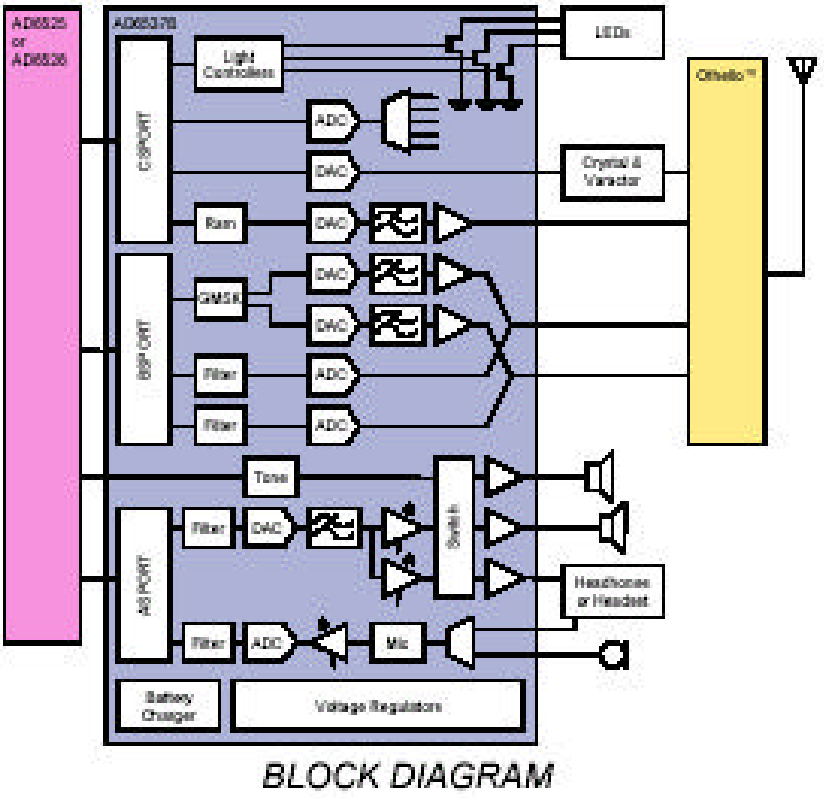
Step3: If the signal output from U1000 is right, continue to check output signal of PA(U1100). Measure the GSM850/EGSM signal at pin6 of PA; Measure DCS/PCS signal at pin31 of PA. If the output signal is not good check PA or parts around PA. Check the operating voltage "VBAT" and control signal.

Step4: Measure the input signal and output signal of RF-ASM (U1300). Also need check and control signal of U1300 . Measure antenna at last. Check J1400,Antenna, if the signal is not good.

3.3 Principle of Logic Circuit and tuning up

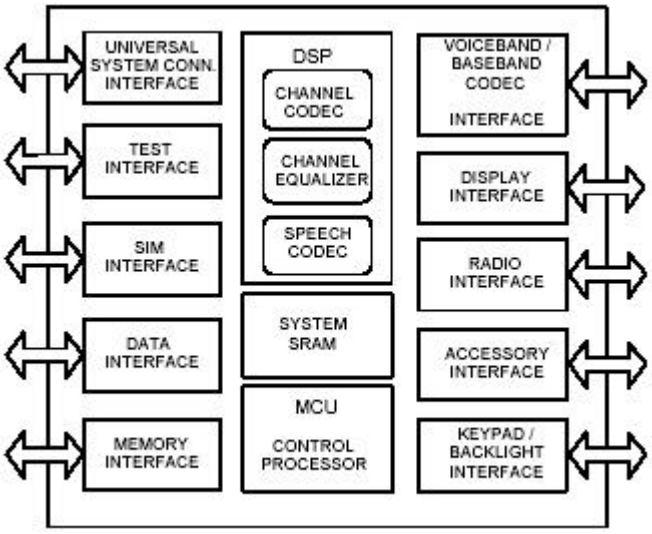
3.3.1 Principle of the logic circuit:

AD6537B Functional Block Diagram:

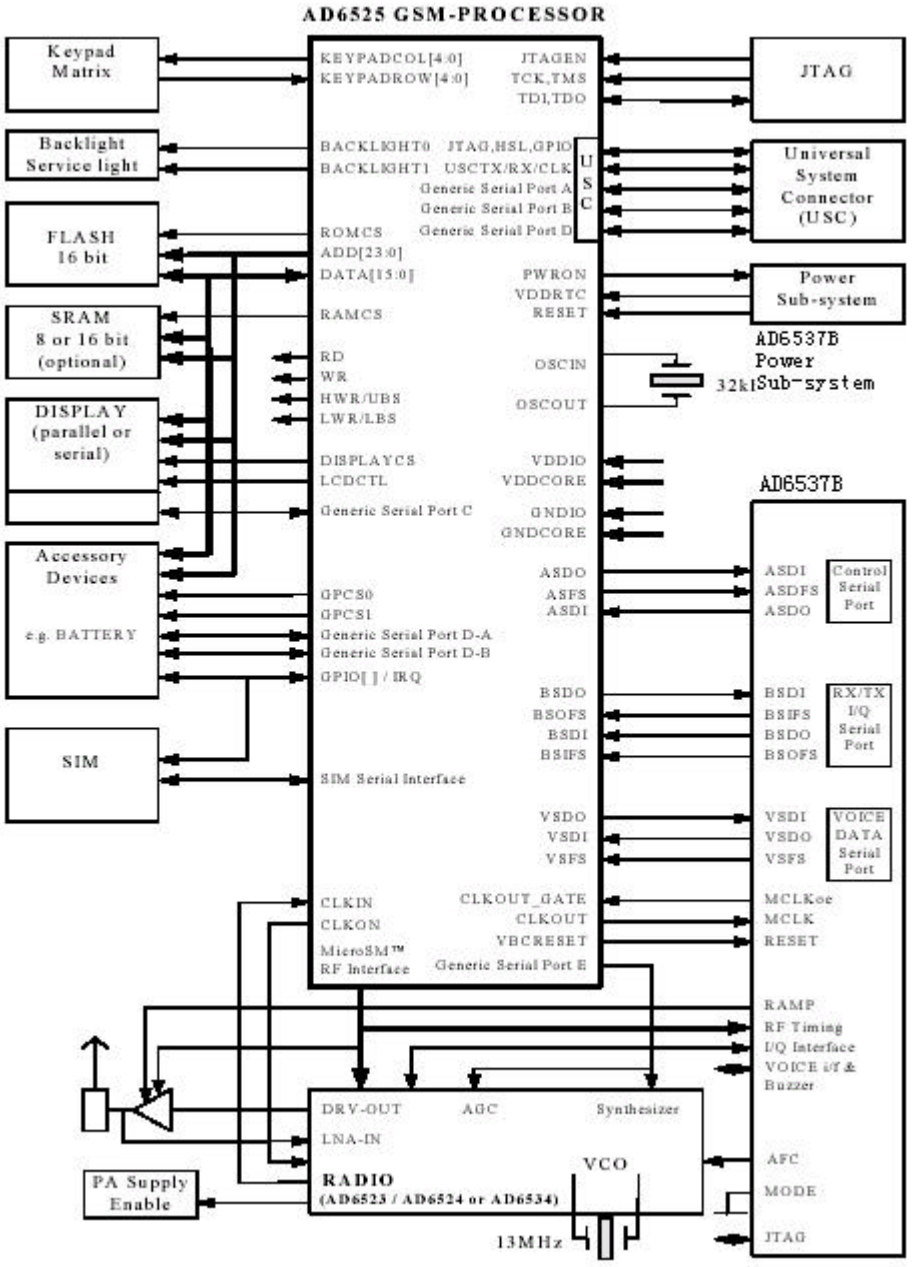


The logic ciucuit adopt two complete circuits inside the chipset, provide basebandprocessor, charge control, power management, EMS memory management and etc. It includes: 1. AD6537B: an analog baseband & audio interface, with baseband tranmit and receiver section, power management section, which include voltage regulations, battery charger and battery protection, etc. 2.AD6525: an individual System Controller with ARM, Digital Signal Procesoor & clock , keypad control and etc. The functional block diagram of individual chipset and signal connections between AD6537B and AD6525 and pin description are as beblow:

AD6525 Functional Block Diagram:



Signal connections between AD6537B and AD6525:



Pins Description of AD6537B:

Name	Type	Initial Condition	Absolute Maximum Ratings Minimum Voltage	Absolute Maximum Ratings Maximum Voltage	Description
Baseband Transmit & Receive Sections (5 terminals)					
IP	voltage input / voltage output	open	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V	I-channel positive input/output
IN	voltage input / voltage output	open	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	I-channel negative input/output
QP	voltage input / voltage output	open	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	Q-channel positive input/output
QN	voltage input / voltage output	open	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	Q-channel negative input/output
PA	voltage output	low	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	power amplifier control output
Auxiliary Section (14 terminals)					
Automatic Frequency Control DAC					
AFCDAC	voltage output	open	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	automatic frequency control DAC output
Voltage Reference					
AGND1	analog ground				voltage reference ground
REF	voltage output		AGND2 - 0.3 V	min(2.75 V, VBAT + 0.3 V)	voltage reference
REFBB	voltage output	open	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	baseband transmit & receive voltage reference
REFOUT	voltage output	open	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	voltage reference output
REFCHG	voltage output	open	AGND2 - 0.3 V	2.75 V	voltage reference output
Auxiliary ADC					
AUXADC1	voltage input / voltage output / current input	open	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	auxiliary ADC input or temp. sensor current reference
AUXADC2	voltage input		AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	auxiliary ADC input
Temperature Sensor					
TEMP1	current output / voltage input	open	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	temp. sensor channel 1 input/output
TEMP2	current output / voltage input	open	AGND2 - 0.3 V	min(2.75 V, VABB + 0.3 V)	temp. sensor channel 2 input/output
Light Controllers					
LGND	analog ground				light driver ground
LIGHT1	open-drain voltage output	open	LGND - 0.3 V	5.5 V	light 1 driver output
LIGHT2	open-drain voltage output	open	LGND - 0.3 V	5.5 V	light 2 driver output
LIGHT3	open-drain voltage output	open	LGND - 0.3 V	5.5 V	light 3 driver output

Name	Type	Initial Condition	Absolute Maximum Ratings		Description
			Minimum Voltage	Maximum Voltage	
Audio Section (18 terminals)					
Analog Audio Output 1					
AOUT1P	voltage output	open	AGND3 - 0.3 V	min(2.75 V, VABB + 0.3 V)	audio output 1 (32 Ω) positive output
AOUT1N	voltage output	open	AGND3 - 0.3 V	min(2.75 V, VABB + 0.3 V)	audio output 1 (32 Ω) negative output
Analog Audio Output 2					
SPWR (2)	voltage input		SGND - 0.3 V	5.5 V	audio output 2 power supply
AOUT2P (2)	voltage output	open	SGND - 0.3 V	min(5.5 V, SPWR + 0.3 V)	audio output 2 (8 Ω) positive output
AOUT2N (2)	voltage output	open	SGND - 0.3 V	min(5.5 V, SPWR + 0.3 V)	audio output 2 (8 Ω) negative output
SGND (2)	analog ground				audio output 2 ground
Analog Audio Output 3					
AOUT3P	voltage output	open	AGND3 - 0.3 V	min(2.75 V, VABB + 0.3 V)	audio output 3 (32 Ω) positive output
AOUT3N	voltage output	open	AGND3 - 0.3 V	min(2.75 V, VABB + 0.3 V)	audio output 3 (32 Ω) negative output
Analog Audio Input 3					
AIN3P	voltage input		AGND3 - 0.3 V	min(2.75 V, VABB + 0.3 V)	audio input 3 positive input
AIN3N	voltage input		AGND3 - 0.3 V	min(2.75 V, VABB + 0.3 V)	audio input 3 negative input
Analog Audio Input 1					
AIN1P	voltage input		AGND3 - 0.3 V	min(2.75 V, VABB + 0.3 V)	audio input 1 positive voiceband input
AIN1N	voltage input		AGND3 - 0.3 V	min(2.75 V, VABB + 0.3 V)	audio input 1 negative voiceband input
Analog Audio Input 2					
AIN2P	voltage input		AGND3 - 0.3 V	min(2.75 V, VABB + 0.3 V)	audio input 2 positive voiceband input
AIN2N	voltage input		AGND3 - 0.3 V	min(2.75 V, VABB + 0.3 V)	audio input 2 negative voiceband input

Name	Type	Initial Condition	Absolute Maximum Ratings		Description
			Minimum Voltage	Maximum Voltage	
Power Management Section (48 terminals)					
Voltage Regulators					
VBAT7	Battery		AGND4 - 0.3 V	5.5 V	digital core regulator input
VCORE (2)	voltage output	open	AGND4 - 0.3 V	2.75 V	digital core supply
VBAT8 (2)	Battery		AGND4 – 0.3 V	5.5 V	memory interface regulator input
VMEM (2)	voltage output	open	AGND4 - 0.3 V	min(5.5 V, VBAT + 0.3 V)	memory interface supply
VMEMSEL	voltage input		AGND4 - 0.3 V	min(5.5 V, VBAT + 0.3 V)	memory supply voltage selection
VBAT3 (2)	battery		AGND4 - 0.3 V	5.5 V	external interface regulator input
VEXT (2)	voltage output	open	AGND4 - 0.3 V	min(5.5 V, VBAT + 0.3 V)	external interface supply
VBAT4	battery		AGND4 - 0.3 V	5.5 V	SIM interface regulator input
VSIM	voltage output	open	AGND4 - 0.3 V	min(5.5 V, VBAT + 0.3 V)	SIM interface supply
VBAT6	battery		AGND4 - O.3 V	5.5 V	real –time clock regulator input
VRTC	voltage output	open	AGND4 - 0.3 V	5.5 V	real-time clock supply
VBAT2 (2)	battery		AGND4 - 0.3 V	5.5 V	analog baseband regulator input
VABB	voltage output	open	AGND2 - 0.3 V	2.75 V	analog baseband supply
AGND2	analog ground				analog baseband ground
AGND3	analog ground				analog audio ground
VBAT1	battery		AGND4 - 0.3 V	5.5 V	voltage-controlled crystal oscillator regulator input
VVCXO	voltage output	open	AGND4 - 0.3 V	min(5.5 V, VBAT + 0.3 V)	voltage-controlled crystal oscillator supply
VMIC	voltage output	open	AGND4 - 0.3 V	2.75 V	microphone supply
AGND4	analog ground				power management analog ground
VBAT5	battery		AGND4 - 0.3 V	5.5 V	regulator input

Name	Type	Initial Condition	Absolute Maximum Ratings		Description
			Minimum Voltage	Maximum Voltage	
Regulator Control					
KEYON	voltage input		AGND4 - 0.3 V	min(5.5 V, VBAT + 0.3 V)	power-on key input
KEYOUT	voltage output		AGND4 - 0.3 V	min(5.5 V, VBAT + 0.3 V)	power-on key output
Battery Charger					
VCHG	voltage input			5.5 V	charger supply
GATEDRIVE	current output	open	AGND2 - 0.3 V	min(5.5 V, VCHG + 0.3 V)	charge DAC output
BATTYPE	current output / voltage input	open	AGND2 - 0.3 V	2.75 V	battery type identification input
ISENSE	voltage input		AGND2 - 0.3 V	min(5.5 V, VBAT + 0.3 V)	charge current sense input
VBATSENSE	battery		AGND2 - 0.3 V	min(5.5 V, VBAT + 0.3 V)	battery voltage
Reserved					
NC_R12					reserved, do not connect
NC_B05					reserved do not connect
NC_B07					reserved do not connect
NC_T15					reserved do not connect
NC_G16					reserved, do not connect
NC_E15					reserved, do not connect
NC_E16					reserved, do not connect
NC_F16					reserved, do not connect
VBAT_NET			VBAT	VBAT	reserved, must be connected to VBAT
NC_R01			VCORE	VCORE	reserved, do not connect
GND_NET1			AGND0	AGND0	reserved, must be connected to ground
GND_NET2			AGND0	AGND0	reserved, must be connected to ground
NC_T12			AGND0	AGND0	reserved, do not connect
RSVD_C16			AGND0	AGND0	reserved, may be connected to RSVD_A16, otherwise do not connect
RSVD_A16			AGND0	AGND0	reserved, may be connected to RSVD_C16, otherwise do not connect