Certification Test Report

433.92 MHz Alarm System

FCC ID: Q6K 1000-7251

FCC Rule Part: 15.231

ACS Report Number: 04-0056-15C231

Manufacturer: 3SI Security Systems
Model: MCU

Theory of Operation

Transceiver Block Diagram
Figure 1 is the schematic of the transceiver, **U7**. Please refer to Figure 1 for the following discussions.

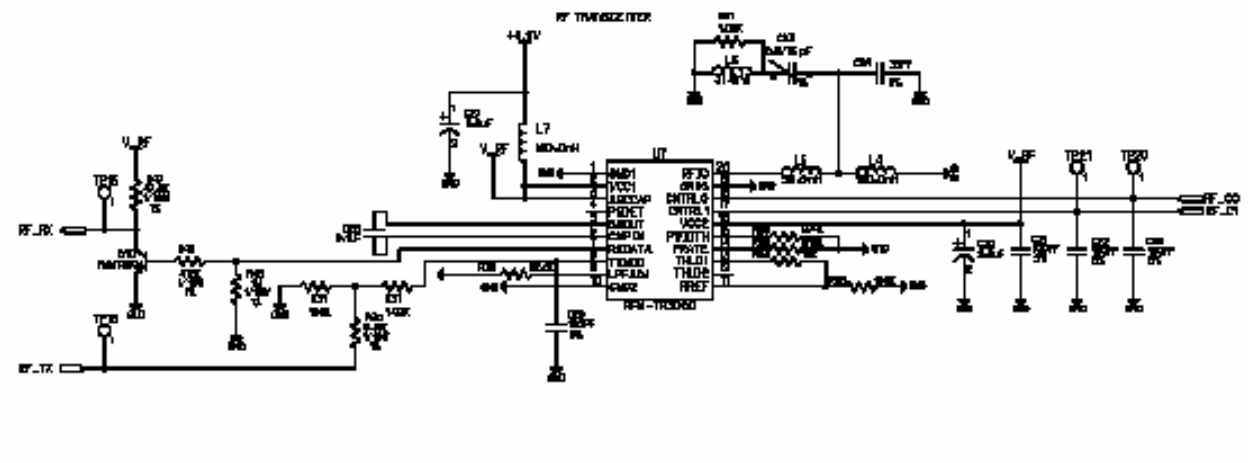

Figure #1

The main voltage to the RF circuitry is filtered by **C27**, **L7**, & **C20** in a "pi" configuration. **C22** & **C35** provide RF bypassing on the transceiver control lines.

Antenna Port
Antennas presenting an impedance in the range of 35 to 72 ohms resistive can be satisfactorily matched to the RFIO pin with a series/shunt matching circuit. A DC path from RFIO to ground is required for ESD protection. This is accomplished by **L4** & **L5** on the schematic. The antenna is **L6** that is resonant matched to 50 Ohms with **C23** & **C24**.

Transmitter Chain
The transmitter chain consists of a SAW delay line oscillator followed by a modulated buffer amplifier. OOK modulation is chosen by setting CNTRL0 =1 and CNTRL1=0. The transmitter output turns completely off between "1" data pulses. The transmitter RF output power is proportional to the input current to the TXMOD pin. A series attenuation circuit (**R30**, **R31**, & **R37**) is used to adjust the peak transmitter output power. Power out is nominally set for 0.1 mW. **C29** is used as a RF bypass and minimize the TX data edges.

Receiver Chain
The receive operation is chosen by setting CNTRL0 =1 and CNTRL1=1. A receive filter provides a three-pole, 0.05 degree equiripple low pass response with excellent group delay flatness and minimal pulse ringing. The 3 dB bandwidth of the filter is set by **R36** and is optimized for a 19.2kBaud data rate. The detected signal, BBOUT is coupled to the CMPIN pin, by **C26**.

Data Slicers
The CMPIN pin drives two data slicers, which convert the analog signal from BBOUT back into a digital stream. Data slicer DS1 is a capacitively coupled comparator with the comparator's slicing level set with resistors **R34** & **R35**

Output Buffer

The output of the transceiver was designed to drive a 500kOhms//10pF load. This was sufficiently high enough that a source-follower buffer, **Q3, R45, R47,** & **R48** had to be incorporated to interface with the uProc.

AGC Control
The purpose of the AGC function is to extend the dynamic range of the receiver, so that two transceivers can operate close together. The AGC operation is presently defeated in this circuitry, by having the AGCCAP pin tied to Vrf. If require, **C21** can be quickly modified to accomplish the AGC function.

Receiver Pulse Generator and RF Amplifier Bias
The receiver amplifier-sequence operation is controlled by the PRATE and PWIDTH input pins. The PWIDTH pin sets the width of the ON pulse with a resistor **R39** to ground. The PRATE pin sets the falling edge of one ON pulse to the rising edge of the next ON pulse with a resistor **R39** to ground.

RF Sleep Mode

The transceiver is put into a sleep mode by setting CNTRL0 =0 and CNTRL1=0. This lowers the current drain to 0.75 uA.