Talladega Short Burst Data Module System Specification

Monaco Family Products

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Revision History

(This table will be filled in from V1.0 onwards, V1.0 being the first complete version of this document.)

Version	Date	Author	Comment
V1.0	4 April, 2005	Richard Davies	First complete version (including RS232) for review by Iridium.
V1.1	18th April 2005	Marion Campbell	Updated after review by Iridium, see IRF-004 V1.1 for review comments.
V1.2	6 May 2005	Richard Davies	Added Appendix B and Appendix C.
V1.3	30 June 2005	Richard Davies	Updated to reflect changes in connectors. Voltage levels corrected in Appendix A.
V1.4	19 July 2005	Richard Davies	Changed RTC supply maximum. Updated approach to EMC and ESD protection to reflect P3 design goals.
V1.5	12 August 2005	Richard Davies	Changed RTC current draw, added DPL data rate in 3.2.8, updated ESD protection, no test connector for P3, added Inmarsat rejection figure at 10 MHz
V1.6	7 September 2005	Richard Davies	Removed external power source for real-time clock for P3 build 2 onwards

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List of References

Ref	Title	Document Number
1	Monaco H1b Transceiver Board circuit diagram	C7032-CD-012 version e
2	Talladega System Block Diagram	C7321-SCH-001
3	Talladega RF System Level Design	C7321-TM-001
4	DPL Protocol and Hardware Specification	C7032-S-018
5	Short Burst Messaging Air Interface Specification, version 0.8	C7321-RD-006
6	Iridium Short Burst Data Service Developers Guide	C7321-RD-004
7	Talladega AT Command Reference	C7321-S-005
8	Talladega Test Interface Card (TIC) Specification	C7321-S-006
9	Custom Digital IC Design Specification	C7321-S-001

Glossary

Abbrev.	Full Name
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
ASIC	Application Specific Integrated Circuit
CP	Call Processor
CPLD	Complex Programmable Logic Device
CW	Carrier Wave (unmodulated)
DAC	Digital to Analogue Converter
DC	Direct Current
DPL	Digital Peripheral Link
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable Read Only Memory
ESR	Equivalent Series Resistance
FPGA	Field Programmable Gate Array

Abbrev.	Full Name
IF	Intermediate Frequency
IMEI	Iridium Mobile Equipment Identifier
INS	Iridium Network Simulator
I/O	Input/Output
IQ	In-phase and Quadrature
JTAG	Joint Test Action Group - test interface used for download and boundary scan
LAC	Location Area Code
LC	Inductive/Capacitive
LNA	Low Noise Amplifier
LO	Local Oscillator
MMI	Man Machine Interface
NF	Noise Figure
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Coded Modulation
PLL	Phase-Locked Loop
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circular Polarised
RRC	Root Raised Cosine
RSSI	Received Signal Strength Indication
RTC	Real Time Clock
Rx	Receiver
SBD	Short Burst Data
SBM	Short Burst Messaging
TMSI	Temporary Mobile Subscriber Identity
TNC	Threaded RF Coaxial Connector
Tx	Transmitter
UART	Universal Asynchronous Receiver/ Transmitter
USART	Universal Synchronous/Asynchronous Receiver/ Transmitter
VAM	Value Added Manufacturer
VAR	Value Added Reseller
VGA	Variable Gain Amplifier
VSWR	Voltage Standing Wave Ratio (measure of relative reflected power)

1 Introduction

The Monaco family of satellite terminals comprises three products based on the same architectural design for the radio modem (or transceiver) and processing elements of the core design.

The three products are:

1. 9505A Monaco Handset,
2. 9522A Daytona L-Band Transceiver, and
3. **Short Burst Data Module.**

This document describes the Short Burst Data Module, internally known as Talladega.

The Short Burst Data Module is a satellite transmitter and receiver that can be built into third party products. The Short Burst Data Module has data capability only: no voice and no MMI. It is a board-level product, which will need to be enclosed in a conductive box for type approval. Value Added Manufacturers (VAMs) will integrate the Short Burst Data Module into higher-level product assemblies.

The Short Burst Data Module does not include an antenna, it has an antenna connector for connection to an external antenna by the VAM.

1.1 Scope

The target audience for this document is the client (Iridium), and the Cambridge Consultants development team. This document may also be of assistance to testers and manufacturers of the Short Burst Data Module as background information. This document is NOT intended for VAMs or VARs who will purchase the Data Module, separate User Documentation will be provided for this audience.

1.2 Numbering of prototype versions

The relationship between the build number and CCL drawing number is shown in the table below.

Build number	CCL drawing number	Description
P1	C7032-CD-001a	First version, 8 Watt PA running at 2 Watts, RS-232
P2	C7032-CD-001b	Second version, 2 Watt PA, RS-232
P2	C7032-CD-001c	Second version, 2 Watt PA, logic levels
P3	C7032-CD-001d	Third version, 2 Watt PA, RS-232
P3	C7032-CD-001e	Third version, 2 Watt PA, logic levels

P3 2nd build	C7032-CD-001f	Fourth version, 2 Watt PA, RS-232
P3 2nd build	C7032-CD-001g	Fourth version, 2 Watt PA, RS-232

2 System Overview

The Data Module consists of a single PCB. When assembled into a product, i.e. in an enclosure and connected to a power supply, data terminal equipment and an antenna it will operate as a short burst data modem on the Iridium satellite system.

The design is derived from the 9505A/9522A H1b transceiver design by removing the audio circuits, the auxiliary receiver, the SIM and MMI interface, and operating at a lower RF power level. There are two user connectors, one for the antenna and one for input/output and DC power.

The Data Module does not support voice, so the audio circuits can be removed.

The Data Module does not need to support intra or inter SV handoff because of the short message length. Therefore it does not need to measure RSSI, so the auxiliary receiver can be removed.

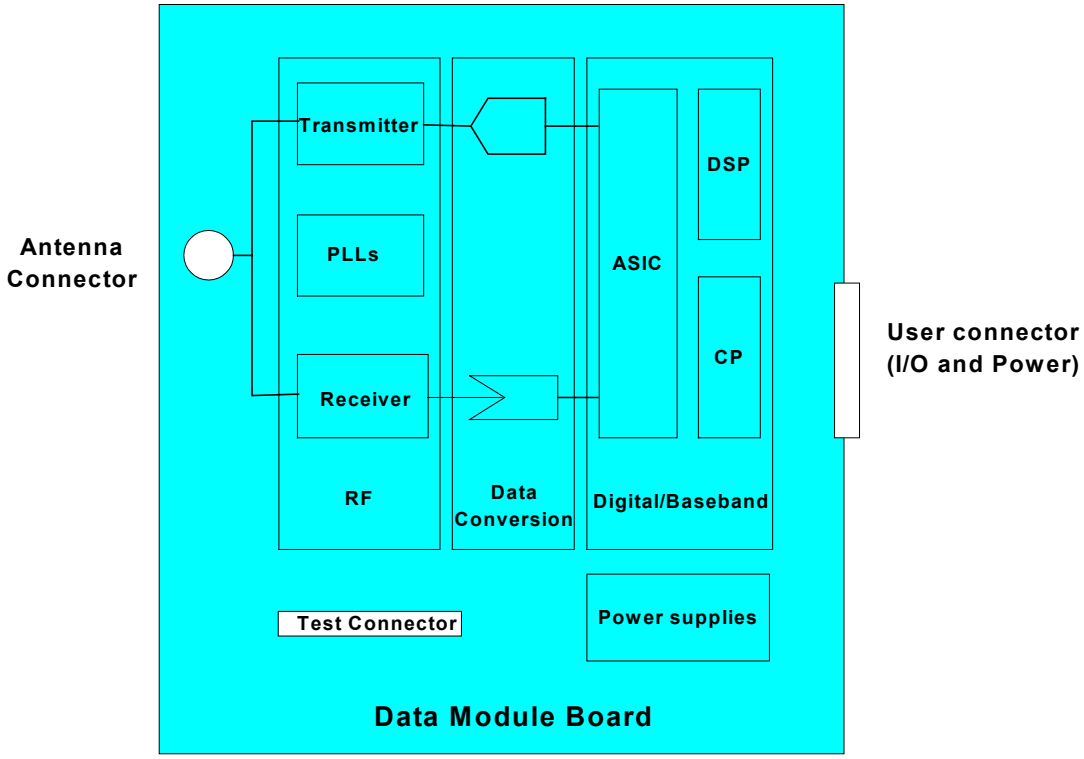
The Data Module has its IMEI, Access Code, TMSI and Location Area Code (LAC) programmed into its EEPROM during production, so it does not need a SIM. The IMSI and Access Code are needed for setting up the SBD call, the TMSI and LAC are normally acquired during location registration and are required for receiving ring alerts. Service Provider configurable functionality, normally configured via the SIM is not supported for the Data Module.

The Data Module will be controlled by an external host via AT commands, rather than a human user. Therefore the MMI can be removed.

The reduction in RF power allows us to reduce the cost, size and power consumption of the Data Module. The reduced RF power level means that the Data Module has a reduced link margin and is therefore more likely to drop an existing connection with a satellite or fail to connect to a satellite. This reduction in performance is acceptable because of the short connection times required for SBD.

The Data Module is powered by a single +5 Volt DC power source. The user interface consists of two serial asynchronous digital interfaces and four additional control signals. The main serial data interface (Data port) has a full set of flow control signals. It operates at a default data rate of 19.2 kbps, and can be programmed to standard data rates between 600 bps and 115.2 kbps. The second serial data interface (DPL port) has no flow control, and operates at a fixed data rate of 115.2 kbps, this is used by production for testing the Data Module.

Figure 1: Data Module Physical Interface Diagram



The antenna connector on the PCB needs a cable to a TNC bulkhead connector suitable for use with existing Iridium antennas. These are right-hand circular polarised and are rotationally symmetric cardoid with a maximum gain of 3 dBi.

A test connector is provided for software development and possible use in manufacturing. This provides JTAG access to the processors and memory, access to the reset line, and some uncommitted input/output signals. When enclosed in a box the test connector is not normally accessible.

3 Interfaces

3.1 Antenna

The data module antenna interface is a pcb-mounted 50 Ohms coaxial connector. The first units (P1) will use a FSC connector, Murata part number MM7329-2700B. The first version with the 2 Watt PA (P2) will use a lower-cost MMCX connector, Amphenol part number 908-22101T. The preferred connector for the production units (P3 and later) is a pcb-mounted SMA connector.

Antenna impedance	50 Ohms nominal
Antenna gain	3 dBi maximum, RHCP
VSWR	3:1 maximum. Above this point the transmitter will shut down to protect the PA[1]. The antenna should ideally present a VSWR of not more than 1.5:1.

3.2 User Connector

The user connector comprises the power input and the user serial interface for control of the Data Module. The connector should be a surface mount 26way 2 mm Ejector Header, Samtec part number EHT-113-01-SM-D-SM. This connector allows a latching connection to a cable-mounted connector, and board-to-board connection for different mechanical configurations of the Talladega and its host.

3.2.1 Power Input

The Data Module requires a 5 VDC ± 10% external power source. The power supply is required to be a stabilised DC supply capable of supplying current peaks of 2 Amperes when transmitting. The current pulses last 8.3 ms every 90 ms. The maximum standby current will be approximately 100 mA.

The power input connections to the Data Module are presented on pins of the interface connector.

Three pins are provided for each power connection (this reduces the current passing through each pin). The current rating of the connector is sufficient that two may be used for power and one for remote sensing. If remote sensing is not used then all three should be connected in parallel.

[1] The action to be taken by the software following a VSWR trip is described in section 8.7.

3.2.1.1 Power Supply Requirements

The reservoir capacitors on the Data Module are 940 µF with an ESR of 50 mOhms. These provide sufficient energy storage to sustain the PA supply voltage over a 40 µs symbol[2]. The external supply needs to guarantee the following:

- The supply voltage droop over a 8.3mS burst should not be more than 0.2 Volts.
- The power supply should limit the inrush current to 4 Amps maximum (this is the current carrying capacity of the connectors when used with remote sensing).

- The supply noise measured at the supply pin on the Data Module (i.e. 940 µF with an ESR of 50 mOhms) should be less than that in the profile below (linear interpolation between these points):
  - 100 mV pk-pk 0Hz to 50 kHz
  - 5 mV pk-pk in 50 kHz bandwidth at 1 MHz
  - 10 mV pk-pk in 1 MHz bandwidth at 1 MHz
  - 5 mV pk-pk in 1 MHz bandwidth above 5 MHz.

3.2.2 Power On/Off Control

An external on/off input is provided on a pin of the interface connector. As long as the input voltage is applied, a continuous logic high on this line turns the module on, a logic low turns it off.

If this line is not required then it must be connected directly to the +5 V supply.

The input logic high threshold is 2.0 V minimum.

The logic low threshold is 0.5 V maximum.

The Data Module starts up when power is applied as long as the power on/off input is high.

3.2.3 RTC Power

This function is not supported from P3 build 2 onwards. The Real-Time Clock is an integral part of the processor, but is only powered when the unit is on.

3.2.4 Data Port

The data port is presented on pins of the interface connector. This port operates at either RS-232 or 2.9 V logic levels depending on the population of the board. It provides the following signals:

- S_TX (transmit serial data input to Data Module),

[2] The PA supply voltage should not change by more than 0.1V over a symbol to prevent spectral regrowth

- S_RX (receive serial data output from Data Module),
- DTR (data terminal ready input to Data Module),
- DSR (data set ready output from Data Module),
- RTS (request to send input to Data Module),
- CTS (clear to send output to Data Module),
- RI (ring indication output from Data Module), and
- DCD (data carrier detect output from Data Module).

When RS-232 is used then the polarity of the data and control signals is as defined in the standard and can be connected directly to a PC RS232 port. When 2.9 V CMOS logic levels are used the transmit and receive data lines are active high and the control signals are active low. In a compact system where the host computer is physically close to the Data Module you can connect directly to its UART from these logic levels.

The data rate default value is 19.2 kbps, 8-bit, no parity. It is programmable by the AT+IPR command to data rates of 600, 1200, 2400, 4800 9600, 19200, 38400 or 115200 bps. The unit does not autobaud.

The data port is the main control interface for the Data Module, instructions being sent in the form of AT commands, see reference [7].

The data port may also be used to upgrade the software on the Data Module. A PC application is provided to perform the software upgrade. When performing software upgrade the data port operates at 115200bps.

When configured for logic level inputs and outputs, these will be protected against accidental connection of RS232 signal levels.

3.2.5 90ms Synchronization Input (Ext 11Hz)

This input, used in testing with the INS or Racal test units only, is presented on the interface connector and operates at 2.9V digital signalling levels. This input is not intended to be used in normal operation by the VAM or VARs; it should be left disconnected or connected to ground.

3.2.6 Network Available

This output pin indicates when the Data Module is in a condition where it can communicate with the satellite network or not. A logic high indicates that the satellite network is available, the Data Module can see a satellite beam and its ring and broadcast channels and therefore should be able to set up a call. A logic low means that this condition is no longer true. An external device can use this signal to determine when to send a command to the Data Module to send SBD.

3.2.7 Supply Output

A digital 2.9 V supply is provided to power a small amount of external circuitry. One possible use is for external RS-232 line drivers and receivers for the Data port.

The maximum recommended current draw is 50mA, the output is not current limited but exceeding this recommended limit may affect the operation of the Data Module.

On P3 units the current available will be limited further by a 220 Ohm resistor which forms part of the EMC and ESD protection.

3.2.8 Digital Peripheral Link (DPL)

The DPL interface in the Data Module is a full duplex asynchronous serial link used for control messages. The protocol used on this port is described in reference [4]; only the asynchronous serial data is supported, not the PCM digital audio. This interface is not intended to be used in normal operation, it is used for testing specifically for TPI commands and the data logging interface. The data rate is 115.2 kb/s.

3.2.9 ESD protection and EMC filtering

A measure of electro-static discharge (ESD) protection and electro-magnetic compatibility filtering is needed on all pins on this connector when the data module is encased in a box and submitted for type approval. EMC filtering is included on all signals, and ESD protection components are used on all power and logic-level signals. The RS-232 signals are protected against ESD within the transceiver chip.

For the logic-level variant the ESD requirements are eased by virtue of a shorter connection cable between the Talladega unit and the host device. In this configuration there will not be any ESD protection devices on the data port.

3.2.10 User Connector Pin Allocation

The user connector will be a 2 row 26-way latching header. Multiple supply grounds are provided to limit the current on any one pin; multiple signal grounds are provided to reduce cross-talk.

Pin No.	Signal Name	Signal direction (wrt module)	Signal function	Signal level
1	+5 V	Input	Supply	+5 +/- 0.5 V
2	+5 V	Input	Supply	+5 +/- 0.5 V
3	+5 V	Input	Supply	+5 +/- 0.5 V
4	0 V		Supply return	0 V
5	0 V		Supply return	0 V

Pin No.	Signal Name	Signal direction (wrt module)	Signal function	Signal level
6	0 V		Supply return	0 V
7	ON/OFFB	Input	On/Off control input	On, 2.0V to Vsupply Off, 0V to 0.5V I = 120 µA max
8	Spare			
9	Ext 11 Hz	Input	Used for testing only	2.9 V CMOS
10	Gnd		Signal ground	
11	DF_S_TX	Input	Data port, serial data into data module	RS-232 or 2.9 V CMOS
12	DF_S_RX	Output	Data port, serial data from data module	RS-232 or 2.9 V CMOS
13	Gnd		Signal ground	
14	DF_ DCD	Output	Data port, Data Carrier Detect	RS-232 or 2.9 V CMOS
15	DF_ DSR	Output	Data port, Data Set Ready	RS-232 or 2.9 V CMOS
16	DF_ CTS	Output	Data port, Clear-to-Send	RS-232 or 2.9 V CMOS
17	DF_RI	Output	Data port, Ring Indicator	RS-232 or 2.9 V CMOS
18	DF_ RTS	Input	Data port, Request-to-Send	RS-232 or 2.9 V CMOS
19	DF_ DTR	Input	Data port, Data Terminal Ready	RS-232 or 2.9 V CMOS
20	Gnd		Signal ground	
21	DPL _TX	Output	DPL serial data output	2.9 V CMOS
22	DPL_RX	Input	DPL serial data input	2.9 V CMOS
23	Gnd		Signal ground	
24	NETWORK_ AVAILABLE	Output	Set to logic 1 when network is visible	2.9 V CMOS

Pin No.	Signal Name	Signal direction (wrt module)	Signal function	Signal level
25	Spare			
26	+2V9	Output	Supply output	+2.9 ± 0.15 V, 50mA maximum (100 Ohm series resistor on P3)

3.3 Test Connector (P1 and P2 only)

The test connector is used to bring additional signals out of the Data Module that are useful during development. These signals (such as JTAG interfaces for the CP, ASIC and DSP) are brought out onto the Test Interface Card, reference [8]. The EMC and ESD filtering requirements introduced for P3 means that these signals are only available as test points on P3 and subsequent versions.

The test connector is a 2-row 34-way 1.27 mm header, Samtec part number FTSH-117-01-LM-DV-K. It will not be fitted on final production versions of the PCB, instead in production a "bed of nails" will be used to access the pins needed for software programming.

Production testing is done via the TPI interface over DPL, which is presented on the user connector.

3.3.1 Software Development Support

A test connector provides the signals needed for software development support. The DSP and CP devices each have debug interfaces provided for software development:

- The CP implements the ARM7's integrated in-circuit emulation debug port over the device's JTAG pins.
- The 'C5416 DSP provides an on-board scan-based debug interface over the device's JTAG port using a TI XDS510 JTAG emulator module.

Additional signals on this connector are:

- Reset input/output. The reset line is an active low signal driven by an open-drain device with a pull-up resistor. It may therefore be used as a reset input, or may be externally asserted by a switch closure to ground.
- Debug UART. This is a two-wire serial interface using one of the CP UARTS.
- Two general purpose PIO lines.

- ASIC JTAG.

3.3.2 Test Connector Pin Allocation

The connector is a 2 row 34 way non-latching header.

Pin No.	Signal name	Signal direction (wrt module)	Signal function	Signal level
1	0 V			
2	CP_DOG	Output	CP watchdog	2.9V CMOS
3	EXT_RESETB	Bi-directional	Reset input or output	Output, 2.9V CMOS Input, switch closure to ground
4	FLASH_WPB	Input	Flash memory write protect. Set high to disable write protect	2.9V CMOS
5	0 V			
6	CP_TDI	Input	CP and JTAG test data in	2.9V CMOS
7	CP_TDO	Output	CP test data out	2.9V CMOS
8	CP_TCK	Input	CP and JTAG test clock	2.9V CMOS
9	CP_TMS	Input	CP and JTAG test mode select	2.9V CMOS
10	CP_TRSTB	Input	CP JTAG and ICE block reset	2.9V CMOS
11	CP_JTAGSEL	Input	CP JTAG / ICE mode select	2.9V CMOS
12	0 V			
13	DSP_TDI	Input	DSP test data in	2.9V CMOS
14	DSP_TDO	Output	DSP test data out	2.9V CMOS
15	DSP_TCK	Input	DSP test clock	2.9V CMOS
16	DSP_TMS	Input	DSP test mode select	2.9V CMOS
17	DSP_TRSTB	Input	DSP test reset	2.9V CMOS
18	DSP_EMU1	Input	DSP emulator signal	2.9V CMOS
19	DSP_EMU0	Input	DSP emulator signal	2.9V CMOS

Pin No.	Signal name	Signal direction (wrt module)	Signal function	Signal level
20	0 V			
21	ASIC_TDI	Input	JTAG data to ASIC	2.9V CMOS
22	ASIC_TDO	Output	JTAG data from ASIC	2.9V CMOS
23	ASIC_TCK	Input	ASIC test clock	2.9V CMOS
24	ASIC_TMS	Input	ASIC test mode select	2.9V CMOS
25	ASIC_TRST	Input	ASIC test reset	2.9V CMOS
26	PIO(1)	TBD	General purpose I/O line	2.9V CMOS
27	PIO(2)	TBD	General purpose I/O line	2.9V CMOS
28	0 V			
29	+2V9	Output	Supply output	+2.9 ± 0.15 V, 50 mA maximum
30	0 V			
31	DSP_IRQB	Output	Interrupt Request Line from DSP to CP	2.9V CMOS
32	DBG_TXD	Output	Debug serial data output	2.9 V CMOS
33	DBG_RXD	Input	Debug serial data input	2.9 V CMOS
34	0 V			

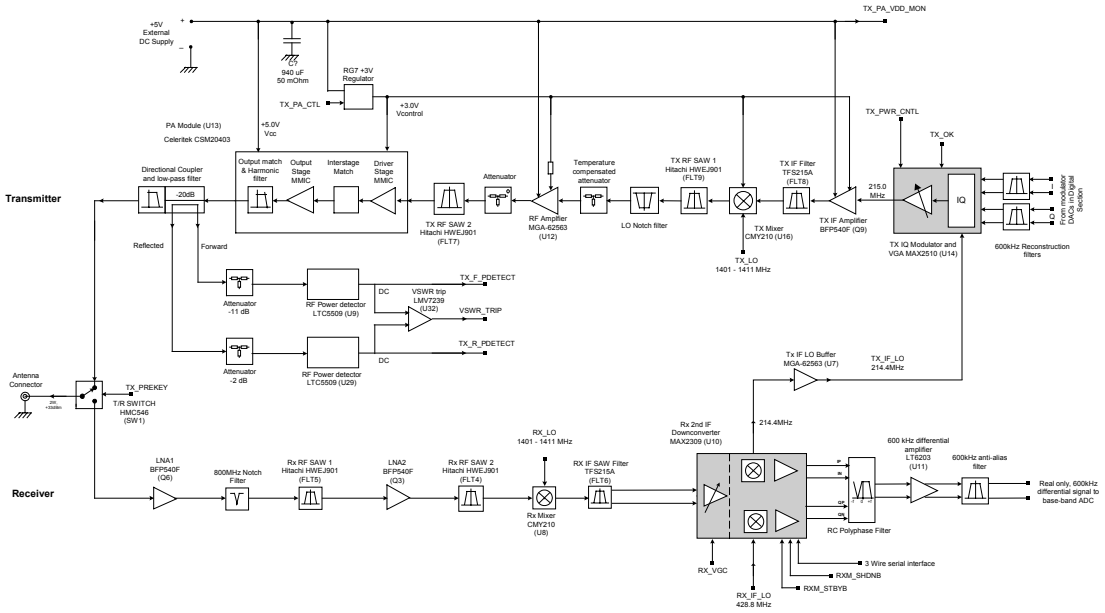
4 Functional Partitioning

On transmit the CP prepares the data for transmission. The DSP processor formats the message and performs the modulation function including the RRC filtering producing a pair of baseband quadrature sample streams at a sample rate of 200 ks/s. The ASIC interpolates up to a sample rate of 2.4 M samples/s and mixes up to 600 kHz (I and Q signals) for conversion to analogue waveforms by the digital-to-analogue converters. The RF circuits translate the frequency up to the output frequency and amplify to the desired power.

On receive the RF circuits provide amplification, frequency conversion and filtering functions producing a 600 kHz IF. The ADC samples this at 2.4M samples/s. The ASIC mixes down to complex baseband signals and decimates to 200k samples/s. The DSP performs channel filtering, gain control, RSSI, synchronisation, demodulation and de-formatting functions.

5 RF Chain Design

Figure 2: Receiver and Transmitter Block Diagram, Analogue Sections



5.1 Frequency Plan

The block diagram for the RF and IF analogue sections of the transmit and receive architecture is shown in Figure 2.[3]

The receiver is a conventional dual conversion superhet with an RF input of 1616MHz to 1626.5MHz, a first IF of 215MHz and a low second IF of 600kHz. A real-only output is provided at the second IF frequency for analogue-to-digital conversion at a sample rate of 2.4 MHz. The image of the second mixing process is suppressed by means of a two-section polyphase filter. The ASIC performs a final frequency conversion to bring the signal to a quadrature pair at zero frequency.

The transmit frequency plan is identical although the architecture is different. The DSP processor generates a pair of baseband quadrature components at a sample rate of 200 kHz. In digital hardware these are translated to an IF of 600 kHz at a sample rate of 2.4 MHz. The two quadrature components are converted to analogue signals in the DACs, filtered to remove alias components and translated in a single-side band mixer to an IF of 215 MHz. After filtering the signal is then mixed to the output frequency of 1616 to 1626.5 MHz.

[3] The first spin on the Talladega PCB will use the H1b 8W PA, all subsequent spins will use the new lower power 2W PA.

The RF local oscillator (LO) is provided by a fractional-N phase-locked loop synthesiser and tunes from 1401 to 1411.5 MHz with a resolution of 4 Hz. The IF LO operates at 428.8 MHz, controlled by an integer-N loop.

5.2 Rejection of Interference from Inmarsat Terminals

The Inmarsat up-link frequency allocation is 1626.5 to 1646 MHz, which is immediately adjacent to the upper edge of the Iridium band. An Inmarsat C terminal uses a 25 Watt transmitter and an omni-directional antenna. The 9522A LBT is designed to work with 3 dB degradation of receiver sensitivity at a distance of 65 metres from an active Inmarsat C terminal (assuming –2dB antenna gain). This corresponds to an input blocking level of –30 dBm. Talladega is designed for an input blocking level of –25 dBm at 5 MHz frequency separation, reducing the distance to below 45 metres and –20 dBm at 10 MHz frequency separation giving 25 metres (again assuming –2dB antenna gain). Any further improvements would probably require corresponding improvements in the design of the Inmarsat terminal.

5.3 Transmit Path

5.3.1 Baseband to IF

The first stage of the transmit analogue signal processing is a single side-band up-conversion from 600 kHz to 215 MHz. The process is split between the digital and analogue sections of the radio. The DSP and ASIC generate a pair of quadrature signals at 600 kHz at a sample rate of 2.4 MHz for the digital-to-analogue converters. The converter outputs pass through a reconstruction and anti-alias filter. An IQ modulator performs a single side-band up-conversion to the second IF of 215MHz.

A Maxim MAX2510 device provides both TX modulator and variable-gain amplifier stages in one package. A bipolar transistor amplifier is followed by a SAW filter to remove carrier leakthrough, image products and broad-band noise from the TX modulator.

5.3.2 RF Section

A Triquint CMY210 is used for the up-conversion mixer, followed by an RF SAW filter and lumped LC notch filter to remove the LO frequency. An Agilent MGA-62563 amplifier is used as the PA driver followed by a second RF SAW filter to gain sufficient image and LO suppression.

5.3.3 PA

The Celeritek CSM20403 2W PA will be used in the Data module. Unlike the 8W PA used in the 9505A/9522A H1b products it will not contain an isolator or provide a coupled port output. The PCB will therefore need to include a directional coupler and a reverse-power detector. If the VSWR exceeds 3:1 the transmitter will shut down. This

function will be performed in hardware inside the ASIC and a status line will be set to inform the CP. The status line signal will remain latched as long as the transmission attempt is in progress, and will clear at the end of the transmission attempt.

5.3.4 RF Power Control

The transmitter operates at only one power setting, which is a nominal 2 Watts at the PA. This is set at manufacture at 31.7 dBm on a transmission consisting of all zeros (equivalent of CW). The output power rises from this value at maximum supply voltage and falls at minimum supply voltage in such a way as to maintain optimum utilisation of the PA. The transmitter is held at this power by a control loop containing the following elements:

- Coupler at the PA output,
- Detector,
- Analogue-to-digital converter,
- Software,
- Digital-to-analogue converter, and
- Variable-gain amplifier (at transmitter 215 MHz IF).

A portion of the forward Tx power is taken from a coupler inside the PA (P1) or outside the PA (P2 and later) as described above. This is applied to a detector to give a DC level which is converted to a digital number in one of the CP auxiliary ADCs. The CP needs to divide this number by the measured power supply voltage and compare the result to a constant that was generated in calibration. The CP can then correct any error in the output power by updating the auxiliary DAC that sets the gain of the Tx variable-gain amplifier. Loop dynamics are controlled by the call processor software.

The detected power value is normalised by the supply voltage, this gives:

- good linearity and efficiency over the range of supply voltages without the need to over-design the PA,
- the output power will fall at minimum supply voltage by 0.9 dB, but all other aspects of performance will be maintained,
- at maximum supply voltage the output power will rise by 0.8 dB.

In order to preserve linear operation (and hence acceptable spectral re-growth) at high VSWR the power control loop will progressively reduce power as VSWR increases beyond 1.5:1.

5.3.5 Tx Burst Control

The PA supply and bias voltages are established just before the burst. The burst ramp profile is controlled by the modulation filters. The bias and supply voltages are removed after the end of the burst.

5.4 Receive Path

5.4.1 Tx / Rx Switch

The Tx/Rx switch is a GaAs FET based switch in a circuit optimised for the Iridium frequency band. A suitable off-the-shelf device is made by Hittite, part number HMC546.

5.4.2 LNA

There are two stages of signal-frequency gain, both using the Infineon BFP540F. There are also two HWEJ901 RF SAW filters. The noise figure of the receiver has been increased to 4 dB compared with the 9505A/9522A H1b products. This allows the compression point to be improved which improves the rejection of unwanted signals, in particular from nearby Inmarsat terminals. Even with this degradation the receive link margin is still significantly better than the transmit link margin.

5.4.3 Mixer

The receiver mixer uses the same device as the transmitter, a Triquint CMY210. This is a very linear mixer and yet low-power, but it is not balanced. The passive networks on each port provide the required isolation of the RF, LO and IF signals. The IF frequency is 215 MHz.

5.4.4 IF Filter

A SAW filter is used at 215 MHz. Measurements made on a 9505A/9522A H1b transceiver board show that the response is better than –40 dB at +/– 5 MHz. This is not sufficient to give the required Inmarsat rejection. Therefore an improved SAW filter from Telefilter will be used.

5.4.5 IF Gain, AGC, Second Conversion and Second IF

A Maxim MAX2309 is used to provide adjustable IF gain and the second frequency conversion. The I/Q demodulator stage is used to convert the 215 MHz IF to a low second IF of 600kHz. The I and Q outputs are combined in a two-stage polyphase network to suppress the unwanted image response. A differential output is amplified, filtered and set at the correct DC level for the analogue-to-digital converter. The filter has a notch at 1.8 MHz to remove the first alias frequency from the ADC input.

The IF gain is set in manufacturing by an auxiliary DAC to give the correct overall gain from the antenna to the ADC.

5.5 Synthesisers

A dual PLL device is used containing a fractional-N PLL synthesiser for the RF LO and an integer-N PLL for the IF LO. The RF synthesiser is used for the transmitter and receiver and need to be able to turn on and lock to frequency within 1ms. The IF synthesiser is unchanged between transmit and receive. The frequency standard is a voltage-controlled temperature-compensated crystal oscillator (VCTCXO) which is tuned by the CP to keep it set to the satellite frequency. The part used in the 9505A/9522A H1b products is not available lead-free, so a revised part from the same manufacturer will be used.

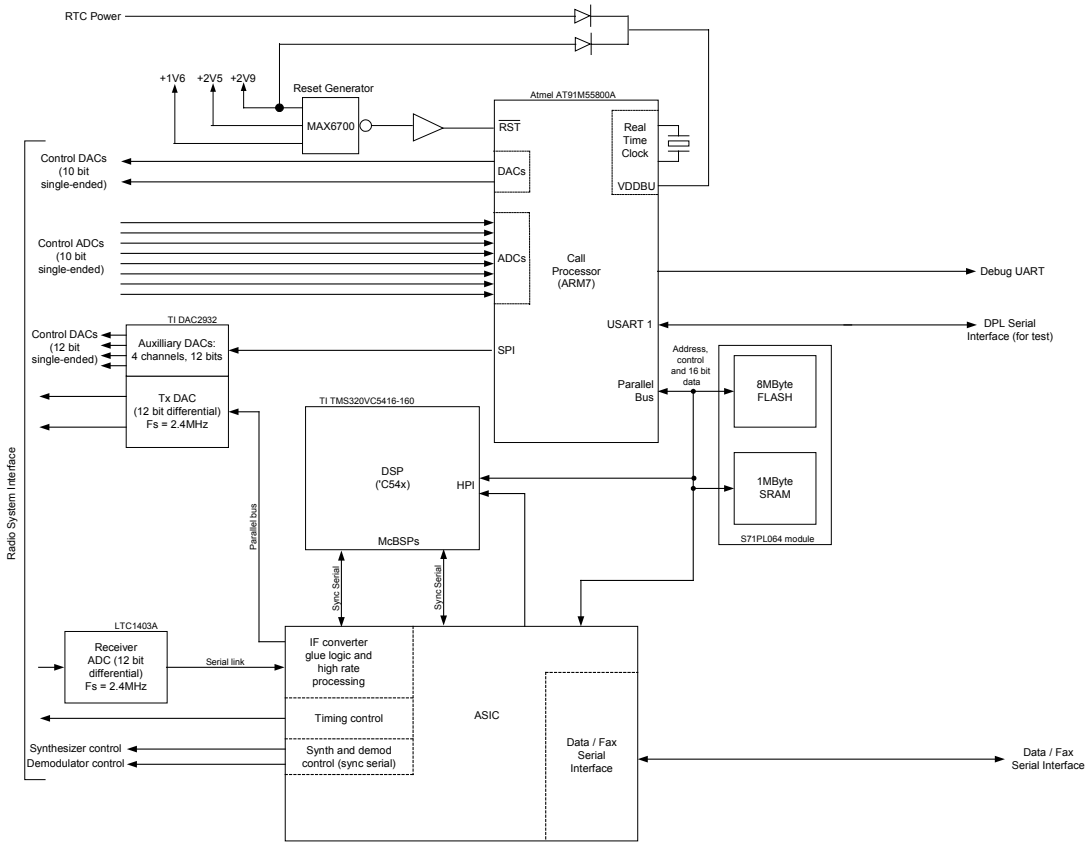
6 Baseband and Digital Design

A block diagram of the design is shown below in Figure 3. The major components are:

- The call processor — an Atmel ARM7 based microprocessor with ADC, DAC and UART peripherals built in. This low cost integrated part removes the need for auxiliary analogue converters in the design. The CP is clocked at 16.8MHz.
- The DSP — a Texas Instruments ‘C5416 part. The DSP is clocked at 151.2MHz.
- An ASIC is used to integrate other logic functions required in the design:
  - high speed signal processing on the IF signals (this lessens the load on the DSP),
  - radio timing control, in conjunction with the call processor,
  - call processor input/output expansion, and
  - UART for the data interface.
- IF analogue/digital interface. The transmit and receive signals are both 600 kHz samples at 2.4 Ms/s. Some of the low-speed converters used for control and monitoring functions are internal devices in the Call Processor and are described there.

A more detailed description of the baseband system is given in the following subsections.

Figure 3: Baseband and Digital Block Diagram



6.1 Call Processor

The call processor (CP), an Atmel AT91M55800A, is the master system processor. It has control of the frame timing: the DSP and all other devices operate as slaves to the CP. The CP device includes not only the processor core, but also the following components in the same part:

- 8k byte of static RAM,
- a power management controller and clock generator block,
- a real time clock (RTC),
- a watchdog timer,
- an interrupt controller,
- three asynchronous serial ports,
- a timer-counter block,
- an SPI interface,
- eight channels of ADC, and

- two channels of DAC.

The built-in peripherals are used as follows.

- Asynchronous serial ports.
  - Digital Peripheral Link
  - Debug
  - Spare.
- ADCs
  - Transmitter output power
  - Supply voltage monitor
  - PCB version detect
  - Five spare
- DACs
  - Frequency trim
  - Transmit output power

6.2 DSP

The DSP, a Texas Instruments TMS320VC5416, uses the EHPI (Enhanced Host Port Interface) for program and data transfer from the CP prior to booting.

The DSP's three Multi-Channel Buffered Serial Ports (McBSPs) are the main data channels in and out of the DSP. They are assigned as shown in Table 1.

McBSP0	IF data: main and auxiliary receiver data to DSP, transmitter data from DSP.
McBSP1	currently spare, used for DSP debug.
McBSP2	Digital Audio (not used in the Data Module)

Table 1: DSP McBSPs

Only McBSP0 is routed to ASIC I/O pins.

The DSP clock input is driven with 16.8MHz from the master oscillator. The DSP code frequency is 151.2MHz, generated from the 16.8MHz input by the internal PLL.

6.3 ASIC

The ASIC contains all the functionality of the FPGA and CPLD used in the Monaco handset and Daytona LBT. Not all of this is used in the Data Module. The IF input is

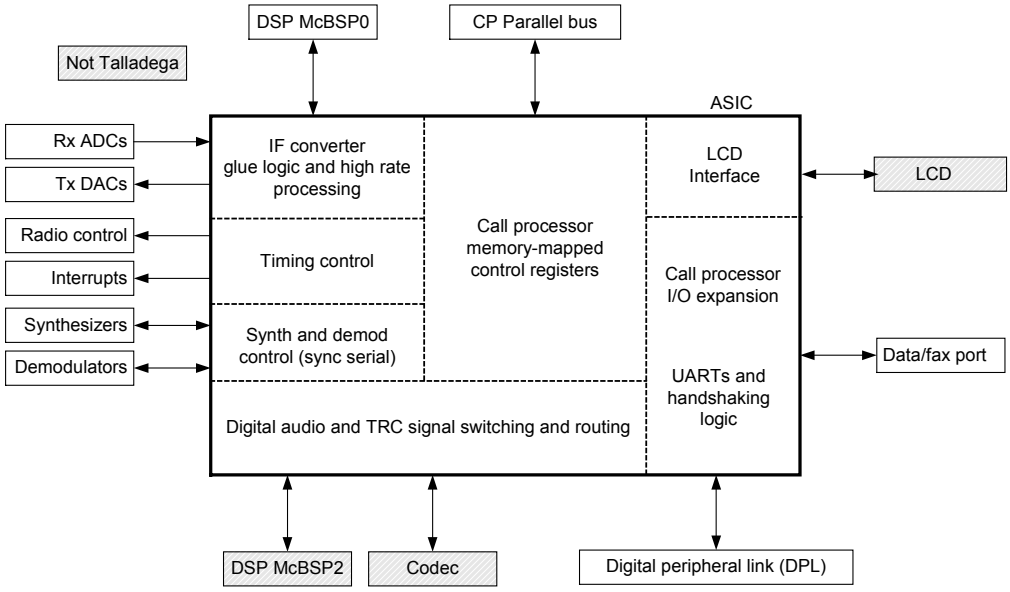
simplified to be compatible with the real-only samples from a single ADC in the receiver chain. The detailed specification is given in reference [9].

Most of the ASIC functions are controlled by the CP, using a memory-mapped interface. The main functions of the ASIC can be summarized as:

- UARTs and PIO expansion for the CP (including ISO 7816-3 SIM interface, not used in the Data Module).
- Timers for control of the radio and other components which must be triggered at specific times within the TDM frame. These process the synthesiser in-lock signal and the transmitter VSWR trip signal.
- IF converter interfacing, between DSP and converters. This includes some high-rate processing operations to reduce the load on the DSP.
- Digital audio switching. Routing of digital audio between the DSP, audio codec, butt connector (not used in the Data Module).
- SPI-like serial interfaces for control of synthesizers and demodulators in the radio (the CP's built-in SPI is limited to 16 bit words, too short for these applications).
- Generation of 11kHz and 700kHz signals.

A block diagram of this arrangement is shown in Figure 4.

Figure 4: ASIC Logic



6.4 IF Converters and Radio Interface

The radio system presents the receiver ADC with the incoming IF signal at 600kHz. This signal is sampled by the receiver ADC at 2.4 M samples/second and fed to the ASIC. A fourteen-bit differential input ADC is used to provide the required noise performance and dynamic range.

In the transmit direction, a dual channel 12-bit differential output DAC is used to provide the 600kHz I and Q IF components to the radio. This DAC is driven at 2.4 M samples/second (per channel) from the ASIC.

The transmit signal DAC contains in addition four auxilliary DAC channels. On the Data Module one of these is used to set the receiver gain, the others are spare.

All timing signals required to enable parts of the radio transmit and receive chains are derived from the timing control block in the ASIC, which in turn is controlled by the CP.

7 DSP Software Design

7.1 Overview

The DSP software is identical to that used in the 9505A/9522A H1b products (DSP version 0x02B). Certain functions are not called, specifically the audio and auxiliary receiver functions.

Figure 5: DSP Subsystem Diagram

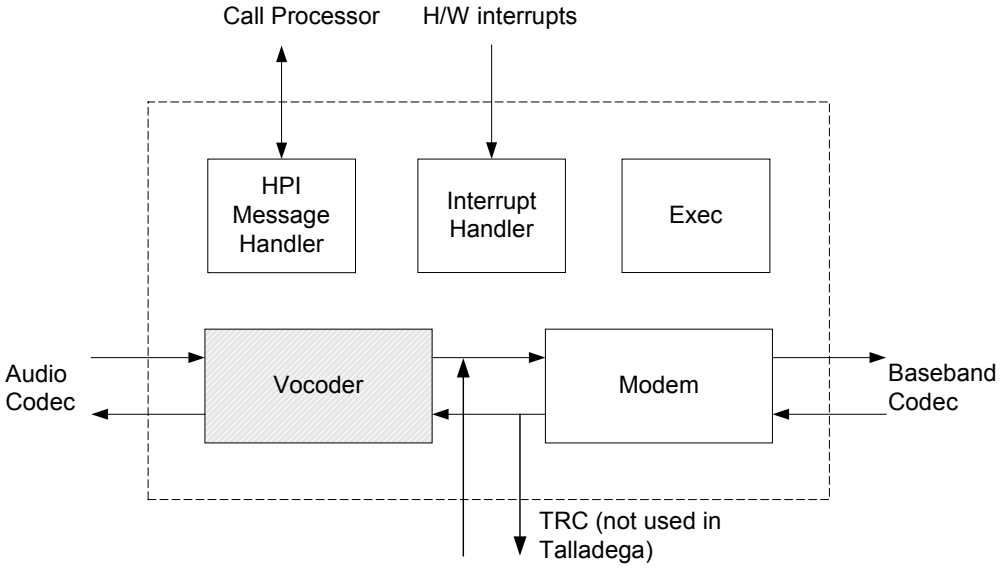


Figure 5 gives a context diagram for the DSP subsystem. There are two top-level signal-oriented processes

- Vocoder: continuous audio sample stream ⇔ bitstream (not used in Tallageda)
- Modem: bitstream ⇔ formatted bursts of RF baseband samples

Additionally, there is an Exec and routines for handling task requests from the call processor (CP) and hardware interrupts. This illustrates that the DSP operates as a slave co-processor for the CP.

7.1.1 Executive

- Scheduling and prioritisation management,
- Bootloader,
- Host port interface,
- Opcode service routine handling, and
- Interrupt service routine handling.

7.1.2 Modem

- The Transmitter modem chain comprises:
  - Packetisation,
  - Coding and interleaving,
  - Remove Envelope Elimination and Reconstruction (EER), and
  - Modulation and root-raised cosine (RRC) filtering.
- The Receiver chain comprises:
  - AGC,
  - Channel filtering,
  - Symbol timing recovery,
  - Phase and frequency offset compensation,
  - QPSK demodulation,
  - De-interleaving and decoding, and
  - Signal quality measurement.

Other DSP modem functions are:

- A second receiver chain giving RSSI (not used),
- Link management measurements,
- Timing management measurements,
- Codec interface (not used),

- Search modes (burst detection), and
- Intra and Inter SV handoff (not used).

7.1.3 Common Routines

General functions used through out the DSP software. This includes code for

- Memory management,
- Library routines, and
- Error handling.

7.2 Operating System

The LEOX operating system is used. LEOX is a pre-emptive exec that is event driven and priority based. It allows the DSP to act as an effective co-processor to the call processor.

8 Call Processor Software Design

8.1 Overview

The Call Processor software is based on the software used in the 9505A/9522A H1b products (CP version IS05001). Several functions of the Call Processor software are obsolete when run on a Data Module, and are therefore removed.

Figure 6: Software Architecture Overview

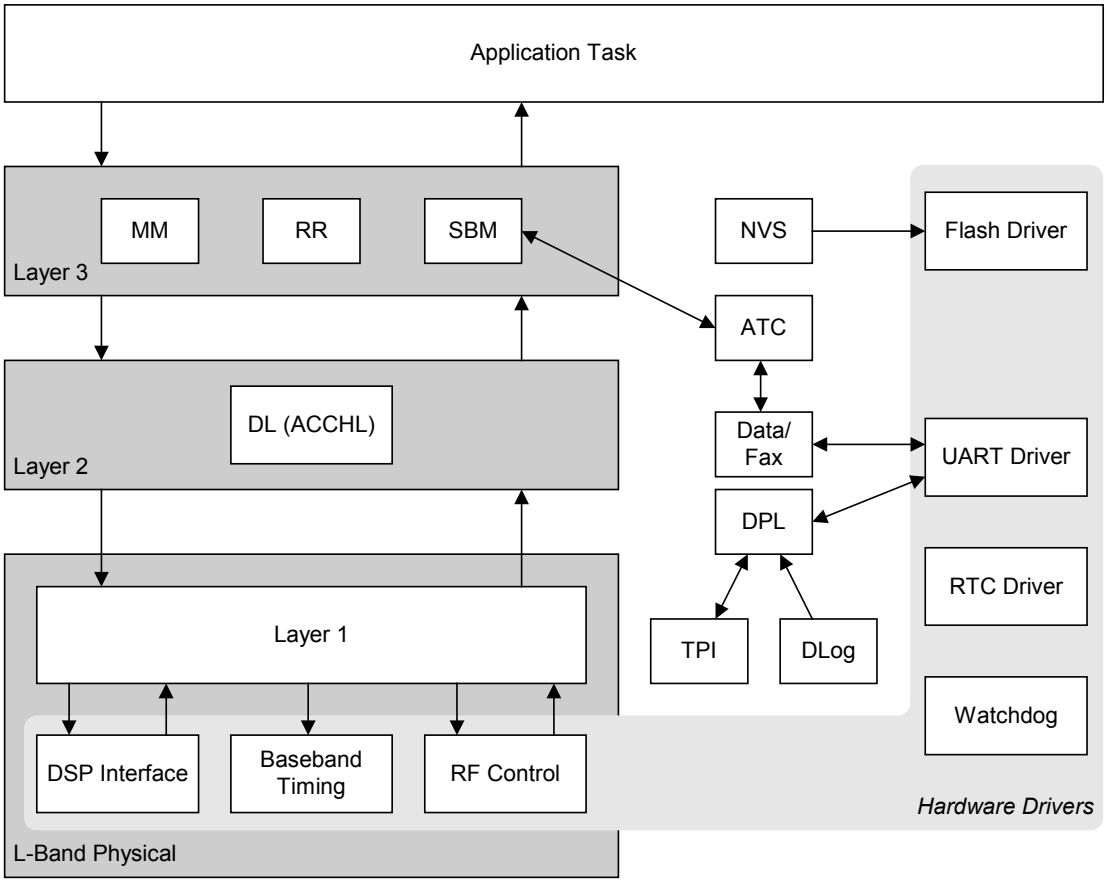


Figure 6 shows an overview of the call processor software architecture. The intention of the diagram is to show the main interactions between software components; please note that there are many interactions not shown in order to reduce the diagram's complexity. In practice the software comprises many smaller components that are either part of, or interact with, those shown.

8.1.1 L-Band Physical

The software implementation of the Iridium L-Band physical layer comprises:

- The Layer 1 task, providing overall control of the physical layer and implementing the L-Band protocol.
- DSP Interface, by which the Layer 1 task instructs the DSP to receive/transmit packets, and the DSP passes received packet information back to Layer 1.
- Control of aspects of the RF chain via interfaces to various DAC and ADC hardware.
- Digital timing of baseband functions, using hardware provided by the CP and by the ASIC.

8.1.2 Layer 2

The Data Link (DL) task provides layer 2 functions. DL implements the Associated Control Channel for L-Band (ACCHL). This is a reliable protocol, and forms the basis of the transfer mechanism used by Short Burst Messaging.

8.1.3 Layer 3

These functions are largely based on adaptations of components of the layer 3 GSM protocol stack.

Mobility Management (MM) is responsible for ensuring that the location of the Data Module is properly registered in the Iridium gateway.

Radio Resources (RR) is responsible for managing link acquisition.

Short Burst Messaging (SBM) implements the SBM air interface, described in reference [5]. It interfaces with ATC to implement the SBM AT commands, described in reference [6]; the other Layer 3 tasks to set up SBM sessions; and Layer 2 to transfer SBM data.

8.1.4 Hardware Drivers

Hardware drivers provide the rest of the software with access to the various hardware devices.

8.1.5 NVS

Non-volatile Storage (NVS) is provided in Flash using the AMD Data Management Software to present EEPROM-like functionality. Data stored in NVS includes the unique identity of the Data Modem, and calibration settings for accurate control of the radio hardware.

8.1.6 ATC

The AT Command (ATC) interface task implements the SBM AT command set (reference [6]), and additional commands useful for the Data Modem (reference [7]).

This allows the device to be used as a modem by an external device via a UART connection.

8.1.7 Data Task

The Data task interfaces the AT command task to the UART driver, providing hardware flow control and initialisation of the port.

8.1.8 Application Task

The Application Task provides overall management of the Data Modem software, including startup/shutdown sequencing and idle state management to conserve power.

8.1.9 DPL

The Digital Peripheral Link (DPL) task implements the serial asynchronous communications link between the Data Modem and external peripherals, as described in reference [4].

This is only used for development and testing; the only peripherals supported by the Data Modem are an external tester and a data logger:

- Test Port Interface (TPI): Interfaces (via DPL) with the external test equipment used during factory test for calibration and verification.
- Data Logger (DLog): Interfaces (via DPL) with an external data logger to capture details of the communication flows between the software tasks for diagnostic purposes.

8.2 DSP Interface

The DSP interfaces to the Call Processor as a memory-mapped peripheral. The interface is defined by Texas Instruments and is known as the enhanced Host-Port Interface (HPI8). The interface operates as an 8-bit wide parallel port providing access to shared memory within the DSP, supported by a DMA controller. Using this interface the call processor is able to access the on-chip DSP memory for sending commands/data to the DSP and reading processed data out. Interrupts are used to provide notification of commands and processed data.

Although the TMS320VC5416-160 DSP has a 16-bit version of HPI, this does not support interrupts, so the interface is used in 8-bit mode.

8.3 Baseband Timing

8.3.1 CP Timers

The CP has a total of 6 timers, grouped into two blocks of three: timer block 0, comprising timer-counters TC0, TC1 and TC2, and timer block 1, comprising timer-

counters TC3, TC4 and TC5. Each timer-counter can drive two CP I/O pins, but these pins can also be controlled as PIO.

Timer block 0 is reserved for internal software timing tasks, nothing in the hardware design requires the use of these timers to drive their associated output pins.

Timer block 1 is used for hardware timing functions. TC3 is used as the Master Frame Timer. This counter is driven by a 700kHz clock and reset by the 90ms frame tick, both generated in the ASIC and fed to the CP timer block 1 via input pins TCLK3 and TCLK4 respectively. Output pin TIOA3 carries the CH_FRM frame tick signal to the ASIC, which is used to reset the Channel Frame Reference timer.

TC4 is unused.

TC5 is used internally to the CP to trigger an ADC conversion of the transmit power detect signal at a specific point in each transmit burst. However, this means that the TIOA5 pin is unavailable for input or output.

8.3.2 ASIC Timers

The CP has insufficient timer outputs to control the radio. The ASIC provides the necessary timers, and the CP controls them using the Timer Action Module (TAM) driver.

8.4 RF Control

The CP provides DAC and ADC hardware that is used to control aspects of the RF such as power measurements.

The Monaco RF control software consists of the following:

- On-chip ADC driver
- On-chip DAC driver
- Driver for off-chip DAC
- Synthesiser tuning driver

8.5 Real Time Clock Driver

The Atmel AT91M55800A microcontroller provides an on-chip real time clock.

8.6 UART driver

The UART driver provides access to the UART hardware through re-implemented standard C library calls (stdio). Additional functions are provided to configure baud rate, character size and parity and for configuring the Data port flow control. The UART driver provides all the buffering and interrupt handling needed to control the three USARTS within the Atmel chip and the additional UARTs on the ASIC.

8.7 Reflected Power Trip

As stated in section 5.3.3 the Talladega Data PA has to be protected against an unacceptably high level of reflected power from the antenna. This is detected by measuring the Voltage Standing Wave Ratio (VSWR). If the antenna were removed the high VSWR would cause the transmitter to be shut down and a status line VSWR_TRIP is set to inform the CP.

The CP aborts the current call (if one is in process), sets an "antenna fault" indicator which will notified the host with an unsolicited result code, log a non-fatal error and revert to normal idle-mode operation listening for the ring channel. Upon a successful receive, the CP clears the antenna fault indicator and returns to normal operation.

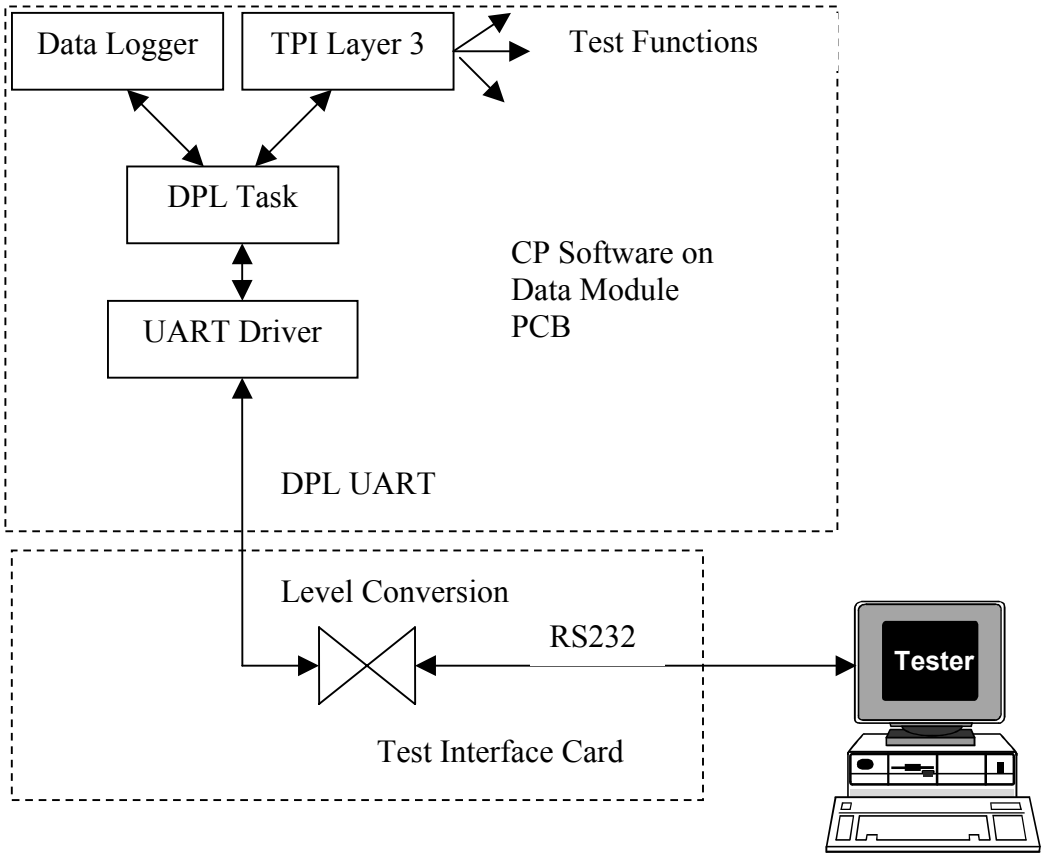
8.8 Operating System

The *Nucleus Plus* RTOS operating system is used.

8.9 Built in Test

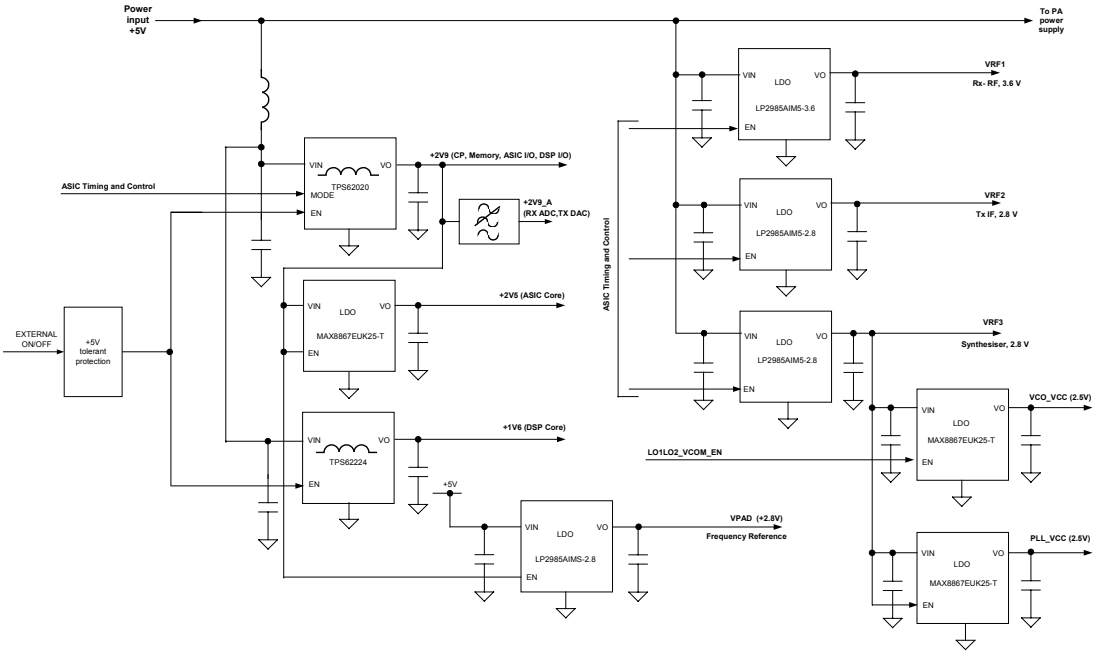
Self-test is performed at startup. Additional built-in test is provided by the Test Port Interface (TPI - See C7032-S-025). Additional logging and error reporting is provided by a datalogging task. DLOG and TPI traffic share the DPL link (See C7032-S-018) which is available on the Data Module's user connector; routing software may be required on the test PC to separate out TPI and DLOG traffic.

Figure 7: Test Configuration



9 Power Supply Design

Figure 8: Power Supply Block Diagram



9.1 PA Supply

The P1 Data Module uses the Celeritek CSM20402 PA module operating at reduced power. From P2 onwards this is replaced by the CSM20403 2W PA. In both cases the PA is powered directly from the 5V input. The PA current during the transmit burst is approximately 1.5 Amps. The PA bias supply is considered to be part of the PA rather than part of the power supply design.

9.2 Other supplies

The digital supplies are produced by two switching regulators operating from the 5 V input. The ASIC core supply is produced from the main digital supply by a linear regulator. The signal path ADC and DAC converters are powered by a filtered version of the main digital supply. The frequency reference will have its own linear regulator.

The radio circuits have three supplies. Two of these are continuously present, one for the synthesiser and one for the receiver IF stage. Both of these have registers which would need re-loading if the supplies were turned off. The third supply is switched on during a transmit burst to power the transmitter IF and RF circuits. The synthesiser uses local sub-regulation for the PLL device and the oscillators.

9.3 Current Consumption

The maximum current consumed by the Data Module does not exceed 1.8A at 5.0V DC.

The average current consumption during a call does not exceed 0.35A at 5.0 V DC.

The average power consumption during a call does not exceed 1.75 Watts at 5.0 V DC.

The peak current will rise to not more than 2 Amps at maximum supply voltage (5.5 V DC).

10 Physical Requirements

10.1 Size

The Data Module must be compact (100mm x 50mm x 15mm) and lightweight (<69g). To this end components selected for this design should be as small as possible (but no smaller that 0402 for passives so as not to increase manufacturing complexity and hence cost).

10.2 Cost

The Data Module must not be too expensive or it will fail to sell into its intended market. The material costs (for 100K volume) should be $234 maximum with a target of $209.

This target impacts on the physical constraints of the Data Module, it must be simple and hence cost effective to manufacture. The number of layers and complexity of the pcb (blind vias, special finishes) should be kept to a minimum to achieve the design within the size constraints.

10.3 Screening

The Data Module must not interfere with itself or with other equipment housed with it, to prevent this the RF side of the Data Module will be screened and the synthesisers screened from the other RF sections. The Transmitter and Receiver do not need to be screened from each other as they are never active at the same time.

The screening can should be simple to make and to assemble onto the board. The plan after discussions with the manufacturer is to have a separate can wall which can be hand soldered over the RF circuits after functional test and then a push on lid, this allows easy access to components under the can during development.

11 Antenna Requirements

Although an antenna is not provided as part of the Talladega Short Burst Data Module, the module does place constraints upon the type of antenna that can be used.

The antenna must be RHCP. It should be nominally omni-directional over a hemisphere and have a maximum gain of 3dBi. The gain at harmonic frequencies should not be any higher than at the fundamental. The VSWR should be not more than 1.5:1 for best performance.

12 Appendix A, internal analogue/digital interfaces

The following tables list the signal, control, status and power signals between the baseband/digital and the analogue/RF sides of the Talladega PCB.

12.1 Analogue IF

Signal Name	Direction	Function	Electrical
RX_P	RF to BB	Receiver 600 kHz IF output	1.875 V dc plus 1.25 V pk-pk ac
RX_N			0.625 V dc plus 1.25 V pk-pk ac
VREF_2V5	BB to RF	ADC reference voltage used by Rx IF to set dc levels	2.5 Volts
TX_I_P	BB to RF	Transmitter 600 kHz drive, I component	0.19 V dc common-mode plus 0.76 V max. pk-pk differential ac
TX_I_N			
TX_Q_P	BB to RF	Transmitter 600 kHz drive, Q component	0.19 V dc common-mode plus 0.76 V max. pk-pk differential ac
TX_Q_N			

12.1.1 Analogue control and sense signals

Signal Name	Direction	Function	Electrical
RXM_VGC	BB to RF	Receiver IF gain control. External DAC 3	0 to 2.55 V, 4096 steps. 2.1 V for max. gain, approx. 45 dB reduction at 1.5 Volt
TX_PWR_CNTL	BB to RF	Controls the transmit IF gain. CP DAC DA1	0 to 2.55 V, 1024 steps. Full scale at DAC for max. output, 20 dB reduction at 60% of full scale

Signal Name	Direction	Function	Electrical
REF_OSC_VC	BB to RF	Reference oscillator frequency adjustment control voltage CP DAC DA0	0 to 2.55 V, 1024 steps Operating range 0.5 to 2.5 V
TX_PA_VDD_ MON	RF to BB	Monitors the main supply rail to the PA module. CP ADC AD5	0 to 2.55 V (10-bit ADC) ADC full scale corresponds to 8 V supply
TX_PDETECT_F	RF to BB	Transmit Output power detector voltage CP ADC AD7	0 to 2.55 V (10-bit ADC) 1.5 V nominal at full power
TX_PDETECT_R	RF to BB	Transmit reflected power detector voltage CP ADC AD3	0 to 2.55 V (10-bit ADC) 2.0 V nominal at full power and 3:1 VSWR

Note that the processor ADCs and DACs, although 10 bits, are only accurate to 8 bits, see Atmel AT91M55800A data sheet.

12.1.2 Digital control bus

There are two serial control buses. One controls the receiver IF chip and is used to set it to use an external VCO. The other serial bus is used to programme the synthesisers.

Signal Name	Direction	Function	Electrical (RF requirements)
RX_SER_DATA	BB to RF	Receiver 3-wire serial bus data	Logic 0, 0 to 0.5V Logic 1, 2.0 to 2.8 V
RX_SER_CLK	BB to RF	Receiver 3-wire serial bus clock	Logic 0, 0 to 0.5V Logic 1, 2.0 to 2.8 V
RXM_SER_ENB	BB to RF	Receiver 3-wire serial bus enable signal	Logic 0, 0 to 0.5V Logic 1, 2.0 to 2.8 V
PLL_SER_DATA	BB to RF	Synthesiser 3-wire serial bus data	Logic 0, 0 to 0.4V Logic 1, 1.6 to 2.5 V
PLL_SER_CLK	BB to RF	Synthesiser 3-wire serial bus clock	Logic 0, 0 to 0.4V Logic 1, 1.6 to 2.5 V

Signal Name	Direction	Function	Electrical (RF requirements)
PLL_LO1MLO2_ ENB	BB to RF	Synthesiser 3-wire serial bus enable	Logic 0, 0 to 0.4V Logic 1, 1.6 to 2.5 V

12.1.3 Discrete digital control and status

Signal Name	Direction	Function	Electrical (RF requirements)
TX_PREKEY	BB to RF	Changes the T/R switch from receive to transmit	Logic 0, 0 to 0.4 V Logic 1, 2.0 to 2.8 V
TX_OK	BB to RF	Enables the Tx IF chip at the same time as TX_PREKEY, provided that the synthesise is locked	Logic 0, 0 to 0.4 V Logic 1, 2.0 to 2.8 V
TX_PA_CTL	BB to RF	Enables the transmitter IF and RF circuits. Goes low in the event of a VSWR trip	Logic 0, 0 to 0.15V Logic 1, 1.6 to 5 V
RXM_SHDNB	BB to RF	Enable line for the receiver IF and second converter	Logic 0, 0 to 0.5V Logic 1, 2.0 to 2.8 V
RXM_STBYB	BB to RF	Allows part of the receiver IF to be disabled. Should be set to 1 during transmit	Logic 0, 0 to 0.5V Logic 1, 2.0 to 2.8 V
LO1LO2_VCOM _EN	BB to RF	Enables the synthesiser LO1 and LO2 VCOs	Logic 0, 0 to 0.4V Logic 1, 2.0 to 2.8 V
LO1_BUFM_EN	BB to RF	Enables the LO1 and LO2 buffers	Logic 0, 0 to 0.5V Logic 1, 2.0 to 5 V
PLL_LOCK_DE TECT	RF to BB	Indicates that the synthesiser phase-locked loops are locked	Logic 0, 0.4V max at 500 μA sink Logic 1, 2.1 V min at 500 μA source
VSWR_TRIP	RF to BB	Indicates that the VSWR trip has shut down the transmitter. Signal clears after the burst.	Logic 0, 0.2V max at 100 μA sink Logic 1, 2.7 V min at 100 μA source

Signal Name	Direction	Function	Electrical (RF requirements)
REF_16M8	RF to BB	16.8 MHz reference clock	Logic 0, 0.2V max. Logic 1, VPAD – 0.2 V minimum
EN_RF1	BB to RF	Enables the receiver RF power supply	Logic 0, 0 to 0.15V Logic 1, 1.6 to 5 V
EN_RF2	BB to RF	Enables the receiver and transmitter IF power supply	Logic 0, 0 to 0.15V Logic 1, 1.6 to 5 V
EN_RF3	BB to RF	Enables the synthesiser power supply	Logic 0, 0 to 0.15V Logic 1, 1.6 to 5 V

12.2 Power supplies for RF circuits

The RF circuits are powered from the5 Volt supply via local sub-regulators. These are under control of the CP. The enable signals for these regulators are included in the table above.

Signal name	Signal function	Electrical
VRF1	Powers the receiver RF circuits. May be turned on and off for each receive burst.	3.6 V, 60 mA maximum
VRF2	Powers the transmitter and receiver IF stages. If turned off then the receiver IF/mixer chip needs re-programming.	2.8 V, 50 mA maximum
VRF3	Powers the synthesisers. If turned off then the synthesiser chip needs re-programming.	2.8 V, 60 mA maximum
VPAD	Supplies 16.8 MHz oscillator and buffer	2.8 V, 80 mA maximum

The transmitter RF circuits are powered directly from the main 5 V input, hence there is no AVCC supply.

13 Appendix B, 25-way D connector pin-out

The P1 units were intended to be mounted in a screened enclosure, and the external user connector was a 25-way male D type connector. The pin out for this connector was chosen so that it would be safe when connected to a Daytona cable. The filter board C7321-CD-006a converts the internal 26-way pin-out to the external 25-way pin-out. The pin-out of this 25-way connector is given in the table.

Feedback from potential customers has resulted in a change to a 26-way external connector for later versions of the Talladega. This will use the same pin-out as the connector on the board.

Contact	Signal	Description
1	ON/OFFB	On/Off control input
2	Ext 11 HZ	90ms “frame sync” signal (used in testing)
3	0V	Power supply negative
4	+5 V	Power input
5		
6	+2V9	Supply output
7	DF_RI	Data port, Ring Indication output
8	DF_RTS	Data port, Request to Send input
9	DF_S_TX	Data port, serial data input
10	DF_DCD	Data port, Data Carrier Detect output
11		
12	NETWORK_AVAILABLE	Network Available logic output
13	DF_S_RX	Data port, serial data output
14	Gnd	Signal ground
15	Gnd	Signal ground
16	+5 V	Power input/sense. May be used for remote sensing, otherwise connect to pin 4.
17	0 V	Power supply negative/sense. May be used for remote sensing, otherwise connect to pin 3.
18	DPL_TX	Digital Peripheral Link serial data output
19	DF_DTR	Data port, Data Terminal Ready input
20	DPL_RX	Digital Peripheral Link serial data input
21	DF_DSR	Data port, Data Set Ready output
22	DF_CTS	Data port, Clear to Send output
23	Gnd	Signal ground
24	RTC power	Optional RTC power input
25	Gnd	Signal ground

Table 2: 25-way connecor pin-out

14 Appendix C, protection requirements for filter board

The Talladega module will be mounted in a metal enclosure for type approval testing. The external connector will be mounted on a filter board with filtering components close to the opening in the metal case. The filter board will have a flexible cable connecting to the user connector on the Talladega pcb. The external connector will be either a 25-way D type connector (early versions) or a 26-way 2mm pitch 2-row latching header connector (later versions). It will be tested for the following susceptibilities and emissions.

1. ESD susceptibility. 4 kV direct contact and 8 kV air discharge, both into unit under test and into a conducting plate.
2. RF field susceptibility. 3V/m 80% AM at 1 kHz, 80 MHz to 1 GHz and 1.4 to 2 GHz.
3. Fast Transient susceptibility. 0.5 kV pulses coupled into connecting cable (ancillary equipment not under test is protected by a Line Impedance |Stabilisation Network).
4. RF conducted susceptibility. 3V rms 80% AM at 1 kHz, 0.15 to 80 MHz, coupled into cables with a clamp transformer.
5. RF conducted emissions on cables other than the antenna cable.

For 4 and 5 above, the coupling point will be different for RS-232 and logic-level configurations. For logic levels the Test Interface Card is close to the Talladega, so the coupling point is between the TIC and the ancillary equipment (PSU and PC). For RS-232 levels the injection point is the cable between the Talladega and the TIC. This has an impact on the protection circuits needed on the DPL interface (the DPL interface is needed to generate activity in the Talladega while the susceptibility tests are performed).