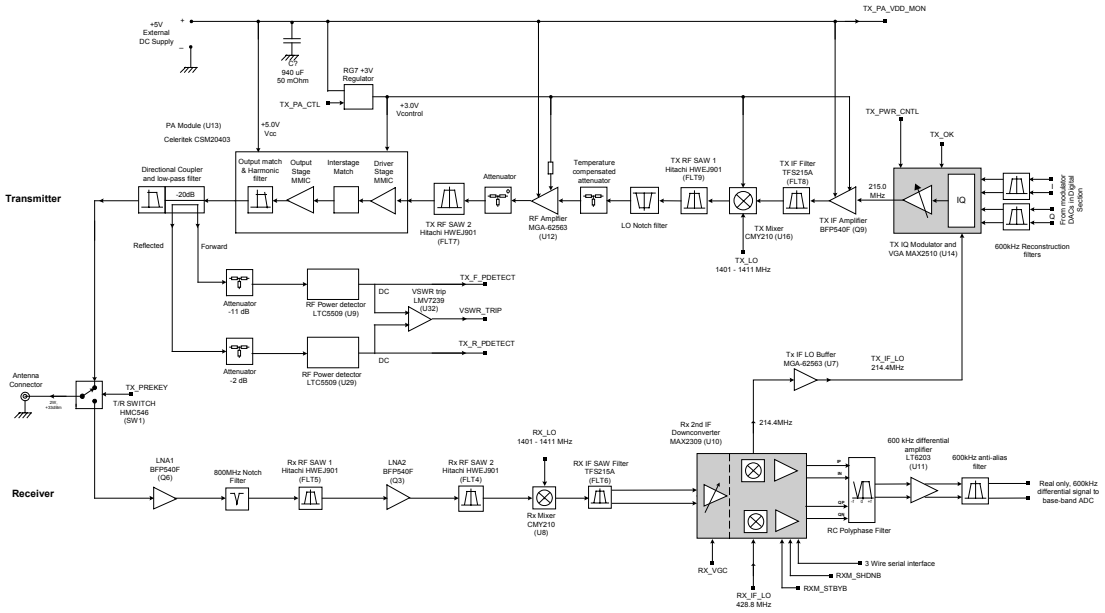
5 RF Chain Design

Figure 2: Receiver and Transmitter Block Diagram, Analogue Sections



5.1 Frequency Plan

The block diagram for the RF and IF analogue sections of the transmit and receive architecture is shown in Figure 2.[3]

The receiver is a conventional dual conversion superhet with an RF input of 1616MHz to 1626.5MHz, a first IF of 215MHz and a low second IF of 600kHz. A real-only output is provided at the second IF frequency for analogue-to-digital conversion at a sample rate of 2.4 MHz. The image of the second mixing process is suppressed by means of a two-section polyphase filter. The ASIC performs a final frequency conversion to bring the signal to a quadrature pair at zero frequency.

The transmit frequency plan is identical although the architecture is different. The DSP processor generates a pair of baseband quadrature components at a sample rate of 200 kHz. In digital hardware these are translated to an IF of 600 kHz at a sample rate of 2.4 MHz. The two quadrature components are converted to analogue signals in the DACs, filtered to remove alias components and translated in a single-side band mixer to an IF of 215 MHz. After filtering the signal is then mixed to the output frequency of 1616 to 1626.5 MHz.

[3] The first spin on the Talladega PCB will use the H1b 8W PA, all subsequent spins will use the new lower power 2W PA.