

Declaration Letter

We hereby declare that our products don't contain NFC functionality

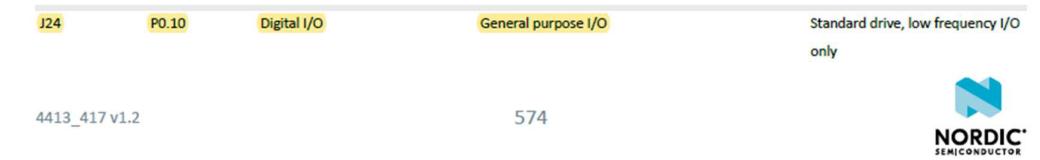
Model No.: [LMSW-610-S](#), [LMSW-611-S](#), [LMSW-622-S](#), [LMSW-641-S](#)

FCC ID: [Q4B-TFFD](#)

IC: [23947-TFFD](#)

The principle of disable the NFC function as below:

In nRF52840, NFCT use two pins to connect the antenna and these pins are shared with GPIOs. In existing design, these pins are not configured as NFCT pins and not add Nordic official NFC library to firmware, these two pins are configured as normal GPIO operation that shorted together, device will not detect NFC field when a NFC field is presence.



Hardware and layout

Pin	Name	Function	Description	Recommended usage
	NFC2	NFC input	NFC antenna connection	
K2	P0.05	Digital I/O	General purpose I/O	
	AIN3	Analog input	Analog input	
L1	P0.06	Digital I/O	General purpose I/O	
L24	P0.09	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only
	NFC1	NFC input	NFC antenna connection	

6.14.3 Pin configuration

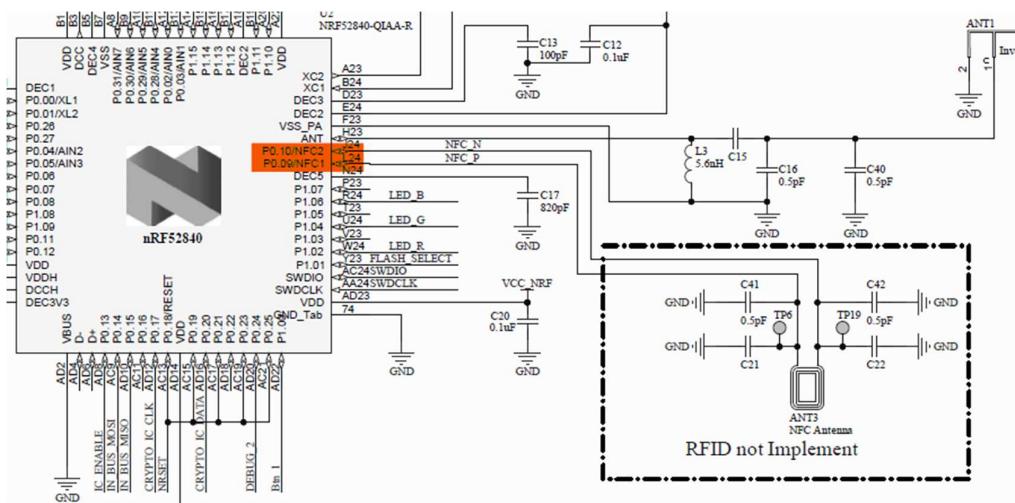
NFCT uses two pins to connect the antenna and these pins are shared with GPIOs.

The PROTECT field in the NFCPINS register in UICR defines the usage of these pins and their protection level against excessive voltages. The content of the NFCPINS register is reloaded at every reset. See [Pin assignments](#) on page 573 for the pins used by the NFCT peripheral.

When NFCPINS.PROTECT=NFC, a protection circuit will be enabled on the dedicated pins, preventing the chip from being damaged in the presence of a strong NFC field. The protection circuit will short the two pins together if voltage difference exceeds approximately 2V. The GPIO function on those pins will also be disabled.

When NFCPINS.PROTECT=Disabled, the device will not be protected against strong NFC field damages caught by a connected NFCT antenna, and the NFCT peripheral will not operate as expected, as it will never leave the DISABLE state.

The pins dedicated to the NFCT antenna function will have some limitation when the pins are configured for normal GPIO operation. The pin capacitance will be higher on those (refer to C_{PAD_NFC} in the Electrical Specification of [GPIO — General purpose input/output](#) on page 147), and some increased leakage current between the two pins is to be expected if they are used in GPIO mode, and are driven to different logical values. To save power, the two pins should always be set to the same logical value whenever entering one of the device power saving modes. For details, refer to I_{NFC_LEAK} in the Electrical Specification of [GPIO — General purpose input/output](#) on page 147.




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