



AW-BT105A

Bluetooth Module IC

For Mobile Phones, DSCs, PMPs and Gaming Devices

Datasheet

Version 0.1

Document release	Date	Modification	Initials	Approved
Version 0.1	2009/1/13	Initial Version	N.C. Chen	CE Huang

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1. General Description

1-1. Product Overview and Functional Description

AzureWave Technologies, Inc. introduces the Bluetooth module IC---AW-BT105A. The module IC is targeted to mobile devices including Mobile Phones, Digital Still Cameras (DSCs), Portable Media Players (PMPs), Personal Digital Assistants (PDAs), and Gaming Devices which need small footprint package, low power consumption, multiple interfaces and OS support. By using AW-BT105A, the customers can easily enable the BT embedded applications with the benefits of high design flexibility, short development cycle, and quick time-to-market.

Compliance with the Bluetooth standard, the AW-BT105A is a **Bluetooth 2.1+Enhanced Data Rate** (EDR) product. Bluetooth 2.1+Enhanced Data Rate (EDR) can make it easier to connect devices, lower power consumption and improved security.

The AW-BT105A supports **High speed UART** interface is available to connect the BT core the host processor. AW-BT105A is suitable for multiple mobile processors for different applications. With the support **cellular phone co-existence**, the AW-BT105A is also the best solution for mobile phones and PDA phones applications.

AW-BT105A module adopts CSR's Bluetooth SoC---BC6. All the other components are implemented by all means to reach the mechanical specification required. AW-BT105A uses IC module integration **package** technology that provides customers mounting mechanism to secure the AW-BT105A module against vibration and shock on the host system. AW-BT105A uses module IC integration package technology can provide more **reliable** and **strong** electrical and mechanical performance.

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1-2. Key Features

- Small footprint: 9.6mm(L) x 9.6mm(W) x 1.2 mm(H)
- **4** Fully Qualified Bluetooth v2.1 + EDR system
- Enhanced Data Rate (EDR) compliant with Bluetooth v2.1 + EDR specification for both 2Mbps and 3Mbps modulation modes
- **4** Full Speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- High speed UART interface for Bluetooth
- **Audio PCM interface**
- **4** 802.11 co-existence support
- Lead-free design

1-3. Block Diagram

 UART
 Ktal

 CSR
 2.4 GHz

 BC6
 2.4 GHz

 BFF
 BFF

Audio
CM
AureWave AW-BT105A

A simplified block diagram of the AW-BT105A module is depicted in the figure below.

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1-4. Specifications Table

Model Name	AW-BT105A
Product Description	Bluetooth Module IC
Bluetooth Standard	Bluetooth 2.1+Enhanced Data Rate (EDR)
Host Interface	UART for Bluetooth
Major Chipset	CSR BC6
Dimension	9.6mm x 9.6mm x 1.2mm
Weight	Less than 10 grams
Package	LGA
Operating Conditions	
Temperature	Operating: -20 ~ 75°C ; Storage: -40 ~ 85°C
Voltage	Module Main Power: 3.3V/ Host I/O Voltage Supply: 1.8V/3.3V
Humidity Non-Operating	50 ~92% RH non-condensing (at temperatures of 25 °C to 80 °C)
Electrical Specifications	
Freq Range	2.4GHz ISM Band
Number of Channels	2.402GHz~2.480GHz, 1MHz/Channel
Modulation	GFSK,DQPSK (2Mbps) and 8DPSK (3Mbps)
Output Power	Typical power: Bluetooth Class 1.5
Receive Sensitivity	GFSK:TBD π /4 DQPSK:TBD 8DPSK:TBD
Medium Access Protocol	CSMA/CA with ACK
Data Rates	2.1+EDR data rates of 1,2, and 3Mbps
Power Consumption	Peak Tx Current : 47mA Peak Rx Current : 47mA Standby host connection (Deep-Sleep) : 59uA
Operating Range	Minimum 10 m indoor for Bluetooth The transmission speed may vary according to the environment)
Operating System Compatibility	Win CE 4.2/.NET, Win CE 5.0, Linux, Pocket PC 2004/2005
Co-Existence	WLAN co-existence

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2. Electrical Characteristics

2-1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Тур	Max	Units
3.3V	3.3V power supply		-0.4	3.3	3.7	V
VIO_X1	I/O power supply		-0.4		3.7	V

2-2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Тур	Max	Units
3.3V	3.3V power supply		2.7	3.3	3.7	V
VIO_X1	1.8Vor 3.3V I/O power supply		1.7		3.7	V

2-3. Power Consumption

Test Conditions								
Module input power	3.3V							
I/O Voltage level	3.3V							
Host Interface	UART							
UART Baud Rate	115200 bps							
Clock Source	26MHz Crystal							
Device Activit	y/State							
Peak Tx Current	47 mA							
Peak Rx Current	47 mA							
Standby host connection (Deep-Sleep)	59 uA							
RF output power	2.2 dBm							

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2-4. Audio CODEC Interface

The AW-BT105A Audio Interface Unit(AIU) consists of an audio interface module.

2-4-1. Audio interface Signals

Pin No	Definition	Basic Description	Туре	
28	BT_PCM_DOUT	PCM Mode:BT_PCM_DOUT BT_PCM_DOUT output	0	
54	BT_PCM_CLK	PCM Mode:BT_PCM_CLK BT_PCM_CLK input/output	I/O	
56	BT_PCM_SYNC	PCM Mode:BT_PCM_SYNC BT_PCM_SYNC input/output(output if PCM initiator, input if PCM target)	0	
58	BT_PCM_DIN	PCM Mode: BT_PCM_DIN BT_PCM data input signal	I	

2-4-2. PCM Interface

The AW-BT105A can operate as the PCM interface master generating an output clock of 128, 256, 512,1536 or 2400kHz. When configured as a PCM interface slave, it can operate with an input clock up to 2400kHz. AW-BT105A is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

2-4-2.1. Protocol Description

When configured as the master of the PCM interface, BlueCore6 generates PCM_CLK and PCM_SYNC



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When configured as the Slave of the PCM interface, BlueCore6 accepts PCM_CLK rates up to 2400kHz



2-4-3. Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore6 is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore6 is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5µs long.

PCM_SYNC										
PCM_CLK										
PCM_OUT		1	2	3	4	5	6	7	8	
PCM_IN	Undefined	1	2	3	4	5	6	7	8	Undefined

Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore6 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.



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2-3-4. Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

PCM_SYNC																				
PCM_CLK								\Box			\Box				Л	\Box		Π	Л	
PCM_OUT		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16-	-		
PCM_IN	Undefined	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	l	Unde	fined

Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore6 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

2-3-5. Multi-Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.



Multi-slot Operation with Two Slots and 8-bit Companded Samples



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2-3-6. Modes of Operation

The PCM interface supports two modes of operation:

- PCM master
- PCM slave

BlueCore6 has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECs use to control power down.



PCM Master Timing Long Frame Sync



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PCM Slave Timing Short Frame Sync

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3. Pin Definition

3-1. Pin Assignment

Pin No	Definition	Basic Description	Туре	
1	GND			
2	RF IN/OUT	RF port for antenna or RF connector(Please keep matching circuit)		50Ohm @2.4GHz
3	GND			
4	GND			
5	WLAN_ACT	NC (for monitoring BT/WLAN coexistence interface)		
6	NC			
7	PIO[2] / CLK_REQ_OUT	Programmable input/output line		
8	SPI_CS#	NC (for monitoring SPI Test chip select (active low))		
9	3.3V	3.3V main power supply		
10	Wake	BB MAC wake-up in		
11	NC			
12	GND			
13	NC			
14	NC			
15	BT_STATE	NC (for monitoring BT/WLAN coexistence interface)		
16	NC			
17	UART_RX	UART data input active high		
18	NC			
19	NC			
20	SPI_MISO	NC (for monitoring SPI Test data output)		
21	UART_CTS	UART CTS input: Clear to send input from the modem, data set, or peripheral device.		
22	CLK_32K	NC (for 32kHz external reference clock input)		
23	SPI_MOSI	NC (for monitoring SPI Test data input)		
24	GND			
25	NC			
26	NC			
27	NC			
28	PCM_OUT	BT_PCM_DOUT output		
29	NC			
30	UART_TX	UART data output active high		
31	NC	NC		
32	BT_PRIORITY	NC (for monitoring BT/WLAN coexistence interface)		
33	NC			

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Pin No	Definition	Basic Description	Туре
34	NC		
35	NC		
36	GND		
37	NC		
38	VIO_X1	1.8V/3.3V Host I/O Voltage Supply	
39	RESETn	Reset if low. Input debounced so must be low for >5ms to cause a reset	
40	NC		
41	NC		
42	NC		
43	NC		
44	NC		
45	NC		
46	GND		
47	GND		
48	GND		
49	GND		
50	NC		
51	GND		
52	GND		
53	GND		
54	PCM_CLK	Synchronous data clock	
55	NC		
56	PCM_SYNC	Synchronous data sync	
57	SPI_CLK	NC (for monitoring SPI Test clock)	
58	PCM_IN	Synchronous data input	
59	NC		
60	NC		
61	GND		
62	NC		
63	UART_RTS	UART request to send active low	
64	GND		

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4. Mechanical Characteristics

The size and thickness of the AW-BT105A System in Package (SiP) module is listed below:



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Unit: mm

Note: AzurWave will provide AW-BT105A Top View FootPrint DXF file for customer reference.

49

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5. Package Information

5-1. Recommended Reflow Profile

Reflow Soldering Profile

Note: 1. Recommend to supply N₂ for reflow oven

2. N₂ atmosphere during reflow (O₂<300ppm)

5-2. Device Handling Instruction(Module IC SMT Preparation)

5-2-1. Shelf life in sealed bag:12 months, At<30℃ and <60% relative humidity(RH)

5-2-2. After bag is opened, devices that will be

- 5-2-2-1. Baked for 24 hours at $125+-5^{\circ}C$ with tray
- 5-2-2-2. Re-baked required after last baked with window time 24 hours

5-2-3. Recommend to Oven bake with N2 supplied

5-2-4. Recommend end to Reflow Oven with N2 supplied

5-2-5. Baked required with 24 hours at 125+-5 $^\circ\!\!\mathbb{C}$ before rework process for two modules, one

is new module and two is board with module

5-2-6. Recommend to store at \leq 10% RH with vacuum packing

5-2-7. If SMT process needs twice reflow:

5-2-7-1. Process flow: (1) Top side SMT and reflow \rightarrow (2) Bottom side SMT and reflow

- 5-2-7-1-1. Case 1: Wifi module mound on Top side. Need to bake when bottom side process over 24 hours window time, no need to bake within 24 hours
- 5-2-7-1-2. Case 2: Wifi module mound on bottom side, follow normal bake rule before process

Note: Window time means from last bake end to next reflow start that has 24 hours space.

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