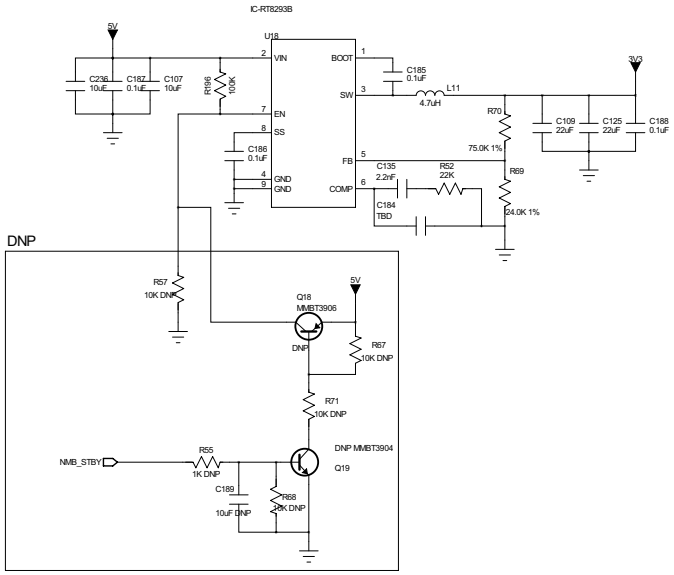
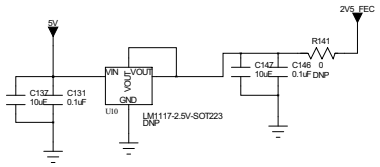
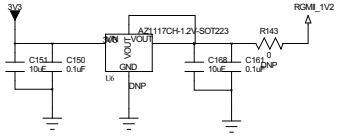
Ver	DATE	UPDATE
VP1.0	DEC. 08 2017	
VP1.1	FEB 08 2018	1. "WL_EN" is connected to I.MX6 U1.F22
		2. "WL_HOST_WAKE" is tied to G22 U1.G22 together with the current PIC
		3. Missing power rails for PCIe on i.MX6 are added
	FEB 28 2018	1. U7 Apple IC's I2C moved to I2C3
		2. U31 Buffer deleted for 2-way BT
		3. D15 Diode added on BT 5V
VP1.2	APR 16 2018	1. RESET_D2A moved to EIMD19 on i.mx
		2. BOOT_FLASH/I2C moved to GPIO5 on I.MX
		3. AMP_STBY moved to i.mx EIM_D25
		4. AMP_STBY : Q1 and R72 DNP/ Bypass R50 Added

NAD ELECTRONICS		
Schematic title : Pulse 2 Gen 2.5		
Rev VP1.0	Sheet Name : REVISION_HISTORY	Size C
2017/DEC/21	Sheet 1 of 17	

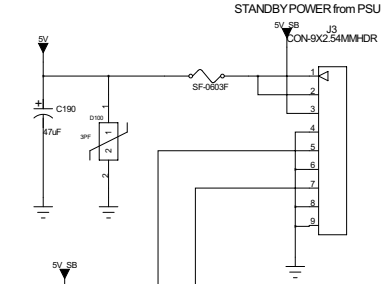
3.3V regulated power for PF0100



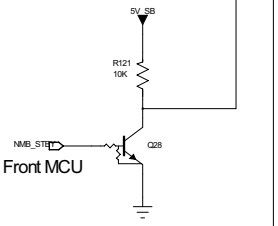


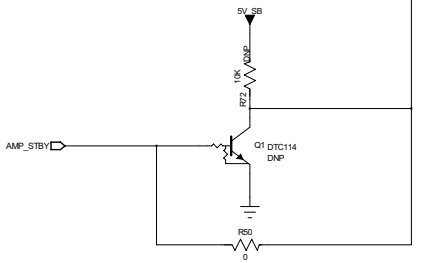


STANDBY POWER from PSU



5V main power CTR from Front MCU





NAD ELECTRONICS		
Schematic title : Pulse 2 Gen 2.5		
Rev VP1.0	Sheet Name : POWER-SUPPLY	Size C
2017/DEC/21	Sheet 2 of 17	

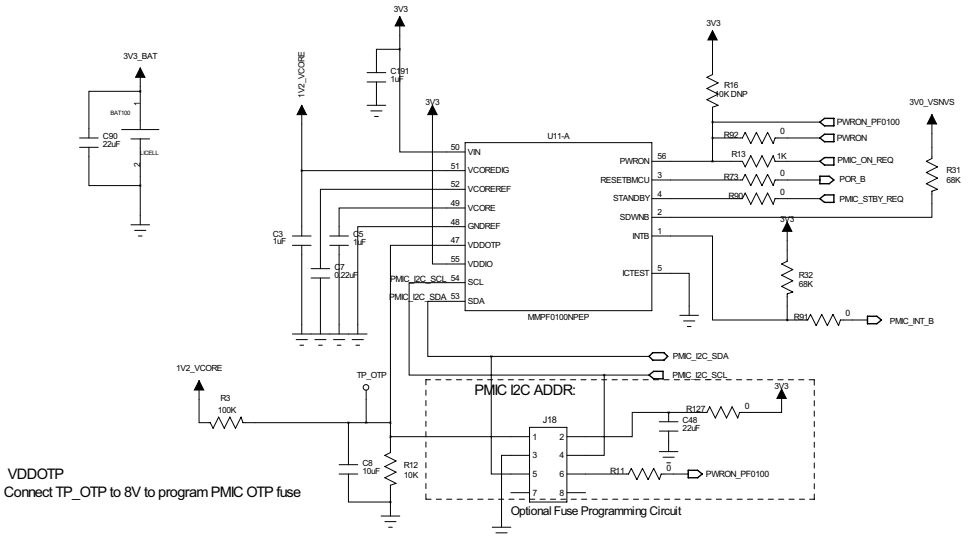
The PMPF0100 has two power-on states when the OTP registers are not configured and the OTP fuses are not blown. They are:

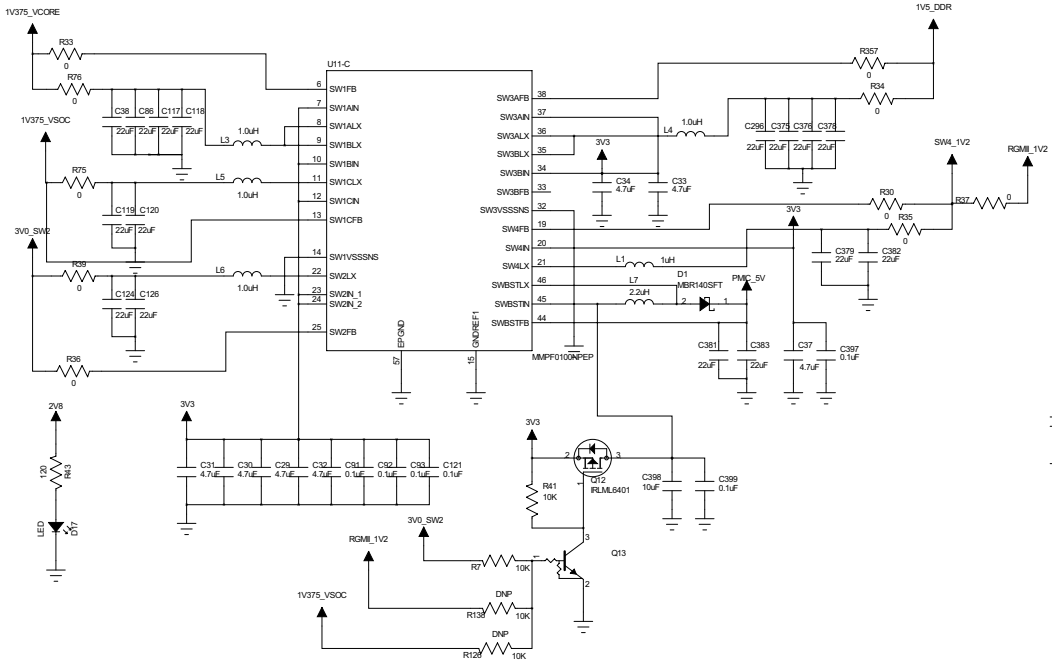
1. If the pin, VDDOTP equals 0V, or 2.5V and a turn-on event occurs, none of the regulators will turn on. This mode allows the PMIC to be configured using the I2C interface to write to One Time Programmable (OTP) registers for developing the desired power on sequence and settings to be used in the system. To use the I2C interface, VIN must be greater than UVDET and VDDIO must be supplied externally as SW2 cannot yet be enabled. Unlike the OTP fuses, the OTP registers settings are not permanent as they allow the customer to "Try Before Buy (TBB)". To avoid confusion with the OTP fuses, the OTP registers will be referred to as "TBBOTP". **WARNING:** The external components on the board for the switching regulators and the LDOs must be configured to match the TBBOTP register settings otherwise the PMIC and any external components may be damaged and the system may fail to power on.
2. If the pin, VDDOTP equals 1.5V(VCOREDIG),the PMIC will always power on in a factory defined mode as shown in the Table 13, regardless of the contents of the TBBOTP register. This mode allows the part to be tested in a known valid PMIC configuration, irrespective of what has been programmed into the OTP fuses, or without requiring the TBBOTP registers to be configured.

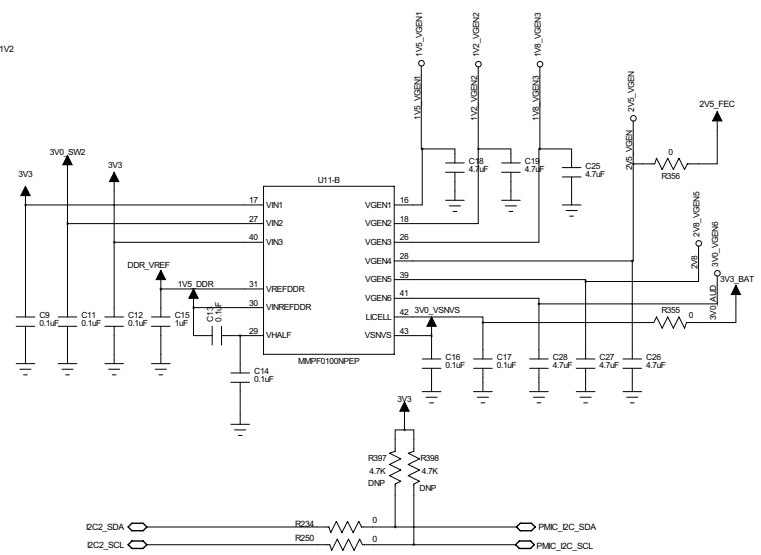
Table 14. Source of Start-up Sequence

VDDOTP(V)	tbb_por	fuse_por	Start-up sequence
0	0	0	None
0	0	1	OTP fuses
0	1	x	TBBOTP registers
1.5	x	x	Factory defined

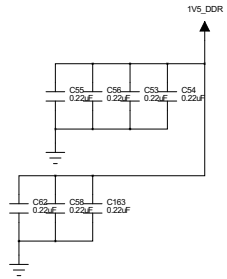
E4	OTP FUSE POR1	R/W	8'b0000_00x0	TBB POR	SOFT FUSE POR	-	-	-	-	FUSE POR1	-
				0	0	0	0	0	0	x	0
E5	OTP FUSE POR1	R/W	8'b0000_00x0	TBB POR	SOFT FUSE POR	-	-	-	-	FUSE POR2	-
				0	0	0	0	0	0	x	0
E6	OTP FUSE POR1	R/W	8'b0000_00x0	TBB POR	SOFT FUSE POR	-	-	-	-	FUSE POR3	-
				0	0	0	0	0	0	x	0

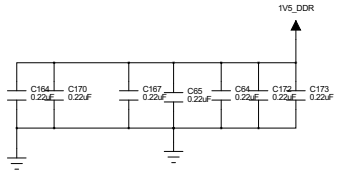


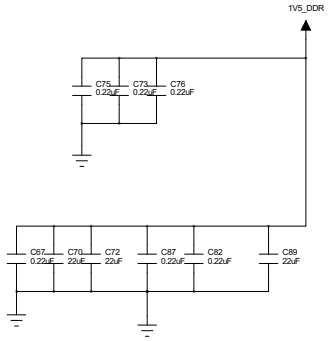




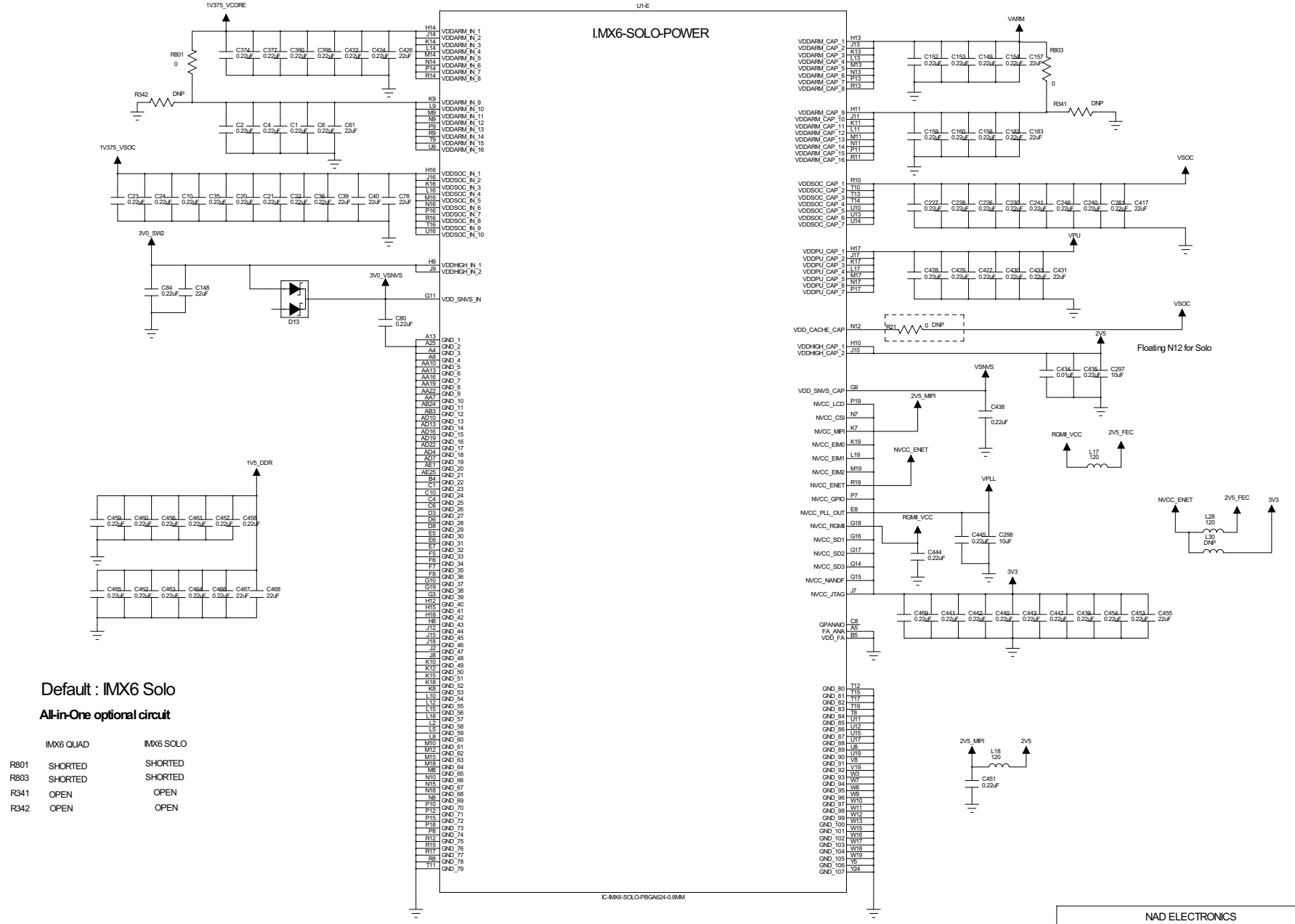
NAD ELECTRONICS	
Pulse 2 Gen 2.5	
VP1.0	POWER-PMIC
2017/DEC/21	Sheet 3 of 17





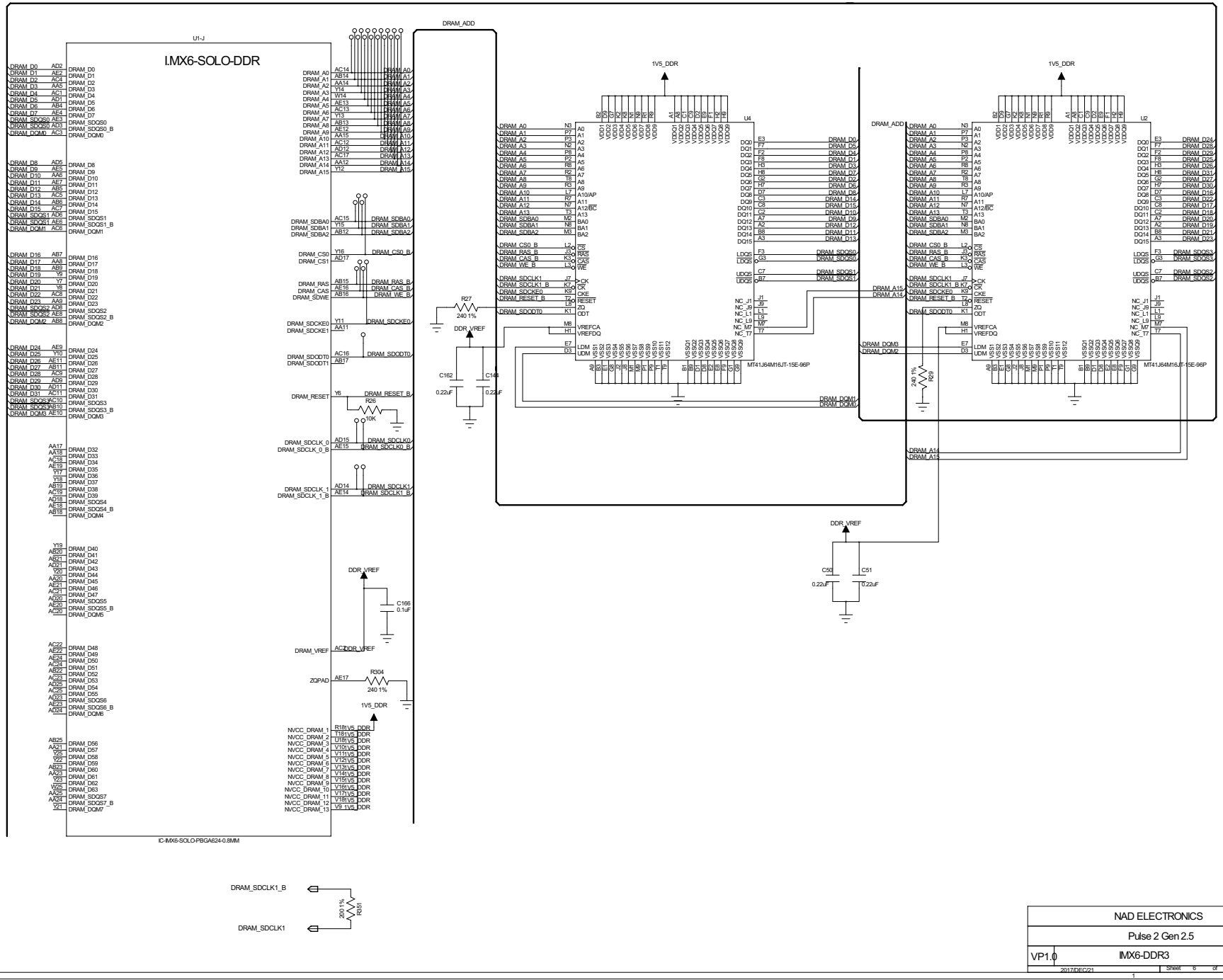


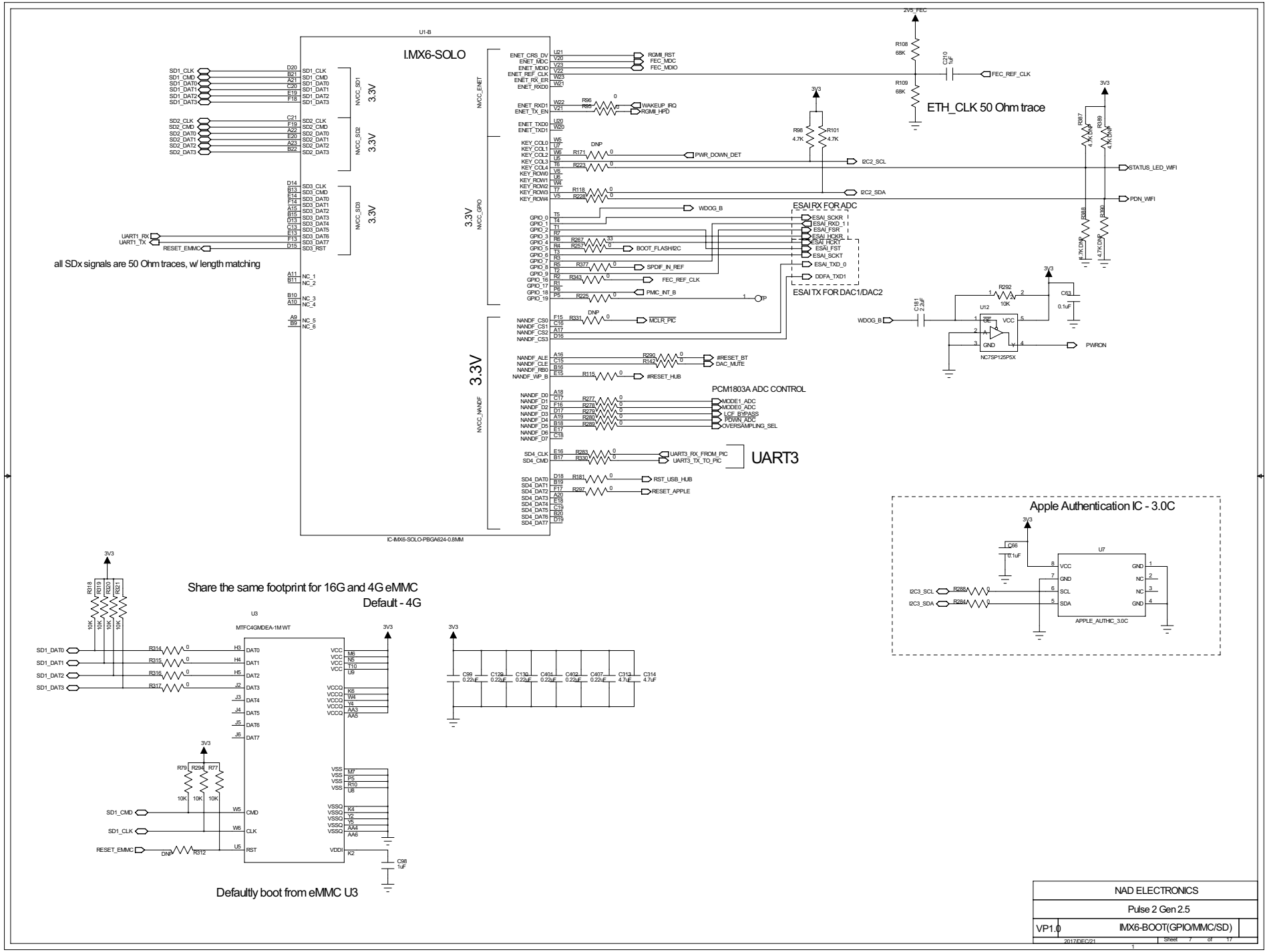
NAD ELECTRONICS			
Pulse 2 Gen 2.5			
VP1.0	POWER-DDR3		
2017/DEC/21		Sheet 4 of 17	

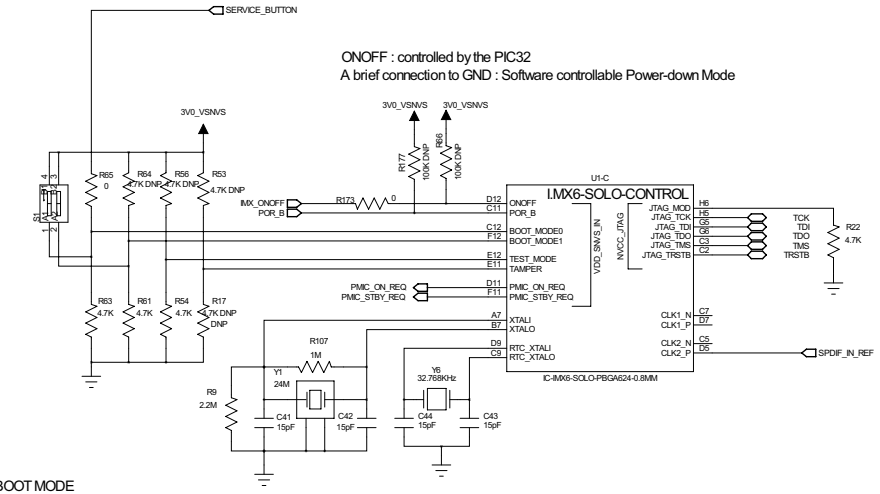


	IMX6 QUAD	IMX6 SOLO
R801	SHORTED	SHORTED
R803	SHORTED	SHORTED
R341	OPEN	OPEN
R342	OPEN	OPEN

NAD ELECTRONICS	
Pulse 2 Gen 2.5	
VP1.0	IMX6-POWER
2017/DEC/21	Sheet 5 of 17


U1-J
I.MX6-SOLO-DDR
IC-IMX6-SOLO-PBGA624-0.8MM
DRAM_ADD
1V5_DDR
U4
U2
MT41J64M16JT-15E-96P
R27
240 1%
DDR_VREF
C162
0.22uF
C146
0.22uF
R29
240 1%
C50
0.22uF
C51
0.22uF
C166
0.1uF
R304
240 1%
R26
10K
DRAM_SDCLK1_B
DRAM_SDCLK1
200 1%
R251
NAD ELECTRONICS
Pulse 2 Gen 2.5
VP1.0
IMX6-DDR3
2017/DEC/21
Sheet 6 of 17


U1-B
I.MX6-SOLO
IC-IMX6-SOLO-PBGA624-0.8MM
all SDx signals are 50 Ohm traces, w/ length matching
ETH_CLK 50 Ohm trace
FEC_REF_CLK
ESAI RX FOR ADC
ESAI TX FOR DAC1/DAC2
PCM1803A ADC CONTROL
UART3
Apple Authentication IC - 3.0C
APPLE_AUTHIC_3.0C
NC7SP125P5X
Share the same footprint for 16G and 4G eMMC
Default - 4G
MTFC4GMDEA-1M WT
Defaultly boot from eMMC U3
NAD ELECTRONICS
Pulse 2 Gen 2.5
VP1.0
IMX6-BOOT(GPIO/MMC/SD)
2017/DEC/21
Sheet 7 of 17



BOOT MODE

Default

00 : Boot from fuses - For Development

R63 - 4.7K

R61 - 4.7K

01 : Serial downloader

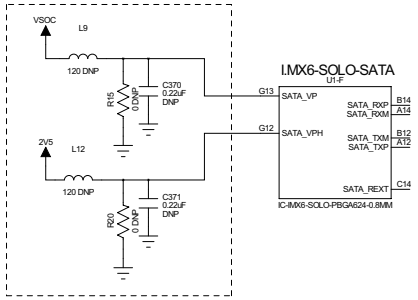
R61 - 4.7K

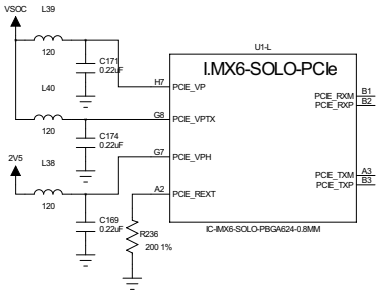
10 : Internal boot - For Production

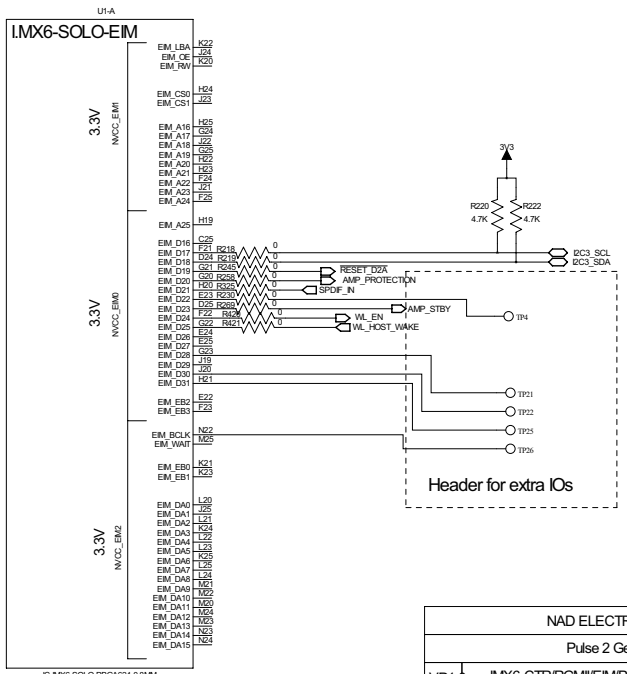
R63 - 4.7K

R64 - 4.7K

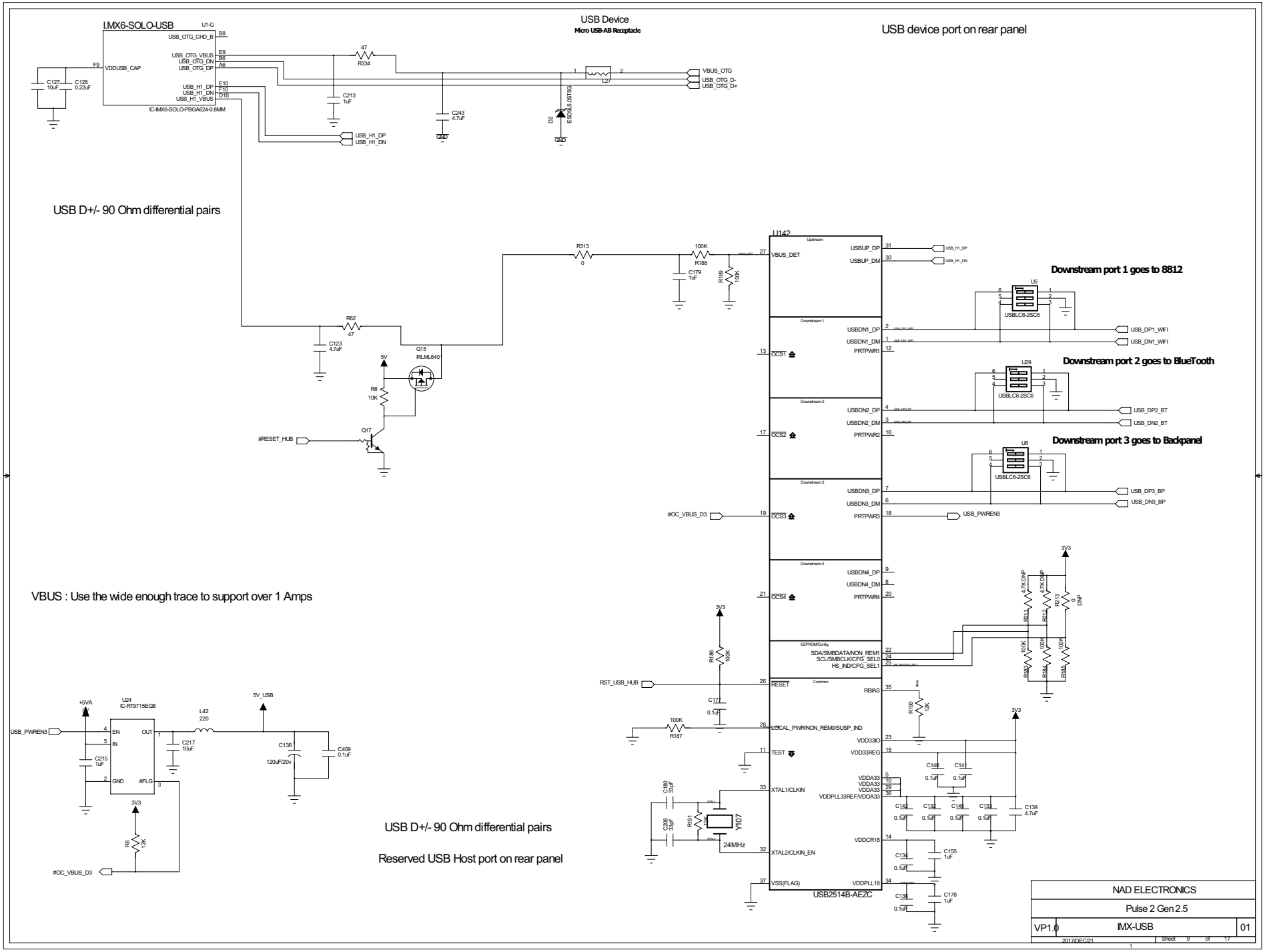
- If SATA is not used in Quad, it is recommended to be grounded by optional resistors by R356 and R357
- For Solo, NC : Default

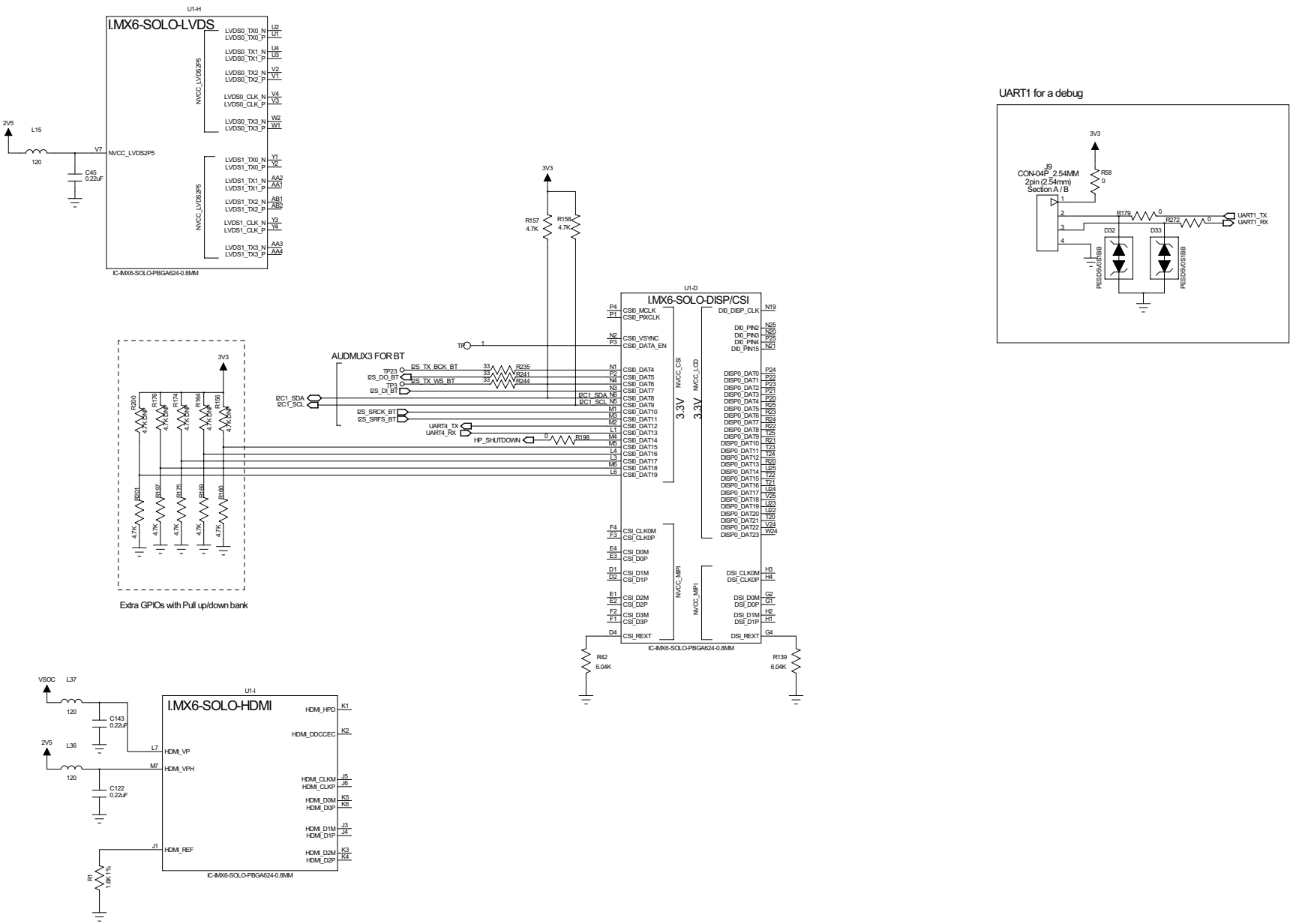






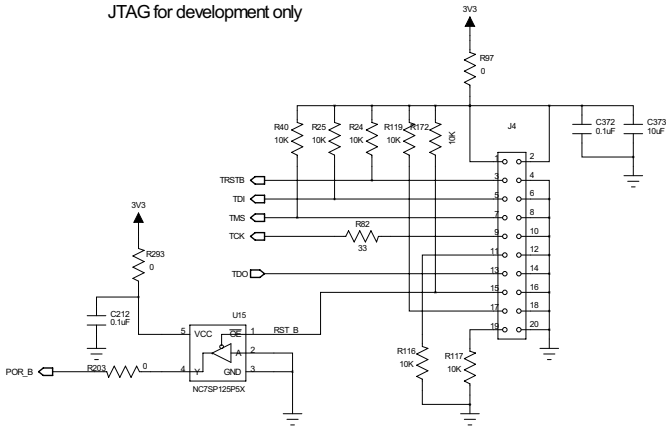
NAD ELECTRONICS	
Pulse 2 Gen 2.5	
VP1.0	IMX6-CTR/RGMII/EIM/PCI/SATA
2017/DEC/21	Sheet 8 of 17


USB Device
Micro USB-AB Receptacle
USB device port on rear panel
IMX6-SOLO-USB
U1-G
USB_OTG_CHD_B
USB_OTG_VBUS
USB_OTG_DN
USB_OTG_DP
VDDUSB_CAP
USB_H1_DP
USB_H1_DN
USB_H1_VBUS
IC-IMX6-SOLO-PBGA624-0.8MM
C127 10uF
C128 0.22uF
C213 1uF
C243 4.7uF
R334 47
L27
D2 ESD5Z5.0ST5G
VBUS_OTG
USB_OTG_D-
USB_OTG_D+
USB_H1_DP
USB_H1_DN
USB D+/- 90 Ohm differential pairs
VBUS : Use the wide enough trace to support over 1 Amps
U142
USB2514B-AEZC
Upstream
USBUP_DP
USBUP_DM
VBUS_DET
R313 0
R188 100K
C179 1uF
R189 100K
Downstream 1
USBDN1_DP
USBDN1_DM
PRTPWR1
OCS1
Downstream 2
USBDN2_DP
USBDN2_DM
PRTPWR2
OCS2
Downstream 3
USBDN3_DP
USBDN3_DM
PRTPWR3
OCS3
Downstream 4
USBDN4_DP
USBDN4_DM
PRTPWR4
OCS4
EEPROM/Config
SDA/SMBDATA/NON_REM1
SCL/SMBCLK/CFG_SEL0
HS_IND/CFG_SEL1
Common
RESET
RBIAS
LOCAL_PWR/NON_REMD/SUSP_IND
TEST
XTAL1/CLKIN
XTAL2/CLKIN_EN
VSS(FLAG)
VDD33IO
VDD33REG
VDDA33
VDDA33
VDDA33
VDDPLL33REF/VDDA33
VDDCR18
VDDPLL18
Downstream port 1 goes to 8812
U5
USBLC6-2SC6
USB_DP1_WIFI
USB_DN1_WIFI
Downstream port 2 goes to BlueTooth
U29
USBLC6-2SC6
USB_DP2_BT
USB_DN2_BT
Downstream port 3 goes to Backpanel
U8
USBLC6-2SC6
USB_DP3_BP
USB_DN3_BP
USB_PWREN3
#OC_VBUS_D3
R211 47K,DNP
R212 47K,DNP
R213 0 DNP
R183 100K
R184 100K
R185 100K
R190 2K
C177 0.1uF
R187 100K
C190 33pF
C208 33pF
R191 0
Y107
24MHz
C149 0.1uF
C141 0.1uF
C142 0.1uF
C132 0.1uF
C145 0.1uF
C133 0.1uF
C139 4.7uF
C134 0.1uF
C155 1uF
C138 0.1uF
C178 1uF
3V3
5V
R82 47
C123 4.7uF
Q15 IRLML6401
R8 10K
Q17
#RESET_HUB
RST_USB_HUB
U24 IC-RT9715EGB
+5VA
L42 220
5V_USB
C215 1uF
C217 10uF
C136 120uF/20v
C409 0.1uF
R6 1K
USB D+/- 90 Ohm differential pairs
Reserved USB Host port on rear panel
NAD ELECTRONICS
Pulse 2 Gen 2.5
VP1.0
IMX-USB
01
2017/DEC/21
Sheet 9 of 17



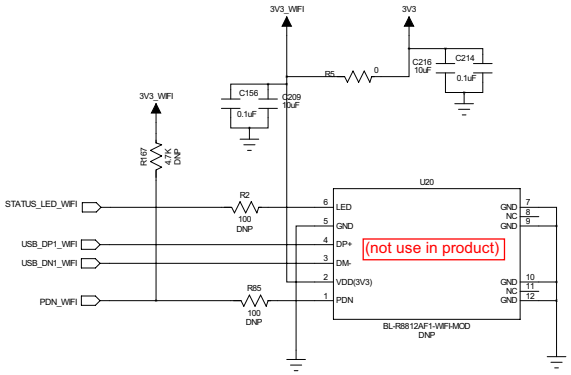
NAD ELECTRONICS	
Pulse 2 Gen 2.5	
VP1.0	IMX6-DISP/CSI
2017/DEC/21	Sheet 10 of 17

JTAG for development only



NAD ELECTRONICS	
Pulse 2 Gen 2.5	
VP1.0	IMX6-BOOT/DEBUG
2017/DEC/21	Sheet 11 of 17

1st 8812 WiFi module - USB : DNP

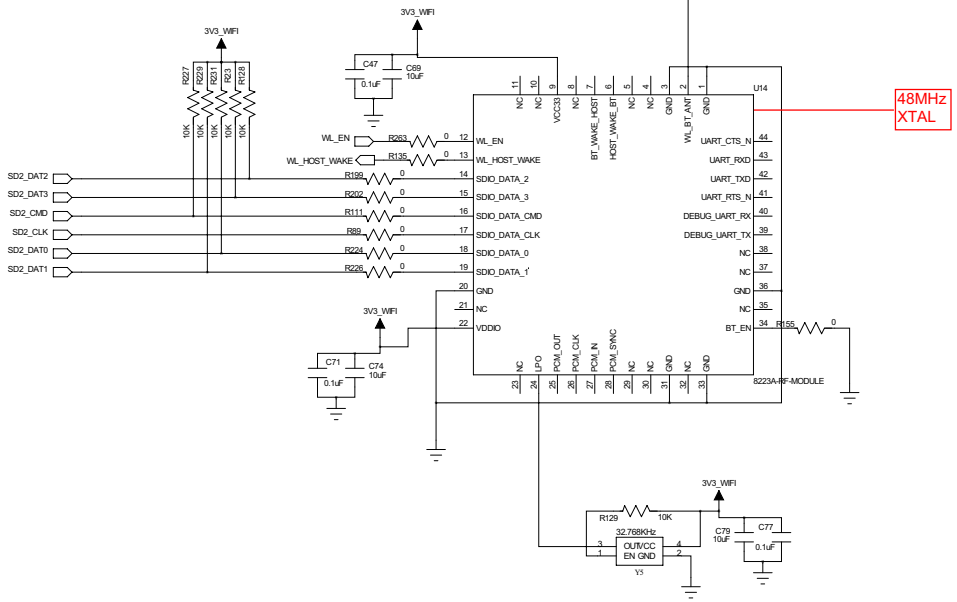


WiFi
2.4G / 5G band

2nd 8223 WiFi module - SDIO

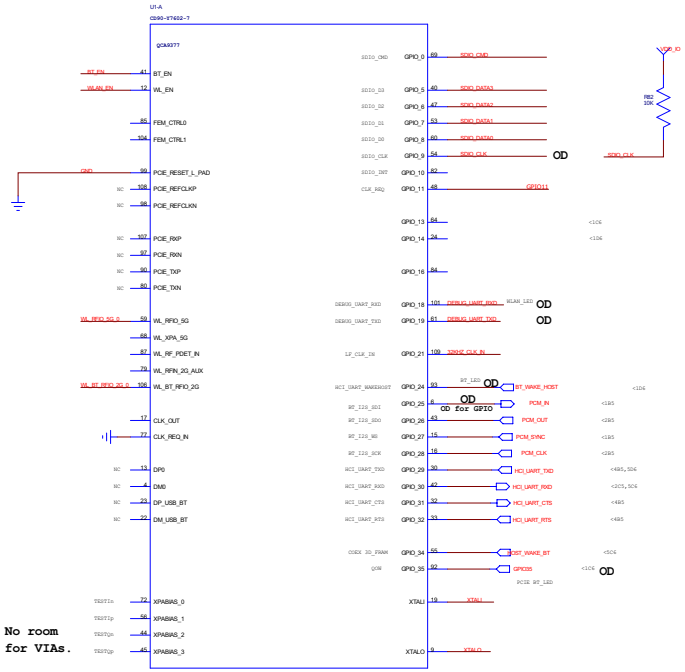
50ohm controlled impedance for RF trace

C83 10pF



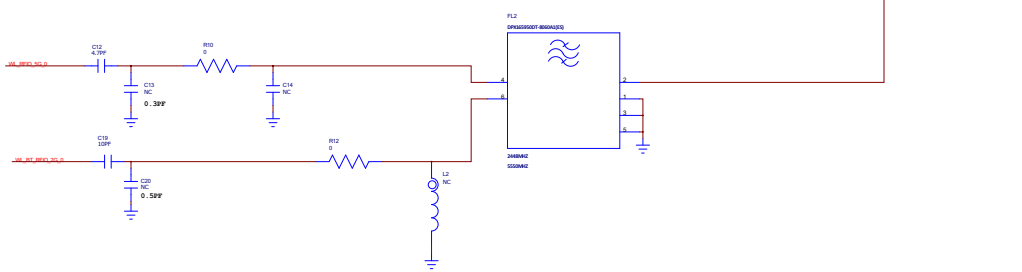
NAD ELECTRONICS	
Schematic title :	Pulse 2 Gen 2.5
Rev VP1.0	Sheet Name : IMX6-WIFI
2017/DEC/21	Sheet 12 of 17

Size C



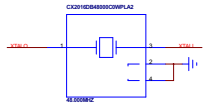
No room
for VIAs.

RF Front-end



FILTER_BP_1ANT_1RXTX3G_5PIN

48M CRYSTAL

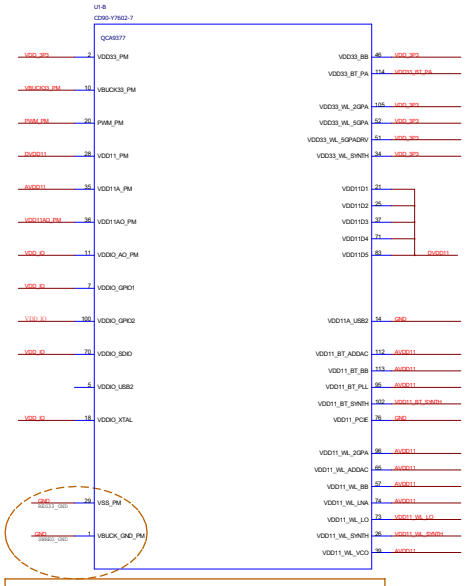


GPIO0, 5-10, VDDIO_SDIO DOMAIN
GPIO11,13-14, 25-32,34, VDDIO_GPIO_1 DOMAIN
GPIO16-18, 21, 24, 35, VDDIO_GPIO_2 DOMAIN
GPIO19, VDDIO_AO_PM DOMAIN

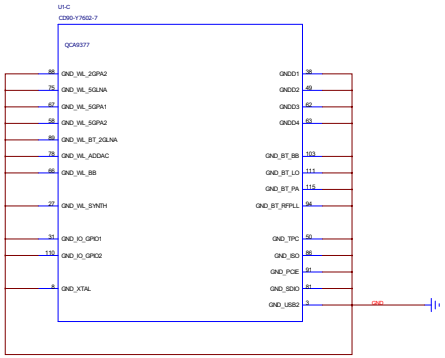
9377 and RF

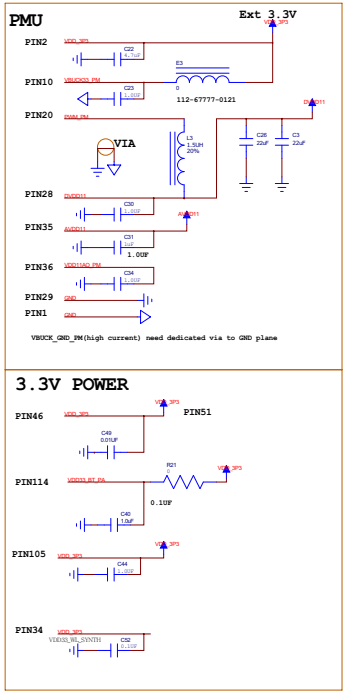
QUALCOMM ATHEROS, INC.
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110
U.S.A.

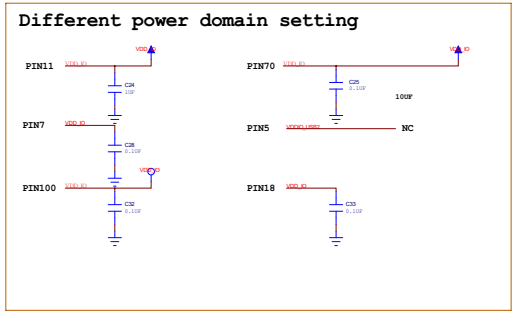
TITLE: SCHEMATIC, CCA, WB396-040, QCA9377, 802.11AC/A/B/G/N, 1X1 WIFI+BT COMBO, SDIO+UART
SIZE: D
DOCUMENT NO: LD20-V9107
REV: A
SCALE: NONE
SHEET 2 OF 5

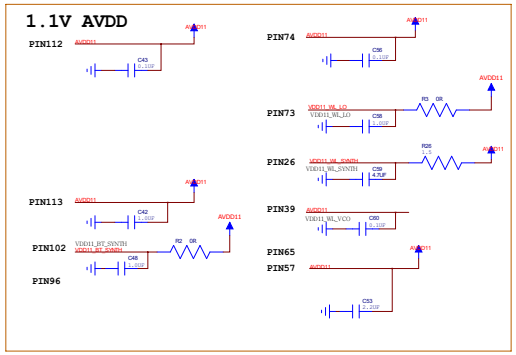


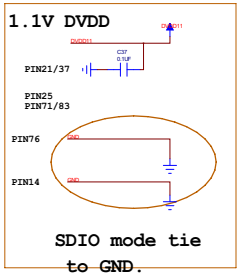
Note: Should isolate REG33_GND and SWREG_GND.
Do not connect VSS_PM and GND_SWREG in top layer.
SWREG_GND (P#1) (High current) : Dedicate GND via to GND plane.
VSS_PM (low current) : Dedicate GND via to GND plane.











Power Rail Domain

Check the Power domain carefully.///

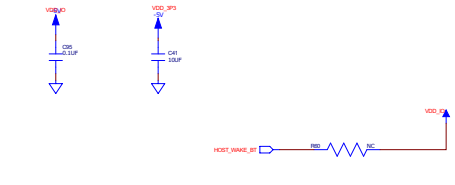
Power Rail Domain	GPIO#	NOTES
VDDIO_SDIO	GPIO0,5-10	GPIO10 1.8V or 3.3V
VDDIO_GPIO1	GPIO11,13-14,25-32,34	1.8V or 3.3V
VDDIO_GPIO2	GPIO16-18,21,24,35	1.8V or 3.3V
VDDIO_AO	GPIO19 WL_EN BT_EN CLK_REQ_IN	1.8V or 3.3V
(VDDIO_AO_PM) VDDIO_XTAL_PAD	CLK_OUT	1.8V or 3.3V

PMU_POWER

QUALCOMM ATHEROS, INC.
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110
U.S.A

TITLE: SCHEMATIC, CCA, WB396-040, QCA9377, 802.11XC/X/B/G/N, 1X1 WIFI_BT COMBO, SDIO+UART
SIZE: D
DOCUMENT NO: LD20-V9107
REV: A
SCALE: NONE
SHEET 3 OF 5

For PI



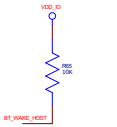
DEBUG UART
GPIO18/19

Boot TRIP

GPIO#	NAME	PULL	Default	VDDIO_SDIO Voltage Domain
GPIO5	SDIO_D3	PU	DFT	VDDIO_SDIO
GPIO6	SDIO_D2	PU		VDDIO_SDIO
GPIO7	SDIO_D1	PU		VDDIO_SDIO
GPIO10	SDIO_INTERRUPT_L	PD		VDDIO_SDIO
GPIO29	HCI_UART_TXD	PU		VDDIO_GPIO1
GPIO30	HCI_UART_RXD	PU		VDDIO_GPIO1
GPIO34	3D_FRAME_SYNC	PD	Always '0'	VDDIO_GPIO1

EJTAG

EJTAG/SDIO mode
3.3V level



When 1.8V Level used NOTE!
Level shifter outside is needed.

In debug mode

GPIO	EJTGA	NetName
GPIO10 (VV)	TDO	SDIO_INTERRUPT_L
GPIO13 (VV)	TCK	LTE_UART_TXD
GPIO14 (VV)	TMS	LTE_UART_RXD
GPIO16	TDI	WLAN_RF_KILL_L
GPIO24	TRSTN	HCI_UART_WAKEHOST_L

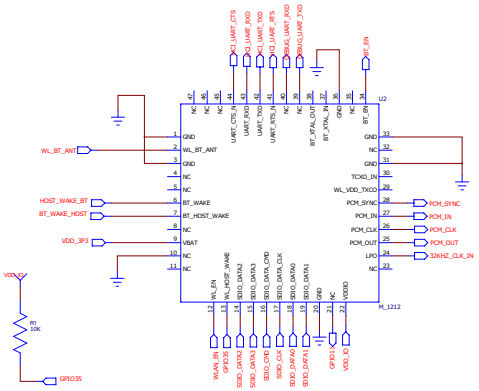
GPIO	DebugUART	NetName
GPIO18	Debug_UART_RX	PCIE_WAKE_L
GPIO19	Debug_UART_TX	PCIE_CLKREQ_L

Boot Strap Table

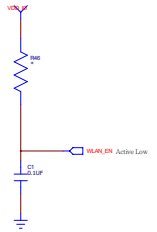
In Debug Mode, BT_LED can not be used.

	GPIO5	GPIO6	GPIO7	GPIO10	GPIO28	GPIO31	GPIO29	GPIO30	GPIO34
Function Mode	-	1	-	-	-	-	-	-	-
Debug Test Mode	1	0	-	-	-	-	-	-	-
~~Test Mode~~	~~0~~	~~0~~	-	-	-	-	-	-	-
WiFi JTAG	1	0	-	-	-	-	1	0	*1 0
BT JTAG	1	0	-	-	-	-	0	1	*2 0
Force SDIO On	1	0	1	-	-	-	-	-	-
PCM Override	-	0	-	1	-	-	-	-	-
~~WL CPU Init Rst/MDK~~	1	0	-	-	-	1	-	-	-
~~Pwr PCIe Short~~	1	0	-	-	1	-	-	-	-

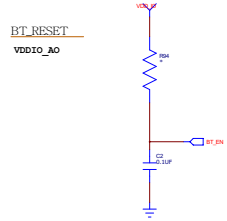
ETJAG group select
"0": GPIO 10/13/14/16/24, Default
"1": GPIO 10/16/21/34/35



WLAN_RESET
VDDIO_AO



BT_RESET
VDDIO_AO



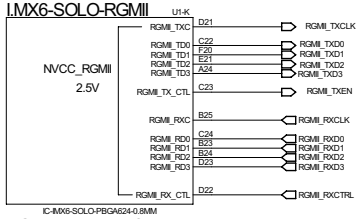
Active Low

QUALCOMM ATHEROS, INC.
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110
U.S.A

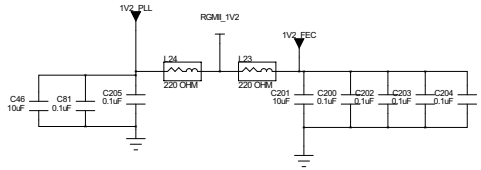
TITLE: SCHEMATIC, CCA, WB396-040, QCA9377, 802.11AC/A/B/G/N 1X1 WIFI+BT COMBO, SDIO+UART

SIZE: D | DOCUMENT NO: LD20-9107 | REV: A

SCALE: NONE | SHEET 4 OF 5



RGMII signals 50 Ohm traces



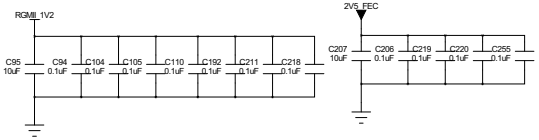
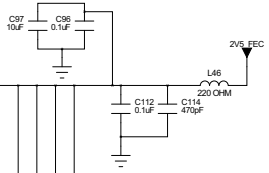


Table 3.5 Hardware Connection Determines Configuration Pin Value (CPV)

CONFIG[X] CONNECTS TO:	VALUE
GND	CPV(0)
100_LED	CPV(1)
1000_LED	CPV(2)
VDD	CPV(3)

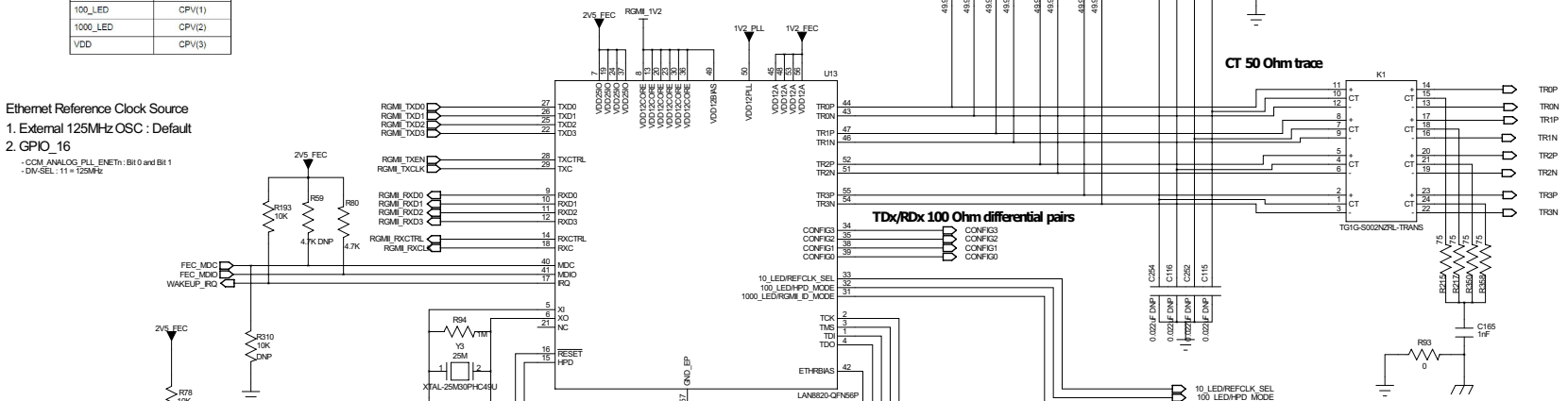
Ethernet Reference Clock Source
1. External 125MHz OSC : Default
2. GPIO_16

- CCM_ANALOG_PLL_ENETn : Bit 0 and Bit 1
- DIV-SEL : 11 = 125MHz



CT 50 Ohm trace

TDx/RDx 100 Ohm differential pairs



Straps

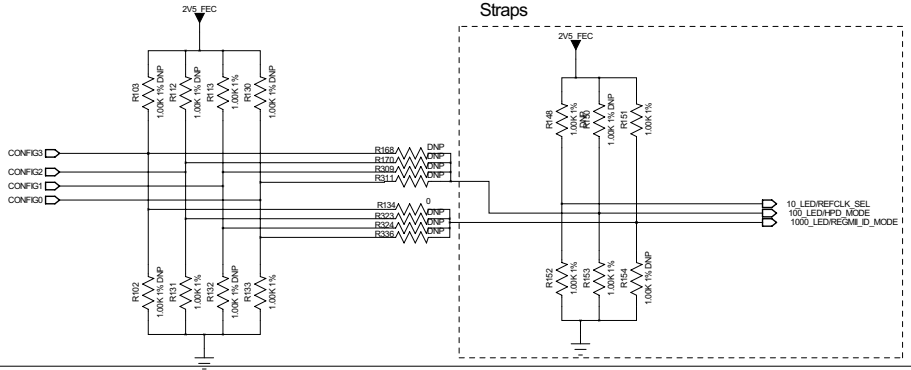
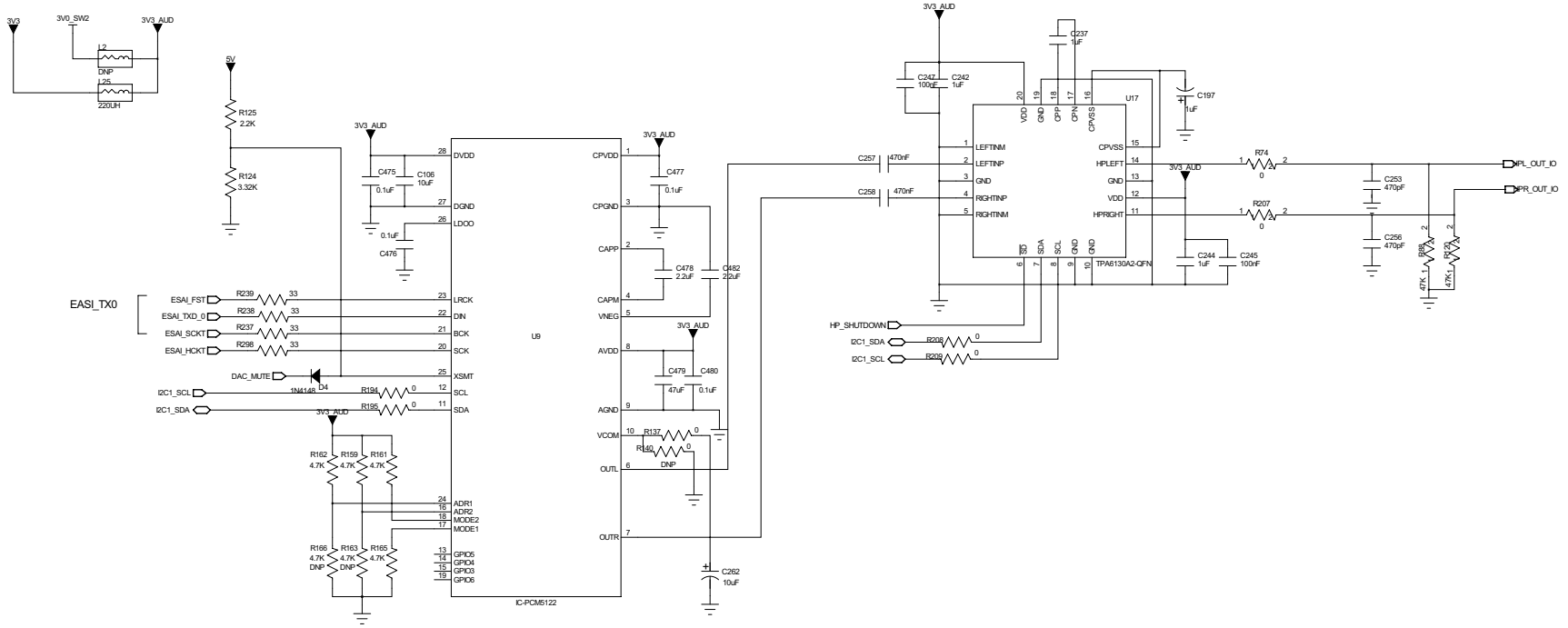


Table 3.4 Configuration Straps

CONFIGURATION STRAP	DESCRIPTION	LOGIC 0 (PD)	LOGIC 1 (PU)
REFCLK_SEL	Selects the reference clock frequency input on the XI pin	25MHz (Default)	125MHz
HPD_MODE	Selects the hardware power-down (HPD) mode	HPD with PLL disabled (Default)	HPD with PLL enabled
RGMII_ID_MODE	Configures the RGMII PHY TXC/RXC delay enable bits of the Control / Status Indications Register (27.[9:8]). Refer to Section 3.3, "RGMII Interface," on page 22 for additional information.	27.[9:8] = 00b (Default)	27.[9:8] = 11b

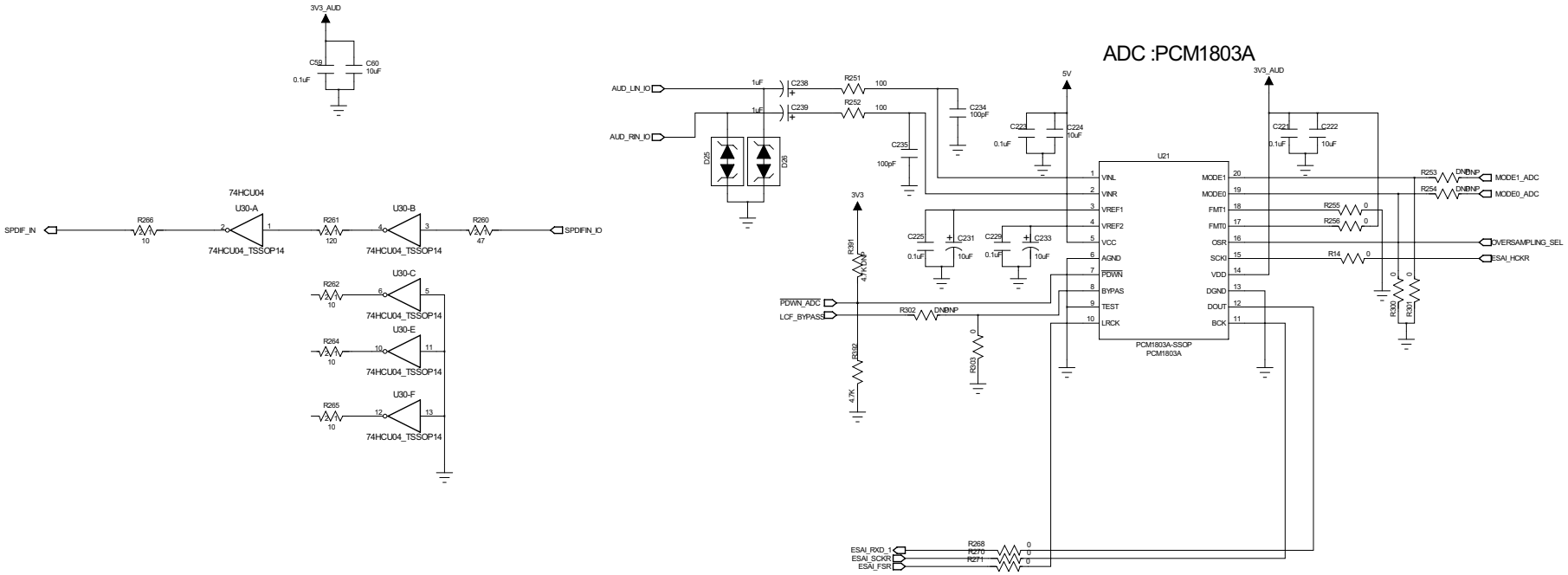
NAD ELECTRONICS		
Schematic title : Pulse 2 Gen 2.5		
Rev VP1.0	Sheet Name : PERIPH-ETHERNET	Size C
2017/DEC/21	Sheet 13 of 17	



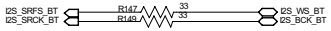
I2C1 ADDR: 0x4F

NAD ELECTRONICS		
Schematic title : Pulse 2 Gen 2.5		
Rev VP1.0	Sheet Name : PERIPH-DAC/HEADPHONE	Size C
2017/DEC/21	Sheet 14 of 17	

DIGITAL/ANALOG INPUT AUDIO

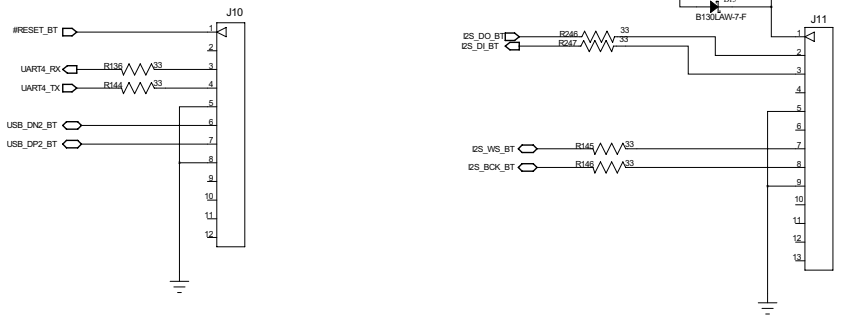


NAD ELECTRONICS	
Pulse 2 Gen 2.5	
VP1.0	PERIPH-ADC
2017/DEC/21	Sheet 15 of 17

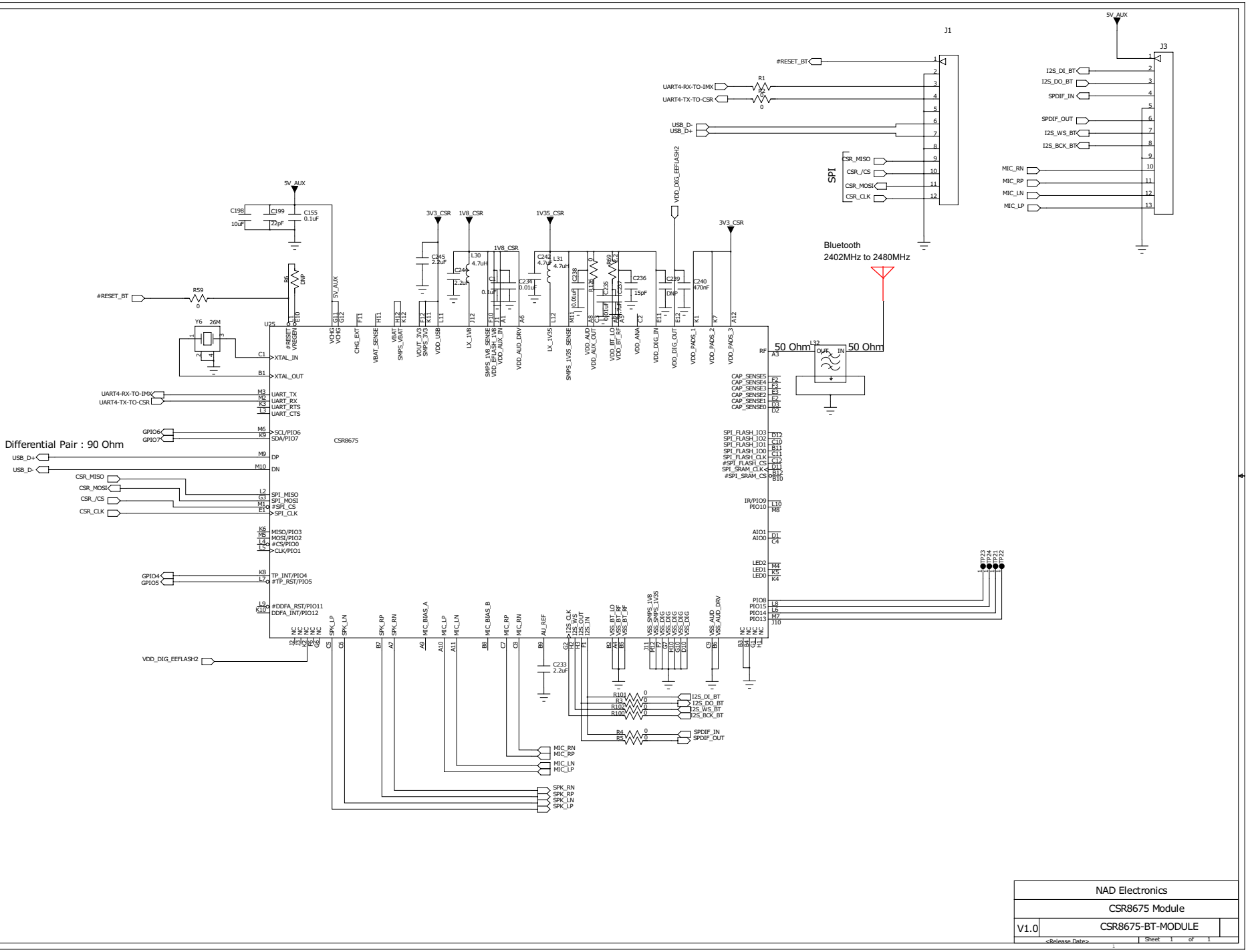


For CSR8675 Module connector

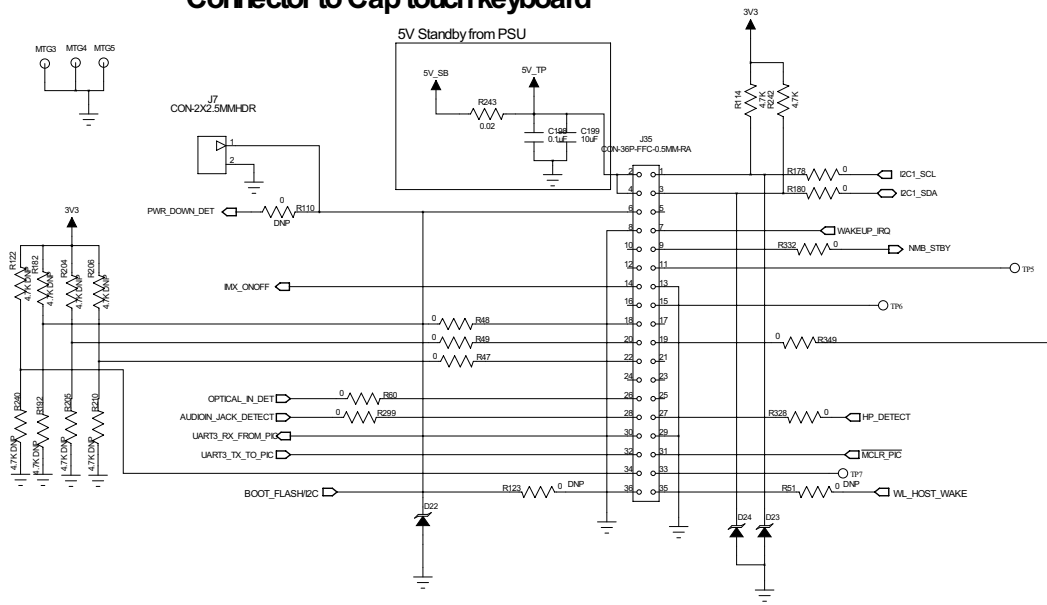
AUDMUX3



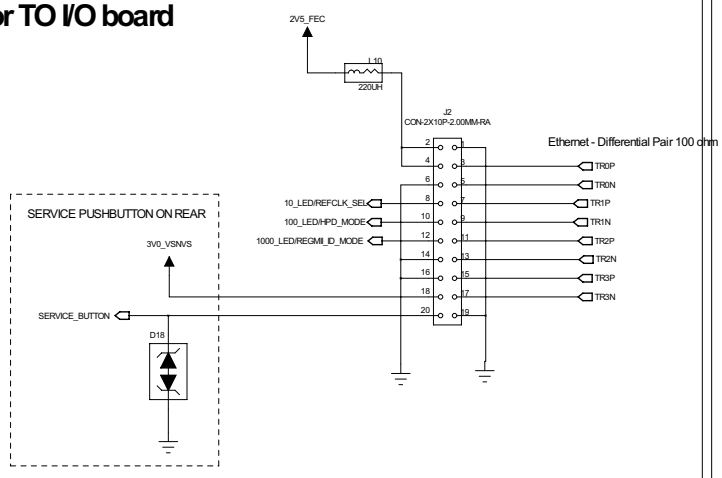
NAD ELECTRONICS		
Schematic title : Pulse 2 Gen 2.5		
Rev VP1.0	Sheet Name : PERIPH-RF	Size C
2017/DEC/21	Sheet 16 of 17	


Differential Pair : 90 Ohm
Bluetooth
2402MHz to 2480MHz
50 Ohm
50 Ohm
CSR8675
SPI
J1
J3
5V_AUX
3V3_CSR
1V8_CSR
1V35_CSR
VDD_DIG_EEFLASH2
#RESET_BT
UART4-RX-TO-IMX
UART4-TX-TO-CSR
USB_D-
USB_D+
CSR_MISO
CSR_/CS
CSR_MOSI
CSR_CLK
I2S_DI_BT
I2S_DO_BT
SPDIF_IN
SPDIF_OUT
I2S_WS_BT
I2S_BCK_BT
MIC_RN
MIC_RP
MIC_LN
MIC_LP
SPK_RN
SPK_RP
SPK_LN
SPK_LP
NAD Electronics
CSR8675 Module
V1.0
CSR8675-BT-MODULE
<Release Date>
Sheet 1 of 1

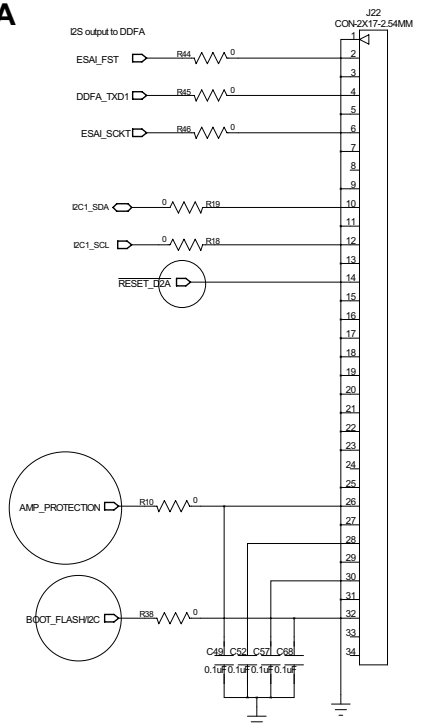
Connector to Cap touch keyboard

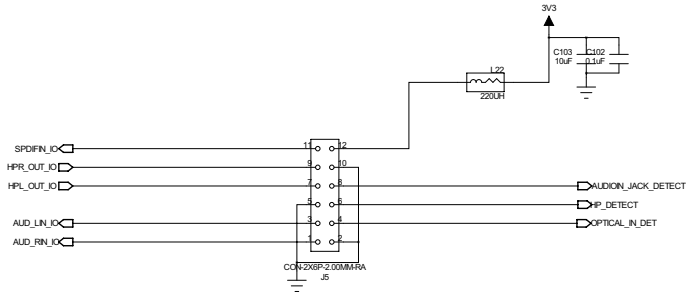


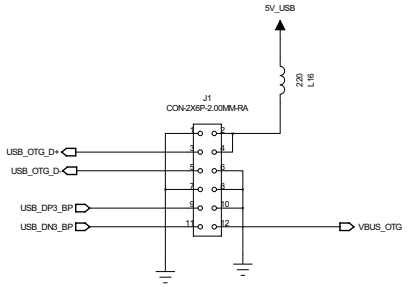
Connector TO I/O board



Connector to D2A







NAD ELECTRONICS	
Schematic title :	Pulse 2 Gen 2.5
Rev VP1.0	Sheet Name : EXTERNAL_IN/OUT
2017/DEC/21	Sheet 17 of 17
	Size C

Rev	Description	Date	Eng
C0.1	Revised half-bridge output circuits. Replace half-bridge outputs 3 and 4 with full bridge. Change C192 and C218 from .1uF to 1uF.	24 May 2018	RDK
C0.2	Revised PWM connections	24 May 2018	RDK
C0.3	Unreleased Version	24 May 2018	RDK
C0.4	Revised output filter on half bridge outputs (L9, C278, C283)	29 May 2018	RDK
C0.4	Input to U20, U21 changed to +5V_SB. 1.8V enabled by +32V_SW, 3.3V enabled by 1.8V. SCAMP powered by +5V_SB. Added R258.	29 May 2018	RDK
C0.4	Changed connector J13 to customer specifed part (2.54mm to 2.50mm)	15 Jun 2018	RDK

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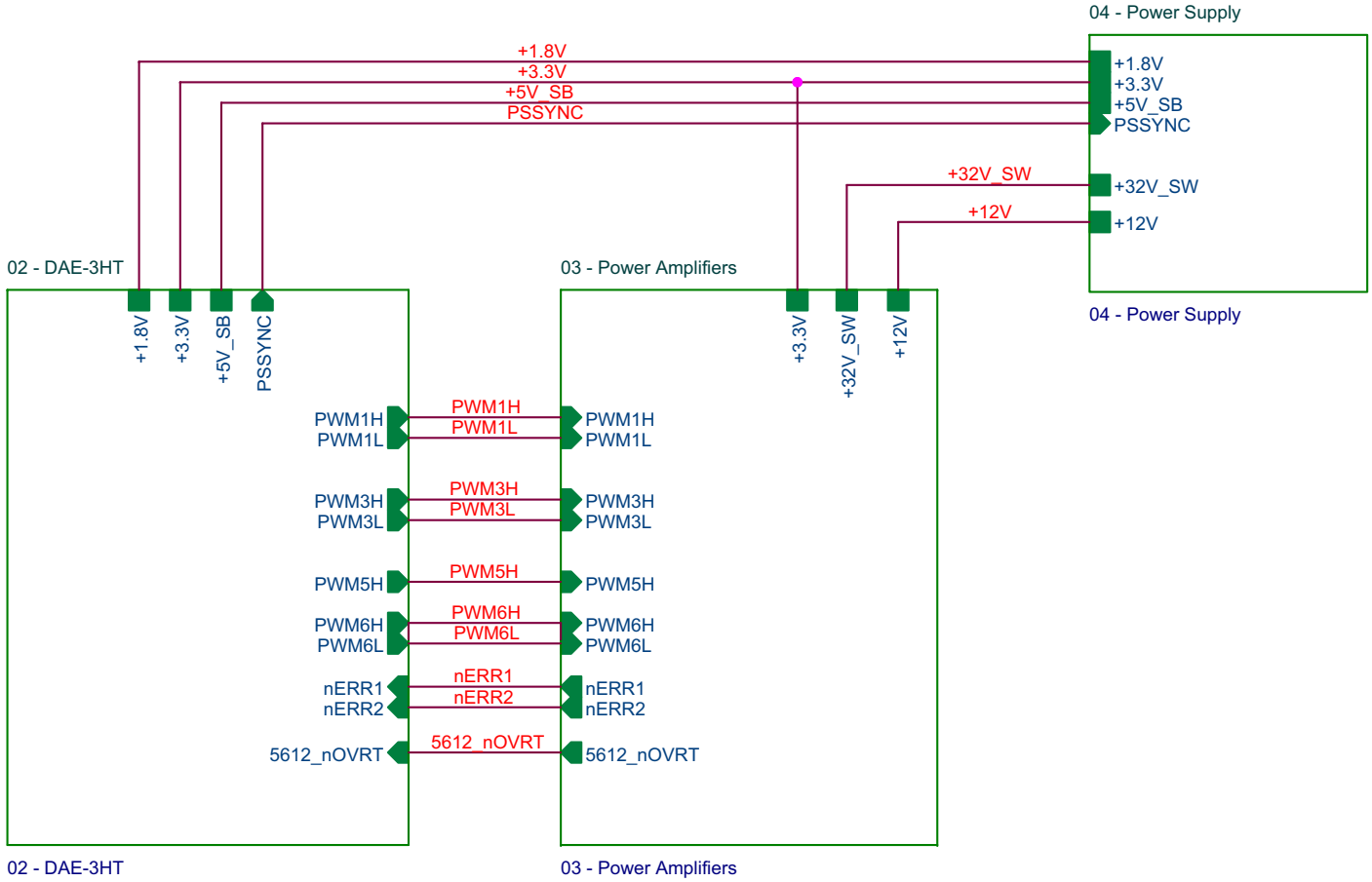
Title: **LENBROOK PULSE-2 REV-C**

Size: B | Document Number: EAS-LENBRK-P2-C | **Revision History** | Rev: C05

Date: Friday, June 15, 2018 | Sheet 1 of 7



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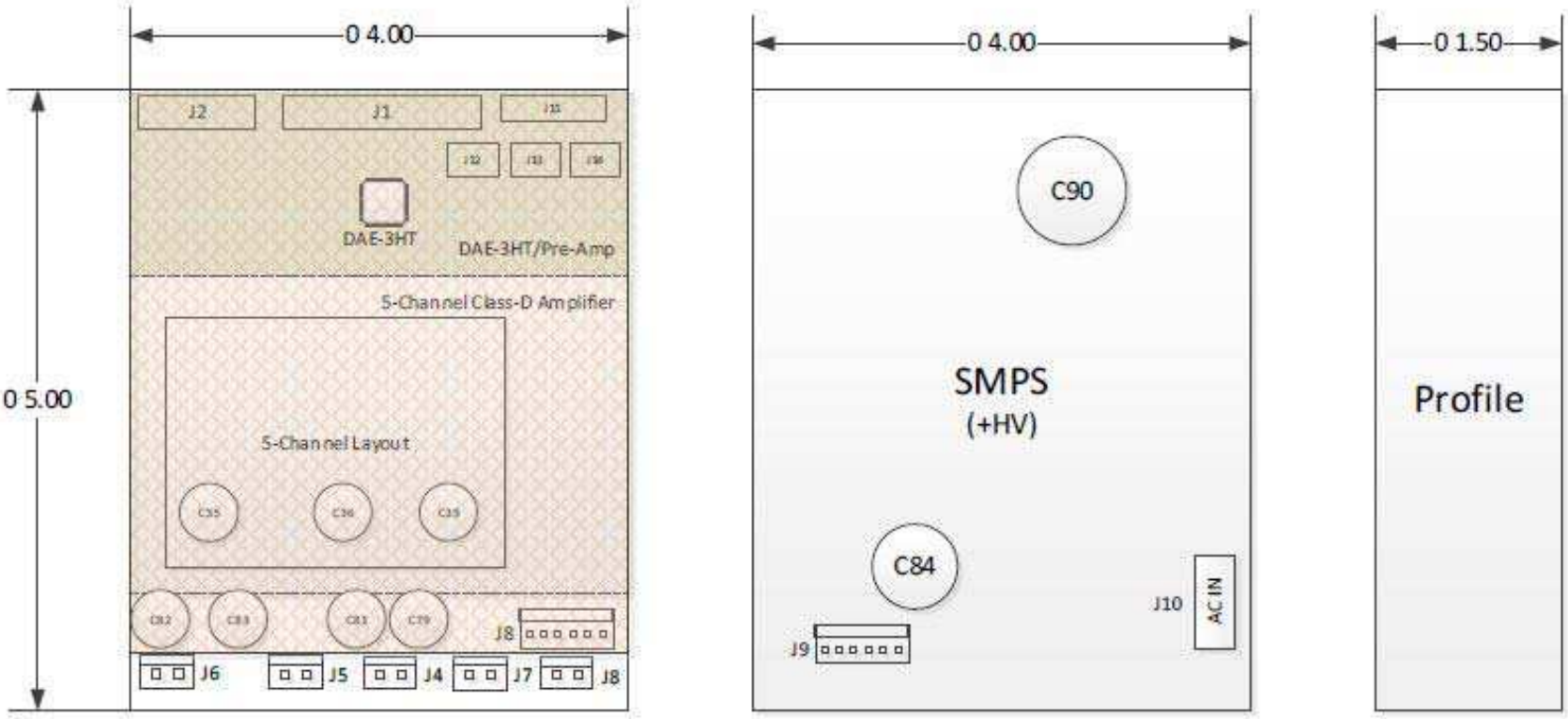
RDK

Title
LENBROOK PULSE-2 REV-C

Size	Document Number	Rev
A	EAS-LENBRK-P2-C	C05

Block Diagram

Date: Friday, June 15, 2018 Sheet 2 of 7



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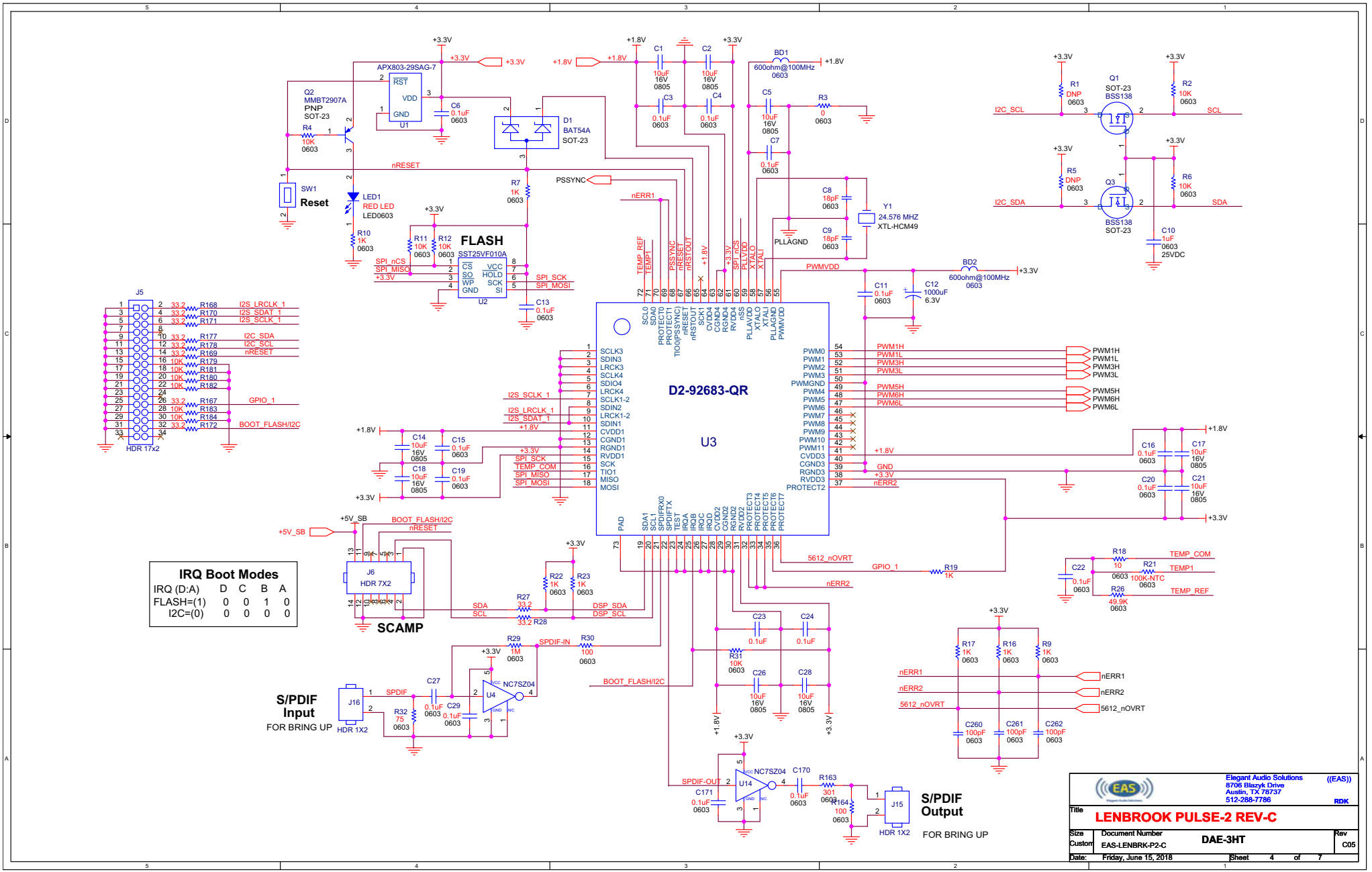
Title
LENBROOK PULSE-2 REV-C

Size	Document Number		Rev
A	EAS-LENBRK-P2-C	PCB FLOOR PLAN	C05
Date:	Friday, June 15, 2018	Sheet 3 of 7	


D2-92683-QR
U3
FLASH
SST25VF010A
U2
SCAMP
J6
HDR 7X2
J5
HDR 17x2
APX803-29SAG-7
U1
Reset
SW1
LED1
RED LED
LED0603
Q2
MMBT2907A
PNP
SOT-23
D1
BAT54A
SOT-23
Y1
24.576 MHZ
XTL-HCM49
BD1
600ohm@100MHz
0603
BD2
600ohm@100MHz
0603
Q1
SOT-23
BSS138
Q3
BSS138
SOT-23
I2C_SCL
I2C_SDA
SCL
SDA
nRESET
PSSYNC
nERR1
nERR2
5612_nOVRT
GPIO_1
BOOT_FLASH/I2C
SPI_nCS
SPI_MISO
SPI_SCK
SPI_MOSI
TEMP_COM
TEMP1
TEMP_REF
DSP_SDA
DSP_SCL
SDA
SCL
SPDIF-IN
SPDIF-OUT
SPDIF
PWMVDD
PLLAGND
+5V_SB
I2S_SCLK_1
I2S_LRCLK_1
I2S_SDAT_1
I2S_SCLK_1
I2C_SDA
I2C_SCL
nRESET
GPIO_1
BOOT_FLASH/I2C
PWM1H
PWM1L
PWM3H
PWM3L
PWM5H
PWM6H
PWM6L
IRQ Boot Modes
IRQ (D:A) D C B A
FLASH=(1) 0 0 1 0
I2C=(0) 0 0 0 0
S/PDIF Input
FOR BRING UP
HDR 1X2
S/PDIF Output
FOR BRING UP
HDR 1X2
Elegant Audio Solutions
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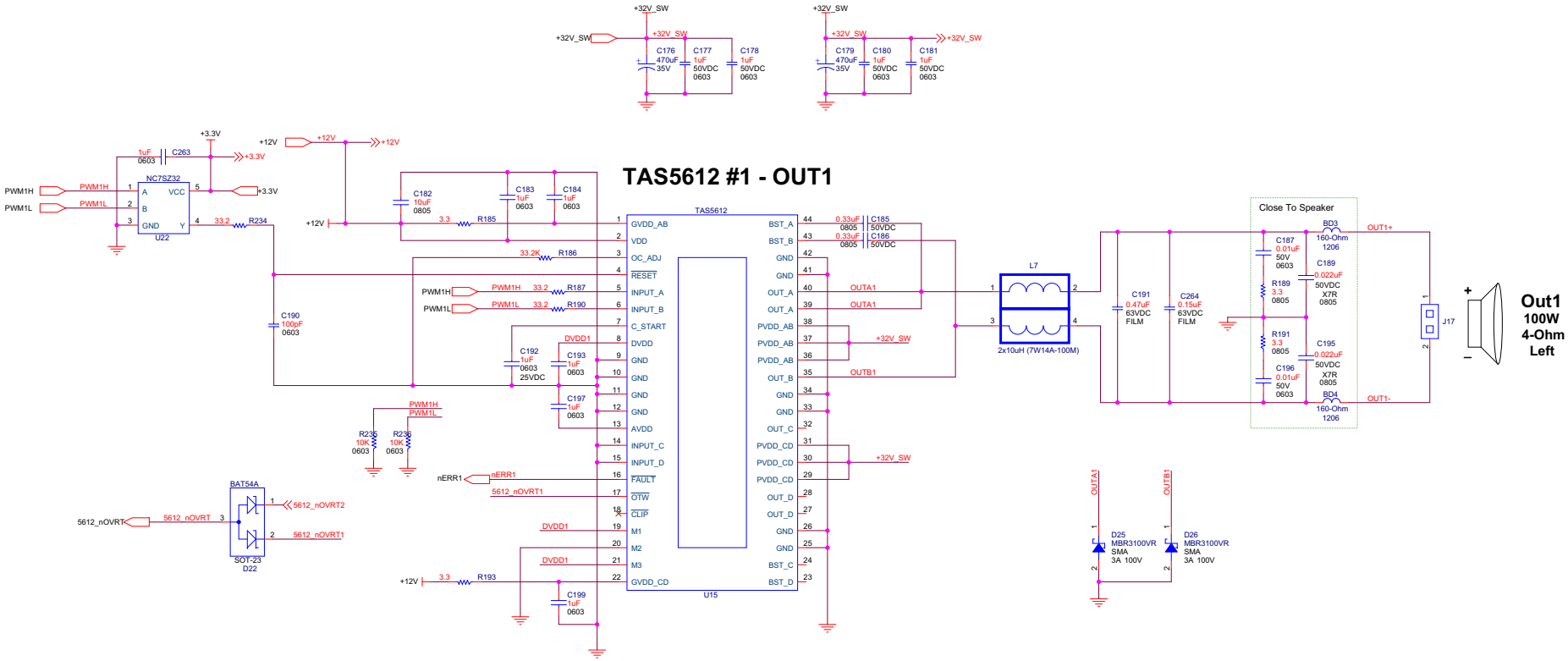
Austin, TX 78737
512-288-7786
((EAS))
RDK
Title
LENBROOK PULSE-2 REV-C
Size
Custom
Document Number
EAS-LENBRK-P2-C
DAE-3HT
Rev
C05
Date:
Friday, June 15, 2018
Sheet
4
of
7

One each bulk cap pair per A/B and B/C Power
Two each 0.1uF cap pair per A/B and B/C Power



MODE SELECTION PINS

MODE PINS			PWM Input[1]	Output Configuration	Input A	Input B	Input C	Input D	MODE
M3	M2	M1							
0	0	0	2N + 1	2 x BTL	PWMa	PWMb	PWMc	PWMd	AD Mode
0	0	1	1N + 1[2]	2 x BTL	PWMa	Unused	PWMc	Unused	AD Mode
0	1	0	2N + 1	2 x BTL	PWMa	PWMb	PWMc	PWMd	BD Mode
0	1	1	1N + 1[2]	1 x BTL + 2 x SE	PWMa	Unused	PWMc	PWMd	AD Mode
1	0	0	2N + 1	1 x PBTL	PWMa	PWMb	0	0	AD Mode
1	0	0	1N + 1[2]	1 x PBTL	PWMa	Unused	0	1	AD Mode
1	0	0	2N + 1	1 x PBTL	PWMa	PWMb	1	0	BD Mode
1	0	1	1N + 1	4 x SE[3]	PWMa	PWMb	PWMc	PWMd	AD Mode

(1) The 1N and 2N naming convention is used to indicate the number of PWM lines to the power stage per channel in a specific mode.
(2) Using 1N interface in BTL and PBTL mode results in increased DC offset on the output terminals.
(3) The 4xSE mode can be used as 1xBTL + 2xSE configuration by feeding a 2N PWM signal to either INPUT_AB or INPUT_CD for improved DC offset accuracy

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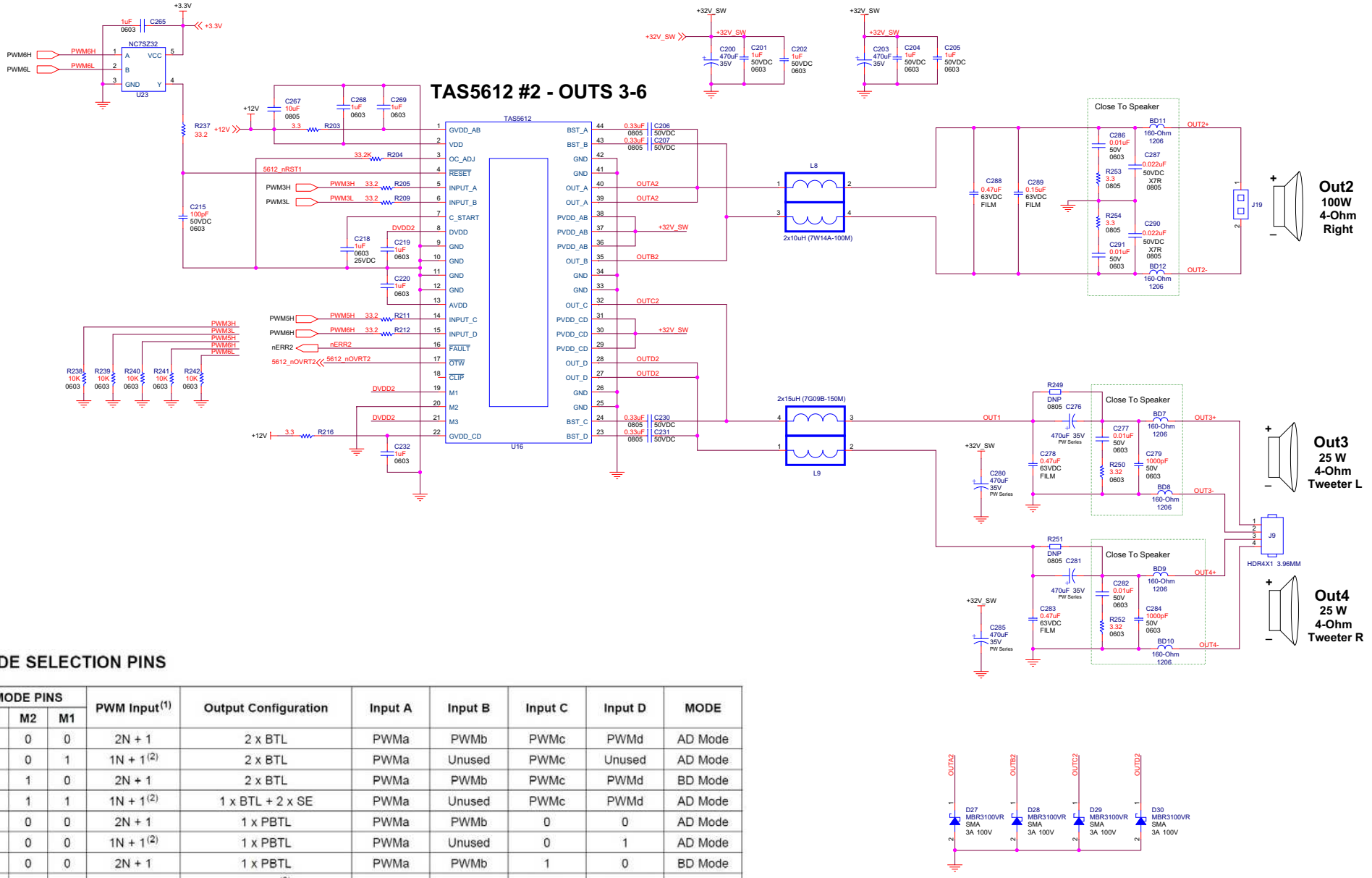
Title	LENBROOK PULSE-2 REV-C	
Size C	Document Number EAS-LENBRK-P2-C	TAS5612 FB Sub Out Rev C05
Date: Friday, June 15, 2018	Sheet 5 of 7	

One each bulk cap pair per A/B and B/C Power

Two each 0.1uF cap pair per A/B and B/C Power



MODE SELECTION PINS

MODE PINS			PWM Input[1]	Output Configuration	Input A	Input B	Input C	Input D	MODE
M3	M2	M1							
0	0	0	2N + 1	2 x BTL	PWMa	PWMb	PWMc	PWMd	AD Mode
0	0	1	1N + 1[2]	2 x BTL	PWMa	Unused	PWMc	Unused	AD Mode
0	1	0	2N + 1	2 x BTL	PWMa	PWMb	PWMc	PWMd	BD Mode
0	1	1	1N + 1[2]	1 x BTL + 2 x SE	PWMa	Unused	PWMc	PWMd	AD Mode
1	0	0	2N + 1	1 x PBTL	PWMa	PWMb	0	0	AD Mode
1	0	0	1N + 1[2]	1 x PBTL	PWMa	Unused	0	1	AD Mode
1	0	0	2N + 1	1 x PBTL	PWMa	PWMb	1	0	BD Mode
1	0	1	1N + 1	4 x SE[3]	PWMa	PWMb	PWMc	PWMd	AD Mode

(1) The 1N and 2N naming convention is used to indicate the number of PWM lines to the power stage per channel in a specific mode.
(2) Using 1N interface in BTL and PBTL mode results in increased DC offset on the output terminals.
(3) The 4xSE mode can be used as 1xBTL + 2xSE configuration by feeding a 2N PWM signal to either INPUT_AB or INPUT_CD for improved DC offset accuracy

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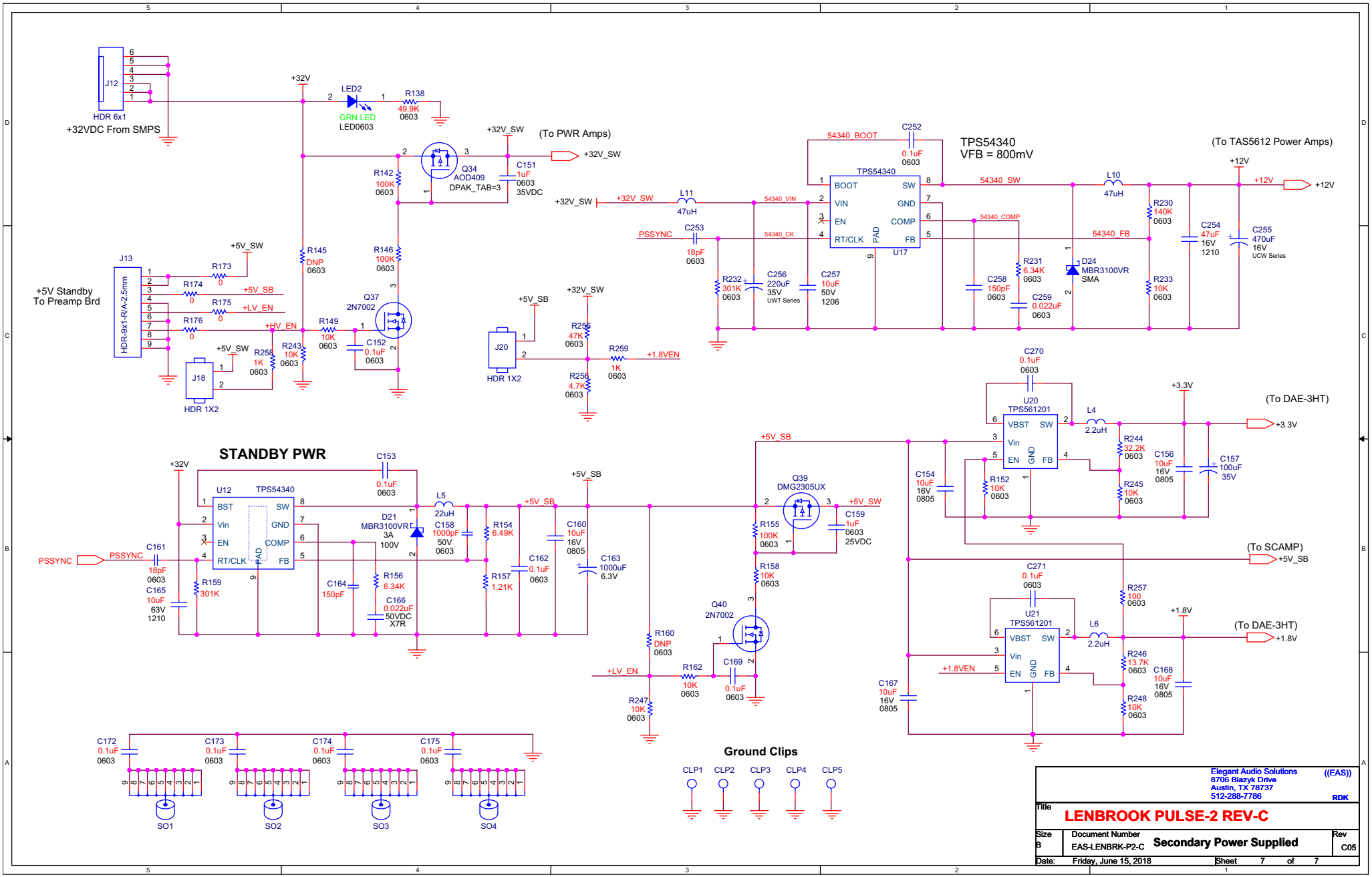
Title	LENBROOK PULSE-2 REV-C		
Size C	Document Number EAS-LENBRK-P2-C	TAS5612 FB Outs 3-6	Rev C05
Date: Friday, June 15, 2018	Sheet 6 of 7		


J12
HDR 6x1
+32VDC From SMPS
+32V
LED2
GRN LED
LED0603
R138
49.9K
0603
+32V_SW
(To PWR Amps)
Q34
AOD409
DPAK_TAB=3
C151
1uF
0603
35VDC
R142
100K
0603
R146
100K
0603
R145
DNP
0603
Q37
2N7002
R149
10K
0603
C152
0.1uF
0603
R243
10K
0603
R258
1K
0603
J13
HDR-9x1-R/A-2.5mm
+5V Standby
To Preamp Brd
R173
0
R174
0
R175
0
R176
0
+5V_SB
+LV_EN
+HV_EN
+5V_SW
J18
HDR 1X2
J20
HDR 1X2
R255
47K
0603
R256
4.7K
0603
R259
1K
0603
+1.8VEN
TPS54340
VFB = 800mV
54340_BOOT
C252
0.1uF
0603
U17
BOOT
VIN
EN
RT/CLK
SW
GND
COMP
FB
PAD
54340_VIN
54340_CK
54340_SW
54340_COMP
54340_FB
L11
47uH
L10
47uH
PSSYNC
C253
18pF
0603
R232
301K
0603
C256
220uF
35V
UWT Series
C257
10uF
50V
1206
C258
150pF
0603
R231
6.34K
0603
C259
0.022uF
0603
D24
MBR3100VR
SMA
R230
140K
0603
R233
10K
0603
C254
47uF
16V
1210
C255
470uF
16V
UCW Series
+12V
(To TAS5612 Power Amps)
STANDBY PWR
U12
TPS54340
C153
0.1uF
0603
L5
22uH
C158
1000pF
50V
0603
D21
MBR3100VR
3A
100V
R154
6.49K
R157
1.21K
C162
0.1uF
0603
C160
10uF
16V
0805
C163
1000uF
6.3V
C161
18pF
0603
C165
10uF
63V
1210
R159
301K
C164
150pF
R156
6.34K
C166
0.022uF
50VDC
X7R
Q39
DMG2305UX
R155
100K
0603
R158
10K
0603
C159
1uF
0603
25VDC
Q40
2N7002
R160
DNP
0603
R162
10K
0603
C169
0.1uF
0603
R247
10K
0603
+LV_EN
U20
TPS561201
VBST
SW
Vin
EN
GND
FB
C270
0.1uF
0603
L4
2.2uH
C154
10uF
16V
0805
R152
10K
0603
R244
32.2K
0603
R245
10K
0603
C156
10uF
16V
0805
C157
100uF
35V
+3.3V
(To DAE-3HT)
(To SCAMP)
+5V_SB
U21
TPS561201
C271
0.1uF
0603
L6
2.2uH
R257
100
0603
R246
13.7K
0603
R248
10K
0603
C167
10uF
16V
0805
C168
10uF
16V
0805
+1.8V
(To DAE-3HT)
C172
0.1uF
0603
C173
0.1uF
0603
C174
0.1uF
0603
C175
0.1uF
0603
SO1
SO2
SO3
SO4
Ground Clips
CLP1
CLP2
CLP3
CLP4
CLP5
Elegant Audio Solutions
8706 Blazyk Drive
Austin, TX 78737
512-288-7786
((EAS))
RDK
Title
LENBROOK PULSE-2 REV-C
Size
B
Document Number
EAS-LENBRK-P2-C
Secondary Power Supplied
Rev
C05
Date:
Friday, June 15, 2018
Sheet
7
of
7

Rev	Description	Date	Eng
B0.1	Removed R3 for direct +32V connection., added 1206 bleed resistors in parallel with C6, TO-220 Heatsink now Kwanhong P2i	13 Jun 2018	DLC
B1.0	Release to PCB	15 Jun 2018	DLC

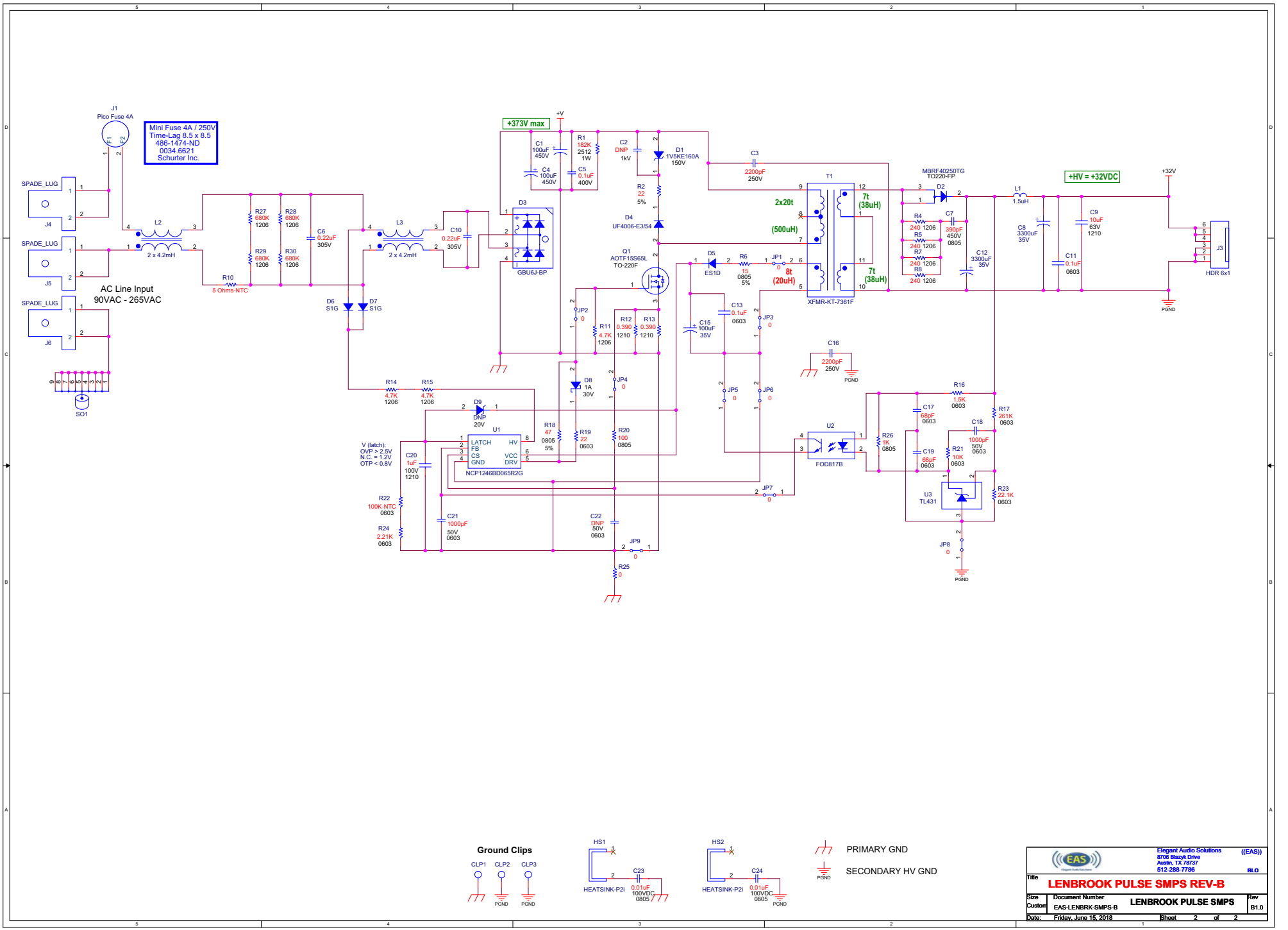
02 - Lenbrook Pulse SMPS

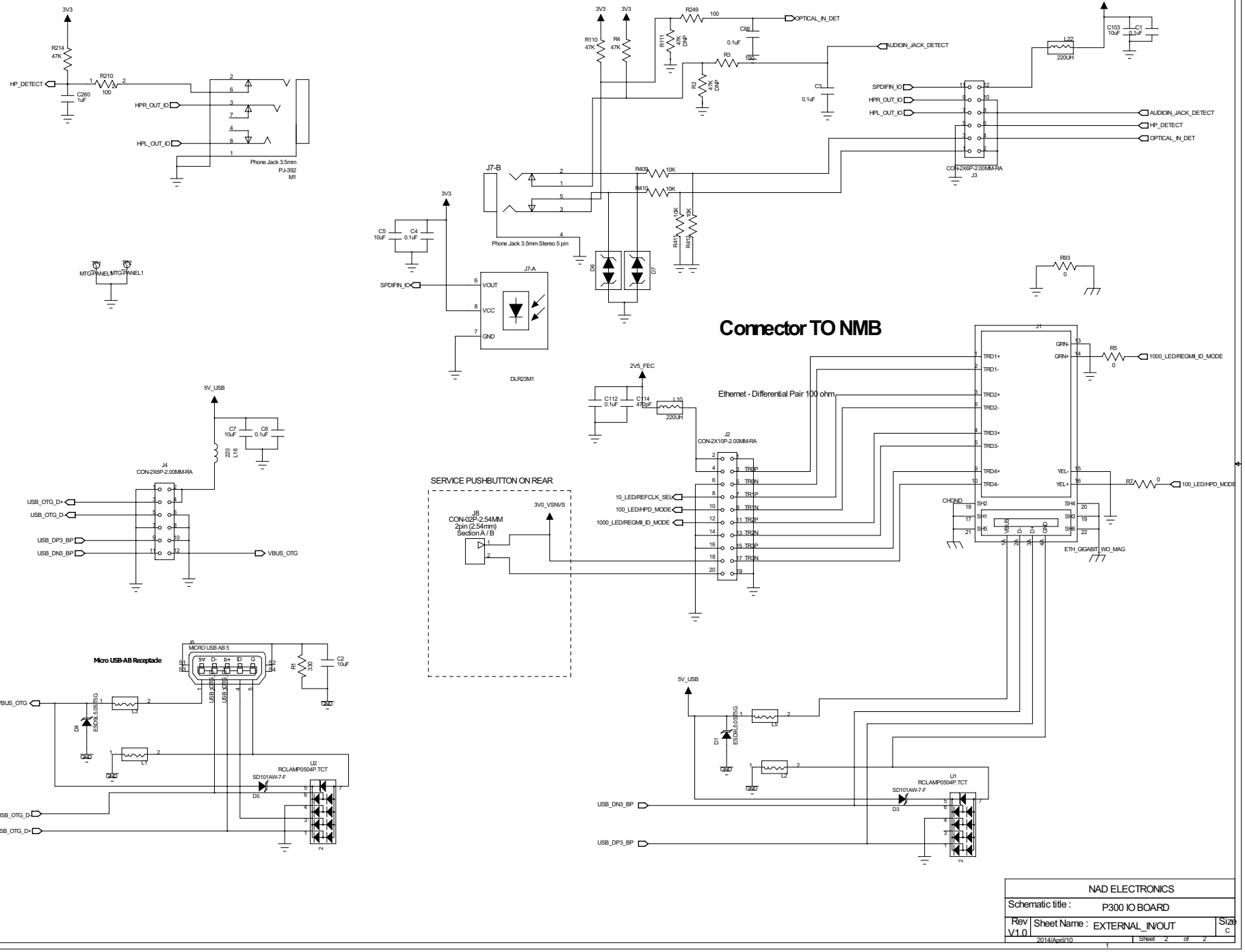
Elegant Audio Solutions
8706 Blazyk Drive
Austin, TX 78737
512-288-7786
((EAS))
BLO

Title: LENBROOK PULSE SMPS REV-B

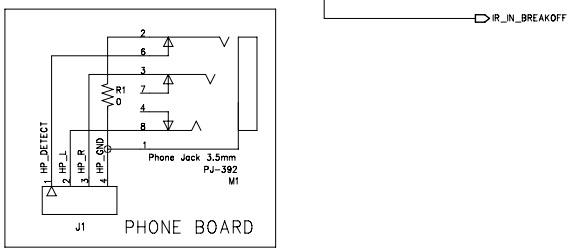
Size: B | Document Number: EAS-LENBRK-SMPS-B | Revision History | Rev: B1.0

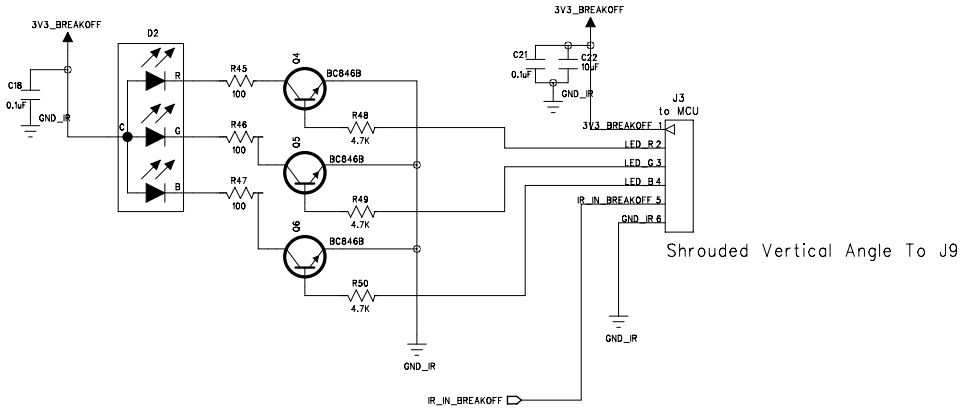
Date: Friday, June 15, 2018 | Sheet 1 of 2


J1
Pico Fuse 4A
Mini Fuse 4A / 250V
Time-Lag 8.5 x 8.5
486-1474-ND
0034.6621
Schurter Inc.
SPADE_LUG
J4
J5
J6
AC Line Input
90VAC - 265VAC
SO1
L2
2 x 4.2mH
L3
2 x 4.2mH
R10
5 Ohms-NTC
R27 680K 1206
R28 680K 1206
R29 680K 1206
R30 680K 1206
C6 0.22uF 305V
C10 0.22uF 305V
D6 S1G
D7 S1G
+373V max
+V
C1 100uF 450V
C4 100uF 450V
C5 0.1uF 400V
R1 182K 2512 1W
C2 DNP 1kV
D1 1V5KE160A 150V
R2 22 5%
D3
GBU6J-BP
D4 UF4006-E3/54
Q1 AOTF15S65L TO-220F
C3 2200pF 250V
T1
2x20t
(500uH)
7t (38uH)
8t (20uH)
7t (38uH)
XFMR-KT-7361F
D5 ES1D
R6 15 0805 5%
JP1 0
JP2 0
JP3 0
JP4 0
JP5 0
JP6 0
JP7 0
JP8 0
JP9 0
R11 4.7K 1206
R12 0.390 1210
R13 0.390 1210
C13 0.1uF 0603
C15 100uF 35V
C16 2200pF 250V
PGND
D8 1A 30V
R14 4.7K 1206
R15 4.7K 1206
D9 DNP 20V
U1
NCP1246BD065R2G
LATCH
FB
CS
GND
HV
VCC
DRV
R18 47 0805 5%
R19 22 0603
R20 100 0805
V (latch):
OVP > 2.5V
N.C. = 1.2V
OTP < 0.8V
C20 1uF 100V 1210
R22 100K-NTC 0603
R24 2.21K 0603
C21 1000pF 50V 0603
C22 DNP 50V 0603
R25 0
U2
FOD817B
R26 1K 0805
R16 1.5K 0603
R17 261K 0603
C17 68pF 0603
C18 1000pF 50V 0603
C19 68pF 0603
R21 10K 0603
U3
TL431
R23 22.1K 0603
MBRF40250TG
TO220-FP
D2
R4 240 1206
R5 240 1206
R7 240 1206
R8 240 1206
C7 390pF 450V 0805
C12 3300uF 35V
L1 1.5uH
C8 3300uF 35V
C9 10uF 63V 1210
C11 0.1uF 0603
+HV = +32VDC
+32V
J3
HDR 6x1
Ground Clips
CLP1
CLP2
CLP3
HS1
HEATSINK-P2i
C23 0.01uF 100VDC 0805
HS2
HEATSINK-P2i
C24 0.01uF 100VDC 0805
PRIMARY GND
SECONDARY HV GND
Elegant Audio Solutions
6706 Blazyk Drive
Austin, TX 78737
512-288-7786
Title
LENBROOK PULSE SMPS REV-B
Size
Custom
Document Number
EAS-LENBRK-SMPS-B
LENBROOK PULSE SMPS
Rev
B1.0
Date:
Friday, June 15, 2018
Sheet 2 of 2

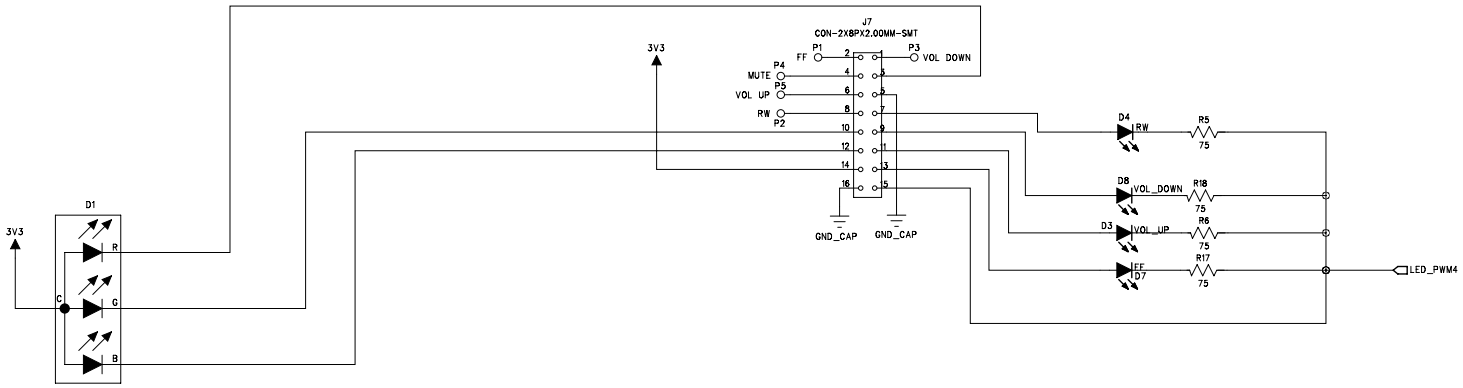

Connector TO NMB
Micro USB-AB Receptacle
SERVICE PUSHBUTTON ON REAR
Ethernet - Differential Pair 100 ohm
Phone Jack 3.5mm PJ-392 M1
Phone Jack 3.5mm Stereo 5 pin
DLR23M1
CON-2X6P-2.00MM-RA J3
CON-2X10P-2.00MM-RA J2
CON-2X6P-2.00MM-RA J4
MICRO USB AB 5
ETH_GIGABIT_WO_MAG
RCLAMP0504P.TCT
SD101AW-7-F
ESD9L5.0ST5G
OPTICAL_IN_DET
AUDIOIN_JACK_DETECT
HP_DETECT
1000_LED/REGMII_ID_MODE
100_LED/HPD_MODE
10_LED/REFCLK_SEL
VBUS_OTG
USB_OTG_D+
USB_OTG_D-
USB_DP3_BP
USB_DN3_BP
SPDIFIN_IO
NAD ELECTRONICS
Schematic title : P300 IO BOARD
Rev V1.0
Sheet Name : EXTERNAL_IN/OUT
Size C
2014/April/10
Sheet 2 of 2

BREAKOFF BOARD of LED/IR Sensor for P series



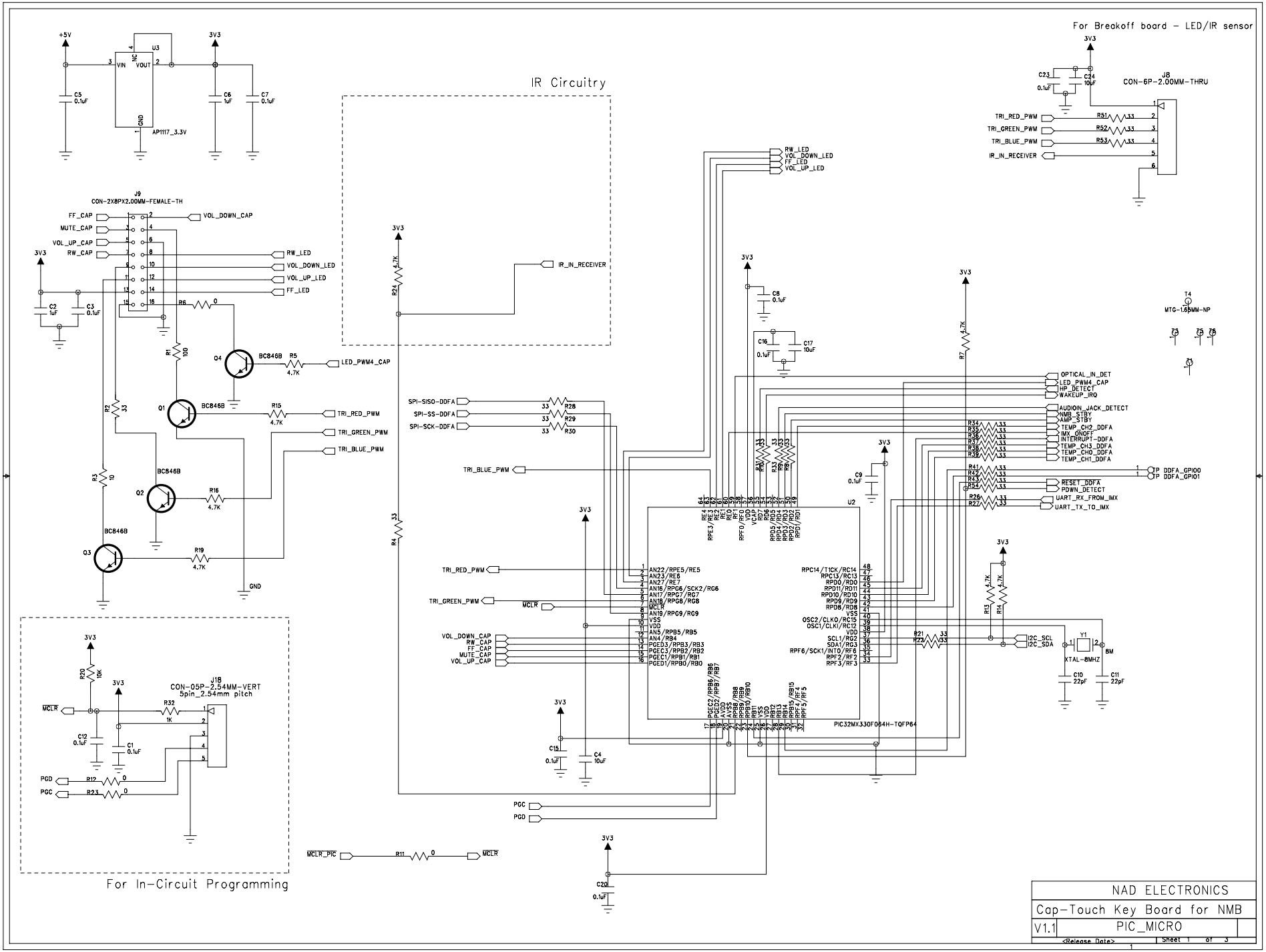


NAD ELECTRONICS	
Cap-Touch Key Board for NMB	
V1.0	BREAK_OFF_IR/RGB
<Release Date>	Sheet 1 of 1

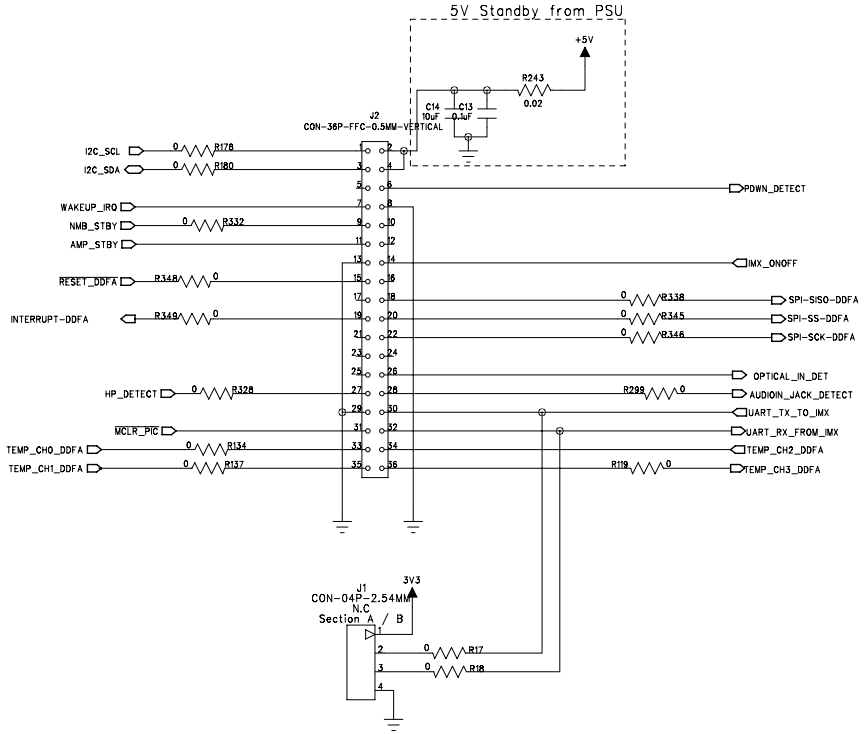


T7 T8 T9 T10

NAD ELECTRONICS	
Cap-Touch Key Board for NMB	
V1.0	CAP_TOUCH_PAD
<Release Date>	Sheet 1 of 1


For Breakoff board – LED/IR sensor
IR Circuitry
For In-Circuit Programming
+5V
3V3
U3
AP1117_3.3V
C5 0.1uF
C6 1uF
C7 0.1uF
J9
CON-2X8PX2.00MM-FEMALE-TH
FF_CAP
MUTE_CAP
VOL_UP_CAP
RW_CAP
VOL_DOWN_CAP
RW_LED
VOL_DOWN_LED
VOL_UP_LED
FF_LED
R6 0
R1 100
R2 33
R3 10
Q1 BC846B
Q2 BC846B
Q3 BC846B
Q4 BC846B
R5 4.7K
R15 4.7K
R16 4.7K
R19 4.7K
LED_PWM4_CAP
TRI_RED_PWM
TRI_GREEN_PWM
TRI_BLUE_PWM
GND
R24 4.7K
IR_IN_RECEIVER
J8
CON-6P-2.00MM-THRU
R51 33
R52 33
R53 33
C23 0.1uF
C24 10uF
C8 0.1uF
C16 0.1uF
C17 10uF
C9 0.1uF
R7 4.7K
T4
MTG-1.65MM-NP
T3
T5
T6
R28 33
R29 33
R30 33
R4 33
SPI-SISO-DDFA
SPI-SS-DDFA
SPI-SCK-DDFA
OPTICAL_IN_DET
LED_PWM4_CAP
HP_DETECT
WAKEUP_IRQ
AUDIOIN_JACK_DETECT
NMB_STBY
AMP_STBY
TEMP_CH2_DDFA
IMX_ONOFF
INTERRUPT-DDFA
TEMP_CH3_DDFA
TEMP_CH0_DDFA
TEMP_CH1_DDFA
DDFA_GPIO0
DDFA_GPIO1
RESET_DDFA
PDWN_DETECT
UART_RX_FROM_IMX
UART_TX_TO_IMX
U2
PIC32MX330F064H-TQFP64
MCLR
VOL_DOWN_CAP
RW_CAP
FF_CAP
MUTE_CAP
VOL_UP_CAP
R13 4.7K
R14 4.7K
R21 33
R22 33
I2C_SCL
I2C_SDA
Y1
XTAL-8MHZ
C10 22pF
C11 22pF
C15 0.1uF
C4 10uF
C20 0.1uF
PGC
PGD
MCLR_PIC
R11 0
J18
CON-05P-2.54MM-VERT
5pin_2.54mm pitch
R20 10K
R32 1K
C12 0.1uF
C1 0.1uF
R12 0
R23 0
NAD ELECTRONICS
Cap-Touch Key Board for NMB
V1.1
PIC_MICRO
<Release Date>
Sheet 1 of 3

Connector to NMB Board



NAD ELECTRONICS		
Cap-Touch Key Board for NMB		
V1.1	CONNECTOR	
<Release Date>		Sheet 2 of 3

Cap-Touch Keyboard				NMB					
MCU Pin Number	MCU Pin Name	Keyboard Net Name	Function	NMB Net Name	N110	N180	P100	P200	P300v2
21	RPB8/RB8	LED3_TIMER5	breakoff board				•	•	•
22	RPB9/RB9	LED2_TIMER4	breakoff board				•	•	•
48	RPC14/T1CK/RC14	LED1_TIMER1	breakoff board				•	•	•
29	RB14	\HYPEX_ONOFF	HYPEX	\HYPEX_ONOFF		•			•
46	RPD0/RD0	HYPEX_FAULT_DETECT	HYPEX	HYPEX_FAULT_DETECT		•			•
47	RPC13/RC13	HYPEX_AUDIO_EN	HYPEX	HYPEX_AUDIO_EN		•			•
1	AN22/RPE5/PMD5/RE5	RED_LED	keyboard						
2	AN23/PMD6/RE6	GREEN_LED	keyboard						
3	AN27/RE7	BLUE_LED	keyboard						
11	AN5/RPB5/RB5	VOL_UP	keyboard						
12	AN4/RB4	MUTE	keyboard						
13	PGED3/RPB3/RB3	VOL_DOWN	keyboard						
14	PGEC3/RPB2/RB2	RW	keyboard						
15	PGEC1/RPB1/RB1	FF	keyboard						
16	PGED1/RPB0/RB0	TRI-LED-PWM	keyboard						
58	RPF0/RF0	LED_PWM4	keyboard						
61	RE1	GPIO for LED FF	keyboard						
62	RE2	GPIO FOR LED VOL UP	keyboard						
63	RPE3/RE3	GPIO FOR LED VOL DN	keyboard						
64	RE4	GPIO FOR LED RW	keyboard						
24	RB11	GPIO0	NMB	GPIO0	•	•	•	•	•
33	RPF3/RF3	UART_TX_TO_IMX	NMB	UART_TX_TO_IMX	•	•	•	•	•
34	RPF2/RF2	UART_RX_FROM_IMX	NMB	UART_RX_FROM_IMX	•	•	•	•	•
35	RPF6/SCK1/INT0/RF6	IR_IN	NMB	IR_IN	•	•			
36	SDA1/RG3	I2C_SDA	NMB	I2C_SDA	•	•	•	•	•
37	SCL1/RG2	I2C_SCL	NMB	I2C_SCL	•	•	•	•	•
43	RPD9/RD9	MUTE_AMP	NMB	MUTE_AMP			•	•	•
44	RPD10/RD10	RESET_AMP	NMB	RESET_AMP			•	•	•
45	RPD11/RD11	THERMAL_WARN	NMB	THERMAL_WARN			•	•	•
49	RPD1/RD1	PDN_AMP	NMB	PDN_AMP			•	•	•
50	RPD2/RD2	AMP_STBY	NMB	AMP_STBY		•			•
51	RPD3/RD3	NMB_STBY	NMB	NMB_STBY	•	•	•	•	•
52	RPD4/RD4	AUDIO_JACK_DETECT	NMB	AUDIO_JACK_DETECT	•	•	•	•	•
53	RPD5/RD5	IRIN_DETECT	NMB	IRIN_DETECT	•	•			
54	RD6	WAKEUP_IRQ	NMB	WAKEUP_IRQ	•	•	•	•	•
55	RD7	HP_DETECT	NMB	HP_DETECT	•	•			
59	RF1	TRIGGER_DETECT	NMB	TRIGGER_DETECT	•	•			
60	RE0	IMX_ONOFF	NMB	IMX_ONOFF	•	•	•	•	•
17	PGEC2/RPB6/RB6	PGEC	PIC program						
18	PGED2/RPB7/RB7	PGED	PIC program						
30	RPB15/RB15	STATUS_LED3	PWM	STATUS_LED3	•	•			
31	RPF4/RF4	STATUS_LED2	PWM	STATUS_LED2	•	•			
32	RPF5/RF5	STATUS_LED1	PWM	STATUS_LED1	•	•			
4	AN16/RPG6/SCK2/RG6	SPI-SCK-DDFA	TO DDFA	SPI-SCK-DDFA		•			•
5	AN17/RPG7/RG7	SPI-SS-DDFA	TO DDFA	SPI-SS-DDFA		•			•
8	AN19/RPG9/RG9	SPI-SISO-DDFA	TO DDFA	SPI-SISO-DDFA		•			•
28	RB13	GPIO0_DDFA	TO DDFA	GPIO0_DDFA		•			•
42	RPD8/RD8	DDFA-GPIO1	TO DDFA	DDFA-GPIO1	•				•

NAD ELECTRONICS	
Cap-Touch Key Board for NMB	
V1.1	PIC_GPIO_ASSIGNMENT
<Release Date>	Sheet 3 of 3