Wireless LAN PC Card WP320

Operational Description

Version 1.0
April 2003

Copyright Statement

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received including interference that may cause undesired operation.

FCC Certifications

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These Limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

FCC Caution:

To assure continued compliance,(example – use only shielded interface cables when connecting to computer or peripheral devices).Any changes or modifications not expressly approved by the part responsible for compliance could void your authority to operate the equipment.

FCC RF Radiation Exposure Statement

This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. SAR compliance has been established in the laptop computer(s) configurations with PCMCIA slot on the side near the center, as tested in the application for Certification, and can be used in laptop computer(s) with substantially similar physical dimensions, construction, and electrical and RF characteristics. This transmitter is restricted for use with the specific antenna(s) tested in the application for Certification. The antenna(s) used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter."

Contents

1. Introduction:

Basically speaking, the schematics could be separate in two parts:
Analog Part: Including RTL8180, SA2400, 2A2411.
Digital Part: Including RTL8180, 93C56.

This document contains circuit operation theory for Wireless LAN PC Card WP320. The Remotek Wireless LAN PC Card WP320 is a flexible data communications facility implemented as an extension to, or as an altemative for, a wired LAN. Using radio frequency(RF) connections. Thus, wireless LANs combine data commectivity with user mobility. Figure 1. shows a simplified block diagram of the Wireless LAN PC Card WP320.

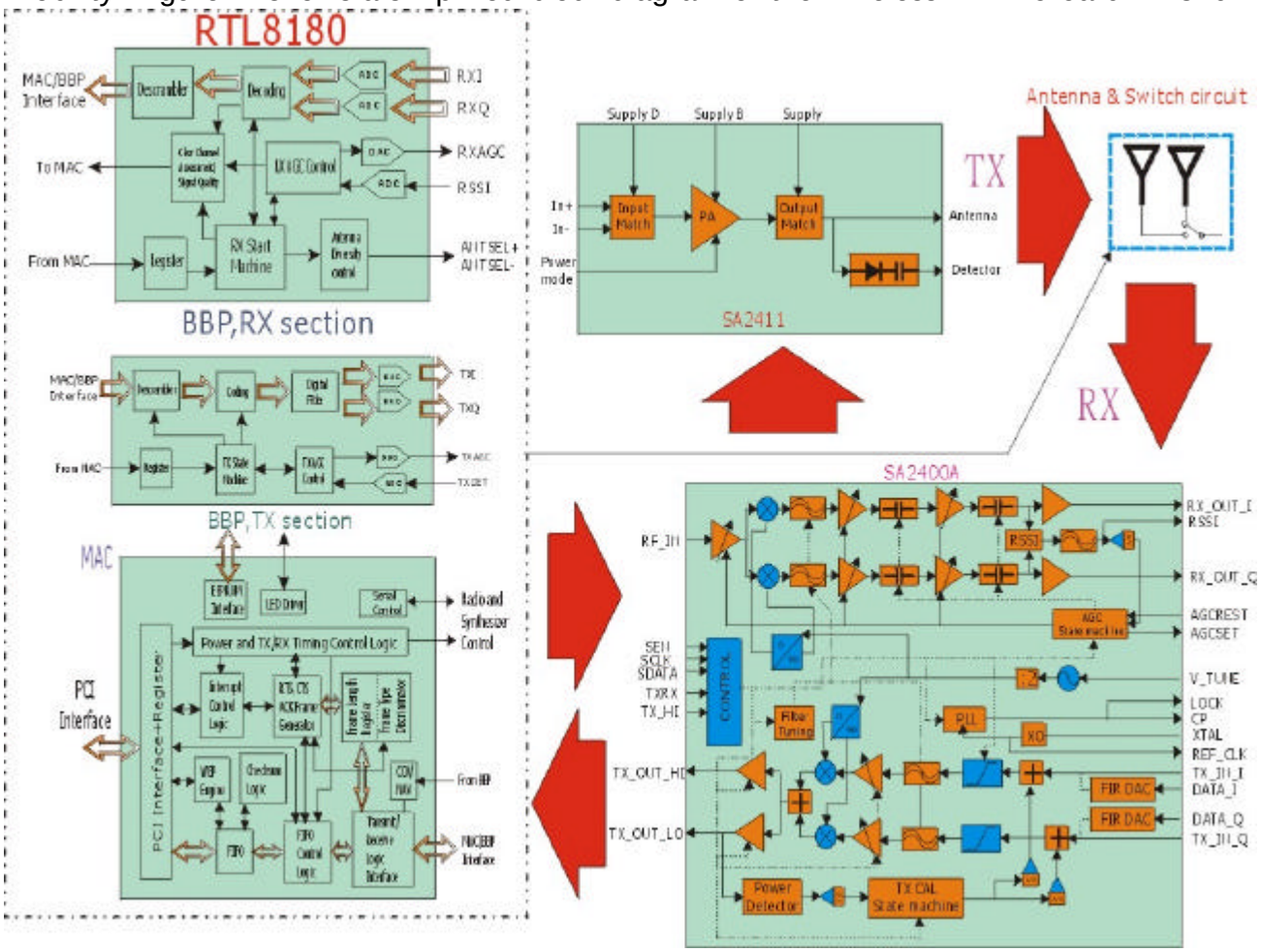


Figure 1. Wireless LAN PC Card WP320 Block Diagram

2. About RTL8180

2.1 General Description

A block diagram that is based on the RTL8180 performs the inter-networking between Ethernet and IEEE802.11b Wireless LAN is shown in Figure 2.

The Realtek RTL8180 is a highly integrated and cost-effective wireless LAN network interface controller that integrates a wireless LAN MAC and a direct sequence spread spectrum baseband processor into one chip. It provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.11 and IEEE 802.11b specifications.

The RTL8180 has on board A/D and D/A converters for analog I and Q inputs and outputs. Differential phase shift keying modulation schemes DBPSK and DQPSK, with data scrambling capability, are available along with complementary code keying to provide a variety of data rates. Both receive and transmit AGC functions obtain maximum performance in the analog portions of the transceiver. The RTL8180 also includes a built-in enhanced signal detector to alleviate severe multipath effects. The target environment for 11Mbps is 125ns RMS delay spread. It also supports short preamble and antenna diversity. For security issues, the RTL8180 also implements a high performance internal WEP engine supporting up to 104 bit WEP.

It also supports Advanced Configuration Power management Interface (ACPI), PCI power management system for modern operating systems that are capable of Operating System directed Power Management (OSPM) to achieve the most efficient power management possible.

In addition to the ACPI feature, the RTL8180 also supports remote wake-up (including AMD Magic Packet and Microsoft® wake-up frame) in both ACPI and APM environments. The RTL8180 is capable of performing an internal reset through the application of auxiliary power. When the auxiliary power is applied and the main power remains off, the RTL8180 is ready and waiting for the Magic Packet or wake-up frame to wake the system up. Also, the LWAKE pin provides four different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the RTL8180 LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality.

PCI Vital Product Data (VPD) is also supported to provide the information that uniquely

identifies hardware (i.e., the RTL8180 LAN card). The information may consist of part number, serial number, and other detailed information.

The RTL8180 supports an enhanced link list descriptor-based buffer management architecture, which is an essential part of a design for a modern network interface card. It contributes to lowering CPU utilization. Also, the RTL8180 boosts its PCI performance by supporting PCI Memory Read Line & Memory Read Multiple when transmitting, and Memory Write and Invalidate when receiving.

The RTL8180 keeps network maintenance costs low and eliminates usage barriers. The RTL8180 is highly integrated and requires no "glue" logic or external memory.

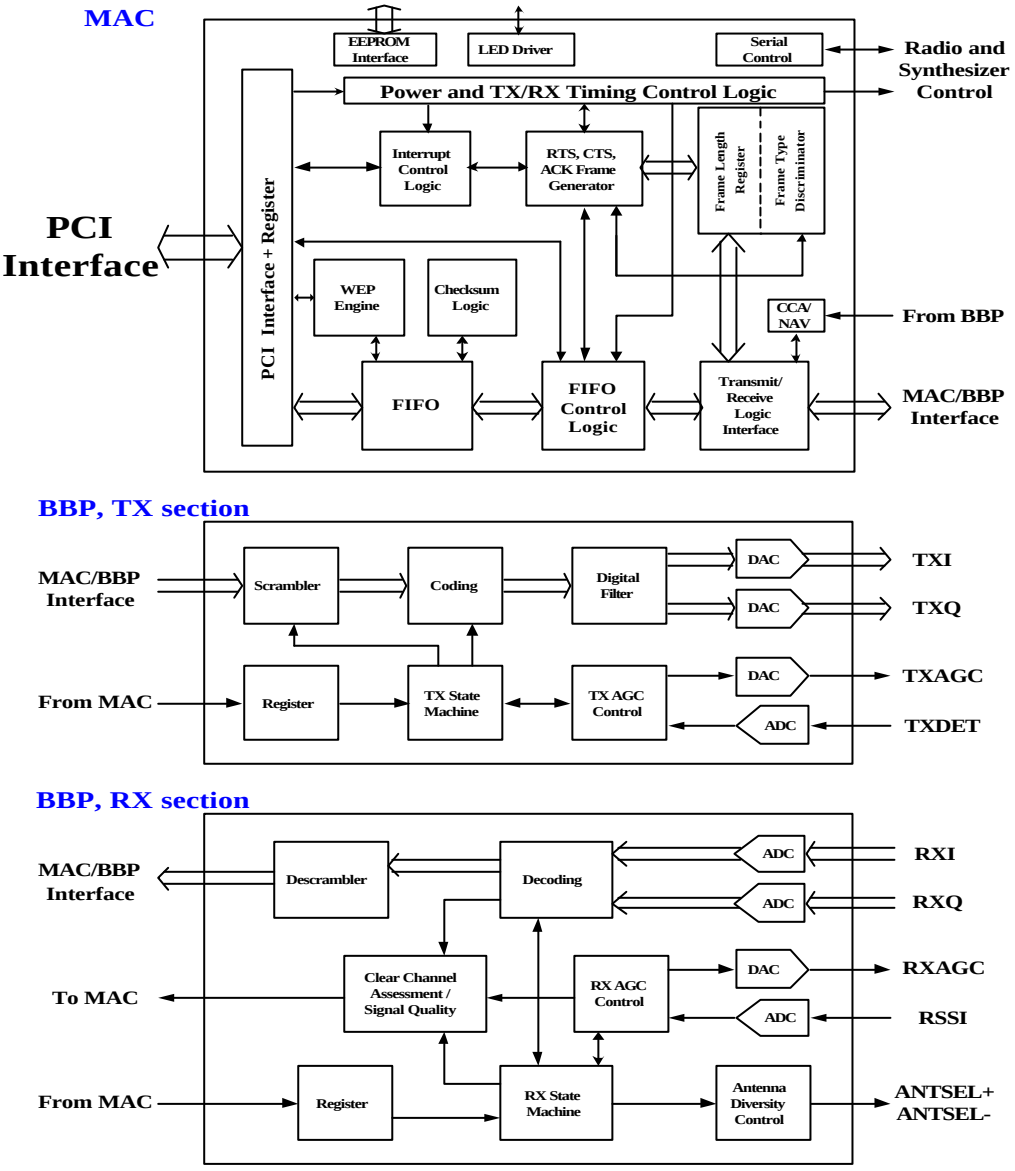


Figure 2. Block Diagram for RTL8180

2.2 Transmit & Receive Operations

The RTL8180 supports a new descriptor-based buffer management that will significantly lower host CPU utilization. The RTL8180 supports up to 64 consecutive descriptors in memory for transmit and receive separately, which means there might be 5 descriptor rings. Transmit descriptor rings have one beacon transmit descriptor ring, one high priority descriptor ring, one normal priority descriptor ring and one low priority descriptor ring. Each transmit descriptor ring may consist of up to 64 8-double-word consecutive descriptors and each receive descriptor ring may consist of up to 64 4-double-word consecutive descriptors, separately. The start address of each descriptor group should be in 256-byte alignment. Software must pre-allocate enough buffers and configure all descriptor rings before transmitting and/or receiving packets. Descriptors can be chained to form a packet, in both Tx and Rx. Please refer to the Realtek RTL8180 programming guide for detailed information. Any Tx buffers pointed to by one of the Tx descriptors should be at least 4 bytes.

2.3 Loopback Operation

Loopback mode is normally used to verify that the logic operations have performed correctly. In loopback mode, the RTL8180 takes frames from the transmit descriptor and transmits them up to internal Rx logic. The loopback function does not apply to an external PHYceiver.

2.4 Tx Encapsulation

While operating in Tx mode, the RTL8180 encapsulates the frames that it transmits according to the Differential Binary Phase Shift Keying (DBPSK) for 1Mbps, Differential Quaternary Phase Shift Keying (DQPSK) for 2Mbps, and Complementary Code Keying (CCK) for 5.5Mbps and 11Mbps modulators. The changes of the original packet data are listed as follows:

1. The PLCP preamble is always transmitted as the DBPSK waveform and used by the receiver to achieve initial PN synchronization.
2. The PLCP header can be configured to be either DBPSK or DQPSK and includes the

necessary data fields of the communications protocol to establish the physical layer link.

3. The MAC frame can be configured for DBPSK, DQPSK or CCK.

2.5 Rx Decapsulation

The RTL8180 continuously monitors the network when reception is enabled. When activity is recognized it starts to process the incoming data. After detecting receive activity on the channel, the RTL8180 starts to process the PLCP preamble and header based on the mode of operation.

The RTL8180 checks CRC16 and CRC32, then reports if CRC16 and CRC32 has error. The RTL8180 also checks the ICV when using the 40-bit WEP and 104-bit WEP module to decrypt and reports if ICV has errors.

2.6 Memory Functions

2.6.1 Memory Read Line (MRL)

The Memory Read Line command reads more than a longword (DWORD), up to the cache line boundary, in a prefetchable address space. The Memory Read Line command is semantically identical to the Memory Read command except that it additionally indicates that the master intends to fetch a complete cache line. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by reading up to a cache line boundary in response to the request rather than a single memory cycle. As with the Memory Read command, pre-fetched buffers must be invalidated before any synchronization events are passed through this access path.

The RTL8180 performs MRL according to the following rules:

i. Read access that reaches the cache line boundary uses the Memory Read Line command (MRL), instead of Memory Read command.

ii. Read access that does not reach the cache line boundary uses Memory Read (MR) command.

iii. Memory Read Line (MRL) command operates in conjunction with Memory Read Multiple command (MRM).

iv. RTL8180 will terminate the read transaction on the cache line boundary when it is out of resources on the transmit DMA. For example, the transmit FIFO is almost full.

2.6.2 Memory Read Multiple (MRM)

The Memory Read Multiple command is semantically identical to the Memory Read command except that it additionally indicates that the master may intend to fetch more than one cache line before disconnecting. The memory controller should continue pipelining memory requests as long as FRAMEB is asserted. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by sequentially reading ahead one or more additional cache line(s) when a software transparent buffer is available for temporary storage.

The RTL8180 performs MRM according to the following rules:

i. When RTL8180 reads full cache lines, it will use Memory Read Multiple command.

ii. If the memory buffer is not cache-aligned, the RTL8180 will use Memory Read Line command to reach the cache line boundary first.

Example:

Assume the packet length = 1514 byte, cache line size = 16 longwords (DWORDs), and Tx buffer start address = 64m+4 (m > 0).

;Step1: Memory Read Line (MRL)

;Data: (0-3) => (4-7) => (8-11) =>… … … … => (56-59) (byte offset of the Tx packet)

;From Address: <64m+4>, <64m+8>, … … … ., <64m+60> (reach cache line boundary)

;Step2. Memory Read Multiple (MRM)

;Data: (60-63) => (64-67) => (68-71) => … … … … … … … … … …. .. => (1454-1467)

;From Address: <64m+64>, <64m+68>, … … … … … … …. ., <64m+64+(16*4)*21+(16-1)*4>

;Step3. Memory Read(MR)

;Data: (1468-1471) => (1472-1475) => … … … … … … … … … … … , => (1510-1513)

;From
Address:<64m+64+(16*4)*22>,<64m+64+(16*4)*22+4>,..,<64m+64+(16*4)*22+42>
Step1: Memory Read Multiple (MRM)
Data: (0-3) => (4-7) => (8-11) =>… … … … .. => (1454-1467)
From Address: <64m+4>, <64m+8>, … … … ., <64m+64+(16*4)*21+(16-1)*4>
Step2. Memory Read(MRL)
Data: (1468-1471) => (1472-1475) => … … … … … … … … … … … , => (1510-1513)
From
Address:<64m+64+(16*4)*22>,<64m+64+(16*4)*22+4>,..,<64m+64+(16*4)*22+42>

2.6.3 Memory Write and Invalidate (MWI)

The Memory Write and Invalidate command is semantically identical to the Memory Write command except that it additionally guarantees a minimum transfer of one complete cache line; i.e., the master intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. Note: All byte enables must be asserted during each data phase for this command. The master may allow the transaction to cross a cache line boundary only if it intends to transfer the entire next line also. This command requires implementation of a configuration register in the master indicating the cache line size and may only be used with Linear Burst Ordering. It allows a memory performance optimization by invalidating a "dirty" line in a write-back cache without requiring the actual write-back cycle, thus shortening access time. The RTL8180 uses MWI command while writing full cache lines, and Memory Write command while writing partial cache lines.

When the following requirements are approved, the RTL8180 issues MWI command, instead of MW command on Rx DMA.

i. The Cache Line Size written in the offset 0Ch of the PCI configuration space is 8 or 16 longwords (DWORDs).
ii. The accessed address is cache line aligned.
iii. The RTL8180 has at least 8/16 longwords (DWORDs) of data in its RX FIFO.
iv. The MWI (bit 4) in the PCI configuration command register should be set to 1.

The RTL8180 uses the Memory Write(MW) command instead of MWI whenever there's any one of the above listed requirements failed. The RTL8180 terminates the WMI cycle at the end of the cache line when a WMI cycle has started and at least one of the requirements are

no longer hold.

Example:

Assume Rx packet length = 1514 byte, cache line size = 16 DWORDs (longwords), and Rx buffer start address = 64m+4 (m > 0).

Step1: Memory Write (MW)

Data: (0-3) => (4-7) => (8-11) => … … … … => (56-59) (byte offset of the Rx packet)

To Address: <64m+4>, <64m+8>, … … … … ., <64m+60> (reach cache line boundary)

Step2. Memory Write and Invalidate (MWI)

Data: (60-63) => (64-67) => (68-71) => … … … … … … … … ….. …. => (1454-1457)

To Address: <64m+64>, <64m+68>, … … … … … … ….. .., <64m+64+(16*4)*21+(16-1)*4>

Step3. Memory Write(MW)

Data: (1458-1461) => (1462-1465) => … … … … … … … … ….. … … => (1512-1513)

To Address: <64m+64+(16*4)*22>, <64m+64+(16*4)*22+4>, , <64m+64+(16*4)*22+42>

2.7 LED Functions

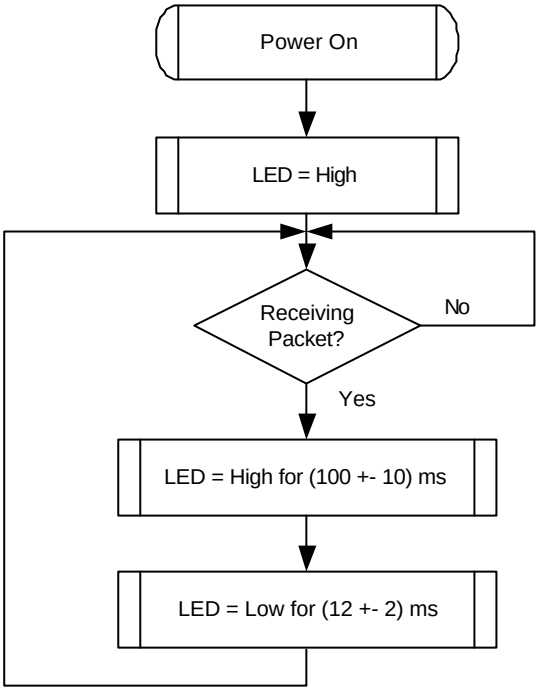
The RTL8180 supports 2 LED signals in 4 different configurable operation modes. The following sections describe the different LED actions.

The Link Monitor senses the link integrity. Whenever link status is established, the specific link LED pin is driven low.

The Infrastructure Monitor senses the link integrity at Infrastructure network. Whenever link ok at Infrastructure network status is established, the specific Infrastructure LED pin is driven low.

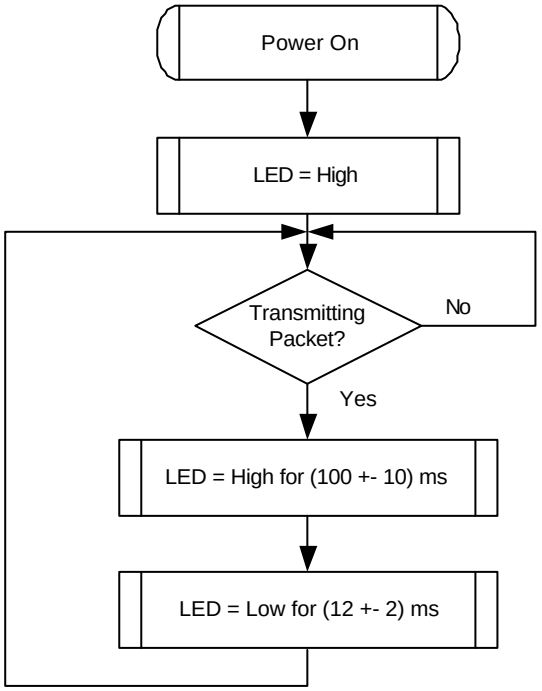
2.7.1 Rx LED

Blinking of the Rx LED indicates that receive activity is occurring.



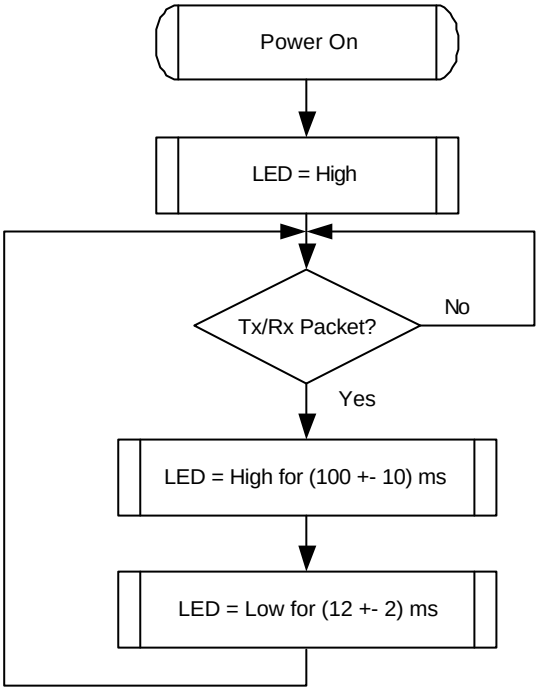
2.7.2 Tx LED

Blinking of the Tx LED indicates that transmit activity is occurring.



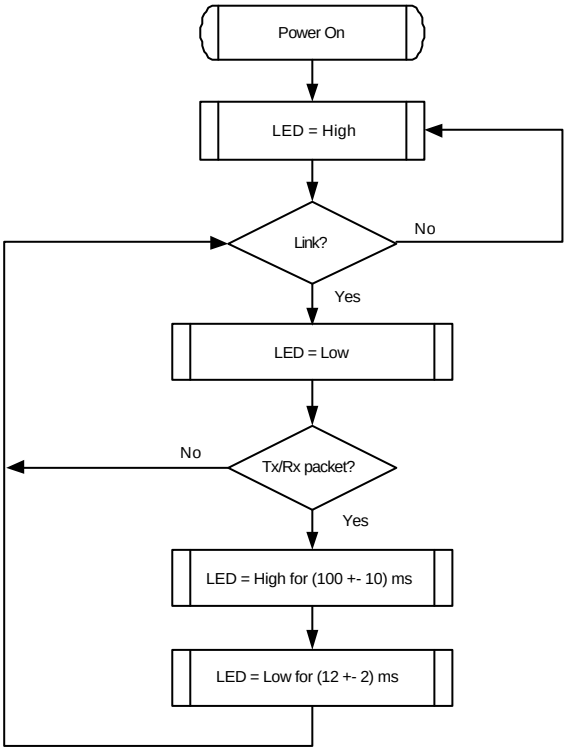
2.7.3 Tx/Rx LED

Blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.



2.7.4 LINK/ACT LED

Blinking of the LINK/ACT LED indicates that the RTL8180 is linked and operating properly. This LED high for extended periods, indicates that a link problem exists.



3. About SA2400 : Transceiver for 2.45 GHz ISM Band

3.1 Description

The SA2400A is a fully integrated single IC RF transceiver designed for 2.45GHz wireless LAN (WLAN) applications. It features a direct conversion radio architecture and is fabricated in an advanced 30GHz f_T BiCMOS process. The SA2400A combines a receiver, transmitter, and LO generation into a single IC. The receiver consists of low-noise amplifier, down-conversion mixers, fully integrated channel filters, and an Automatic Gain Control (AGC) with an on-chip closed loop. The transmitter contains power ramping, filters, up-conversion, and pre-drivers. The LO generation is formed by an entirely on-chip VCO and a fractional-N synthesizer.

Typical system performance parameters for the receiver are 93dB gain, 7.5dB noise figure, input-referred third-order intercept point (IIP3) of +1dBm, AGC settling time of 8 us, and Tx-to-Rx switching time of 3 us. The transmitter typical system performance parameters are an output power range from –7dBm to +8dBm in 1 dB steps, -40dBc carrier leakage after calibration, 22 dB sideband suppression, in-band common mode rejection of 30dB, and Rx-to-Tx switching time of 3 us.

3.2 Functional Blocks and Features

The block diagram of the SA2400A Direct Conversion transceiver is given in Fig 3. It consists of the following functional blocks:

A 79 dB adjustable gain range direct conversion zero IF receiver with 3 usec (typical) Tx to Rx switching time, and comprising the following:

- ✧ Front end LNA with two internal gain states
- ✧ A fast on-chip closed loop composite RF and IF AGC with zoomed analog RSSI output and 8 usec settling time
- ✧ Quadrature downconverters from 2.45 GHz RF directly to zero IF
- ✧ On-chip fast baseband DC cancellation with automatically stepped bandwidths of 10 MHz, 1 MHz, 100 kHz and 10 kHz, settling within 8-13 usec for a DC error of 10% that decays to 1%.
- ✧ Fully integrated channel filters, appropriate for 11 Msymbols/s QPSK modulation RF bandwidth.

An I/Q upconverter from base band directly to 2.45 GHz, with +18.23 dBm output power, -40dBc typical carrier leakage (calibrated) and 3 μs (typical) Rx to Tx switching time, and comprising the following:

Wide band IQ modulator producing better than 14% EVM for 11 Msymbols/sec QPSK modulation

Integrated reconstruction and spectral shaping filters at I and Q modulation input that is driven by an external D/A. High common mode rejection to input ground bounce.

FIR-DACs for digital I/Q input feeding the analog signal path and including additional filtering for spectral shaping.

✧2.45 GHz Power Amplifier driver with +18.23 dBm maximum output, 15 dB adjustable gain in 1 dB steps and a second switched output at –1.5 dBm power level with similar gain adjustments that are set by a separate register.

✧ Completely on-chip calibration for Carrier Leakage compensation.

✧ Internal power ramping with 2 us delay and 0.5 us ramp-up time.

A fractional N frequency synthesizer with on-chip VCO and XO,

A 3-wire bus for control of most blocks.

An additional high speed 3 wire bus for full control of Rx-Gain and DC-offset compensation parameters with 44Mbits/s.

Fast Tx-Rx switching based on a single digital input pin.

Reference currents and voltage for supply of Baseband Processor and PA-chip.

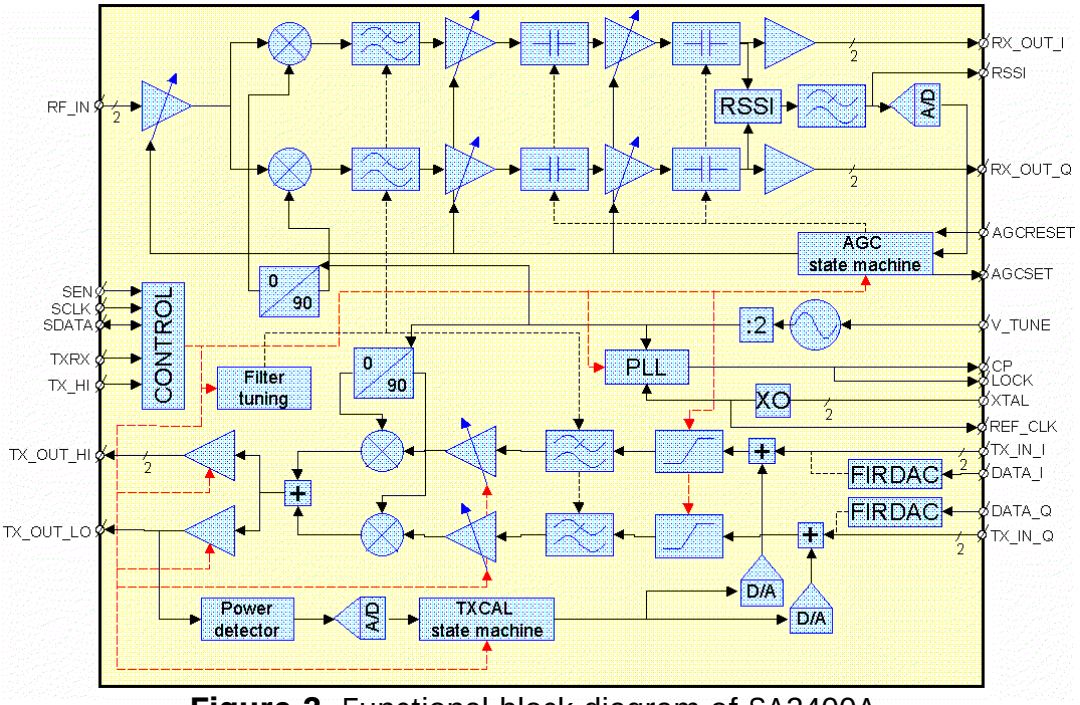


Figure 3. Functional block diagram of SA2400A

4. About SA2411 : +18.23 dBm Power amplifier

4.1 DESCRIPTION

The SA2411 is a linear power amplifier designed for the WLAN in the 2.4 GHz band. Together with the SA2400A the chips form a complete 802.11b transceiver. The SA2411 is a Si power amplifier with integrated matching and a possibility to adjust the linearity.The functional block diagram of SA2411 is shown in figure 4.

4.2 FUNCTIONAL DESCRIPTION

The main building-blocks are:

- ✧ Fixed gain amplifier (PA)
- ✧ Output matching
- ✧ Input matching
- ✧ Power Detector
- ✧ Power Mode

Input

The PA has differential inputs and a balun is needed in the case of single ended operation. Input impedance is 100 W per input. The inputs can be DC biased with the pin “Supply D”. The “D” stands for Driver. The input matching is optimized to interface with the SA2400A WLAN transceiver chip.

Amplifier

The amplifier has a fixed gain. It is a class AB amplifier. There is an additional pin to adjust the class A bias current. Reducing the class A currents reduces the gain. This option is available to allow a lower gain combined with a higher linearity and reduced current consumption. The biasing is supplied by pin “Supply B”. The “B” stands for Bias.

Output Matching

The output of the amplifier is matched to 50 W The matching includes the supply feed for the power amplifier. The pin “Supply” is the main supply for the amplifier. The matching is also a filter for harmonics. No additional filtering is needed to meet the 802.11b spec.

Power Detector

The power detector detects the power level and transforms it into a low frequency current. The detector output must be loaded with a resistor to ground for the highest accuracy. This resistor has an optimal value of 5.6 kW. Lower values can be used to comply with maximum input sensitivity of ADC's but sacrifice dynamic range.. At 5.6 kW the maximum voltage detected is 2.3 V.

Power Mode

This pin selects the desired gain and linearity level (14 dB or 15 dB gain). The low gain is more applicable to high voltage applications from 3.3 V to 3.6 V. The high gain is more applicable to low voltage applications lower than 3.3 V.

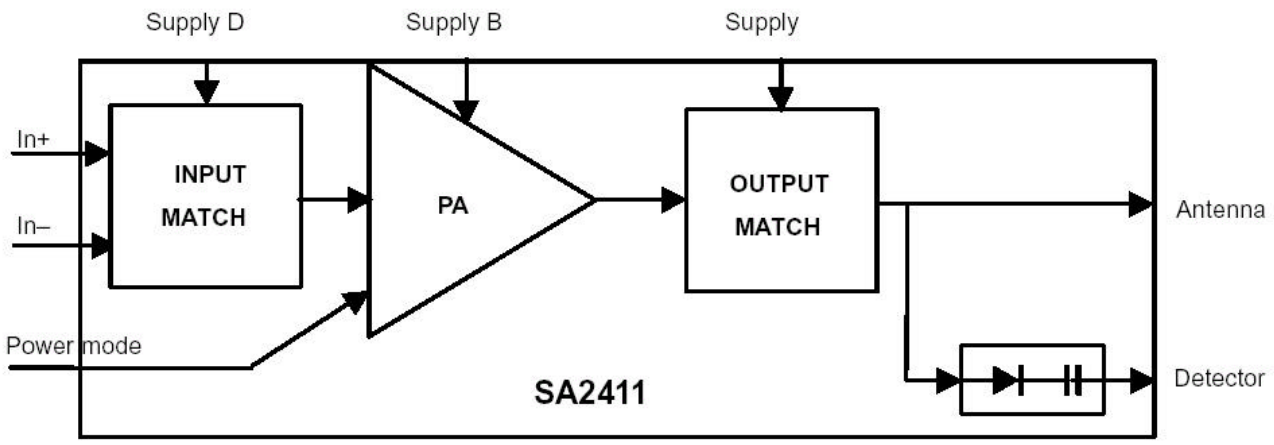


Figure 4. Functional block diagram of SA2411