FVG318 Product Operation Principle

Instructions
DUT: FVG318

    A: Need three PCs, which are PC1,PC2,PC3.

    B: Use UL/AU/UK/EU 12VDC@1A power adapters.

    C: Power on FVG318,link one of the Device's LAN port to the PC1,which can get the IP address automatically when the device start to work; link WAN port of Device to another PC2,then input 192.168.0.1 in IE page, and you can enter FVG318 setup pages, click WAN setting to get IP of WAN port.

EMI Test:

1. Put the device FVG318 and PC3 in the EMI chamber,PC3 need have wireless card, so that it can be used to link to the device's WLAN port.
2. Put the PC1,PC2 out of the chamber, link the PC1 which can get IP Address automatically to the LAN port of FVG318 using one UTP cable, and link the PC2 to the WAN port of FVG318 device using another UTP cable. Set the PC2 address:192.168.0.2, IP Subnet Mask:255.255.255.0,Gateway IP Address: 192.168.0.1.
3. Power on FVG318,do the command" ping 192.168.0.2 –t" at the PC1,it can get responses from PC2;The PC3 in the chamber link to the WLAN port of FVG318 device, and you can run art.exe in art_v53_build5_all file getting from Atheros corporation to setup wireless working mode, please run art \remote=192.168.0.20 to setup TX/RX/Link mode to test.
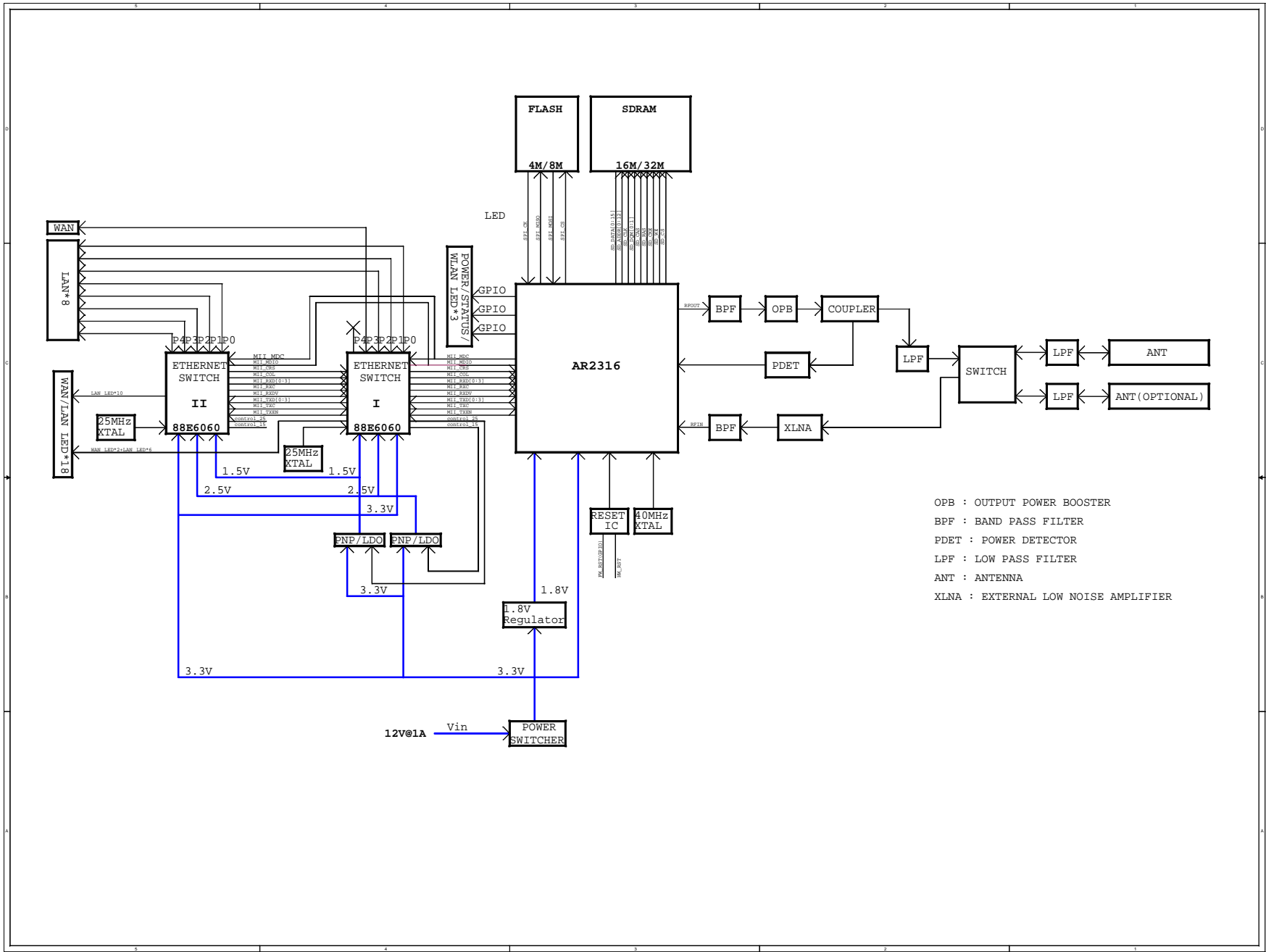
Block Diagram:

    FVG318 Block Diagram as below:

1. CPU, U3, AR2316 Single Chip MAC/ Baseband/ Radio/ Processor for 2.4GHz Wireless LANs.

The Atheros AR2316 integrated the MAC/ baseband/ radio and processor into a single chip for wireless access point and router applications. It includes a 2.4GHz radio, MIPS 4000 processor, 802.11 MAC/ baseband processor, 802.3 Ethernet MAC and MII interface, SDRAM controller, external memory interface for Flash, ROM, or UART, GPIOs, LED controls.

The AR2316 implements an 802.11 MAC/ baseband processor supporting all IEEE 802.11g data rates (1 to 54 Mbps) and all IEEE 802.11b complementary key coding (CCK) data rates (1 to 11 Mbps). In Atheros super G^{TM} mode, AR2316 supports data rates up to 108 Mbps. Additional features include forward error correction coding at rates for 1/2, 2/3, and 3/4, signal detection, automatic gain control, frequency offset estimation, symbol timing, channel estimation, error recovery, enhanced security, and quality of service (QoS).The AR2316 performs receive and transmit filtering for IEEE 802.3 and 802.11 network.

2. 2.4GHz – 2.5GHz Power Amplifier, U4, GP1214

GP1214 is a low cost and high performance power amplifier IC based on the highly reliable InGaP/GaAs HBT technology. With a 3x3 mm2 16-pin LCC package, GP1214 can be easily configured for high power/high efficiency application with superb power added efficiency while operating over the 2.4~2.5 GHz frequency band. It typically provides 30dB gain with 22% power added efficiency @ Pout= 22 dBm for 802.11g and 27% power added efficiency @ Pout= 24 dBm for 802.11b. GP1214 has excellent linearity, typically <4% added EVM up to 20 dBm output power which is essential for 54 Mbps 802.11g operation while meeting 802.11g spectrum mask at 23 dBm. GP1214 also has wide-range (>25dB) temperature stable (~1dB over 80℃) single-ended/differential power detectors which lower users' cost on power control. The power amplifier IC also features easy board level usage along with high speed power up/down control. Ultra-low reference current (total Iref<4mA) makes GP1214 controllable by on/off switching signal directly from baseband chip. These features coupled with low operating current make GP1214 ideal for the final stage power amplification in battery powered 802.11g/b WLAN transmitter applications.

FLASH
4M/8M

SDRAM
16M/32M

WAN

LAN*8

WAN/LAN LED*18

25MHz XTAL

POWER/STATUS/WLAN LED*3

ETHERNET SWITCH II
88E6060

ETHERNET SWITCH I
88E6060

25MHz XTAL

P4P3P2P1P0

P4P3P2P1P0

LAN LED*10

WAN LED*2+LAN LED*6

LED

GPIO
GPIO
GPIO

MII_MDC
MII_MDIO
MII_CRS
MII_COL
MII_RXD[0:3]
MII_RXC
MII_RXDV
MII_TXD[0:3]
MII_TXC
MII_TXEN
control_25
control_15

MII_MDC
MII_MDIO
MII_CRS
MII_COL
MII_RXD[0:3]
MII_RXC
MII_RXDV
MII_TXD[0:3]
MII_TXC
MII_TXEN
control_25
control_15

AR2316

RESET IC

40MHz XTAL

RFOUT

RFIN

BPF

BPF

OPB

PDET

XLNA

COUPLER

LPF

SWITCH

LPF

LPF

ANT

ANT(OPTIONAL)

1.5V
2.5V

1.5V
2.5V
3.3V

PNP/LDO

PNP/LDO

3.3V

1.8V

1.8V Regulator

3.3V

3.3V

12V@1A   Vin

POWER SWITCHER

OPB : OUTPUT POWER BOOSTER
BPF : BAND PASS FILTER
PDET : POWER DETECTOR
LPF : LOW PASS FILTER
ANT : ANTENNA
XLNA : EXTERNAL LOW NOISE AMPLIFIER

MAC/Baseband/Radio Processor Control Unit(U3)

The FVG318 is a 802.11b/g Wireless Broadband Router with 8-ports Fast Ethernet Switch ,With a web-based UI, it is easy to setup and maintain.   All functions can be configured with the exclusive, easy and friendly user interface via web browsers.

The AR2316 integrated the MAC/baseband/radio and processor into a single chip for wireless access point and router applications. It includes a 2.4 GHz radio, MIPS 4000 processor,802.11 MAC/baseband processor,802.3 ethernet MAC and MII interface,

The AR2316 implements an 802.11 MAC/baseband processor supporting all IEEE 802.11g data rate(1 to 54 Mbps) and all IEEE 802.11b complementary key coding (CCK) data rates(1 to 11 Mbps).In Super G mode,AR2316 supports data rates up to 108 Mbps. Additional features include forward error correction coding at rates for 1/2,2/3,and 3/4,signal detection, automatic gain control, frequency offset estimation, symbol timing, channel estimation, error recovery, enhanced security, and quality of service(QoS).The AR2316 performs receive and transmit filtering for 802.3/802.11.

Fast Ethernet Switch with 10Base-T/100Base-TX(U1,U9)

The Marvell 88E6060 is a single chip integration of a complete 6-port Fast Ethernet switch with support for a CPU connection. It contains five 10BASE-T/100BASE-TX transceivers(PHYs),two that can be used to set-port 100 BASE-FX; six independent Fast Ethernet media access controllers(MACs),a high-speed nonblocking switch fabric, a high-performance address lookup engine, and a 1/2 Mbit frame buffer memory. It is designed for cost-sensitive low port count switch systems and firewall routers.

The Marvell 88E6060 is designed to work in all environments. True Plug-n-Play is supported with Auto Cross Over, Auto Polarity and Auto Negotiation in both the PHYs, along with bridge loop prevention(using Port States implementing Spanning Tree support).

The shared memory-based switch fabric uses the latest Marvell switch architecture that provides non-blocking switching performance in all traffic environments. Back-pressure and pause-frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion. The lookup engine allows for up to 1024 active nodes to be connected with the switch.

The 6th port "always on" RMII/MII/SNI interface supports a direct connection to Management or Router CPUs with integrated MACs. It can be configured in either RMII mode, MII-PHY or MII-MAC mode or SNI mode. These interfaces along with BPDU handling, programmable per port VLAN configurations, and Port States, support Spanning Tree and truly isolated WAN vs. LAN firewall applications.

Power Regulator(VR1,U7,U8,U11)