Application

- IEEE802.11 a/b/g/n Wireless Local Area Networks
- USB 2.0 Wi-Fi Dongle

The RT3572 is a highly integrated MAC/BBP and 2.4 / 5 GHz RF single chip with 300Mbps PHY rate supporting. It fully complies with IEEE 802.11n draft 8.0 and IEEE 802.11 a/b/g standards, delivers reliable, cost-effective, feature rich wireless connectivity at high throughput from an extended distance. Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient USB engine and hardware data processing accelerators without overloading the host processor. The RT3572 is designed to support standard based features in the areas of security, quality of service and international regulation, giving end users the greatest performance anytime in any circumstance.

Features

- CMOS Technology with RF, Baseband, and MAC Integrated.
- 2T2R Mode with 300Mbps PHY Rate for Both Transmit and Receiving.
- Legacy and High Throughput Modes
- 20MHz/40MHz Bandwidth
- Reverse Direction Data Flow and Frame Aggregation
- WEP 64/128, WPA, WPA2
- QoS-WMM, WMM-PS
- Multiple BSSID Support
- USB 2.0
- International Regulation - 802.11d + h
- Cisco CCX Support
- Bluetooth Co-existence
- Low Power with Advanced Power Management
- Operating Systems - Windows XP, 2000, ME, 98SE, Vista, Linux, MAC

Order Information

Part Number	Temp Range	Package
RT3572L	-10~70 ^{0}C	Green/RoHS Compliant 88LD QFN (10mmx10mm)

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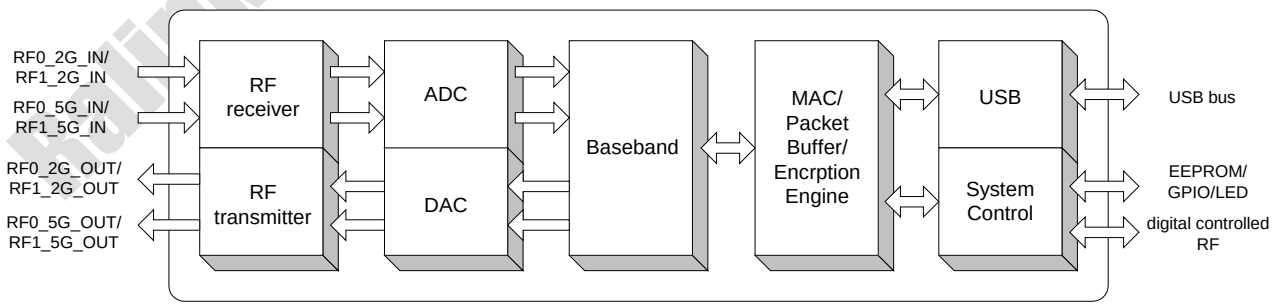
Functional Block Diagram



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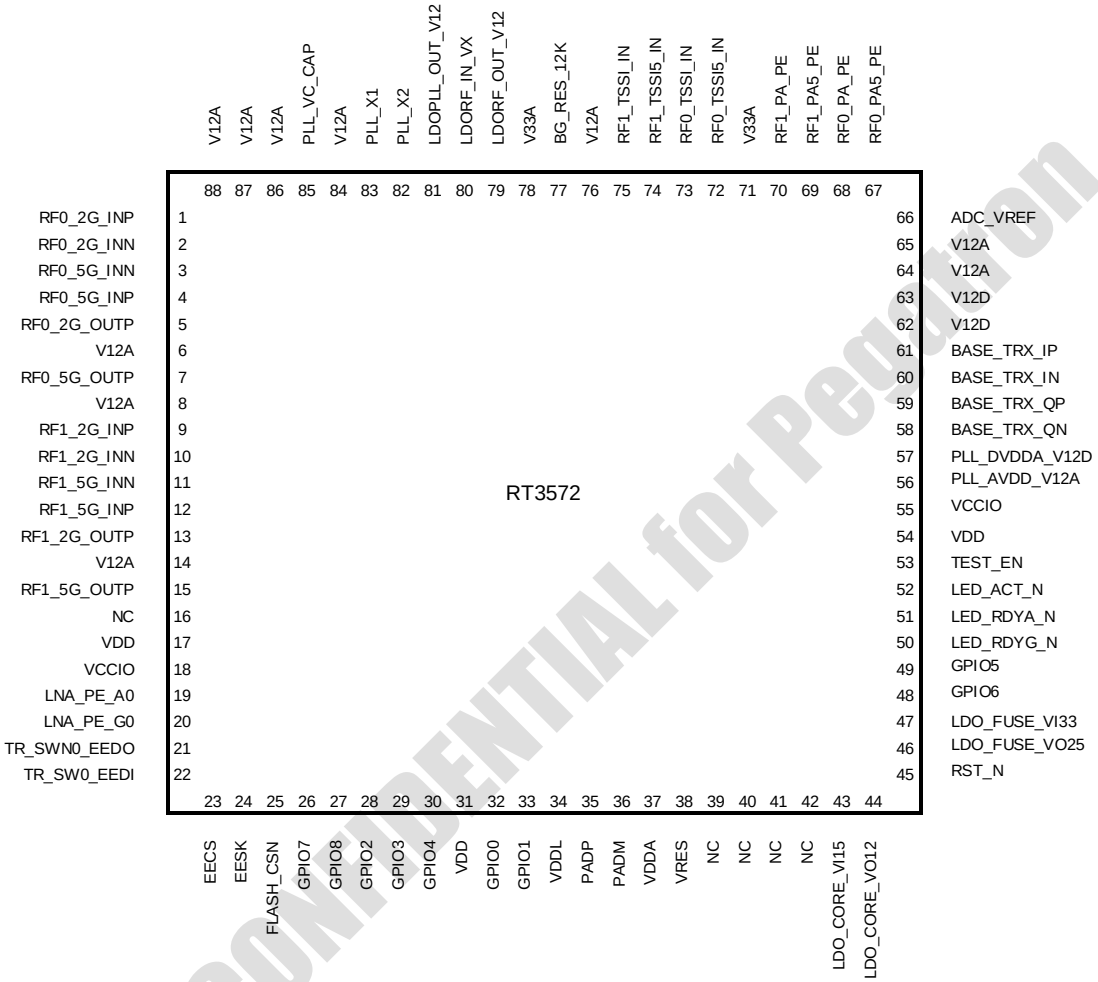
1 Pin DescriptionPin Layout



1.2 Pin Description

Pin	Name	Type*	Description
RF TX/RX: 12 pins			
1	RF0_2G_INP	I	2.4GHz RX0 input (positive)
2	RF0_2G_INN	I	2.4GHz RX0 input (negative)
4	RF0_5G_INP	I	5.0GHz RX0 input (positive)
3	RF0_5G_INN	I	5.0GHz RX0 input (negative)
5	RF0_2G_OUTP	O	2.4GHz TX0 output
7	RF0_5G_OUTP	O	5.0GHz TX0 output
9	RF1_2G_INP	I	2.4GHz RX1 input (positive)
10	RF1_2G_INN	I	2.4GHz RX1 input (negative)
12	RF1_5G_INP	I	5.0GHz RX1 input (positive)
11	RF1_5G_INN	I	5.0GHz RX1 input (negative)
13	RF1_2G_OUTP	O	2.4GHz TX1 output
15	RF1_5G_OUTP	O	5.0GHz TX1 output
RF Power: 14 pins			
6,8,14,64,65,76 ,84,86,87,88	V12A	P	1.2V Power Supply
71,78	V33A	P	3.3V Power Supply
62,63	V12D	P	1.2V Digital Power Supply
RF LDO: 3 pins			
79	LDORF_OUT_V12	O	LDO 1.2V 200mA output for RF Core
80	LDORF_IN_VX	P	LDO 1.5~2V 300mA input for RF core and PLL
81	LDOPLL_OUT_V12	O	LDO 1.2V 50mA output for RF PLL
RF PLL: 2 pins			
82	PLL_X2	O	Crystal oscillator (output)
83	PLL_X1	I	Crystal oscillator (input)
RF REF: 3 pins			
66	ADC_VREF	IO	Main ADC reference voltage
77	BG_RES_12K	IO	External reference resistor (12K ohm)
85	PLL_VC_CAP	IO	PLL external loop filter
RF Misc.: 8 pins			
72	RF0_TSSI5_IN	I	A mode TX0 TSSI monitoring (0.3 ~1.5V)
73	RF0_TSSI_IN	I	G mode TX0 TSSI monitoring (0.3 ~1.5V)
74	RF1_TSSI5_IN	I	A mode TX1 TSSI monitoring (0.3 ~1.5V)
75	RF1_TSSI_IN	I	G mode TX1 TSSI monitoring (0.3 ~1.5V)
58	BASE_TRX_QN	IO	Baseband Q differential input/output
59	BASE_TRX_QP	IO	Baseband Q differential input/output
60	BASE_TRX_IN	IO	Baseband I differential input/output
61	BASE_TRX_IP	IO	Baseband I differential input/output
Digital LDO: 4 pins			
43	LDO_CORE_VI15	P	1.5V power supply for internal LDO
44	LDO_CORE_VO12	O	1.2V LDO power output
46	LDO_FUSE_VO25	O	2.5V LDO power output
47	LDO_FUSE_VI33	P	3.3V power supply for internal LDO
RF Control: 8 pins			
67	RF0_PA5_PE	O	0~3.3V control for A mode external PA0 (20mA)
68	RF0_PA_PE	O	0~3.3V control for G mode external PA0 (20mA)
69	RF1_PA5_PE	O	0~3.3V control for A mode external PA1 (20mA)

70	RF1_PA_PE	O	0~3.3V control for G mode external PA1 (20mA)
22	TR_SW0_EEDI	O	Multifunction pins. Positive signal of Tx/RX switching control and EEPROM's serial data
21	TR_SWN0_EEDO	IO	Multifunction pins. Negative signal of Tx/RX switching control(output) and EEPROM's serial(input)
19	LNA_PE_A0	O	Enable control for A mode external LNA
20	LNA_PE_G0	O	Enable control for G mode external LNA
LED: 3 pins			
50	LED_RDYG_N	OD	Driving LED when wireless is transmitting, for G mode
51	LED_RDYA_N	OD	Driving LED when wireless is transmitting, for A mode
52	LED_ACT_N	OD	Driving LED when wireless is active
GPIO: 9 pins			
32	GPIO0	IO	GPIO
33	GPIO1	IO	GPIO
28	GPIO2	IO	GPIO
29	GPIO3	IO	GPIO
30	GPIO4	OD	GPIO
49	GPIO5	IO	GPIO
48	GPIO6	IO	GPIO
26	GPIO7	IO	GPIO
27	GPIO8	IO	GPIO
USB: 5 pins			
34	VDDL	P	1.2 V USB power
35	PADP	IO	D+ line of USB
36	PADM	IO	D- line of USB
37	VDDA	P	3.3 V USB power
38	VRES	IO	Connect to external 8.2K resistor (the 8.2K resistor connects one end to VRES and another end to PCB ground)
EEPROM: 2 pins			
24	EESK	O	EEPROM clock
23	EECS	O	EEPROM chip select
PLL Power: 2 pins			
56	PLL_AVDD_V12A	P	1.2V PLL power
57	PLL_DVDD_V12D	P	1.2V PLL power
Core Power: 3 pins			
17,31,54	VDD	P	1.2V for digital circuit
IO Power: 2 pins			
18,55	VCCIO	P	3.3V for digital IO
Misc.: 8 pins			
45	RST_N	I	0: reset the whole chip 1: normal function active
53	TEST_EN	I	1: enable test mode. For normal function, tie to GND.
25	FLASH_CSN	OD	External serial flash control.
16,39,40,41,42	NC	IO	No connect
GND: exposed pad			

*Notation of Type:
I : input
O : output
OD: open-drain
IO :bi-direction
P : power

2 Maximum Ratings and Operating Conditions Absolute Maximum Ratings

Supply Voltage 1.38V
I/O Supply Voltage..... 3.6V
Input, Output or I/O Voltage..... GND –0.3V to Vcc+0.3V

2.2 Thermal Information

Maximum Junction Temperature (Plastic Package) .....125°C
Maximum Lead Temperature (Soldering 10s)..... 260°C

Thermal characteristics in still air condition

Thermal Resistance	θ_{JA}(°C/W) for JEDEC 2Lsystem PCB	54.4°C /W
Thermal Resistance	θ_{JA}(°C/W) for JEDEC 4Lsystem PCB	20.9°C /W
Thermal Resistance	θ_{JC}(°C/W) for JEDEC 2Lsystem PCB	7.9°C /W
Thermal Resistance	θ_{JC}(°C/W) for JEDEC 4Lsystem PCB	7.6°C /W
Thermal Characterization parameter	Ψ_{Jt} (°C/W) for JEDEC 2L system PCB	4.5°C /W
Thermal Characterization parameter	Ψ_{Jt} (°C/W) for JEDEC 4L system PCB	2.2°C /W

Note: JEDEC 51-9 system FR4 PCB size: 3"x4.5" (76.2x114.3mm)

2.3 Operating Conditions

Ambient Temperature Range ..... -10 to 70°C
Core Supply Voltage..... 1.14V to 1.38V
I/O Supply Voltage ..... 3.0V to 3.6V

2.4 Storage Condition

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

a) Mounted within 168-hours of factory conditions < 30 **°C** /60%RH
b) Storage humidity needs to maintained at <10% RH
c) Baking is necessary if customer expose the component to air over 168 hrs, baking condition: 125°C / 8hrs

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2.5 DC Electrical Characteristics

Parameters	Sym	Conditions	Min	Typ	Max	Unit
3.3V Supply Voltage	Vcc33		3.0	3.3	3.6	V
1.2V Supply Voltage	Vcc12		1.14	1.2	1.38	V
Low-Band Receiving						
3.3V Current Consumption	Icc33	HT40 MCS15		50		mA
1.2V Current Consumption	Icc12	HT40 MCS15		435		mA
High-Band Receiving						
3.3V Current Consumption	Icc33	HT40 MCS15		50		mA
1.2V Current Consumption	Icc12	HT40 MCS15		480		mA
Low-Band Transmission						
3.3V Current Consumption	Icc33	HT40 MCS15		30		mA
1.2V Current Consumption	Icc12	HT40 MCS15		185		mA
High-Band Transmission						
3.3V Current Consumption	Icc33	HT40 MCS15		35		mA
1.2V Current Consumption	Icc12	HT40 MCS15		230		mA

2.6 AC Electrical Characteristics

Ta=25 °C, unless otherwise specified.

2.6.1 RF Low-Band Receiver

f_{RF} = 2437MHz, f_{LO} = 3256MHz, $f_{baseband}$ = 5MHz, unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Unit
RF Frequency Range		2400		2500	MHz
LO Frequency Range		3216		3312	MHz
Conversion Voltage Gain (agc<5:1> = 11111)	lna_gain<1:0> = 11	88	90	92	dB
	lna_gain<1:0> = 10		74		
	lna_gain<1:0> = 01		61		
Gain Variation over RF Frequency	lna_gain<1:0> = 11			1	dB
Baseband Output Amplitude (Pin = -90 dBm, AGC code = 11111)	lna_gain<1:0> = 11		316		mV
	lna_gain<1:0> = 10		50		
	lna_gain<1:0> = 01		11.2		
Double-Sideband Noise Figure	lna_gain<1:0> = 11, agc<5:1> = 11111		5		dB
Input P1dB	lna_gain<1:0> = 11		-30		dBm
	lna_gain<1:0> = 10		-16		
	lna_gain<1:0> = 01		0		
LNA Gain Switching Time	RF to Baseband Filter Input			0.1	μs
LO Leakage	RF Input				dBm

2.6.2 RF High-Band Receiver

f_{RF} = 5505MHz, f_{LO} = 4400MHz, $f_{baseband}$ = 5MHz, unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Unit
RF Frequency Range		4900		5800	MHz
LO Frequency Range		3930		4644	MHz
Conversion Voltage Gain (agc<5:1> = 11111)	lna_gain<1:0> = 11	83	85	87	dB
	lna_gain<1:0> = 10		70		
	lna_gain<1:0> = 01		55		
Gain Variation over RF Frequency	lna_gain<1:0> = 11		2		dB
Baseband Output Amplitude (Pin = -90 dBm, AGC code = 11111)	lna_gain<1:0> = 11		300		mV
	lna_gain<1:0> = 10		60		
	lna_gain<1:0> = 01		9.5		
Double-Sideband Noise Figure	lna_gain<1:0> = 11, agc<5:1> = 11111		8		dB
Input P1dB	lna_gain<1:0> = 11	-32	-30	-28	dBm
	lna_gain<1:0> = 10	-18	-15	-14	
	lna_gain<1:0> = 01	-2	0	2	
LNA Gain Switching Time	RF to Baseband Filter Input			0.15	μs
LO Leakage	RF Input				dBm

2.6.3 RF Low-Band Transmitter

f_{RF} = 2437MHz, f_{LO} = 3256MHz, $f_{baseband}$ = 5MHz, unless otherwise specified.

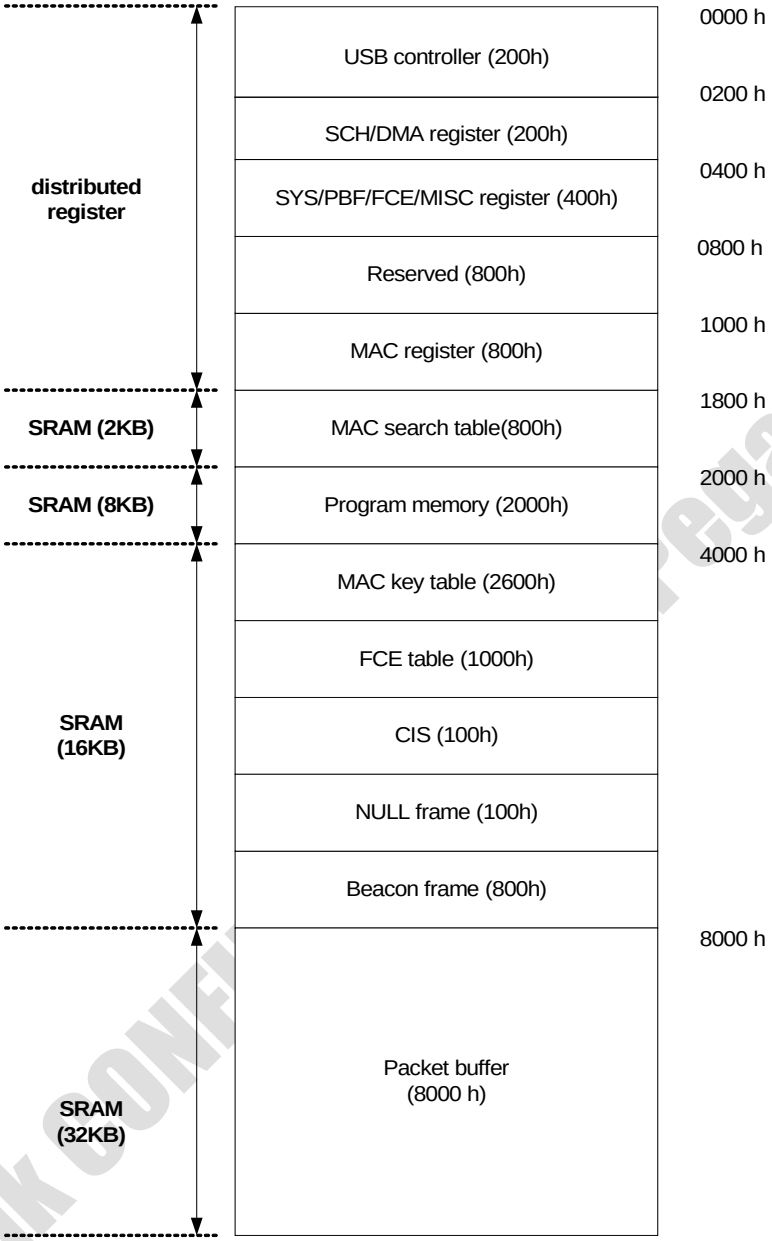
Parameters	Conditions	Min	Typ	Max	Unit
RF Frequency Range		2400		2500	MHz
LO Frequency Range		3216		3312	MHz
Output Power (OFDM)	Vin(rms)=45mV, ALC Code = 11000		-6		dBm
Output Power (CCK)	Vin(rms)=90mV, ALC Code = 11000		0		dBm
Output Power Variation over RF Frequency				1	dB
Output P1dB			4		dBm
ACPR (OFDM)	Pout=-6dBm, OFDM, 10MHz offset		-48	-45	dBc
Output Noise Floor	Pout=-6dBm, ALC Code = 10010		-141		dBm/Hz
LO Suppression	Pout=-6dBm		30		dBc
Carrier Suppression			20		dBc
Single-Sideband Suppression	$2f_{LO} - f_{RF}$	35	40		dBc
Tx ALC Gain Control Step	5-bit control = 32 levels		0.5		dB/step

2.6.4 RF High-Band Transmitter

f_{RF} = 5505MHz, f_{LO} = 4400MHz, $f_{baseband}$ = 5MHz, unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Unit
RF Frequency Range		4900		5850	MHz
LO Frequency Range		3930		4644	MHz
Output Power (OFDM)	Vin(rms)=45mV, ALC Code = 11000		-6		dBm
Output Power Variation over RF Frequency				3	dB
Output P1dB			4		dBm
ACPR (OFDM)	Pout=-6dBm, OFDM, 10MHz offset		-48	-45	dBc
Output Noise Floor	Pout=-6dBm, ALC Code = 10010		-141		dBm/Hz
LO Suppression	Pout=-6dBm		40		dBc
Carrier Suppression			20		dBc
Single-Sideband Suppression	$2f_{LO} - f_{RF}$	35	40		dBc
Tx ALC Gain Control Step	4-bit control = 16 levels		1		dB/step
	Additional attenuation (Tx4 = 0)		4		dB

3 Register map



3.1 SCH/DMA registers

INT_STATUS (offset: 0x0200,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:18			Reserved	
17	R/W	TX_COHERENT	TX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	0
16	R/W	RX_COHERENT	RX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	0
15	R/W	MAC_INT_4	MAC interrupt 4: GP timer interrupt	0
14	R/W	MAC_INT_3	MAC interrupt 3: Auto wakeup interrupt	0
13	R/W	MAC_INT_2	MAC interrupt 2: TX status interrupt	0
12	R/W	MAC_INT_1	MAC interrupt 1: Pre-TBTT interrupt	0
11	R/W	MAC_INT_0	MAC interrupt 0: TBTT interrupt	0
10	RO	TX_RX_COHERENT	When TX_COHERENT or RX_COHERENT is on, this bit is set	0
9	R/W	MCU_CMD_INT	MCU command interrupt	0
8	R/W	TX_DONE_INT5	TX Queue#5 packet transmit interrupt Write 1 to clear the interrupt.	0
7	R/W	TX_DONE_INT4	TX Queue#4 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
6	R/W	TX_DONE_INT3	TX Queue#3 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
5	R/W	TX_DONE_INT2	TX Queue#2 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
4	R/W	TX_DONE_INT1	TX Queue#1 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
3	R/W	TX_DONE_INT0	TX Queue#0 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
2	R/W	RX_DONE_INT	RX packet receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
1	R/W	TX_DLY_INT	Summary of the whole WPDMA TX related interrupts Write 1 to clear the interrupt. Read to get the raw interrupt status	0
0	R/W	RX_DLY_INT	Summary of the whole WPDMA RX related interrupts Write 1 to clear the interrupt. Read to get the raw interrupt status	0

INT_MASK (offset:0x0204,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:18			Reserved	
17	R/W	TX_COHERENT_EN	Enable for TX_DMA data coherent interrupt	0
16	R/W	RX_COHERENT_EN	Enable for RX_DMA data coherent interrupt	0
15	R/W	MAC_INT4_EN	MAC interrupt 4: GP timer interrupt	0
14	R/W	MAC_INT3_EN	MAC interrupt 3: Auto wakeup interrupt	0
13	R/W	MAC_INT2_EN	MAC interrupt 2: TX status interrupt	0

12	R/W	MAC_INT1_EN	MAC interrupt 1: Pre-TBTT interrupt	0
11	R/W	MAC_INT0_EN	MAC interrupt 0: TBTT interrupt	0
10			Reserved	
9	R/W	MCU_CMD_INT_MSK	MCU command interrupt enable	0
8	R/W	TX_DONE_INT_MSK5	TX Queue#5 packet transmit interrupt	0
7	R/W	TX_DONE_INT_MSK4	TX Queue#4 packet transmit interrupt	0
6	R/W	TX_DONE_INT_MSK 3	TX Queue#3 packet transmit interrupt	0
5	R/W	TX_DONE_INT_MSK 2	TX Queue#2 packet transmit interrupt	0
4	R/W	TX_DONE_INT_MSK 1	TX Queue#1 packet transmit interrupt	0
3	R/W	TX_DONE_INT_MSK 0	TX Queue#0 packet transmit interrupt	0
2	R/W	RX_DONE_INT_MSK	RX packet receive interrupt	0
1	R/W	TX_DLY_INT_MSK	Summary of the whole WPDMA TX related interrupts	0
0	R/W	RX_ DLY_INT_MSK	Summary of the whole WPDMA RX related interrupts	0

WPDMA_GLO_CFG (offset:0x0208,default :0x00000060)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:8		HDR_SEG_LEN	Specify the header segment size in byte to support RX header/payload scattering function, when set to a non-zero value. When set to zero, the header/payload scattering feature is disabled.	8'b0
7	R/W	BIG_ENDIAN	The endian mode selection. DMA applies the endian rule to convert payload and TX/RX information. DMA won't apply endian rule to register or descriptor. 1: big endian. 0: little endian.	0
6	R/W	TX_WB_DDONE	0 :Disable TX_DMA writing back DDONE into TXD 1 : Enable TX_DMA writing back DDONE into TXD	1'b1
5:4	R/W	WPDMA_BT_SIZE	Define the burst size of WPDMA 0 : 4 DWORD (16bytes) 1 : 8 DWORD (32 bytes) 2 : 16 DWORD (64 bytes) 3 : 32 DWORD (128 bytes)	2'd2
3	RO	RX_DMA_BUSY	1 : RX_DMA is busy 0 : RX_DMA is not busy	0
2	R/W	RX_DMA_EN	1 : Enable RX_DMA 0 : Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop.)	0
1	RO	TX_DMA_BUSY	1 : TX_DMA is busy 0 : TX_DMA is not busy	0
0	R/W	TX_DMA_EN	1 : Enable TX_DMA 0 : Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.)	0

WPDMA_RST_IDX (offset:0x020C,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:17			Reserved	
16	W1C	RST_DRX_IDX0	Write 1 to reset to RX_DMARX_IDX0 to 0	1'b0
15:6			Reserved	
5	W1C	RST_DTX_IDX3	Write 1 to reset to TX_DMATX_IDX5 to 0	1'b0
4	W1C	RST_DTX_IDX2	Write 1 to reset to TX_DMATX_IDX4 to 0	1'b0
3	W1C	RST_DTX_IDX3	Write 1 to reset to TX_DMATX_IDX3 to 0	1'b0
2	W1C	RST_DTX_IDX2	Write 1 to reset to TX_DMATX_IDX2 to 0	1'b0
1	W1C	RST_DTX_IDX1	Write 1 to reset to TX_DMATX_IDX1 to 0	1'b0
0	W1C	RST_DTX_IDX0	Write 1 to reset to TX_DMATX_IDX0 to 0	1'b0

DELAY_INT_CFG (offset:0x0210,default :0x00000000)

Bits	Type	Name	Description	Init Value
31	RW	TXDLY_INT_EN	1: Enable TX delayed interrupt mechanism. 0: Disable TX delayed interrupt mechanism.	1'b0
30:24	RW	TXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final TX_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'b0
23:16	RW	TXMAX_PTIME	Specified Max pending time for the internal TX_DONE_INT0-5. When the pending time equal or grater TXMAX_PTIME x 20us or the # of pended TX_DONE_INT0-5 equal or grater than TXMAX_PINT (see above), an Final TX_DLY_INT is generated Set to 0 will disable pending interrupt time check	8'b0
15	RW	RXDLY_INT_EN	1: Enable RX delayed interrupt mechanism. 0: Disable RX delayed interrupt mechanism.	1'b0
14:8	RW	RXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final RX_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'b0
7:0	RW	RXMAX_PTIME	Specified Max pending time for the internal RX_DONE_INT. When the pending time equal or grater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or grater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated Set to 0 will disable pending interrupt time check	8'b0

WMM_AIFSN_CFG (offset:0x0214,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:12	RW	AIFSN3	WMM parameter AIFSN3	4'h0
11:8	RW	AIFSN2	WMM parameter AIFSN2	4'h0
7:4	RW	AIFSN1	WMM parameter AIFSN1	4'h0
3:0	RW	AIFSN0	WMM parameter AIFSN0	4'h0

WMM_CWMIN_CFG (offset:0x0218,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:12	RW	CW_MIN3	WMM parameter Cw_min3	4'h0
11:8	RW	CW_MIN2	WMM parameter Cw_min2	4'h0
7:4	RW	CW_MIN1	WMM parameter Cw_min1	4'h0
3:0	RW	CW_MIN0	WMM parameter Cw_min0	4'h0

WMM_CWMAX_CFG (offset:0x021C,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:12	RW	CW_MAX3	WMM parameter Cw_max3	4'h0
11:8	RW	CW_MAX2	WMM parameter Cw_max2	4'h0
7:4	RW	CW_MAX1	WMM parameter Cw_max1	4'h0
3:0	RW	CW_MAX0	WMM parameter Cw_max0	4'h0

WMM_TXOP0_CFG (offset:0x0220,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16	RW	TXOP1	WMM parameter TXOP1	16'h0
15:0	RW	TXOP0	WMM parameter TXOP0	16'h0

WMM_TXOP1_CFG (offset:0x0224,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16	RW	TXOP3	WMM parameter TXOP3	16'h0
15:0	RW	TXOP2	WMM parameter TXOP2	16'h0

GPIO_CTRL (offset:0x0228,default : 0x0100_FF00)

Bits	Type	Name	Description	Init Value
31:25	R		Reserved	7'b0
24	RW	GPIO8_D	GPIO8 direction 0: Output 1: Input	1'b1
23:17	R		Reserved	7'b0
16	RW	GPIO8_O	GPIO8 data	1'b0
15:8	RW	GPIO7_0_D	GPIO7~0 direction 0: Output 1: Input	8'hFF
7:0	RW	GPIO7_0_O	GPIO7~0 data	8'h00

MCU_CMD_REG (offset:0x022C,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	RW	MCU_CMD	MCU command register. Internal 8051 write this register will trigger MCU command interrupt (0x0200 bit 9) to host.	8'h0

TX_BASE_PTR0 (offset:0x0230,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:0	R/W	TX_BASE_PTR0	Point to the base address of TX_Ring0 (4-DWORD aligned address)	0

TX_MAX_CNT0 (offset:0x0234,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11:0	R/W	TX_MAX_CNT0	The maximum number of TXD count in TXD_Ring0.	0

TX_CTX_IDX0 (offset:0x0238,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11:0	R/W	TX_CTX_IDX0	Point to the next TXD CPU wants to use	0

TX_DTX_IDX0 (offset:0x023C,default :0x00000000)

Bits	Type	Name	Description	Init Value
11:0	RO	TX_DTX_IDX0	Point to the next TXD DMA wants to use	0

TX_BASE_PTR2 (offset:0x0250,default :0x00000000)
TX_MAX_CNT2 (offset:0x0254,default :0x00000000)
TX_CTX_IDX2 (offset:0x0258,default :0x00000000)
TX_DTX_IDX2 (offset:0x025C,default :0x00000000)
TX_BASE_PTR3 (offset:0x0260,default :0x00000000)
TX_MAX_CNT3 (offset:0x0264,default :0x00000000)
TX_CTX_IDX3 (offset:0x0268,default :0x00000000)
TX_DTX_IDX3 (offset:0x026C,default :0x00000000)
TX_BASE_PTR4 (offset:0x0270,default :0x00000000)
TX_MAX_CNT4 (offset:0x0274,default :0x00000000)
TX_CTX_IDX4 (offset:0x0278,default :0x00000000)
TX_DTX_IDX4 (offset:0x027C,default :0x00000000)
TX_BASE_PTR5 (offset:0x0280,default :0x00000000)
TX_MAX_CNT5 (offset:0x0284,default :0x00000000)
TX_CTX_IDX5 (offset:0x0288,default :0x00000000)
TX_DTX_IDX5 (offset:0x028C,default :0x00000000)

RX_BASE_PTR (offset:0x0290,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:0	R/W	RX_BASE_PTR0	Point to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address	0

RX_MAX_CNT (offset:0x0294,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11:0	R/W	RX_MAX_CNT0	The maximum number of RXD count in RXD Ring #0.	0

RX_CALC_IDX (offset:0x0298,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11:0	R/W	RX_CALC_IDX0	Point to the next RXD CPU wants to allocate to RXD Ring #0.	0

FS _DRX_IDX (offset:0x029C,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11:0	R/W	RX_DRX_IDX0	Point to the next RXD DMA wants to use in FDS Ring#0. It should be a 4-DWORD aligned address.	0

USB_DMA_CFG (offset:0x02A0,default :0x00000000)

Bits	Type	Name	Description	Init Value
31	R	TX_BUSY	USB DMA TX FSM busy	0
30	R	RX_BUSY	USB DMA RX FSM busy	0
29:24	R	EPOUT_VLD	OUT endpoint data valid	0
23	R/W	UDMA_TX_EN	USB DMA TX enable	0
22	R/W	UDMA_RX_EN	USB DMA RX enable	0
21	R/W	RX_AGG_EN	RX bulk aggregation enable	0
20	R/W	TXOP_HALT	Halt TXOP count down when TX buffer is full. 0: disable 1: enable	0
19	R/W	TX_CLEAR	Clear USB DMA TX path	0
18:17			Reserved	
16	R/W	PHY_WD_EN	USB PHY watch-dog enable	0
15:8	RW	RX_AGG_LMT	RX bulk aggregation limit. Unit is 1024 bytes	00
7:0	RW	RX_AGG_TO	RX bulk aggregation time-out count. Unit is 1us	00

US_CYC_CNT (offset:0x02A4,default :0x00F00021)

Bits	Type	Name	Description	Init Value
31:25			Reserved	
24	R/W	TEST_EN	Test mode enable	0
23:16	R/W	TEST_SEL	Test mode selection	8'hf0
15:9			Reserved	
8	R/W	BT_MODE_EN	Blue-tooth mode enable	0
7:0	RW	US_CYC_CNT	Clock cycle count in 1us. It's dependent on the interface clock rate. For PCI 33, set 8'h21. For PCI express, set 8'h7D. For USB, set 8'h1E.	8'h21

3.2 PBF registers

SYS_CTRL (offset: 0x0400,default :0x00002000)

Bits	Type	Name	Description	Init Value
31:18			Reserved	
17	R/W	PBF_MSEL	Packet buffer memory access selection. 0: address 0x8000 – 0xFFFF mapping to lower 32kB of packet buffer. 1: address 0x8000 – 0xBFFF mapping to higher 16kB of packet buffer.	0
16	R/W	HST_PM_SEL	Host program ram write selection. This bit is only for PCI/PCIe mode.	0
15			Reserved	
14	R/W	CAP_MODE	Packet buffer capture mode. 0: packet buffer in normal mode. 1: packet buffer in BBP capture mode.	0
13	R/W	PME_OEN	PCI and PCIE mode: PCI PME OEN USB mode: 1: force TR_PE=0, RF_PE = 0. 0: normal function.	1
12	R/W	CLKSELECT	MAC/PBF clock source selection. 0: from PLL 1: from 40MHz clock input	0
11	R/W	PBF_CLKEN	PBF clock enable.	0
10	R/W	MAC_CLK_EN	MAC clock enable.	0
9	R/W	DMA_CLK_EN	DMA clock enable.	0
8			Reserved	
7	R/W	MCU_READY	MCU ready. 8051 writes '1' to this bit to inform host internal MCU is ready.	0
6:5			Reserved	
4	R/W	ASY_RESET	ASYNC interface reset. Write '1' to put ASYNC into reset state.	0
3	R/W	PBF_RESET	PBF hardware reset. Write '1' to put PBF into reset state.	0
2	R/W	MAC_RESET	MAC hardware reset. Write '1' to put MAC into reset state.	0
1	R/W	DMA_RESET	DMA hardware reset. Write '1' to put DMA into reset state.	0
0	W1C	MCU_RESET	MCU hardware reset. This bit will be auto-cleared after several clock cycles.	0

HOST_CMD (offset: 0x0404,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:0	R/W	HST_CMD	Host command code. Host write this register will trigger interrupt to 8051.	0

PBF_CFG (offset: 0x0408,default : 0x07F40016)

Bits	Type	Name	Description	Init Value
31:27			Reserved	
26:24	R/W	NULL2_SEL	NULL2 frame buffer selection (reuse beacon buffer).	3'h7

			0: use beacon #0 buffer (address set by 0x42C[7:0]) 1: use beacon #1 buffer (address set by 0x42C[15:8]) 2: use beacon #2 buffer (address set by 0x42C[23:16]) 3: use beacon #3 buffer (address set by 0x42C[31:24]) 4: use beacon #4 buffer (address set by 0x430[7:0]) 5: use beacon #5 buffer (address set by 0x430[15:8]) 6: use beacon #6 buffer (address set by 0x430[23:16]) 7: use beacon #7 buffer (address set by 0x430[31:24])	
23:21	R/W	TX1Q_NUM	Queue depth of Tx1Q. The maximum number is 7.	3'h7
20:16	R/W	TX2Q_NUM	Queue depth of Tx2Q. The maximum number is 20.	5'h14
15	R/W	NULL0_MODE	NULL0 frame auto mode. In this mode, all TXQ2 will be enabled NULL0 frame transmitted. 0: disable 1: enable	0
14	R/W	NULL1_MODE	NULL1 frame auto mode. In this mode, all TXQ (0/1/2) will be disabled after NULL1 frame transmitted. 0: disable 1: enable	0
13	R/W	RX_DROP_MODE	Rx drop mode. When set, PBF will drop Rx packet before into DMA. 0: normal mode 1: drop mode	0
12	R/W	TX0Q_MODE	Tx0Q operation mode. 0: auto mode 1: manual mode	0
11	R/W	TX1Q_MODE	Tx1Q operation mode. 0: auto mode 1: manual mode	0
10	R/W	TX2Q_MODE	Tx2Q operation mode. 0: auto mode 1: manual mode	0
9	R/W	RX0Q_MODE	Rx0Q operation mode. 0: auto mode 1: manual mode	0
8	R/W	HCCA_MODE	HCCA auto mode. In this mode, TXQ1 will be enabled when CF-POLL arriving. 0: disable 1: enable	0
7:5			Reserved	
4	R/W	TX0Q_EN	Tx0Q enable	1
3	R/W	TX1Q_EN	Tx1Q enable	0
2	R/W	TX2Q_EN	Tx2Q enable	1
1	R/W	RX0Q_EN	Rx0Q enable	1
0			Reserved	

MAX_PCNT (offset: 0x040C,default :0x1F3F9F9F)

Bits	Type	Name	Description	Init Value
31:24	R/W	MAX_TX0Q_PCNT	Maximum buffer page count of Tx0Q.	8'h1f
23:16	R/W	MAX_TX1Q_PCNT	Maximum buffer page count of Tx1Q.	8'h3f
15:8	R/W	MAX_TX2Q_PCNT	Maximum buffer page count of Tx2Q.	8'h9f
7:0	R/W	MAX_RX0Q_PCNT	Maximum buffer page count of Rx0Q.	8'h9f

BUF_CTRL (offset:0x0410,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11	W1C	WRITE_TX0Q	Manual write Tx0Q.	0
10	W1C	WRITE_TX1Q	Manual write Tx1Q.	0
9	W1C	WRITE_TX2Q	Manual write Tx2Q	0
8	W1C	WRITE_RX0Q	Manual write Rx0Q	0
7	W1C	NULL0_KICK	Kick out NULL0 frame. This bit will be cleared after NULL0 frame is transmitted.	0
6	W1C	NULL1_KICK	Kick out NULL1 frame. This bit will be cleared after NULL1 frame is transmitted.	0

5	W1C	BUF_RESET	Buffer reset.	0
4	W1C	NULL2_KICK	Kick out NULL2 frame. This bit will be cleared after NULL1 frame is transmitted.	0
3	W1C	READ_TX0Q	Manual read Tx0Q.	0
2	W1C	READ_TX1Q	Manual read Tx1Q.	0
1	W1C	READ_TX2Q	Manual read Tx2Q	0
0	W1C	READ_RX0Q	Manual read Rx0Q	0

MCU_INT_STA (offset:0x0414,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:28			Reserved	
27	R/W	MAC_INT_11	MAC interrupt 11: Reserved	0
26	R/W	MAC_INT_10	MAC interrupt 10: Reserved	0
25	R/W	MAC_INT_9	MAC interrupt 9: Reserved	0
24	R/W	MAC_INT_8	MAC interrupt 8: RX QoS CF-Poll interrupt	0
23	R/W	MAC_INT_7	MAC interrupt 7: TXOP early termination interrupt	0
22	R/W	MAC_INT_6	MAC interrupt 6: TXOP early timeout interrupt	0
21	R/W	MAC_INT_5	MAC interrupt 5: Reserved	0
20	R/W	MAC_INT_4	MAC interrupt 4: GP timer interrupt	0
19	R/W	MAC_INT_3	MAC interrupt 3: Auto wakeup interrupt	0
18	R/W	MAC_INT_2	MAC interrupt 2: TX status interrupt	0
17	R/W	MAC_INT_1	MAC interrupt 1: Pre-TBTT interrupt	0
16	R/W	MAC_INT_0	MAC interrupt 0: TBTT interrupt	0
15:13			Reserved	
12	R/W	N2TX_INT	NULL2 frame Tx complete interrupt.	0
11	R/W	DTX0_INT	DMA to TX0Q frame transfer complete interrupt.	0
10	R/W	DTX1_INT	DMA to TX1Q frame transfer complete interrupt.	0
9	R/W	DTX2_INT	DMA to TX2Q frame transfer complete interrupt.	0
8	R/W	DRX0_INT	RX0Q to DMA frame transfer complete interrupt.	0
7	R/W	HCMD_INT	Host command interrupt.	0
6	R/W	N0TX_INT	NULL0 frame Tx complete interrupt.	0
5	R/W	N1TX_INT	NULL1 frame Tx complete interrupt.	0
4	R/W	BCNTX_INT	Beacon frame Tx complete interrupt.	0
3	R/W	MTX0_INT	TX0Q to MAC frame transfer complete interrupt.	0
2	R/W	MTX1_INT	TX1Q to MAC frame transfer complete interrupt.	0
1	R/W	MTX2_INT	TX2Q to MAC frame transfer complete interrupt.	0
0	R/W	MRX0_INT	MAC to RX0Q frame transfer complete interrupt.	0

***This register is only for 8051**

MCU_INT_ENA (offset:0x0418,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:28			Reserved	
27	R/W	MAC_INT11_EN	MAC interrupt 11 enable	0
26	R/W	MAC_INT10_EN	MAC interrupt 10 enable	0
25	R/W	MAC_INT9_EN	MAC interrupt 9 enable	0
24	R/W	MAC_INT8_EN	MAC interrupt 8 enable	0
23	R/W	MAC_INT7_EN	MAC interrupt 7 enable	0
22	R/W	MAC_INT6_EN	MAC interrupt 6 enable	0
21	R/W	MAC_INT5_EN	MAC interrupt 5 enable	0
20	R/W	MAC_INT4_EN	MAC interrupt 4 enable	0
19	R/W	MAC_INT3_EN	MAC interrupt 3 enable	0
18	R/W	MAC_INT2_EN	MAC interrupt 2 enable	0
17	R/W	MAC_INT1_EN	MAC interrupt 1 enable	0
16	R/W	MAC_INT0_EN	MAC interrupt 0 enable	0
15:13			Reserved	

12	R/W	N2TX_INT_EN	NULL2 frame Tx complete interrupt enable.	0
11	R/W	DTX0_INT_EN	DMA to TX0Q frame transfer complete interrupt enable.	0
10	R/W	DTX1_INT_EN	DMA to TX1Q frame transfer complete interrupt enable.	0
9	R/W	DTX2_INT_EN	DMA to TX2Q frame transfer complete interrupt enable.	0
8	R/W	DRX0_INT_EN	RX0Q to DMA frame transfer complete interrupt enable.	0
7	R/W	HCMD_INT_EN	Host command interrupt enable.	0
6	R/W	N0TX_INT_EN	NULL0 frame Tx complete interrupt enable.	0
5	R/W	N1TX_INT_EN	NULL1 frame Tx complete interrupt enable.	0
4	R/W	BCNTX_INT_EN	Beacon frame Tx complete interrupt enable.	0
3	R/W	MTX0_INT_EN	TX0Q to MAC frame transfer complete interrupt enable.	0
2	R/W	MTX1_INT_EN	TX1Q to MAC frame transfer complete interrupt enable.	0
1	R/W	MTX2_INT_EN	TX2Q to MAC frame transfer complete interrupt enable.	0
0	R/W	MRX0_INT_EN	MAC to RX0Q frame transfer complete interrupt enable.	0

***This register is only for 8051**

TX0Q_IO (offset: 0x041C,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:0	R/W	TX0Q_IO	TX0Q IO port. This register is used in manual mode.	0

TX1Q_IO (offset: 0x0420,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:0	R/W	TX1Q_IO	TX1Q IO port. This register is used in manual mode.	0

TX2Q_IO (offset: 0x0424,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:0	R/W	TX2Q_IO	TX2Q IO port. This register is used in manual mode.	0

RX0Q_IO (offset: 0x0428,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:0	R/W	RX0Q_IO	RX0Q IO port. This register is used in manual mode.	0

BCN_OFFSET0 (offset: 0x042C,default :0xECE8E4E0)

Bits	Type	Name	Description	Init Value
31:24	R/W	BCN3_OFFSET	Beacon #3 address offset in shared memory. Unit is 64 byte.	8'hec
23:16	R/W	BCN2_OFFSET	Beacon #2 address offset in shared memory. Unit is 64 byte.	8'he8
15:8	R/W	BCN1_OFFSET	Beacon #1 address offset in shared memory. Unit is 64 byte.	8'he4
7:0	R/W	BCN0_OFFSET	Beacon #0 address offset in shared memory. Unit is 64 byte.	8'he0

BCN_OFFSET1 (offset: 0x0430,default :0xFCF8F4F0)

Bits	Type	Name	Description	Init Value
31:24	R/W	BCN7_OFFSET	Beacon #7 address offset in shared memory. Unit is 64 byte.	8'hfc
23:16	R/W	BCN6_OFFSET	Beacon #6 address offset in shared memory. Unit is 64 byte.	8'hf8
15:8	R/W	BCN5_OFFSET	Beacon #5 address offset in shared memory. Unit is 64 byte.	8'hf4
7:0	R/W	BCN4_OFFSET	Beacon #4 address offset in shared memory. Unit is 64 byte.	8'hf0

TXRXQ_STA (offset: 0x0434,default :0x22020202)

Bits	Type	Name	Description	Init Value
31:24	RO	RX0Q_STA	RxQ status	8'h22
23:16	RO	TX2Q_STA	Tx2Q status	8'h02
15:8	RO	TX1Q_STA	Tx1Q status	8'h02
7:0	RO	TX0Q_STA	Tx0Q status	8'h02

TXRXQ_PCNT (offset: 0x0438,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:24	RO	RX0Q_PCNT	Page count in RxQ	8'h00
23:16	RO	TX2Q_PCNT	Page count in Tx2Q	8'h00

15:8	RO	TX1Q_PCNT	Page count in Tx1Q	8'h00
7:0	RO	TX0Q_PCNT	Page count in Tx0Q	8'h00

PBF_DBG (offset: 0x043C,default :0x00000FE)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	RO	FREE_PCNT	Free page count	8'hFE

CAP_CTRL (offset: 0x0440,default :0x01400000)

Bits	Type	Name	Description	Init Value
31	R/W	CAP_ADC_FEQ	Data source. 0: data from the ADC output 1: Data from the FEQ output	0
30	WC	CAP_START	Data capture start 0: No action 1: Start data capture (cleared automatically after capture finished)	0
29	W1C	MAN_TRIG	Manual capture trigger	0
28:16	R/W	TRIG_OFFSET	Starting address offset before trigger point.	13'h140
15:13			Reserved	
12:0	RO	START_ADDR	Starting address of captured data.	13'h000

3.3 TEST registers

RF_CSR_CFG (offset: 0x0500, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:18	R		Reserved	0
17	R/W1	RF_CSR_KICK	Write – kick RF register read/write 0: do nothing 1: kick read/write process Read – Polling RF register read/write 0: idle 1: busy	0
16	R/W	RF_CSR_WR	0: read 1: write	0
15:13	R		Reserved	0
12:8	R/W	TESTCSR_RFACC_REGNUM	RF register ID 0 for R0, 1 for R1 and so on.	0
7:0	R/W	RF_CSR_DATA	Write – DATA written to RF Read – DATA read from RF	0

RF_SETTING (offset: 0x0504, default: 0x0000_0005)

Bits	Type	Name	Description	Init Value
31	R		Reserved	0
30:29	R/W	TESTCSR_RF_LNA1	RF_LNA1 value in test mode	0
28:24	R/W	TESTCSR_RF_VGA1	RF_VGA1 value in test mode	0
23	R		Reserved	0
22:21	R/W	TESTCSR_RF_LNA0	RF_LNA0 value in test mode	0
20:16	R/W	TESTCSR_RF_VGA0	RF_VGA0 value in test mode	0
15:14	R		Reserved	0
13	R/W	TESTCSR_RF_PA_PE_A1	RF_PA_PE_A1 value in test mode	0
12	R/W	TESTCSR_RF_PA_PE_A0	RF_PA_PE_A0 value in test mode	0
11	R/W	TESTCSR_RF_PA_PE_G1	RF_PA_PE_G1 value in test mode	0
10	R/W	TESTCSR_RF_DC_CAL_EN1	RF_DC_CAL_EN1 value in test mode	0
9	R/W	TESTCSR_RF_PA_PE_G0	RF_PA_PE_G0 value in test mode	0
8	R/W	TESTCSR_RF_DC_CAL_EN0	RF_DC_CAL_EN0 value in test mode	0
7:3	R		Reserved	0
2	R/W	TESTCSR_RF_LDO123_PE	LDO123_PE value in test mode	1
1	R/W	TESTCSR_RF_TR	RF_TR value in test mode	0
0	R/W	TESTCSR_RF_PE	RF_PE value in test mode	1

RF_TEST_CONTROL (offset: 0x0508, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:2	R		Reserved	0
1	R/W	TSSI0PSI1	0: ADC5 is used for TSSI 1: ADC5 is used for PSI	0
0	R/W	BYPASS_RF	When set, RF control signals come from RF_SETTING instead of MAC/BBP in normal operation mode	0

PTN_CTRL (offset: 0x0540, default: 0x0808_1000)

Bits	Type	Name	Description	Init Value
31:28	R		Reserved	0
27	R/W	PTN_LPBK_SEL_RX0	PTN loop back path via RX0	1
26:25	R/W	PTN_MODE	PTN mode selection: 0: RAMP 1: SINE 2: MEM_I 3:MEM_Q	0
24	R/W	PTN_ACCESS_MEM (PTN_KICK)	Indicate PTN is accessing MEM When write this bit, it will kick-off PTN run.	0
23:20	R/W	LATENCY	LATENCY of updated time of RAMP data. The unit is 32 times of clock cycle.	0
19	R/W	AUTO_ADJUST	When Running SINE mode, if turn on this bit then it will use former trained value in RAMP MODE.	1
18:16	R/W	EXT_ADJUST_SCALE	When disable above bit (auto_adjust = 0), then it will use this value for normalization. (The full scale is 15, the mapping relationship is: 0: 8 1:9 2:10 3:11 4:12 5:13 6:14 7:15	0
15:14	R		Reserved	0
13:0	R/W	RD_START_ADDRESS	The start address of read when taking data from PBF memory in MEM mode.	14'h1000

PTN_WRITE_ADDRESS (offset: 0x0544, default: 0x03ff_0000)

Bits	Type	Name	Description	Init Value
31:30	R		Reserved	0
29:16	R/W	WR_END_ADDRESS	The end address of write when storing data to PBF memory in MEM mode.	14'h03ff
15:14	R		Reserved	0
13:0	R/W	WR_START_ADDRESS	The start address of write when storing data to PBF memory in MEM mode.	0

PTN_DETECTED_MIN_THRESHOLD_I (offset: 0x0548, default: 0x00FF_03FF)

Bits	Type	Name	Description	Init Value
31:24	R		Reserved	0
23:16	R	ADC_MIN_VALUE_I	The minimum output value of ADC I-channel.	8'hff
15:10	R		Reserved	0
9:0	R	DAC_MIN_LEVEL_I	The corresponding input value of DAC I-channel.	10'h3ff

PTN_DETECTED_MAX_THRESHOLD_I (offset: 0x054c, default: 0x00FF_03FF)

Bits	Type	Name	Description	Init Value
31:24	R		Reserved	0
23:16	R	ADC_MAX_VALUE_I	The maximum output value of ADC I-channel.	0
15:10	R		Reserved	0
9:0	R	DAC_MAX_LEVEL_I	The corresponding input value of DAC I-channel.	0

PTN_DETECTED_MIN_THRESHOLD_Q (offset: 0x0550, default: 0x00FF_03FF)

Bits	Type	Name	Description	Init Value
31:24	R		Reserved	0
23:16	R	ADC_MIN_VALUE_Q	The minimum output value of ADC Qchannel.	8'hff
15:10	R		Reserved	0
9:0	R	DAC_MIN_LEVEL_Q	The corresponding input value of DAC Q-channel.	10'h3ff

PTN_DETECTED_MAX_THRESHOLD_Q (offset: 0x0554, default: 0x00FF_03FF)

Bits	Type	Name	Description	Init Value
31:24	R		Reserved	0
23:16	R	ADC_MAX_VALUE_Q	The maximum output value of ADC Q-channel.	0
15:10	R		Reserved	0
9:0	R	DAC_MAX_LEVEL_Q	The corresponding input value of DAC Q-channel.	0

EFUSE_CTRL (offset: 0x0580, default: 0000_8800)

Bits	Type	Name	Description	Init Value
31	R	SEL_EFUSE	Currently used NVM(Non-Volatile Memory) 0: external EEPROM 1: internal effuse PROM	0
30	R/W1	EFSROM_KICK	Write it – kick off efuse read/write. 0: idle 1: start read/write Read it – busy bit to efuse read/write 0: read/write done 1: busy	0
29:26	R		Reserved	0
25:16	R/W	EFSROM_AIN	Address to be read from/written to efuse PROM. The address must be 16-byte alignment. (This is to say, the last 4 bits must be 0)	0
15:14	R/W	EFSROM_LDO_ON_TIME	LDO read time (in 128us)	0x2
13:8	R/W	EFSROM_LDO_OFF_TIME	LDO discharge time (in 128us)	0x8
7:6	R/W	EFSROM_MODE	e-fuse PROM access mode: 11: Write in physical view 10: reserved 01: Read in physical view 00: Read in logical view	0
5:0	R	EFSROM_AOUT	Corresponding usage map entity number to the data read back in logical view	0

RFUSE_DATA3 (offset: 0x0590, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	EFSROM_DATA3	For write: data to be written to efuse PROM For read: data read back from efuse PROM	0

RFUSE_DATA2 (offset: 0x0594, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	EFSROM_DATA2	For write: data to be written to efuse PROM For read: data read back from efuse PROM	0

RFUSE_DATA1 (offset: 0x0598, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	EFSROM_DATA1	For write: data to be written to efuse PROM For read: data read back from efuse PROM	0

RFUSE_DATA0 (offset: 0x059c, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	EFSROM_DATA0	For write: data to be written to efuse PROM For read: data read back from efuse PROM	0

OSC_CTRL (offset: 0x05a4, default: 0x0003_ff11)

Bits	Type	Name	Description	Init Value
31:29	R		Reserved	0
28:8	R/W	OSC_DIV	Used to divide ring clock to get wanted OSC clock.	3ff
7:5	R		Reserved	0
4	R/W	OSC_EN	Enable OSC clock generation	0
3	R/W	OSC_CAL_EN	Enable OSC clock calibration	0
2:0	R/W	OSC_RATE_SEL	OSC clock rate selection. 000: 1d16M 001: 1d32M	1

			010: 1d64M 011: 1d128M 100: 1d256M 101: 1d512M 110: 1d1024M 111: 1d2048M	

OSC_CAL_OUT (offset: 0x05a8, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:21	R	Reserved		0
20:0	R	OSC_CAL_OUT	Oscillator calibration result	0

BIST_0 (offset: 0x05C0, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31	W1	BBP_BIST_START	Write 1 to start BBP BIST, write 0 do nothing	0
30	W1	MAC_BIST_START	Write 1 to start MAC BIST, write 0 do nothing	0
29	W1	USBPHYBIST_BIST_START	Write 1 to start USBPHY BIST, write 0 do nothing	0
28	W	USB_BIST_SPEED_W	USB BIST select high speed mode 0: full speed 1: high speed	0
27	R	P_DATAQ_BIST_FAIL	PCIE endpoint P_DATAQ bist fail	0
26	R	Q_HDRQ_BIST_FAIL	PCIE endpoint Q_HDRQ bist fail	0
25	R	RETRYRAM_BIST_FAIL	PCIE endpoint RETRYRAM bist fail	0
24	R	RETRYSOTRAM_BIST_FAIL	PCIE endpoint RETRYSOTRAM bist fail	0
23	R	BIST_FAIL_ROM	8051 ROM bist fail	0
22:16	R	BIST_EFSROM_FAIL	Efuse ROM bist fail	0
15	R	BIST_PBF_FAIL	PBF buffer bist fail	0
14	R	BIST_SMEM_FAIL	PBF shared memory bist fail	0
13:12	R	BIST_SEC_FAIL	SEC bist fail	0
11:8	R	NMAC_BIST_FAIL	NMAC bist fail	0
7	R	BIST_FAIL_DM	8051 DM bist fail	0
6	R	BIST_FAIL_M0	USB M0 bist fail	0
5	R	BIST_FAIL_M1	USB M1 bist fail	0
4	R	BIST_FAIL_PM	8051 program memory bist fail	0
3	R	BIST_RX_FAIL	Asynchronous interface RX bist fail	0
2	R	BIST_TX_FAIL	Asynchronous interface TX bist fail	0
1	R	ANY_OTHER_FAIL	ANY bist fail	0
0	R	BIST_DONE	Whole bist finish	0

BIST_1 (offset: 0x05C4 default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:19	R		Reserved	0
18	R	USB _BIST_SPEED_R	USB BIST select high speed mode 0: full speed 1: high speed	0
17	R	BIST_USB_PHY_FINISH	USB PHY bist finish	0
16	R	BIST_USB_PHY_FAIL	USB_PHY bist finish	0
15:8	R	BB_PMDO1	BBP PMDO1	0
7:0	R	BB_PMDO	BBP PMDO0	0

INTERNAL_1 (offset: 0x05C8 default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	INTERNAL_1	Reserved for future usage	0

INTERNAL_2 (offset: 0x05CC default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	INTERNAL_2	Reserved for future usage	0

BBP_CFG (offset: 0x05D0 default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:21	R		Reserved	0
20	R/W	BBP_PLL_PD	PLL_PD value in test mode	0
19	R/W	BBP_IDDQ_PD	IDDQ_PD value in test mode	0
18	R/W	BBP_TEST_ADCDAC	TEST_ADCDAC value in test mode	0
17	R/W	BBP_ADC5_ON	ADC5_ON value in test mode	0
16	R/W	BBP_PLLBYPASS	PLLBYPASS value in test mode	0
15:10	R		Reserved	0
9:0	R/W	BBP_PMDI	BBP_PMDI value in test mode	0

LDO_CFG0 (offset: 0x05D4 default: 0x0104_0f14)

Bits	Type	Name	Description	Init Value
31	R/W	LDO25_LARGEA	LDO25_LARGEA value in test mode	0
30:29	R/W	LDO25_LEVEL	LDO25_LEVEL value in test mode	0
28:26	R/W	LDO_CORE_VLEVEL	LDO_CORE_VLEVEL value in test mode	0
25:24	R/W	BGSEL	BGSEL value in test mode	1
23:16	R/W	DELAY1	Latency from usb suspend to pll_pd=1 (in 0.4us)	4
15:8	R/W	DELAY2	Latency from usb suspend to ldo_pd=0 (in 0.4us)	15
7:0	R/W	DELAY3	Latency from usb suspend to ldo_core_pd=1 (in 0.4us)	20

LDO_CFG1 (offset: 0x05D8 default: 0x0032_0037)

Bits	Type	Name	Description	Init Value
31:28	R		RESERVED	0
27:16	R/W	DELAY4	Latency from usb resume to ldo_pd=1 (in 0.4us)	50
15:12	R		RESERVED	0
11:0	R/W	DELAY5	Latency from usb resume to pll_pd=0 (in 0.4us)	55

GPIO_SWITCH (offset: 0x05DC default: 0x0000_00FF)

Bits	Type	Name	Description	Init Value
31:8	R		RESERVED	0
7:0	R/W	GPIO_SWTCH	When turn on these bit, it will enable GPIO function.	0xff

BBP_UTIF_CTRL (offset: 0x05E0 default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31	R/W	BBP_UTIF_EN	UTIF enable	0
30:24	R/W	BBP_UTIF_SEL	UTIF test item selection: 0: BBP memory BIST 1: ADC0 test 2: ADC1 test 3: reserved for ADC2 test 4: BBP TX0 5: Optional BBP memory BIST 6: ADCDAC standby & iddq_pd 8: CCK state 9: TSSI ADC test 10: BBP TX1 11: RX function test 14: PLL output test 15: BBP Debug	0x0
23:0	R/W	BBP_UTIF_IN	RESERVED	0

BBP_UTIF_DATA (offset: 0x05E4 default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:25	R		RESERVED	0
24	R	BBP_UTIF_WIDTH	Output data bus width (default is narrow bus) 0: 16bit width 1: 24bit width	0x0
23:0	R	BBP_UTIF_OUT	Output data	0

3.4 MAC registers

MAC System configuration registers (offset:0x1000)

Reserved (offset:0x1000, default :0x3572_0210)

Bits	Type	Name	Description	Initial value
31:0	R	-	Reserved	16'h3572

MAC_SYS_CTRL (offset:0x1004, default :0x0000_0003)

Bits	Type	Name	Description	Initial value
31:15	R		Reserved	0
14:12	R/W	WLAN_ACT_MASK	Bit12: TX is reported as WLAN active Bit13: RX is reported as WLAN active Bit14: SIFS is reported as WLAN active 0: disable 1: enable	0
11:8	R/W	BT_HALT_WLAN_EN	Bit 8: BT will halt WLAN when {LNA_PE_G1, GPIO0}=2'b00 Bit 9: BT will halt WLAN when {LNA_PE_G1, GPIO0}=2'b01 Bit 10: BT will halt WLAN when {LNA_PE_G1, GPIO0}=2'b10 Bit 11: BT will halt WLAN when {LNA_PE_G1, GPIO0}=2'b11 0: disable 1: enable	0
7	R/W	RX_TS_EN	Write 32-bit hardware RX timestamp instead of (RXWI->RSSI), and write (RXWI->RSSI) instead of (RXWI->SNR). Note: For QA RX sniffer mode only. 1: enable 0: disable	0
6	R/W	WLAN_HALT_EN	Enable external WLAN halt control signal 1: enable 0: disable	0
5	R/W	PBF_LOOP_EN	Packet buffer loop back enable (TX->RX) 1: enable 0: disable	0
4	R/W	CONT_TX_TEST	Continuous TX production test; override MAC_RX_EN, MAC_TX_EN 1: enable 0: disable	0
3	R/W	MAC_RX_EN	MAC RX enable 1: enable 0: disable	0
2	R/W	MAC_TX_EN	MAC TX enable 1: enable 0: disable	0
1	R/W	BBP_HRST	BBP hard-reset 1: BBP in reset state 0: BBP in normal state Note: Whole BBP including BBP registers will be reset.	1
0	R/W	MAC_SRST	MAC soft-reset 1: MAC in reset state 0: MAC in normal state Note: MAC registers and tables will NOT be reset.	1

Note: MAC hard-reset is outside the scope of MAC registers.

MAC_ADDR_DW0 (offset:0x1008, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	MAC_ADDR_3	MAC address byte3	0
23:16	R/W	MAC_ADDR_2	MAC address byte2	0
15:8	R/W	MAC_ADDR_1	MAC address byte1	0
7:0	R/W	MAC_ADDR_0	MAC address byte0	0

MAC_ADDR_DW1 (offset:0x100C, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	MAC_ADDR_5	MAC address byte5	0
7:0	R/W	MAC_ADDR_4	MAC address byte4	0

Note: Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

MAC_BSSID_DW0 (offset:0x1010, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	BSSID_3	BSSID byte3	0
23:16	R/W	BSSID_2	BSSID byte2	0
15:8	R/W	BSSID_1	BSSID byte1	0
7:0	R/W	BSSID_0	BSSID byte0	0

MAC_BSSID_DW1 (offset: 0x1014, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:21	R		Reserved	0
20:18	R/W	MULTI_BCN_NUM	Multiple BSSID Beacon number 0: one back-off beacon 1-7: SIFS-burst beacon count	0
17:16	R/W	MULTI_BSSID_MODE	Multiple BSSID mode In multiple-BSSID AP mode, BSSID shall be the same as MAC_ADDR, that is, this device owns multiple MAC_ADDR in this mode. The multiple MAC_ADDR/BSSID are distinguished by [bit2: bit0] of byte5. 0: 1-BSSID mode (BSS index = 0) 1: 2-BSSID mode (byte5.bit0 as BSS index) 2: 4-BSSID mode (byte5.bit1:0 as BSS index) 3: 8-BSSID mode (byte5.bit2:0 as BSS index)	0
15:8	R/W	BSSID_5	BSSID byte5	0
7:0	R/W	BSSID_4	BSSID byte4	0

MAX_LEN_CFG (offset: 0x1018, default: 0x000A_0FFF)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	MIN_MPDU_LEN	Minimum MPDU length (unit: bytes) MAC will drop the MPDU if the length is less than this limitation. Applied only in MAC RX.	10
15:14	R		Reserved	0
13:12	R/W	MAX_PSDU_LEN	Maximum PSDU length (power factor) 0: 2^13 = 8K bytes 1: 2^14 = 16K bytes 2: 2^15 = 32K bytes 3: 2^16 = 64K bytes MAC will NOT generate A-MPDU with length greater than this limitation. Applied only in MAC TX.	0
11:0	R/W	MAX_MPDU_LEN	Maximum MPDU length (unit: bytes) MAC will drop the MPDU if the length is greater than this limitation. Applied only in MAC RX.	4095

BBP_CSR_CFG (offset: 0x101C, default: 0x0008_0000)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19	R/W	BBP_RW_MODE	BBP Register R/W mode 1: parallel mode 0: serial mode	1
18	R/W	BBP_PAR_DUR	BBP Register parallel R/W pulse width 0: pulse width = 62.5ns	0

			1: pulse width = 112.5ns Note: Please set BBP_PAR_DUR=1 in 802.11J mode	
17	R/W	BBP_CSR_KICK	Write - kick BBP register read/write 0: do nothing 1: kick read/write process Read - Polling BBP register read/write progress 0: idle 1: busy	0
16	R/W	BBP_CSR_RW	0: Write 1: Read	0
15:8	R/W	BBP_ADDR	BBP register ID 0 for R0, 1 for R1, and so on.	0
7:0	R/W	BBP_DATA	Write - Data written to BBP Read - Data read from BBP	0

RF_CSR_CFG0 (offset: 0x1020, default: 0x1600_0000)

Bits	Type	Name	Description	Initial value
31	R/W	RF_REG_CTRL	Write: 1 - RF_REG0/1/2 to RF chip Read: 0 – idle, 1 - busy	0
30	R/W	RF_LE_SEL	RF_LE selection 0:RF_LE0 activate 1:RF_LE1 activate	0
29	R/W	RF_LE_STBY	RF_LE standby mode 0: RF_LE is high when standby 1: RF_LE is low when standby	0
28:24	R/W	RF_REG_WIDTH	RF register bit width	22
23:0	R/W	RF_REG_0	RF register0 ID and content	0

RF_CSR_CFG1 (offset: 0x1024, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:25	R		Reserved	0
24	R/W	RF_DUR	Gap between BB_CONTROL_RF and RF_LE 0: 3 system clock cycle (37.5usec) 1: 5 system clock cycle (62.5usec)	0
23:0	R/W	RF_REG_1	RF register1 ID and content	0

RF_CSR_CFG2 (offset: 0x1028, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23:0	R/W	RF_REG_2	RF register2 ID and content	0

Note: Software should make sure the first bit (MSB in the specified bit number) written to RF is 0 for RF chip mode selection.

LED_CFG (offset: 0x102C, default: 0x0003_1E46)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30	R/W	LED_POL	LED polarity 0: active low 1: active high	0
29:28	R/W	Y_LED_MODE	Yellow LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on	0
27:26	R		Reserved	0
25:24	R/W	R_LED_MODE	Red LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on	0
23:22	R		Reserved	0

21:16	R/W	SLOW_BLK_TIME	Slow blinking period (unit: 1sec)	3
15:8	R/W	LED_OFF_TIME	TX blinking off period (unit: 1ms)	30
7:0	R/W	LED_ON_TIME	TX blinking on period (unit: 1ms)	70

AMPDU_MAX_LEN_20M1S (offset: 0x1030, default: 0x7777_7777)

Bits	Type	Name	Description	Initial value
31:28	R/W	AMPDU_MAX_BW20_MCS7	Maximum AMPDU for BW20 MCS7*	7
27:24	R/W	AMPDU_MAX_BW20_MCS6	Maximum AMPDU for BW20 MCS6*	7
23:20	R/W	AMPDU_MAX_BW20_MCS5	Maximum AMPDU for BW20 MCS5*	7
19:16	R/W	AMPDU_MAX_BW20_MCS4	Maximum AMPDU for BW20 MCS4*	7
15:12	R/W	AMPDU_MAX_BW20_MCS3	Maximum AMPDU for BW20 MCS3*	7
11:08	R/W	AMPDU_MAX_BW20_MCS2	Maximum AMPDU for BW20 MCS2*	7
07:04	R/W	AMPDU_MAX_BW20_MCS1	Maximum AMPDU for BW20 MCS1*	7
03:00	R/W	AMPDU_MAX_BW20_MCS0	Maximum AMPDU for BW20 MCS0*	7

Note1*: **0-2:** 2K bytes, **3:** 4K bytes, **4:** 8K, **5:** 16K, **6:** 32K, **7:** 64K
Note2: The value applied together with 0x1018 MAX_PSDU_LEN.

AMPDU_MAX_LEN_20M2S (offset: 0x1034, default: 0x7777_7777)

Bits	Type	Name	Description	Initial value
31:28	R/W	AMPDU_MAX_BW20_MCS15	Maximum AMPDU for BW20 MCS15*	7
27:24	R/W	AMPDU_MAX_BW20_MCS14	Maximum AMPDU for BW20 MCS14*	7
23:20	R/W	AMPDU_MAX_BW20_MCS13	Maximum AMPDU for BW20 MCS13*	7
19:16	R/W	AMPDU_MAX_BW20_MCS12	Maximum AMPDU for BW20 MCS12*	7
15:12	R/W	AMPDU_MAX_BW20_MCS11	Maximum AMPDU for BW20 MCS11*	7
11:08	R/W	AMPDU_MAX_BW20_MCS10	Maximum AMPDU for BW20 MCS10*	7
07:04	R/W	AMPDU_MAX_BW20_MCS9	Maximum AMPDU for BW20 MCS9*	7
03:00	R/W	AMPDU_MAX_BW20_MCS8	Maximum AMPDU for BW20 MCS8*	7

Note1*: **0-2:** 2K bytes, **3:** 4K bytes, **4:** 8K, **5:** 16K, **6:** 32K, **7:** 64K
Note2: The value applied together with 0x1018 MAX_PSDU_LEN.

AMPDU_MAX_LEN_40M1S (offset: 0x1038, default: 0x7777_7777)

Bits	Type	Name	Description	Initial value
31:28	R/W	AMPDU_MAX_BW40_MCS7	Maximum AMPDU for BW40 MCS7*	7
27:24	R/W	AMPDU_MAX_BW40_MCS6	Maximum AMPDU for BW40 MCS6*	7
23:20	R/W	AMPDU_MAX_BW40_MCS5	Maximum AMPDU for BW40 MCS5*	7
19:16	R/W	AMPDU_MAX_BW40_MCS4	Maximum AMPDU for BW40 MCS4*	7
15:12	R/W	AMPDU_MAX_BW40_MCS3	Maximum AMPDU for BW40 MCS3*	7
11:08	R/W	AMPDU_MAX_BW40_MCS2	Maximum AMPDU for BW40 MCS2*	7
07:04	R/W	AMPDU_MAX_BW40_MCS1	Maximum AMPDU for BW40 MCS1*	7
03:00	R/W	AMPDU_MAX_BW40_MCS0	Maximum AMPDU for BW40 MCS0*	7

Note1*: **0-2:** 2K bytes, **3:** 4K bytes, **4:** 8K, **5:** 16K, **6:** 32K, **7:** 64K
Note2: The value applied together with 0x1018 MAX_PSDU_LEN.

AMPDU_MAX_LEN_40M2S (offset: 0x103C, default: 0x7777_7777)

Bits	Type	Name	Description	Initial value
31:28	R/W	AMPDU_MAX_BW40_MCS15	Maximum AMPDU for BW40 MCS15*	7
27:24	R/W	AMPDU_MAX_BW40_MCS14	Maximum AMPDU for BW40 MCS14*	7
23:20	R/W	AMPDU_MAX_BW40_MCS13	Maximum AMPDU for BW40 MCS13*	7
19:16	R/W	AMPDU_MAX_BW40_MCS12	Maximum AMPDU for BW40 MCS12*	7
15:12	R/W	AMPDU_MAX_BW40_MCS11	Maximum AMPDU for BW40 MCS11*	7
11:08	R/W	AMPDU_MAX_BW40_MCS10	Maximum AMPDU for BW40 MCS10*	7
07:04	R/W	AMPDU_MAX_BW40_MCS9	Maximum AMPDU for BW40 MCS9*	7
03:00	R/W	AMPDU_MAX_BW40_MCS8	Maximum AMPDU for BW40 MCS8*	7

Note1*: **0-2:** 2K bytes, **3:** 4K bytes, **4:** 8K, **5:** 16K, **6:** 32K, **7:** 64K
Note2: The value applied together with 0x1018 MAX_PSDU_LEN.

AMPDU_MAX_LEN_40M2S (offset: 0x1040, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:07	R		Reserved	0
06	R/W	FORCE_BA_WINSIZE_EN	Enable forced BA window size over BA window size value in TXWI 0: disable, 1: enable	0
05:00	R/W	FORCE_BA_WINSIZE	Forced BA window size	0

MAC Timing Control Registers (offset:0x1100)

XIFS_TIME_CFG (offset:0x1100, default :0x33A4_100A)

Bits	Type	Name	Description	Initial value
31:30	R		Reserved	
29	R/W	BB_RXEND_EN	BB_RX_END signal enable Refer BB_RX_END signal from BBP RX logic to start SIFS defer. 0: disable 1: enable	1
28:20	R/W	EIFS_TIME	EIFS time (unit: 1us) EIFS is the defer time after reception of a CRC error packet. After deferring EIFS, the normal back-off process may proceed.	314
19:16	R/W	OFDM_XIFS_TIME	Delayed OFDM SIFS time compensator (unit: 1us) When BB_RX_END from BBP is a delayed version the SIFS deferred will be (OFDM_SIFS_TIME - OFDM_XIFS_TIME)	4
15:8	R/W	OFDM_SIFS_TIME	OFDM SIFS time (unit: 1us) Applied after OFDM TX/RX.	16
7:0	R/W	CCK_SIFS_TIME	CCK SIFS time (unit: 1us) Applied after CCK TX/RX.	10

Note1: EIFS = SIFS + ACK @ 1Mbps + DIFS = 10us (SIFS) + 192us (long preamble) + 14*8us (ACK) + 50us (DIFS) = 364. However, MAC should start back-off procedure after (EIFS-DIFS).

Note2: EIFS is not applied if MAC is a TXOP initiator that owns the channel.

Note3: EIFS is not started if AMPDU is only partial corrupted.

Caution: It is recommended that both (CCK_SIFS_TIME) and (OFDM_SIFS_TIME) are no less than TX/RX transition time. If the SIFS value is not long enough, a SIFS burst transmission may be replaced with a PIFS burst one.

BKOFF_SLOT_CFG (offset:0x1104, default : 0x0000_0214)

Bits	Type	Name	Description	Initial value
31:12	R/W		Reserved	
11:8	R/W	CC_DELAY_TIME	Channel clear delay (unit: 1-us) This value specifies TX guard time after channel is clear.	2
7:0	R/W	SLOT_TIME	Slot time (unit: 1-us) This value specifies the slot boundary after deferring SIFS time. Note: Default 20us is for 11b/g. 11a and 11g-short-slot-mode is 9us.	20

NAV_TIME_CFG (offset:0x1108, default :0x0000_8000)

Bits	Type	Name	Description	Initial value
31	WC	NAV_UPD	NAV timer manual update command 0: Do nothing 1: Update NAV timer with NAV_UPD_VAL	0
30:16	R/W	NAV_UPD_VAL	NAV timer manual update value (unit: 1us)	0
15	R/W	NAV_CLR_EN	NAV timer auto-clear enable	1

			When enabled, MAC will auto clear NAV timer after the reception of CF-End frame from previous NAV holder STA. 0: disable 1: enable	
14:0	R	NAV_TIMER	NAV timer (unit: 1us) The timer is set by other STA and will auto countdown to zero. The STA who set the NAV timer is called the NAV holder. When NAV timer is nonzero, MAC will not send any packet.	0

CH_TIME_CFG (offset:0x110C, default: 0x0000_001E)

Bits	Type	Name	Description	Initial value
31:5	R		Reserved	0
4	R/W	EIFS_AS_CH_BUSY	Count EIFS as channel busy 0: disable 1: enable	1
3	R/W	NAV_AS_CH_BUSY	Count NAV as channel busy 0: disable 1: enable	1
2	R/W	RX_AS_CH_BUSY	Count RX busy as channel busy 0: disable 1: enable	1
1	R/W	TX_AS_CH_BUSY	Count TX busy as channel busy 0: disable 1: enable	1
0	R/W	CH_STA_TIMER_EN	Channel statistic timer enable 0: disable 1: enable	0

PBF_LIFE_TIMER (offset:0x1110, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	PBF_LIFE_TIMER	TX/RX MPDU timestamp timer (free run) Unit: 1us	0

BCN_TIME_CFG (offset:0x1114, default: 0x00000640)

Bits	Type	Name	Description	Initial value
31:24	R/W	TSF_INS_COMP	TSF insertion compensation value (unit: 1us) When inserting TSF, add this value with local TSF timer as the TX timestamp.	0
23:21	R		Reserved	0
20	R/W	BCN_TX_EN	BEACON frame TX enable When enabled, MAC sends BEACON frame at TBTT interrupt. 0: disable 1: enable	0
19	R/W	TBTT_TIMER_EN	TBTT timer enable When enabled, TBTT interrupt will be issued periodically with period specified in (BCN_INTVAL). 0: disable 1: enable	0
18:17	R/W	TSF_SYNC_MODE	Local 64-bit TSF timer synchronization mode 00: disable 01: (STA infra-structure mode) Upon the reception of BEACON frame from associated BSS, local TSF is always updated with remote TSF. 10: (STA ad-hoc mode) Upon the reception of BEACON frame from associated BSS, local TSF is updated with remote TSF only if the remote TSF is greater than local TSF. 11: (AP mode) SYNC with nobody	0
16	R/W	TSF_TIMER_EN	Local 64-bit TSF timer enable When enabled, TSF timer will re-start from zero. 0: disable 1: enable	0

15:0	R/W	BCN_INTVAL	BEACON interval (unit: 64us) This value specified the interval between Maximum beacon interval is about 4sec.	1600

TBTT_SYNC_CFG (offset:0x1118, default: 0x0042_2010)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23:20	R/W	BCN_CWMIN	Beacon transmission CWMIN after TBTT interrupt (unit: slot)	4
19:16	R/W	BCN_AIFSN	Beacon transmission AIFSN after TBTT interrupt (unit: slot)	2
15:8	R/W	BCN_EXP_WIN	Beacon expecting window duration (unit: 64us) The window starts from TBTT interrupt. The phase of "TBTT interrupt train" will NOT be adjusted by the beacon arrived within the window.	32
7:0	R/W	TBTT_ADJUST	IBSS mode TBTT phase adaptive adjustment step (unit: 1us), default value is 16us. In IBSS mode (Ad hoc), if consecutive TX beacon failures (or consecutive success) happened, TBTT timer will adjust it phase to meet the external Ad hoc TBTT time.	16

TSF_TIMER_DW0 (offset:0x111C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	TSF_TIMER_DW0	Local TSF timer LSB 32 bits (unit: 1us)	0

TSF_TIMER_DW1 (offset:0x1120, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	TSF_TIMER_DW1	Local TSF timer MSB 32 bits (unit: 1us)	0

TBTT_TIMER (offset:0x1124, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16:0	R	TBTT_TIMER	TBTT Timer (unit: 32us) The time remains till next TBTT. When TBTT_TIMER_EN is enabled, the timer will down count from BCN_INTVAL to zero. When TBTT_TIMER_EN is disabled, the timer will stay in zero.	0

INT_TIMER_CFG (offset:0x1128, default: 0x0000_0320)

Bits	Type	Name	Description	Initial value
31:16	R/W	GP_TIMER	Period of general purpose interrupt timer (Unit: 64us)	0
15:0	R/W	PRE_TBTT_TIMER	Pre-TBTT interrupt time (unit: 64us) The value specified the interrupt timing before TBTT interrupt.	0

INT_TIMER_EN (offset:0x112C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:2	R		Reserved	0
1	R/W	GP_TIMER_EN	Periodic general purpose interrupt timer enable 0: disable 1: enable	0
0	R/W	PRE_TBTT_INT_EN	Pre-TBTT interrupt enable 0: disable 1: enable	0

CH_IDLE_STA (offset:0x1130, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value

31:0	RC	CH_IDLE_TIME	Channel idle time (unit: 1us)	0

In application, the channel busy time can be derived by the equation:
CH_BUSY_TIME = host polling period – CH_IDLE_TIME

CH_BUSY_STA (offset:0x1134, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	RC	CH_BUSY_TIME	Channel busy time (unit: 1us)	0

EXT_CH_BUSY_STA (offset:0x1138, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	RC	EXT_CH_BUSY_TIME	Extension Channel busy time (unit: 1us)	0

MAC Power save configuration registers (offset:0x1200)

MAC_STATUS_REG (offset:0x1200, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:2	R		Reserved	0
1	R	RX_STATUS	RX status 0: Idle 1: Busy	0
0	R	TX_STATUS	TX status 0: Idle 1: Busy	0

PWR_PIN_CFG (offset:0x1204, default: 0x0000_000A)

Bits	Type	Name	Description	Initial value
31:4	R		Reserved	0
3	R/W	IO_ADDA_PD	AD/DA power down	1
2	R/W	IO_PLL_PD	PLL power down	0
1	R/W	IO_RA_PE	RA_PE	1
0	R/W	IO_RF_PE	RF_PE	0

AUTO_WAKEUP_CFG (offset:0x1208, default: 0x0000_0014)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15	R/W	AUTO_WAKEUP_EN	Auto wakeup interrupt enable Auto wakeup interrupt will be issued after #(SLEEP_TBTT_NUM) TBTTs' at WAKEUP_LEAD_TIME before the target TBTT. 0: disable 1: enable Note: Please make sure TBTT_TIMER_EN is enabled.	0
14:8	R/W	SLEEP_TBTT_NUM	Number of sleeping TBTT	0
7:0	R/W	WAKEUP_LEAD_TIME	Auto wakeup lead time (unit: 1TU=1024us)	20

MAC TX configuration registers (offset: 0x1300)

EDCA_AC0_CFG (BE) (offset: 0x1300, default: 0x0007_3200)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC0_CWMAX	AC0 CWMAX (unit: power of 2)	7
15:12	R/W	AC0_CWMIN	AC0 CWMIN (unit: power of 2)	3
11:8	R/W	AC0_AIFSN	AC0 AIFSN (unit: # of slot time)	2
7:0	R/W	AC0_TXOP	AC0 TXOP limit (unit: 32us)	0

EDCA_AC1_CFG (BK) (offset: 0x1304, default: 0x0007_3200)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC1_CWMAX	AC1 CWMAX (unit: power of 2)	7
15:12	R/W	AC1_CWMIN	AC1 CWMIN (unit: power of 2)	3
11:8	R/W	AC1_AIFSN	AC1 AIFSN (unit: # of slot time)	2
7:0	R/W	AC1_TXOP	AC1 TXOP limit (unit: 32us)	0

EDCA_AC2_CFG (VI) (offset: 0x1308, default: 0x0007_3200)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC2_CWMAX	AC2 CWMAX (unit: power of 2)	7
15:12	R/W	AC2_CWMIN	AC2 CWMIN (unit: power of 2)	3
11:8	R/W	AC2_AIFSN	AC2 AIFSN (unit: # of slot time)	2
7:0	R/W	AC2_TXOP	AC2 TXOP limit (unit: 32us)	0

EDCA_AC3_CFG (VO) (offset: 0x130C, default: 0x0007_3200)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC3_CWMAX	AC3 CWMAX (unit: power of 2)	7
15:12	R/W	AC3_CWMIN	AC3 CWMIN (unit: power of 2)	3
11:8	R/W	AC3_AIFSN	AC3 AIFSN (unit: # of slot time)	2
7:0	R/W	AC3_TXOP	AC3 TXOP limit (unit: 32us)	0

EDCA_TID_AC_MAP (offset: 0x1310, default: 0000_FA14)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:14	R/W	TID7_AC_MAP	AC value as TID=7	3
13:12	R/W	TID6_AC_MAP	AC value as TID=6	3
11:10	R/W	TID5_AC_MAP	AC value as TID=5	2
9:8	R/W	TID4_AC_MAP	AC value as TID=4	2
7:6	R/W	TID3_AC_MAP	AC value as TID=3	0
5:4	R/W	TID2_AC_MAP	AC value as TID=2	1
3:2	R/W	TID1_AC_MAP	AC value as TID=1	1
1:0	R/W	TID0_AC_MAP	AC value as TID=0	0

Note: default according 802.11e Table 20.23—User priority to Access Category mappings

TX_PWR_CFG_0 (offset: 0x1314, default: 0x6666_6666)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_OFDM_12	TX power for OFDM 12M/18M	0x66
23:16	R/W	TX_PWR_OFDM_6	TX power for OFDM 6M/9M	0x66
15:8	R/W	TX_PWR_CCK_5	TX power for CCK5.5M/11M	0x66
7:0	R/W	TX_PWR_CCK_1	TX power for CCK1M/2M	0x66

TX_PWR_CFG_1 (offset: 0x1318, default: 0x6666_6666)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_MCS_2	TX power for HT MCS=2,3	0x66
23:16	R/W	TX_PWR_MCS_0	TX power for HT MCS=0,1	0x66
15:8	R/W	TX_PWR_OFDM_48	TX power for OFDM 48M/54M	0x66
7:0	R/W	TX_PWR_OFDM_24	TX power for OFDM 24M/36M	0x66

TX_PWR_CFG_2 (offset: 0x131C, default: 0x6666_6666)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_MCS_10	TX power for HT MCS=10,11	0x66
23:16	R/W	TX_PWR_MCS_8	TX power for HT MCS=8,9	0x66
15:8	R/W	TX_PWR_MCS_6	TX power for HT MCS=6,7	0x66
7:0	R/W	TX_PWR_MCS_4	TX power for HT MCS=4,5	0x66

TX_PWR_CFG_3 (offset: 0x1320, default: 0x6666_6666)

Bits	Type	Name	Description	Initial value
31:16	R/W	Reserved		0x6666
15:8	R/W	TX_PWR_MCS_14	TX power for HT MCS=14,15	0x66
7:0	R/W	TX_PWR_MCS_12	TX power for HT MCS=12,13	0x66

TX_PWR_CFG_4 (offset: 0x1324, default: 0x0000_6666)

Bits	Type	Name	Description	Initial value

31:16	R	Reserved		0
15:0	R/W	Reserved		0x6666

TX_PIN_CFG (offset: 0x1328, default: 0x0005_0F0F)

Bits	Type	Name	Description	Initial value
31:20	R	Reserved		0
19	R/W	TRSW_POL	TRSW_EN polarity	0
18	R/W	TRSW_EN	TRSW_EN enable	1
17	R/W	RFTR_POL	RF_TR polarity	0
16	R/W	RFTR_EN	RF_TR enable	1
15	R/W	LNA_PE_G1_POL	LNA_PE_G1 polarity	0
14	R/W	LNA_PE_A1_POL	LNA_PE_A1 polarity	0
13	R/W	LNA_PE_G0_POL	LNA_PE_G0 polarity	0
12	R/W	LNA_PE_A0_POL	LNA_PE_A0 polarity	0
11	R/W	LNA_PE_G1_EN	LNA_PE_G1 enable	1
10	R/W	LNA_PE_A1_EN	LNA_PE_A1 enable	1
9	R/W	LNA_PE_G0_EN	LNA_PE_G0 enable	1
8	R/W	LNA_PE_A0_EN	LNA_PE_A0 enable	1
7	R/W	PA_PE_G1_POL	PA_PE_G1 polarity	0
6	R/W	PA_PE_A1_POL	PA_PE_A1 polarity	0
5	R/W	PA_PE_G0_POL	PA_PE_G0 polarity	0
4	R/W	PA_PE_A0_POL	PA_PE_A0 polarity	0
3	R/W	PA_PE_G1_EN	PA_PE_G1 enable	1
2	R/W	PA_PE_A1_EN	PA_PE_A1 enable	1
1	R/W	PA_PE_G0_EN	PA_PE_G0 enable	1
0	R/W	PA_PE_A0_EN	PA_PE_A0 enable	1

TX_BAND_CFG (offset: 0x132C, default: 0x0000_0004)

Bits	Type	Name	Description	Initial value
31:3	R	Reserved		0
2	R/W	5G_BAND_SEL_N	5G band selection PIN (complement of 5G_BAND_SEL_P)	1
1	R/W	5G_BAND_SEL_P	5G band selection PIN	0
0	R/W	TX_BAND_SEL	0: use lower 40Mhz band in 20Mhz TX 1: use upper 40Mhz band in 20Mhz TX	0

Note1: TX_BAND_SEL is effective only when TX/RX bandwidth control register R4 of BBP is set to 40Mhz.

TX_SW_CFG0 (offset: 0x1330, default: 0x0004_080C)

Bits	Type	Name	Description	Initial value
31:24	R/W	DLY_RFTR_EN	Delay of RF_TR assertion	0x0
23:16	R/W	DLY_TRSW_EN	Delay of TR_SW assertion	0x4
15:8	R/W	DLY_PAPE_EN	Delay of PA_PE assertion	0x8
7:0	R/W	DLY_TXPE_EN	Delay of TX_PE assertion	0xC

Note1: The timing unit is 0.25us.

Note2: SIFS_TIME should compensate with DLY_TXPE_EN.

TX_SW_CFG1 (offset: 0x1334, default: 0x000C_0808)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23:16	R/W	DLY_RFTR_DIS	Delay of RF_TR de-assertion	0xC
15:8	R/W	DLY_TRSW_DIS	Delay of TR_SW de-assertion	0x8
7:0	R/W	DLY_PAPE_DIS	Delay of PA_PE de-assertion	0x8

Note1: The timing unit is 0.25us.

Note2: The delay is started from TX_END event of BBP.

Note3: TX_PE is de-asserted automatically as last data byte passed to BBP.

TX_SW_CFG2 (offset: 0x1338, default: 0x000C_0408)

Bits	Type	Name	Description	Initial value

31:24	R/W	DLY_LNA_EN	Delay of LNA* assertion	0x0
23:16	R/W	DLY_LNA_DIS	Delay of LNA* de-assertion	0xC
15:8	R/W	DLY_DAC_EN	Delay of DAC_PE assertion	0x4
7:0	R/W	DLY_DAC_DIS	Delay of DAC_PE de-assertion	0x8

Note1: The timing unit is 0.25us.
Note 2: LNA* includes LNA_A0, LNA_A1, LNA_G0, LNA_G1.

TXOP_THRES_CFG (offset: 0x133C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	TXOP_REM_THRES	Remaining TXOP threshold, unit: 32us As the remaining TXOP is less than the threshold, the TXOP is passed silently.	0
23:16	R/W	CF_END_THRES	CF-END threshold, unit: 32us As the remaining TXOP is greater than the threshold, the CF-END will be send to release the remaining TXOP reserved by long NAV. Set 0xFF to disable CF_END transmission.	0
15:8	R/W	RDG_IN_THRES	RX RDG threshold, unit: 32us As the remaining TXOP (specified in the duration field of the RX frame with RDG=1) is greater than or equal to the threshold, the granted reverse direction TXOP may be used.	0
7:0	R/W	RDG_OUT_THRES	TX RDG threshold, unit: 32us As the remaining TXOP is greater than or equal to the threshold, RDG in the TX frame may be set to one.	0

TXOP_CTRL_CFG (offset: 0x1340, default: 0x0000_243F)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	EXT_CW_MIN	Cwmin for extension channel backoff When EXT_CCA_EN is enabled, 40Mhz transmission will be suppressed to 20Mhz if the extension CCA is busy or extension channel backoff is not finished. Default: Cwmin=0, disable.	0
15:8	R/W	EXT_CCA_DLY	Extension CCA signal delay time (unit: usec) Create delayed version of extension CCA signal reference time for extension channel IFS. Default: (ofdm SIFS) + (long slot time) = 16+20 = 36 (us)	36
7	R/W	EXT_CCA_EN	Extension CCA reference enable When transmit in 40Mhz mode, defer until extension CCA is also clear. 0: disable 1: enable	0
6	R/W	LSIG_TXOP_EN	L-SIG TXOP protection enable Extension of mix mode L-SIG protection range to following ACK/CTS.	0
5:0	R/W	TXOP_TRUN_EN	TXOP truncation enable Bit5: reserved Bit4: truncation for MIMO power save RTS/CTS Bit3: truncation for user TXOP mode Bit2: truncation for TX rate group change Bit1: truncation for AC change Bit0: TXOP timeout truncation 0: disable 1: enable	0x3F

TX_RTS_CFG (offset: 0x1344, default: 0x00FF_FF07)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0

24	R/W	RTS_FBK_EN	RTS rate fallback enable	0
23:8	R/W	RTS_THRES	RTS threshold (unit: byte) MPDU or AMPDU with length greater than RTS threshold will be protected with RTS/CTS exchange at the beginning of the TXOP.	65535
7:0	R/W	RTS_RTY_LIMIT	Auto RTS retry limit	7

TX_TIMEOUT_CFG (offset: 0x1348, default: 0x000F_0A90)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23:16	R/W	TXOP_TIMEOUT	TXOP timeout value for TXOP truncation (Unit: us) Note: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT) Default: For 20us long slot time.	15
15:8	R/W	RX_ACK_TIMEOUT	RX ACK/CTS timeout value for TX procedure (Unit: us) Note: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT) Default: For 20us long slot time.	10
7:4	R/W	MPDU_LIFE_TIME	TX MPDU expiration time Expiration time = 2^(9+MPDU_LIFE_TIME) us Default value is 2^(9+9) ~= 256ms	9
3:0	R/W		Reserved	0

TX_RTY_CFG (offset: 0x134C, default: 0x6BB8_0407)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30	R/W	TX_AUTOFB_EN	TX retry PHY rate auto fallback enable 0: disable 1: enable	1
29	R/W	AGG_RTY_MODE	Aggregate MPDU retry mode 0: expired by retry limit 1: expired by MPDU life timer	1
28	R/W	NAG_RTY_MODE	Non-aggregate MPDU retry mode 0: expired by retry limit 1: expired by MPDU life timer	0
27:16	R/W	LONG_RTY_THRES	Long retry threshold MPDU with length over this threshold is applied with long retry limit.	3000
15:8	R/W	LONG_RTY_LIMIT	Long retry limit	4
7:0	R/W	SHORT_RTY_LIMIT	Short retry limit	7

TX_LINK_CFG (offset: 0x1350, default: 0x007f_0020)

Bits	Type	Name	Description	Initial value
31:24	R	REMOTE_MFS	Remote MCS feedback sequence number	*
23:16	R	REMOTE_MFB	Remote MCS feedback	0x7F
15:13	R		Reserved	0
12	R/W	TX_CFACK_EN	Piggyback CF-ACK enable 0: disable 1: enable	0
11	R/W	TX_RDG_EN	RDG TX enable 0: disable 1: enable	0
10	R/W	TX_MRQ_EN	MCS request TX enable 0: disable 1: enable	0
9	R/W	REMOTE_UMFS_EN	Remote un-solicit MFB enable 0: do not apply remote un-solicit MFB (MFS=7) 1: apply un-solicit MFB	0
8	R/W	TX_MFB_EN	TX apply remote MFB 0: disable 1: enable	0

7:0	R/W	REMOTE_MFB_LITETIME	Remote MFB life time Unit: 32us	32

HT_FBK_CFG0 (offset: 0x1354, default: 0x6543_2100)

Bits	Type	Name	Description	Initial value
31:28	R/W	HT_MCS7_FBK	Auto fall back MCS as HT MCS =7	6
27:24	R/W	HT_MCS6_FBK	Auto fall back MCS as HT MCS =6	5
23:20	R/W	HT_MCS5_FBK	Auto fall back MCS as HT MCS =5	4
19:16	R/W	HT_MCS4_FBK	Auto fall back MCS as HT MCS =4	3
15:12	R/W	HT_MCS3_FBK	Auto fall back MCS as HT MCS =3	2
11:8	R/W	HT_MCS2_FBK	Auto fall back MCS as HT MCS =2	1
7:4	R/W	HT_MCS1_FBK	Auto fall back MCS as HT MCS =1	0
3:0	R/W	HT_MCS0_FBK	Auto fall back MCS as HT MCS =0	0

HT_FBK_CFG1 (offset: 0x1358, default: 0xEDCB_A988)

Bits	Type	Name	Description	Initial value
31:28	R/W	HT_MCS15_FBK	Auto fall back MCS as HT MCS =15	14
27:24	R/W	HT_MCS14_FBK	Auto fall back MCS as HT MCS =14	13
23:20	R/W	HT_MCS13_FBK	Auto fall back MCS as HT MCS =13	12
19:16	R/W	HT_MCS12_FBK	Auto fall back MCS as HT MCS =12	11
15:12	R/W	HT_MCS11_FBK	Auto fall back MCS as HT MCS =11	10
11:8	R/W	HT_MCS10_FBK	Auto fall back MCS as HT MCS =10	9
7:4	R/W	HT_MCS9_FBK	Auto fall back MCS as HT MCS =9	8
3:0	R/W	HT_MCS8_FBK	Auto fall back MCS as HT MCS =8	8

Note1. The MCS is a fallback stopping state, as the fallback MCS is the same as current MCS.
Note2. HT TX PHY rates will not fallback to legacy PHY rates.

LG_FBK_CFG0 (offset: 0x135C, default: 0xEDCB_A988)

Bits	Type	Name	Description	Initial value
31:28	R/W	OFDM7_FBK	Auto fall back MCS as previous TX rate is OFDM 54Mbps.	14
27:24	R/W	OFDM6_FBK	Auto fall back MCS as previous TX rate is OFDM 48Mbps.	13
23:20	R/W	OFDM5_FBK	Auto fall back MCS as previous TX rate is OFDM 36Mbps.	12
19:16	R/W	OFDM4_FBK	Auto fall back MCS as previous TX rate is OFDM 24Mbps.	11
15:12	R/W	OFDM3_FBK	Auto fall back MCS as previous TX rate is OFDM 18Mbps.	10
11:8	R/W	OFDM2_FBK	Auto fall back MCS as previous TX rate is OFDM 12Mbps.	9
7:4	R/W	OFDM1_FBK	Auto fall back MCS as previous TX rate is OFDM 9Mbps.	8
3:0	R/W	OFDM0_FBK	Auto fall back MCS as previous TX rate is OFDM 6Mbps.	8

LG_FBK_CFG1 (offset: 0x1360, default: 0x0000_2100)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:12	R/W	CCK3_FBK	Auto fall back MCS as previous TX rate is CCK 11Mbps.	2
11:8	R/W	CCK2_FBK	Auto fall back MCS as previous TX rate is CCK 5.5Mbps.	1
7:4	R/W	CCK1_FBK	Auto fall back MCS as previous TX rate is CCK 2Mbps.	0
3:0	R/W	CCK0_FBK	Auto fall back MCS as previous TX rate is CCK 1Mbps.	0

Note1. Bit3 of each legacy fallback rate is selection of OFDM/CCK. 0=CCK, 1=OFDM.

CCK_PROT_CFG (offset: 0x1364, default: 0x0010_0003)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	CCK_RTSTH_EN	RTS threshold enable on CCK TX 0: disable 1: enable	0

25:20	R/W	CCK_TXOP_ALLOW	CCK TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	1
19:18	R/W	CCK_PROT_NAV	TXOP protection type for CCK TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	CCK_PROT_CTRL	Protection control frame type for CCK TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	CCK_PROT_RATE	Protection control frame rate for CCK TX (Including RTS/CTS-to-self/CF-END) Default: CCK 11M	0x0003

OFDM_PROT_CFG (offset: 0x1368, default: 0x0020_0003)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	OFDM_RTSTH_EN	RTS threshold enable on OFDM TX 0: disable 1: enable	0
25:20	R/W	OFDM_PROT_TXOP	OFDM TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	2
19:18	R/W	OFDM_PROT_NAV	TXOP protection type for OFDM TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	OFDM_PROT_CTRL	Protection control frame type for OFDM TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	OFDM_PROT_RATE	Protection control frame rate for OFDM TX (Including RTS/CTS-to-self/CF-END) Default: CCK 11M	0x0003

MM20_PROT_CFG (offset: 0x136C, default: 0x0040_4004)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	MM20_RTSTH_EN	RTS threshold enable on MM20 TX 0: disable 1: enable	0
25:20	R/W	MM20_PROT_TXOP	MM20 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX	4

			Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	
19:18	R/W	MM20_PROT_NAV	TXOP protection type for MM20 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	MM20_PROT_CTRL	Protection control frame type for MM20 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	MM20_PROT_RATE	Protection control frame rate for MM20 TX (Including RTS/CTS-to-self/CF-END) Default: OFDM 24M	0x4004

MM40_PROT_CFG (offset: 0x1370, default: 0x0080_4084)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	MM40_RTSTH_EN	RTS threshold enable on MM40 TX 0: disable 1: enable	0
25:20	R/W	MM40_PROT_TXOP	MM40 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	8
19:18	R/W	MM40_PROT_NAV	TXOP protection type for MM40 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	MM40_PROT_CTRL	Protection control frame type for MM40 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	MM40_PROT_RATE	Protection control frame rate for MM40 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x4084

GF20_PROT_CFG (offset: 0x1374, default: 0x0100_4004)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	GF20_RTSTH_EN	RTS threshold enable on GF20 TX 0: disable 1: enable	0
25:20	R/W	GF20_PROT_TXOP	GF20 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX	16

			Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	
19:18	R/W	GF20_PROT_NAV	TXOP protection type for GF20 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	GF20_PROT_CTRL	Protection control frame type for GF20 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	GF20_PROT_RATE	Protection control frame rate for GF20 TX (Including RTS/CTS-to-self/CF-END) Default: OFDM 24M	0x4004

GF40_PROT_CFG (offset: 0x1378, default: 0x0200_4084)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	GF40_RTSTH_EN	RTS threshold enable on GF40 TX 0: disable 1: enable	0
25:20	R/W	GF40_PROT_TXOP	GF40 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	16
19:18	R/W	GF40_PROT_NAV	TXOP protection type for GF40 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	GF40_PROT_CTRL	Protection control frame type for GF40 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	GF40_PROT_RATE	Protection control frame rate for GF40 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x4084

EXP_CTS_TIME (offset: 0x137C, default: 0x0038_013A)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30:16	R/W	EXP_OFDM_CTS_TIME	Expected time for OFDM CTS response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 6Mbps CTS	56
15	R		Reserved	0
14:0	R/W	EXP_CCK_CTS_TIME	Expected time for CCK CTS response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 1Mbps CTS	314

EXP_ACK_TIME (offset: 0x1380, default: 0x0024_00CA)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30:16	R/W	EXP_OFDM_ACK_ TIME	Expected time for OFDM ACK response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 6Mbps ACK preamble	36
15	R		Reserved	0
14:0	R/W	EXP_CCK_ACK_TIME	Expected time for OFDM ACK response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 1Mbps ACK preamble	202

MAC RX configuration registers (offset: 0x1400)

RX_FILTR_CFG (offset: 0x1400, default: 0x0001_5F9F)

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16	R/W	DROP_CTRL_RSV	Drop reserve control subtype	1
15	R/W	DROP_BAR	Drop BAR	0
14	R/W	DROP_BA	Drop BA	1
13	R/W	DROP_PSPOLL	Drop PS-Poll	0
12	R/W	DROP_RTS	Drop RTS	1
11	R/W	DROP_CTS	Drop CTS	1
10	R/W	DROP_ACK	Drop ACK	1
9	R/W	DROP_CFEND	Drop CF-END	1
8	R/W	DROP_CFACK	Drop CF-END + CF-ACK	1
7	R/W	DROP_DUPL	Drop duplicated frame	1
6	R/W	DROP_BC	Drop broadcast frame	0
5	R/W	DROP_MC	Drop multicast frame	0
4	R/W	DROP_VER_ERR	Drop 802.11 version error frame	1
3	R/W	DROP_NOT_MYBSS	Drop frame that is not my BSSID	1
2	R/W	DROP_UC_NOME	Drop not to me unicast frame	1
1	R/W	DROP_PHY_ERR	Drop physical error frame	1
0	R/W	DROP_CRC_ERR	Drop CRC error frame	1

Note: 1: enable, 0: disable.

AUTO_RSP_CFG (offset: 0x1404, default: 0x0000_0003)

Bits	Type	Name	Description	Initial value
31:8	R		Reserved	0
7	R/W	CTRL_PWR_BIT	Power bit value in control frame	0
6	R/W	BAC_ACK_POLICY	BA frame -> BAC -> Ack policy bit value	0
5	R/W	CTRL_WRAP_EN	ACK/CTS Control Wrapper frame auto-responding enable 0: disable 1: enable	0
4	R/W	CCK_SHORT_EN	CCK short preamble auto response enable 0: disable 1: enable	0
3	R/W	CTS_40M_REF	In duplicate legacy CTS response mode, refer to extension CCA to decide duplicate or not. 0: disable 1: enable	0
2	R/W	CTS_40M_MODE	Duplicate legacy CTS response mode 0: disable 1: enable	0
1	R/W	BAC_ACKPOLICY_EN	BAC ACK policy bit enable 0: disable; don't care this bit 1: enable; no BA auto responding upon reception of BAR with no ACK policy	1
0	R/W	AUTO_RSP_EN	Auto responder enable	1

LEGACY_BASIC_RATE (offset: 0x1408, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31: 12	R/W		Reserved	0
11: 0	R/W	LEGACY_BASIC_ RATE	Legacy basic rate bit mask Bit0: 1 Mbps is basic rate Bit1: 2 Mbps is basic rate Bit2: 5.5 Mbps is basic rate Bit3: 11 Mbps is basic rate Bit4: 6 Mbps is basic rate Bit5: 9 Mbps is basic rate Bit6: 12 Mbps is basic rate Bit7: 18 Mbps is basic rate Bit8: 24 Mbps is basic rate Bit9: 36 Mbps is basic rate Bit10: 48 Mbps is basic rate Bit11: 54 Mbps is basic rate 0: disable 1: enable	0

HT_BASIC_RATE (offset: 0x140C, default: 0x8200_8000)

Bits	Type	Name	Description	Initial value
31: 0	R/W	Reserved		0

HT_CTRL_CFG (offset: 0x1410, default: 0x0000_0100)

Bits	Type	Name	Description	Initial value
31: 9	R		Reserved	0
8: 0	R/W	HT_CTRL_THRES	Remaining TXOP threshold for HT control frame auto responding (unit: us)	256

SIFS_COST_CFG (offset: 0x1414, default: 0x0000_100A)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	
15:8	R/W	OFDM_SIFS_COST	OFDM SIFS time (unit: 1us) Applied after OFDM TX/RX.	16
7:0	R/W	CCK_SIFS_COST	CCK SIFS time (unit: 1us) Applied after CCK TX/RX.	10

Note: The OFDM_SIFS_COST and CCK_SIFS_COST are used only for duration field calculation. It will not affect the responding timing.

RX_PARSER_CFG (offset: 0x1418, default: 0x0FFF_0000)

Bits	Type	Name	Description	Initial value
31:28	R		Reserved	
27:16	R/W	LSIG_LEN_THRES	When the length in L-SIG is longer than this threshold, the L-SIG TXOP will not be applied as NAV channel reservation.	4095
15:02	R		Reserved	
1	R/W	RX_LSIG_TXOP_EN	Respect LSIG-TXOP as channel reservation 0: disable 1: enable	0
0	R/W	NAV_ALL_EN	Set NAV for all received frames 0: disable (unicast to me frame will not set the NAV) 1: enable	0

MAC Security Configuration Registers (offset:0x1500)

TX_SEC_CNT0 (offset:0x1500, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_SEC_ERR_CNT	TX SEC packet error count	0
15:0	RC	TX_SEC_CPL_CNT	TX SEC packet complete count	0

RX_SEC_CNT0 (offset:0x1504, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16			Reserved	0
15:0	RC	RX_SEC_CPL_CNT	RX SEC packet complete count	0

CCMP_FC_MUTE (offset:0x1508, default: 0xC78F_C78f)

Bits	Type	Name	Description	Initial value
31:16	R/W	HT_CCMP_FC_MUTE	HT rate CCMP FC mute	0xc78f
15:0	R/W	LG_CCMP_FC_MUTE	Legacy rate CCMP FC mute	0xc78f

MAC HCCA/PSMP CSR (offset:0x1600)

TXOP_HLDR_ADDR0 (offset:0x1600, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	TXOP_HOL_3	TXOP holder MAC address byte3	0
23:16	R/W	TXOP_HOL_2	TXOP holder MAC address byte2	0
15:8	R/W	TXOP_HOL_1	TXOP holder MAC address byte1	0
7:0	R/W	TXOP_HOL_0	TXOP holder MAC address byte0	0

TXOP_HLDR_ADDR1 (offset:0x1604, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	TXOP_HOL_5	TXOP holder MAC address byte5	0
7:0	R/W	TXOP_HOL_4	TXOP holder MAC address byte4	0

Note: Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

TXOP_HLDR_ET (offset:0x1608, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:25	R		Reserved	0
24	R/W	AMPDU_ACC_EN	Accumulate AMPDU enable 0: disable, 1: enable	0
23:19	R/W	TX_DMA_TIMEOUT	When AMPDU_ACC_EN is enabled: Wait at most (TX_DMA_TIMEOUT * 32) usec for the MPDU for aggregation	0
18	R/W	TX_FBK_THRES_EN	Transmission MCS fallback threshold enable 0: disable, 1: enable	0
17:16	R/W	TX_FBK_THRES	When TX_FBK_THRES_EN is enabled, fallback when 0: less than 25% in AMPDU are success. 1: less than 50% in AMPDU are success. 2: less than 75% in AMPDU are success. 3: less than 100% in AMPDU are success.	0
15:5	R		Reserved	0
4	R/W	PAPE_MAP	When PAPE_MAP1S_EN is enabled: 0: only turn on PAPE0 for 1S transmission 1: only turn on PAPE1 for 1S transmission	0
3	R/W	PAPE_MAP1S_EN	Turn on only on PAPE in 1S transmission 0: disable, 1: enable	0
2	R/W	TX_BCN_HIPRI_DIS	Disable high priority beacon transmisson 1: disable, 0: enable	0
1	R/W	TX40M_BLK_EN	Block 40Mhz transmission as extension CCA is busy 0: disable, 1: enable	0
0	R/W	PER_RX_RST_EN	Baseband RX_PE per RX reset enable 0: disable, 1: enable	0

QOS_CFPOLL_RA_DW0 (offset:0x160C, default :0xXXXX_XXXX)

Bits	Type	Name	Description	Initial value
31:24	R	CFPOLL_A1_BYTE3	Byte3 of A1 of received QoS Data (+) CF-Poll frame	X
23:16	R	CFPOLL_A1_BYTE2	Byte2 of A1 of received QoS Data (+) CF-Poll frame	X

15:8	R	CFPOLL_A1_BYTE1	Byte1 of A1 of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_A1_BYTE0	Byte0 of A1 of received QoS Data (+) CF-Poll frame	X

QOS_CFPOLL_A1_DW1 (offset:0x1610, default :0x0000_XXXX)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
16	R	CFPOLL_A1_TOME	1: QoS CF-Poll to me 0: Qos CF-Poll not to me	X
15:8	R	CFPOLL_A1_BYTE5	Byte5 of A1 of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_A1_BYTE4	Byte4 of A1 of received QoS Data (+) CF-Poll frame	X

QOS_CFPOLL_QC (offset:0x1614, default :0x0000_XXXX)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
15:8	R	CFPOLL_QC_BYTE1	Byte1 of QC of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_QC_BYTE0	Byte0 of QC of received QoS Data (+) CF-Poll frame	X

Note: CFPOLL_RA_DW0, CFPOLL_RA_DW1, and CFPOLL_QC are updated after the reception of QoS Data (+) CF-Poll frame and RX QoS CF-Poll interrupt (RX_QOS_CFPOLL_INT) is launched then.

MAC Statistic Counters (offset:0x1700)

RX_STA_CNT0 (offset:0x1700, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	PHY_ERRCNT	RX PHY error frame count	0
15:0	RC	CRC_ERRCNT	RX CRC error frame count	0

Note1: RX PHY error means PSDU length is shorter than indicated by PLCP.
Note2: RX PHY error is also treated as CRC error.

RX_STA_CNT1 (offset:0x1704, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	PLPC_ERRCNT	RX PLCP error count	0
15:0	RC	CCA_ERRCNT	CCA false alarm count	0

Note1: CCA false alarm means there is no PLCP after CCA indication.
Note2: RX PLCP error means there is no PSDU after PLCP indication.

RX_STA_CNT2 (offset:0x1708, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	RX_OVFL_CNT	RX FIFO overflow frame count	0
15:0	RC	RX_DUPL_CNT	RX duplicated filtered frame count	0

Note: MAC will NOT auto respond ACK/BA to the frame originator when frame is lost due to RXFIFO overflow. However, MAC will respond when frame is duplicated filtered.

TX_STA_CNT0 (offset:0x170C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_BCN_CNT	TX beacon count	0
15:0	RC	TX_FAIL_CNT	Failed TX count	0

TX_STA_CNT1 (offset:0x1710, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_RTY_CNT	TX retransmission count	0
15:0	RC	TX_SUCC_CNT	Successful TX count	0

TX_STA_CNT2 (offset:0x1714, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_UDFL_CNT	TX underflow count	0
15:0	RC	TX_ZERO_CNT	TX zero length frame count	0

TX_STAT_FIFO (offset:0x1718, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R	TXQ_RATE	TX success rate	*
15:8	R	TXQ_WCID	TX WCID	*
7	R	TXQ_ACKREQ	TX acknowledge required 0: not required 1: required	*

6	R	TXQ_AGG	TX aggregate 0: non-aggregated 1: aggregated	*
5	R	TXQ_OK	TX success 0: failed 1: success	*
4:1	R	TXQ_PID	TX Packet ID (Latched from TXWI)	*
0	RC	TXQ_VLD	TX status queue valid 0: queue empty 1: valid	0

Note: TX status FIFO size = 16.

TX_NAG_AGG_CNT (offset:0x171C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_CNT	Aggregate TX count	0
15:0	RC	TX_NAG_CNT	Non-aggregate TX count	0

TX_AGG_CNT0 (offset:0x1720, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_2_CNT	Aggregate Size = 2 MPDU count	0
15:0	RC	TX_AGG_1_CNT	Aggregate Size = 1 MPDU count	0

TX_AGG_CNT1 (offset:0x1724, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_4_CNT	Aggregate Size = 4 MPDU count	0
15:0	RC	TX_AGG_3_CNT	Aggregate Size = 3 MPDU count	0

TX_AGG_CNT2 (offset:0x1728, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_6_CNT	Aggregate Size = 6 MPDU count	0
15:0	RC	TX_AGG_5_CNT	Aggregate Size = 5 MPDU count	0

TX_AGG_CNT3 (offset:0x172C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_8_CNT	Aggregate Size = 8 MPDU count	0
15:0	RC	TX_AGG_7_CNT	Aggregate Size = 7 MPDU count	0

TX_AGG_CNT4 (offset:0x1730, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_10_CNT	Aggregate Size = 10 MPDU count	0
15:0	RC	TX_AGG_9_CNT	Aggregate Size = 9 MPDU count	0

TX_AGG_CNT5 (offset:0x1734, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_12_CNT	Aggregate Size = 12 MPDU count	0
15:0	RC	TX_AGG_11_CNT	Aggregate Size = 11 MPDU count	0

TX_AGG_CNT6 (offset:0x1738, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_14_CNT	Aggregate Size = 14 MPDU count	0
15:0	RC	TX_AGG_13_CNT	Aggregate Size = 13 MPDU count	0

TX_AGG_CNT7 (offset:0x173C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_16_CNT	Aggregate Size > 16 MPDU count	0
15:0	RC	TX_AGG_15_CNT	Aggregate Size = 15 MPDU count	0

MPDU_DENSITY_CNT (offset:0x1740, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	RX_ZERO_DEL_CNT	RX zero length delimiter count	0
15:0	RC	TX_ZERO_DEL_CNT	TX zero length delimiter count	0

RTS_TX_CNT (offset:0x1744, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	RTS_TX_FAIL_CNT	RTS TX fail count	0
15:0	RC	RTS_TX_OK_CNT	RTS TX OK count	0

CTS_TX_CNT (offset:0x1748, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	RC	CTSTS_TX_CNT	CTS-to-self TX count	0

3.5 MAC search table (offset: 0x1800)

RX WCID search entry format (8 bytes)

Offset	Type	Name	Description	Initial value
0x00	R/W	WC_MAC_ADDR0	Client MAC address byte0	0x00
0x01	R/W	WC_MAC_ADDR1	Client MAC address byte1	0x00
0x02	R/W	WC_MAC_ADDR2	Client MAC address byte2	0x00
0x03	R/W	WC_MAC_ADDR3	Client MAC address byte3	0x00
0x04	R/W	WC_MAC_ADDR4	Client MAC address byte4	0x00
0x05	R/W	WC_MAC_ADDR5	Client MAC address byte5	0x00
0x06	R/W	BA_SESS_MASK0	BA session mask (lower) Bit0 for TID0 Bit7 for TID7	0x00
0x07	R/W	BA_SESS_MASK1	BA session mask (upper) Bit8 for TID8 Bit15 for TID15	0x00

RX WCID search table (offset:0x1800)

Offset	Type	Name	Description	Initial value
0x1800	R/W	WC_ENTRY_0	WC MAC address with WCID=0	0
0x1808	R/W	WC_ENTRY_1	WC MAC address with WCID=1	0
....	R/W	....	WC MAC address with WCID=2~253	0
0x1FF0	R/W	WC_ENTRY_254	WC MAC address with WCID=254	0
0x1FF8	R/W	WC_ENTRY_255	Reserved (shall not be used)	0

Note1: WCID=Wireless Client ID

3.6 Security table/CIS/Beacon/NULL frame (offset: 0x4000)

Security Entry format

Security Key Format (8DW)

Offset	Type	Name	Description	Initial value
0x00	R/W	SECKEY_DW0	Security key byte3~0	*
0x04	R/W	SECKEY_DW1	Security key byte7~4	*
0x08	R/W	SECKEY_DW2	Security key byte11~8	*
0x0C	R/W	SECKEY_DW3	Security key byte15~12	*
0x10	R/W	TXMIC_DW0	TX MIC key byte3~0	*
0x14	R/W	TXMIC_DW1	TX MIC key byte7~4	*
0x18	R/W	RXMIC_DW0	RX MIC key byte3~0	*
0x1C	R/W	RXMIC_DW1	RX MIC key byte7~4	*

Note:

1. For WEP40, CKIP40, only byte4~0 of security key are valid.
2. For WEP104, CKIP104, only byte12~0 of security key are valid.
3. For TKIP, AES, all the bytes of security key are valid.
4. TX/RX MIC key is used only for TKIP MIC calculation.

IV/EIV format (2 DW)

When TXINFO.WIV=0, hardware will auto lookup IV/EIV from this table and update IV/EIV after encryption is finished.

Offset	Type	Name	Description	Initial value
0x00	R/W	IV_FIELED	IV field	*
0x04	R/W	EIV_FIELED	EIV field	*

Note1: The key index and extension IV bit shall be initialized by software. The MSB octet of IV will not be modified by hardware.

Note2: IV/EIV packet number (PN) counter modes:

a. For WEP40, WEP104, CKIP40, CKIP104, CKIP128 mode, PN=IV[23:0]. EIV[31:0] is not used.

b. For TKIP mode, PN = {EIV[31:0], IV[7:0], IV[23:16]}, IV[15:8]=(IV[7:0] | 0x20) & 0x7f) is generated by hardware.

c. For AES-CCMP, PN = {EIV[31:0], IV[15:0]}.

d. PN = PN + 1 after each encryption.

Note3: Software may initialize the PN counter to any value.

WCID attribute entry format (1DW)

Offset	Type	Name	Description	Initial value
31:10	R/W		Reserved	*
9:7	R/W	RXWI_UDF	RXWI user define field This field is tagged in the RXWI.UDF fields for the WCID.	*
6:4	R/W	BSS_IDX	Multiple-BSS index for the WCID	*
3:1	R/W	RX_PKEY_MODE	Pair-wise key security mode 0: No security 1: WEP40 2: WEP104 3: TKIP 4: AES-CCMP 5: CKIP40 6: CKIP104 7: CKIP128	*
0	R/W	RX_PKEY_EN	Key table selection 0: shared key table 1: pair-wise key table	*

Share key mode entry format (1DW)

Bits	Type	Name	Description	Initial value
31	R/W		Reserved	*
30:28	R/W	SKEY_MODE_7+	Shared key7+(8x) mode, x=0~3	*
27	R/W		Reserved	*
26:24	R/W	SKEY_MODE_6+	Shared key6+(8x) mode, x=0~3	*
23	R/W		Reserved	*
22:20	R/W	SKEY_MODE_5+	Shared key5+(8x) mode, x=0~3	*
19	R/W		Reserved	*
18:16	R/W	SKEY_MODE_4+	Shared key4+(8x) mode, x=0~3	*
15	R/W		Reserved	*
14:12	R/W	SKEY_MODE_3+	Shared key3+(8x) mode, x=0~3	*
11	R/W		Reserved	*
10:8	R/W	SKEY_MODE_2+	Shared key2+(8x) mode, x=0~3	*
7	R/W		Reserved	*
6:4	R/W	SKEY_MODE_1+	Shared key1+(8x) mode, x=0~3	*
3	R/W		Reserved	*
2:0	R/W	SKEY_MODE_0+	Shared key0+(8x) mode, x=0~3	*

Key mode definition:

0: No security 1: WEP40 2: WEP104 3: TKIP

4: AES-CCMP 5: CKIP40 6: CKIP104 7: CKIP128

Security Table

Pair-wise key table (offset:0x4000)

Offset	Type	Name	Description	Initial value
0x4000	R/W	PKEY_0	Pair-wise key for WCID0	*
0x4020	R/W	PKEY_1	Pair-wise key for WCID1	*

….	R/W	….	Pair-wise key for WCID2~253	*
0x5FC0	R/W	PKEY_254	Pair-wise key for WCID254	*
0x5FE0	R/W	PKEY_255	Pair-wise key for WCID255 (not used)	*

IV/EIV table (offset:0x6000)

Offset	Type	Name	Description	Initial value
0x6000	R/W	IVEIV_0	IV/EIV for WCID0	*
0x6008	R/W	IVEIV_1	IV/EIV for WCID1	*
….	R/W	….	IV/EIV for WCID2~253	*
0x67F0	R/W	IVEIV_254	IV/EIV for WCID254	*
0x67F8	R/W	IVEIV_255	IV/EIV for WCID255 (not used)	*

WCID attribute table (offset:0x6800)

Offset	Type	Name	Description	Initial value
0x6800	R/W	WCID_ATTR_0	WCID Attribute for WCID0	*
0x6804	R/W	WCID_ATTR_1	WCID Attribute for WCID1	*
….	R/W	….	WCID Attribute for WCID2~253	*
0x6BF8	R/W	WCID_ATTR_254	WCID Attribute for WCID254	*
0x6BFC	R/W	WCID_ATTR_255	WCID Attribute for WCID255	*

Shared Key Table (offset:0x6C00)

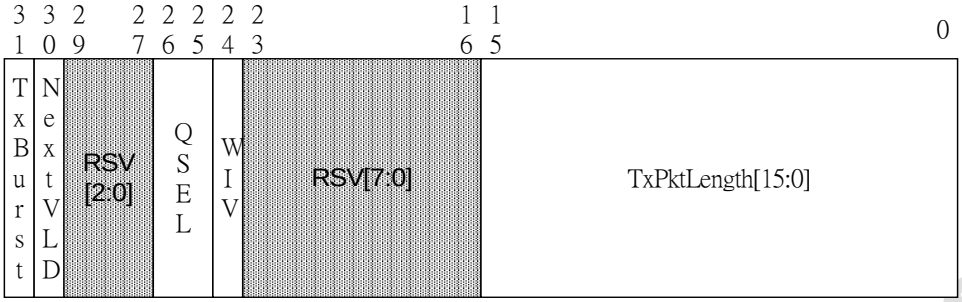
Offset	Type	Name	Description	Initial value
0x6C00	R/W	SKEY_0	Shared key for BSS_IDX=0, KEY_IDX=0	*
0x6C20	R/W	SKEY_1	Shared key for BSS_IDX=0, KEY_IDX=1	*
0x6C40	R/W	SKEY_2	Shared key for BSS_IDX=0, KEY_IDX=2	*
0x6C60	R/W	SKEY_3	Shared key for BSS_IDX=0, KEY_IDX=3	*
0x6C80	R/W	SKEY_4	Shared key for BSS_IDX=1, KEY_IDX=0	*
0x6CA0	R/W	SKEY_5	Shared key for BSS_IDX=1, KEY_IDX=1	*
0x6CC0	R/W	SKEY_6	Shared key for BSS_IDX=1, KEY_IDX=2	*
0x6CE0	R/W	SKEY_7	Shared key for BSS_IDX=1, KEY_IDX=3	*
0x6D00	R/W	SKEY_8	Shared key for BSS_IDX=2, KEY_IDX=0	*
0x6D20	R/W	SKEY_9	Shared key for BSS_IDX=2, KEY_IDX=1	*
0x6D40	R/W	SKEY_10	Shared key for BSS_IDX=2, KEY_IDX=2	*
0x6D60	R/W	SKEY_11	Shared key for BSS_IDX=2, KEY_IDX=3	*
0x6D80	R/W	SKEY_12	Shared key for BSS_IDX=3, KEY_IDX=0	*
0x6DA0	R/W	SKEY_13	Shared key for BSS_IDX=3, KEY_IDX=1	*
0x6DC0	R/W	SKEY_14	Shared key for BSS_IDX=3, KEY_IDX=2	*
0x6DE0	R/W	SKEY_15	Shared key for BSS_IDX=3, KEY_IDX=3	*
0x6E00	R/W	SKEY_16	Shared key for BSS_IDX=4, KEY_IDX=0	*
0x6E20	R/W	SKEY_17	Shared key for BSS_IDX=4, KEY_IDX=1	*
0x6E40	R/W	SKEY_18	Shared key for BSS_IDX=4, KEY_IDX=2	*
0x6E60	R/W	SKEY_19	Shared key for BSS_IDX=4, KEY_IDX=3	*
0x6E80	R/W	SKEY_20	Shared key for BSS_IDX=5, KEY_IDX=0	*
0x6EA0	R/W	SKEY_21	Shared key for BSS_IDX=5, KEY_IDX=1	*
0x6EC0	R/W	SKEY_22	Shared key for BSS_IDX=5, KEY_IDX=2	*
0x6EE0	R/W	SKEY_23	Shared key for BSS_IDX=5, KEY_IDX=3	*
0x6F00	R/W	SKEY_24	Shared key for BSS_IDX=6, KEY_IDX=0	*
0x6F20	R/W	SKEY_25	Shared key for BSS_IDX=6, KEY_IDX=1	*
0x6F40	R/W	SKEY_26	Shared key for BSS_IDX=6, KEY_IDX=2	*
0x6F60	R/W	SKEY_27	Shared key for BSS_IDX=6, KEY_IDX=3	*
0x6F80	R/W	SKEY_28	Shared key for BSS_IDX=7, KEY_IDX=0	*
0x6FA0	R/W	SKEY_29	Shared key for BSS_IDX=7, KEY_IDX=1	*
0x6FC0	R/W	SKEY_30	Shared key for BSS_IDX=7, KEY_IDX=2	*
0x6FE0	R/W	SKEY_31	Shared key for BSS_IDX=7, KEY_IDX=3	*

Shared Key Mode (offset:0x7000)

Offset	Type	Name	Description	Initial value
0x7000	R/W	SKEY_MODE_0_7	Shared mode for SKEY0-SKEY7	*
0x7004	R/W	SKEY_MODE_8_15	Shared mode for SKEY8-SKEY15	*
0x7008	R/W	SKEY_MODE_16_23	Shared mode forSKEY16-SKEY23	*
0x700C	R/W	SKEY_MODE_24_31	Shared mode for SKEY24-SKEY31	*

4 Descriptor and Wireless information

4.1 TXINF



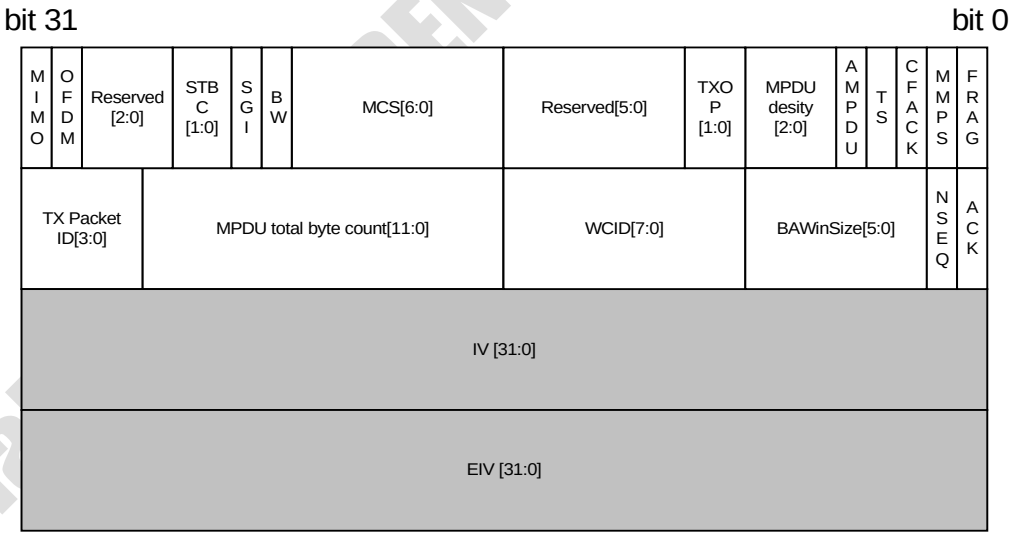
TXINF is prepared by host driver and used for passing information to DMA. Its size is 1 DW and put at the head of each Tx frame. Following is the detail description of each field of TXINF:

- TxBurst: force DMA transmit frame from current selected endpoint.
- NextVLD: host driver info DMA current frame is not he last frame in current Tx queue.
- QSEL[1:0]: packet buffer Q selection.

QSEL	Dest. In PBF	Function	Tx Priority
2'b00	Tx0Q	Management	Highest
2'b01	Tx1Q	HCCA	Medium
2'b10	Tx2Q	EDCA	Lowest
2'b11	N/A	N/A	N/A

- WIV: wireless information (WI) valid.
- TxPacketLength[15:0]: this field specify the frame length in unit of byte. It includes WI, 802.11 header, and payload, but TXINF is not included.

4.2 TXWI format

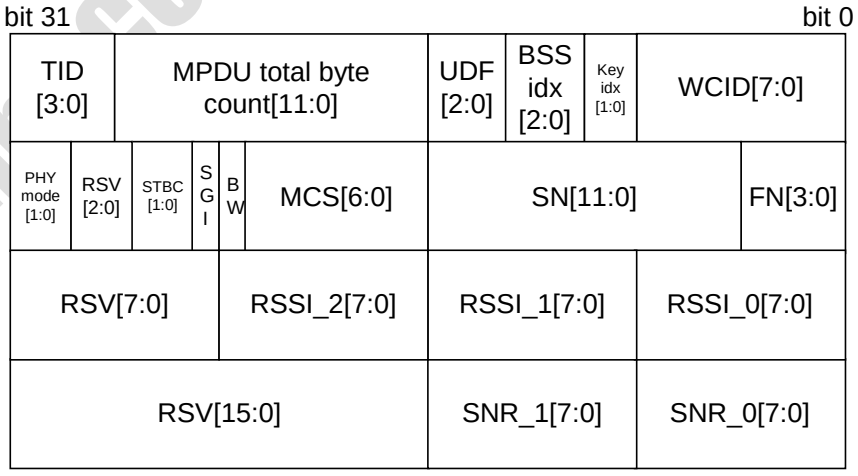


- ***FRAG***: 1: to inform TKIP engine this is a fragment, so that TKIP MIC is appended by driver at the last fragment; hardware TKIP engine only need to insert IV/EIV and ICV.
- ***MMPS***: 1: the remote peer is in dynamic MIMO-PS mode
- ***CFACK***: 1: if an ACK is required to the same peer as this outgoing DATA frame, then MAC TX will send a single DATA+CFACK frame instead of separate ACK and DATA frames. 0: no piggyback ACK allowed for the RA of this frame.
- ***TS***: 1: This is a BEACON or ProbeResponse frame and MAC needs to auto insert 8-byte timestamp after 802.11 WLAN header.
- ***AMPDU***: this frame is eligible for AMPDU. MAC TX will aggregate subsequent outgoing frames having

<same RA, same TID, AMPDU=1> whenever TXOP allows. Even there's only one DATA frame to be sent, as long as the AMPDU bit in TXWI is ON, MAC will still package it as AMPDU with implicit BAR. This adds only 4-byte AMPDU delimiter overhead into the outgoing frame and imply the response frame is a BA instead of ACK. NOTE: driver should set AMPDU=1 only after a BA session is successfully negotiated, because Block ACK is the only way to acknowledge in AMPDU case.

- ***MPDU density***: 1/4usec ~ 16usec per-peer parameter used in outgoing A-MPDU. (This field complies with the "minimum MDPU Starting Spacing" of the A-MPDU parameter field of draft 1.08).
  000- no restriction
  001- 1/4 µsec
  010- 1/2 µsec
  011- 1 µsec
  100- 2 µsec
  101- 4 µsec
  110- 8 µsec
  111- 16 µsec
- ***TXOP***: TX back off mode. 0: HT TXOP rule; 1: PIFS TX; 2: SIFS (only when previous frame exchange is successful); 3: Back off.
- ***"MCS/BW/ShortGI/ /OFDM/MIMO"***: TX data rate & MIMO parameters for this outgoing frame to be filled into BBP
- ***ACK***: this bit informs MAC to wait for ACK or not after transmission of the frame. Event though QOD DATA frame has ACK policy in its QOS CONTROL field, MAC TX solely depends on this ACK bit to decide waiting of ACK or not.
- ***NSEQ***: 1: to use the special h/w SEQ number register in MAC block.
- ***BA window size***: tell MAC the maximum number of to-be-BAed frames is allowed of the RA (RA's BA re-ordering buffer size)
- ***WCID (Wireless Client Index)*** : lookup result of ADDR1 in the peer table (255=not found). This index is also used to find all the attributes of the wireless peer (e.g. TX rate, TX power, pair-wise KEY, IV, EIV,). This index has consistent meaning in both driver and hardware.
- ***MSDU total byte count:*** total length of this frame.
- ***Packet ID:*** as a cookie specified by driver and will be latched into the TX result register stack. Driver use this field to identify special frame's TX result.
- ***IV***: used by encryption engine.
- ***EIV***: used by encryption engine.

4.3 RXWI format



- ***WCID***: index of ADDR2 in the pair wise KEY table. This value uniquely identifies the TA. WCID=255 means not found.
- ***KEY Index***: 0~3 extracted from IV field. For driver reference only, no particular usage so far.
- ***BSSID index***: 0~7 for BSSID0~7. Extract from 802.11 header (the last three bits of BSSID field).
- ***UDF***: User Defined Field.

- ***MPDU total byte count***: the entire MPDU length.
- ***TID***: extracted from 8002.11 QOS control field.
- ***FN***: fragment number of the received MPDU. Extract from 802.11 header.
- ***SN***: sequence number of the received MPDU. Used for BA re-ordering especially that AMSDU are auto segregated by hardware and lost the 802.11 header.
- ***"MCS/BW/SGI/PHYmode"***: RX data rate & related MIMO parameters of this frame got from PLCP header. See next section for the detail.
- ***RSSI0, RSSI1, RSSI2***: BBP reported RSSI information of the received frame.
- ***SNR0, SNR1***: BBP reported SNR information of the received frame.

4.4 Brief PHY rate format and definition

A 16-bit brief PHY rate is used in MAC hardware.
It is the same PHY rate field described in TXWI and RXWI.

Bit	Name	Description
15:14	PHY MODE	Preamble mode 0: Legacy CCK, 1: Legacy OFDM, 2: HT mix mode, 3: HT green field
13:9		Reserved
8	SGI	Short Guard Interval, only support for HT mode 0: 800ns, 1: 400ns
7	BW	Bandwidth. Support both legacy and HT modes 40Mhz in legacy mode means duplicate legacy 0: 20Mhz, 1: 40Mhz
6:0	MCS	Modulation Coding Scheme

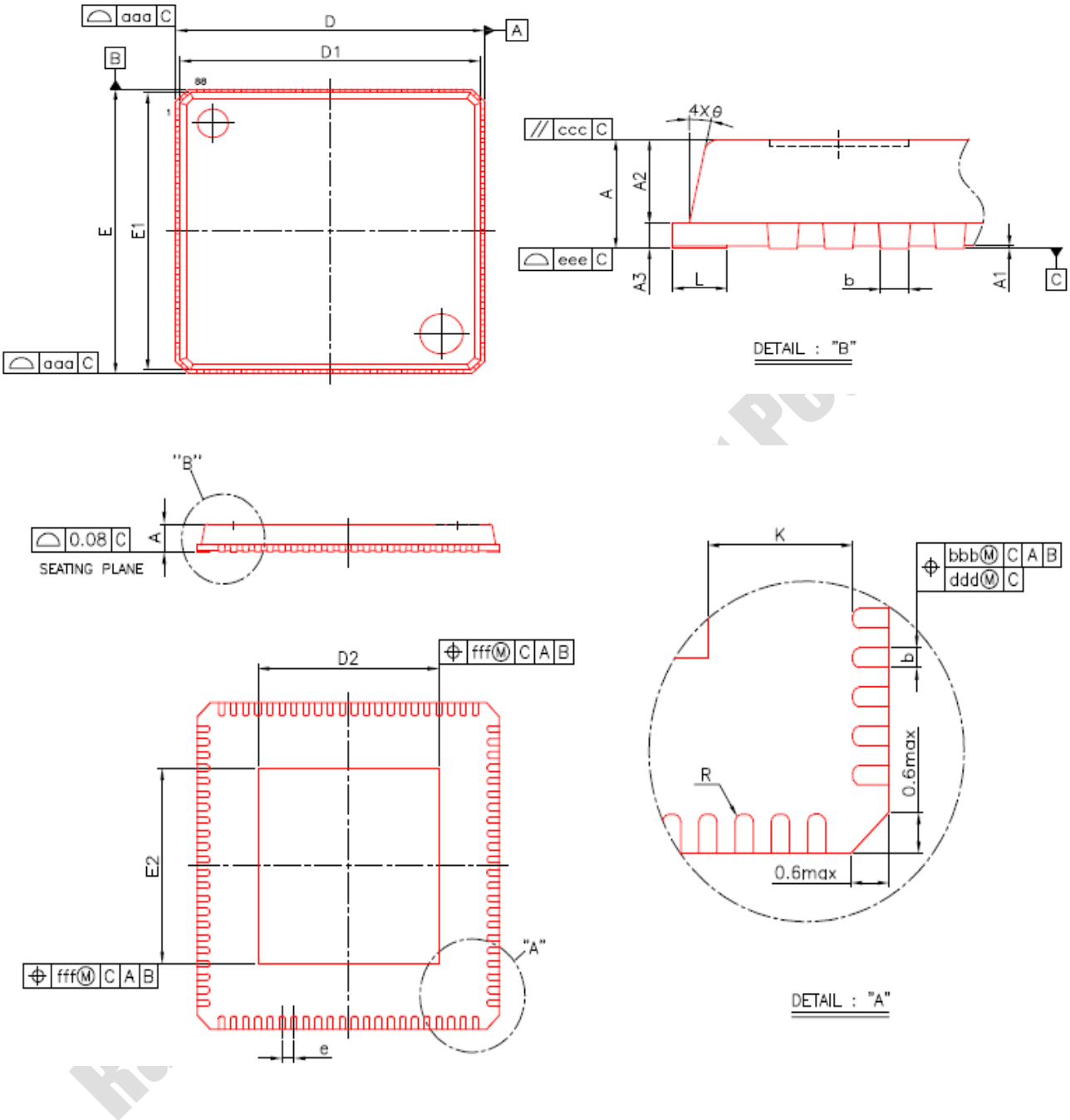
Table. Brief PHY rate format

MODE = Legacy CCK	
MCS = 0	Long Preamble CCK 1Mbps
MCS = 1	Long Preamble CCK 2Mbps
MCS = 2	Long Preamble CCK 5.5Mbps
MCS = 3	Long Preamble CCK 11Mbps
MCS = 8	Short Preamble CCK 1Mbps (illegal rate)
MCS = 9	Short Preamble CCK 2Mbps
MCS = 10	Short Preamble 5.5Mbps
MCS = 11	Short Preamble 11Mbps
Other MCS codes are reserved in legacy CCK mode. BW and SGI are reserved in legacy CCK mode.	
MODE = Legacy OFDM	
MCS = 0	6Mbps
MCS = 1	9Mbps
MCS = 2	12Mbps
MCS = 3	18Mbps
MCS = 4	24Mbps
MCS = 5	36Mbps
MCS = 6	48Mbps
MCS = 7	54Mbps

Other MCS code in legacy CCK mode are reserved When BW = 1, duplicate legacy OFDM is sent. SGI are reserved in legacy OFDM mode.			
MODE = HT mix mode / HT green field			
MCS = 0 (1S)	(BW=0, SGI=0) 6.5Mbps	MCS = 8 (2S)	(BW=0, SGI=0) 13Mbps
MCS = 1 (1S)	(BW=0, SGI=0) 13Mbps	MCS = 9 (2S)	(BW=0, SGI=0) 26Mbps
MCS = 2 (1S)	(BW=0, SGI=0) 19.5Mbps	MCS = 10 (2S)	(BW=0, SGI=0) 39Mbps
MCS = 3 (1S)	(BW=0, SGI=0) 26Mbps	MCS = 11 (2S)	(BW=0, SGI=0) 52Mbps
MCS = 4 (1S)	(BW=0, SGI=0) 39Mbps	MCS = 12 (2S)	(BW=0, SGI=0) 78Mbps
MCS = 5 (1S)	(BW=0, SGI=0) 52Mbps	MCS = 13 (2S)	(BW=0, SGI=0) 104Mbps
MCS = 6 (1S)	(BW=0, SGI=0) 58.5Mbps	MCS = 14 (2S)	(BW=0, SGI=0) 117Mbps
MCS = 7 (1S)	(BW=0, SGI=0) 65Mbps	MCS = 15 (2S)	(BW=0, SGI=0) 130Mbps
MCS = 32	(BW=1, SGI=0) HT duplicate 6Mbps		
When BW=1, PHY_RATE = PHY_RATE * 2 When SGI=1, PHY_RATE = PHY_RATE * 10/9 The effects of BW and SGI are accumulative. When MCS=0~7(1S), SGI option is supported. BW option is supported. When MCS=8~15(2S), SGI option is supported. BW option is supported. When MCS=32, only SGI option is supported. BW option are not supported. (BW =1) Other MCS code in HT mode are reserved			

5 Package Physical Dimension

5.1 QFN 88LD（10×10mm）



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.13	0.19	0.25	0.006	0.008	0.010
D/E	10.00 BSC			0.394 BSC		
D1/E1	9.75 BSC			0.384 BSC		
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.075	---	---	0.003	---	---
K	0.20	---	---	0.008	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

Exposed Pad Size						
L/F	D2/E2 (mm)			D2/E2 (inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
②	6.75	7.125	7.5	0.266	0.272	0.278

6 Revision History

Rev	Date	From	Description
3.0	2/6/09	Mark Liu	Initiate the data sheet.
3.1	2009/6/5	Mark Liu John Chang	1.Modify 2.2 Thermal Information 2.Modify 5 Package Information