
PRINCIPLE DESCRIPTION OF WA211P

The PESI-AP (IEEE 802.11b, 11 Mbps WLAN Access Point) is an internetworking device for interconnecting a WLAN with other WLANs and legacy LANs, which provides a 2.4 GHz RF network and bridges to an Ethernet backbone. The

Access Point is the wireless equivalent of a LAN hub. It receives, buffers and transmits data between the WLAN and the wired network, supporting a group of wireless user devices. An Access Point is typically connected with the wired backbone through a standard Ethernet cable, and communicates with wireless devices by means of an antenna. The Access Point, or the antenna connected to it, is generally mounted high on a wall or on the ceiling. Like the cells in a cellular phone network.

Figure 1 illustrates the block diagram of WA211P. The block diagram is comprised of 5 parts:

- HFA3683 2.4GHz RF/IF Converter and Synthesizer
- HFA3783 AGC Quadrature Modem and Synthesizer
- HFA3983 PA with Detector
- HFA3861 Baseband Processor with Rake Receiver
- AT76C510 Media Access Controller

The WA211P operates in half-duplex mode the up/down conversions and modulation/demodulation functions have been combined into HFA3683 and HFA3783 chip set. The HFA3683 features an integrated gain selectable low noise amplifier to amplify the incoming RF. Doubly balanced mixers are used for up and down conversion in the transmit and receive modes. A high performance transmit preamplifier provides 12dB of power gain and an integrated PLL synthesizer provides the LO for the mixers.

The HFA3783, in addition to providing quadrature modulation and demodulation, also has an integrated AGC IF amplifier, IF level detection, second order I and Q antialiasing filters, and a transmit amplifier with 70dB of gain control range. Transmit and receive IF paths share a common differential matching network to reduce the IF filter component count.



Wireless LAN - Access Point

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The HFA3983 features two stages of RF power amplifiers that operate from a single 3.3V supply. A peak detector allows the user to implement a closed loop transmit power control function in conjunction with the HFA3861B Baseband Processor. The HFA3861B Baseband Processor contains all of the functions necessary for a full or half duplex DSSS packet baseband transceiver. It has 7-bit transmit and receive DACs for the AGC functions and meets FCC processing gain requirements at 1MBPS, 2MBPS, 5.5MBPS and 11MBPS. A RAKE receiver in the HFA3861A coherently resolves and combines multi-path reflections for improved SNR in hostile environments.

Medium access control is performed by the AT76C510 MAC, which provides the necessary interface between the baseband HFA3861B and the Ethernet PHY device. The MAC utilizes a processor AT76C510 is also optimized for control of the WLAN protocol in order to support the 11 Mbps data rate with low power low power consumption.



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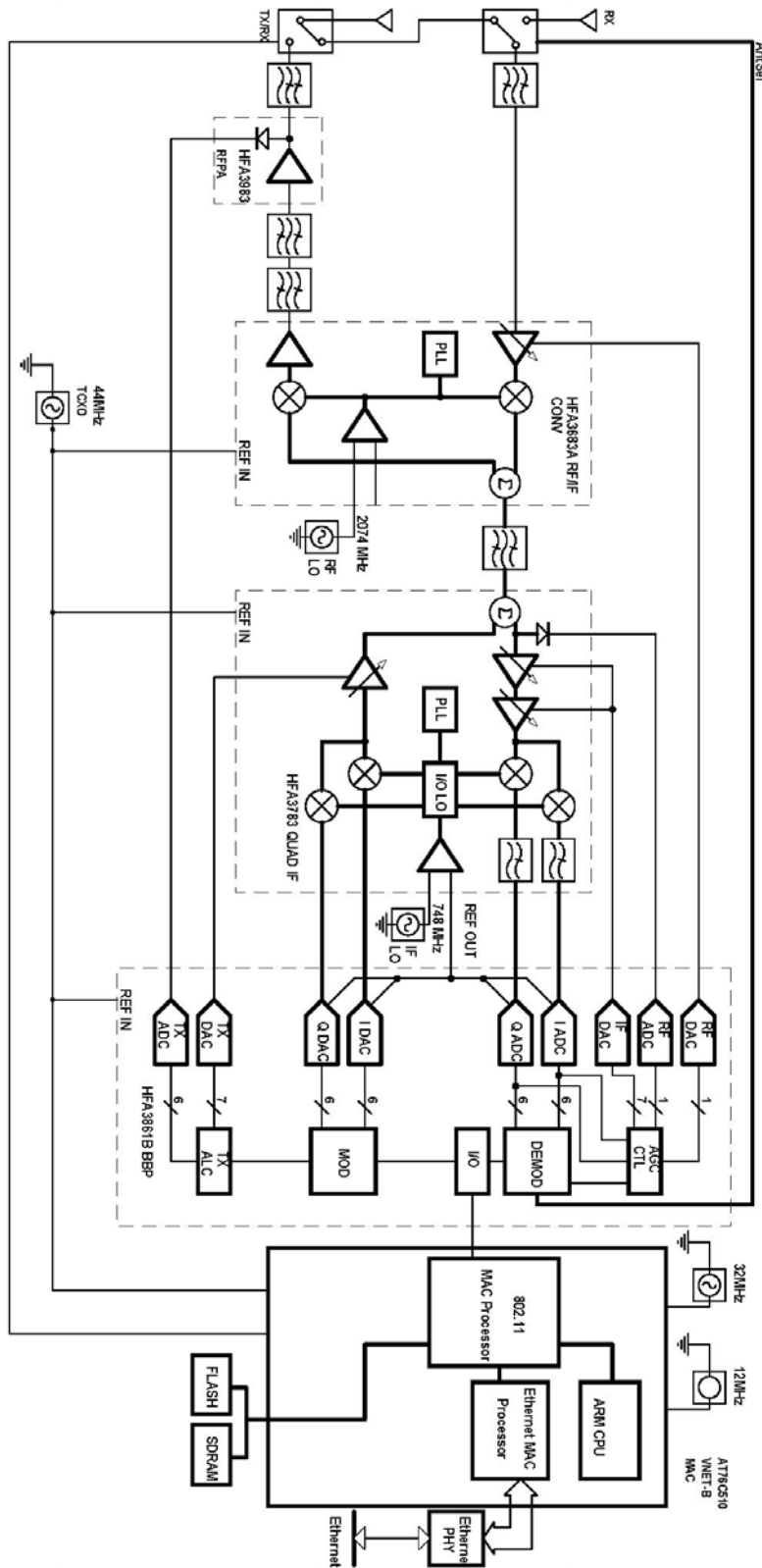


Figure 1. The block diagram of the WA211P