Technical Description

The Equipment Under Test (EUT) is a portable 2.4GHz RF transceiver (Vehicle) of a RC Car system with 17 channels operating at 2410.875MHz ï 2464.875MHz MHz. The EUT is powered by a 9.0 V DC source (6 x 1.5V AA batteries). The EUT has an ON/OFF switch.

After switching ON the EUT and the transceiver (Controller) of the RC Car, the EUT can be controlled to move forward, backward left and right by the transceiver (Controller).

Modulation Type: GFSK
Antenna Type: Integral, Internal (PCB Trace)
Frequency Range: 2410.875MHz – 2464.875MHz, 17 channels
Antenna Type: Internal and integral
Antenna Gain: 0dBi
Nominal rated field strength: 101.9dBµV/m at 3m
Maximum allowed field strength of production tolerance: +/- 2dB

The functions of main ICs are mentioned below.

1. U4 (KA-2431-TA2) acts as 2.4GHz RF module.
2. U2 (CE6200A 18P) acts as power regulator.
3. U1 (acts as DC/DC converter.

2.4GHz RF module U3 (KA-2431-TA2):

1. U6 (SNRC13AFG) acts as MCU.
2. Y2 (12MHz) acts as clock for U6 (wireless processor)
3. U4 (XC6204-25) acts as regulator.
4. U1 (AP1110) acts as RF amplifier.
5. VT1 (2520) acts as band pass filter.
6. U5 (A7121IC) acts as radio core of 2.4GHz transceiver.
7. Y1 (18MHz) provides system clock for U5 (2.4GHz transceiver).

70436 频率表

1CH	2410.875
2CH	2414.25
3CH	2417.625
4CH	2421
5CH	2424.375
6CH	2427.75
7CH	2431.125
8CH	2434.5
9CH	2437.875
10CH	2441.25
11CH	2444.625
12CH	2448
13CH	2451.375
14CH	2454.75
15CH	2458.125
16CH	2461.5
17CH	2464.875

Document Title

2.4GHz GFSK Transceiver with 3Mbps

Revision History

Rev. No.	History	Issue Date	Remark
1.0	Transfer from AMIC. Modify ordering information.	Nov. 9th, 2005	Released
1.1	Revise Dimensions in Package Information	Apr. 28th, 2006	Released
1.2	AMICCOM LOGO Changed.	Oct. 5th, 2007	Released
1.3	Add final version logo, top marking info., reflow profile, Carry tape & reel dimensions	Jun. 26th, 2008	Released
1.4	Change English Company Name	Nov. 30, 2010	
1.5	Correct ordering information and remove A7122.	Jan. 06, 2011	

Important Notice:

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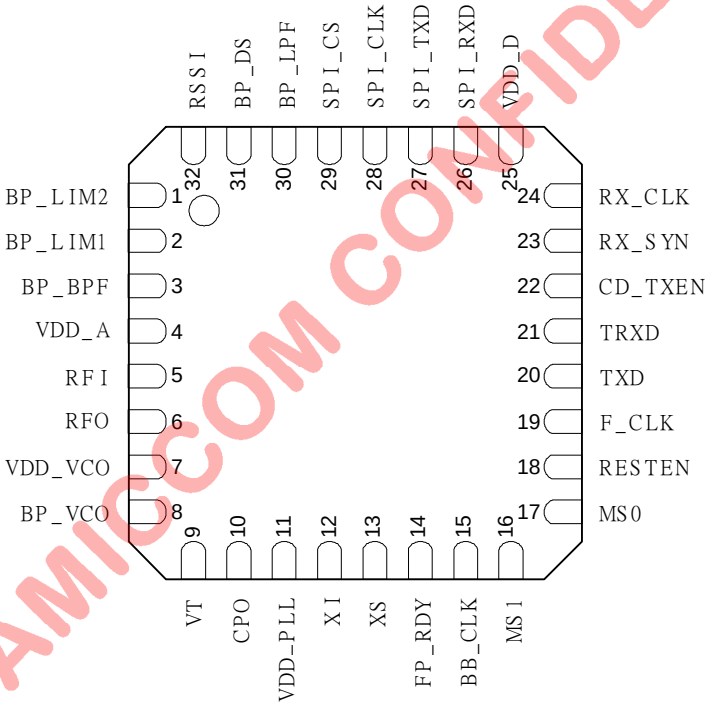
Typical Applications

- Wireless digital audio
- Wireless Mouse and Keyboard
- 2.4GHz ISM Band Communication System
- Wireless game pad
- Wireless toy

General Description

A7121 is a monolithic CMOS integrated circuit for wireless applications in 2.4GHz ISM band. The device is provided in a 32-lead plastic QFN5X5 packaging and is designed as a complete GFSK transceiver up to 3Mbps/ 1Mbps data rate. The chip features a fully programmable frequency synthesizer with integrated VCO circuitry.

Pin Configurations



A7121 QFN Package Top View

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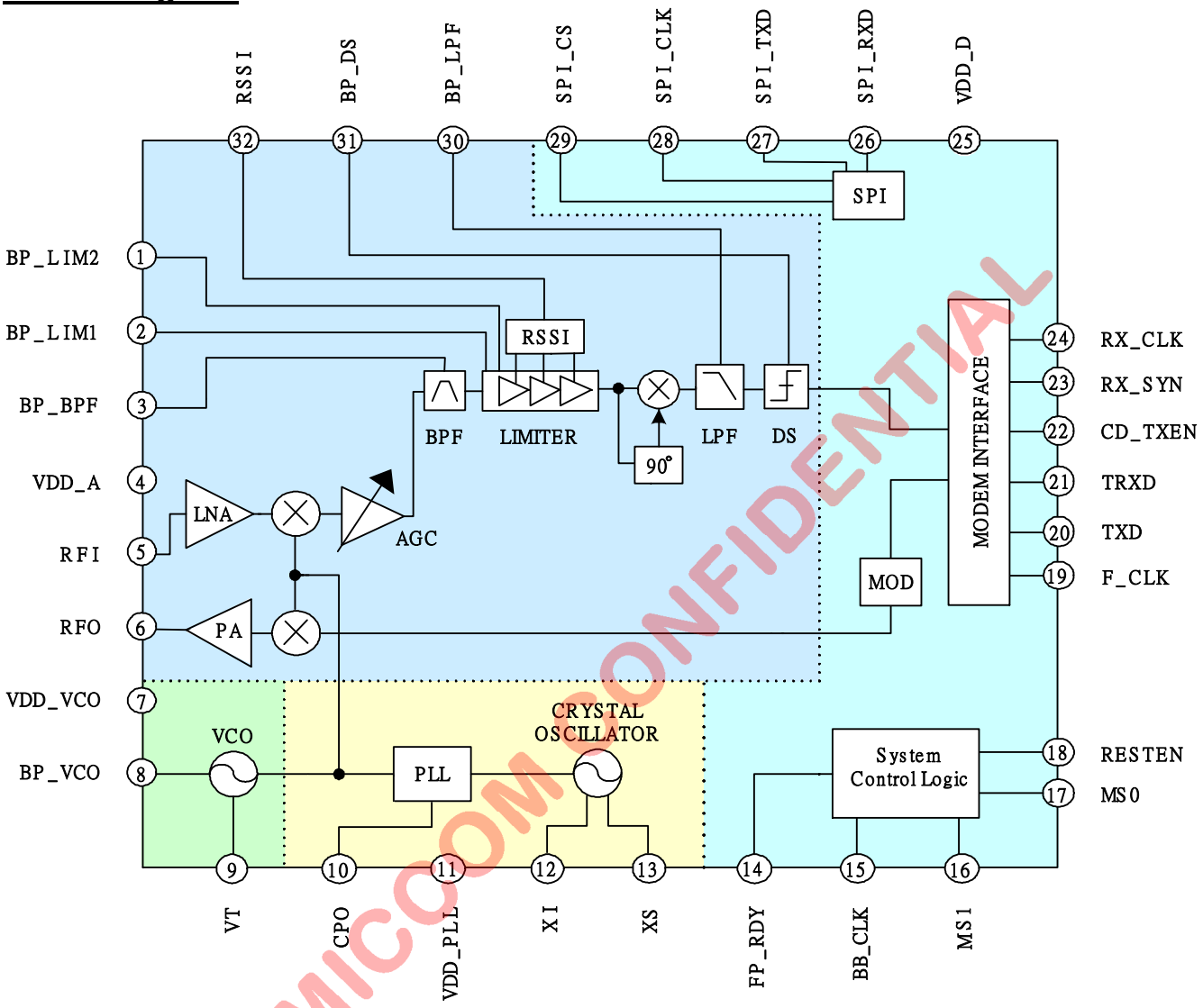
Block Diagram



System Block Diagram

Specification (Ta=25℃, VDD=2.5V, data rate= 3Mbps, TX data without Gaussian shaping unless otherwise noted.)

Parameter	Description	Minimum	Typical	Maximum	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage		2.25	2.5	2.75	V
Current Consumption	RX Mode		28		mA
Transceiver Circuit	TX Mode @0dBm output		34		mA
	TX Mode @-6dBm output		24		mA
	Synthesizer Mode		10		mA
	Standby Mode		1.5		mA
	Sleep Mode		2		μA
Phase Locked Loop					
X'TAL Settling Time			5		ms
X'TAL Frequency	@1M Mode [1]		4, 8, 12, 16, 20		MHz
	@3M Mode [1]		9,18		
VCO Operation Frequency			2400~2484		MHz
PLL Settling Time @settle to 20KHz	@ Loop BW = 30 KHz		150		μs
Transmitter					
TX Power	@ Maximum Power Setting		0	4	dBm
Power Control Range			6		dB
In-band Spurious	Adjacent Channel			-20	dBc
	Second Channel			-20	dBm
	≧Third Channel			-40	dBm
Out-band Spurious [2]	30MHz~1GHz			-36	dBm
(Operating Mode)	1GHz~12.75GHz			-30	
	1.8GHz~ 1.9GHz			-47	
	5.15GHz~ 5.3GHz			-47	
Frequency Deviation	@1M Mode		250		KHz
	@3M Mode		750		
TX Settling Time	@ Loop BW = 30 KHz		30		μs
Receiver					
Sensitivity @BER=0.001	@1M Mode		-85		dBm
	@3M Mode		-80		
IF Frequency	@1M Mode		2		MHz
	@3M Mode		4.5		
Image Rejection			20		dB
Maximum Input Power	@RF input			-20	dBm
Spurious Emission [2]	30MHz~1GHz			-57	dBm
	1GHz~12.75GHz			-47	
AGC Gain Control			0, 5, 15, 20		dB
RSSI Range	@RF input	-95		-55	dBm
RSSI Slope Accuracy	@RF input= -70 and –80 dBm		20		%
RX Settling Time	@ Loop BW = 30 KHz		30		μs

Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V

Note:

1. Data rate= 1Mbps @1M Mode, Data rate= 3Mbps @3M Mode.
2. With external RF filter that provides minimum 17dB of attenuation in the band: 30MHz ~ 2GHz and 3GHz ~12.75GHz.

Pin Descriptions (I: input; O: output; OD: open drain output)

Pin No.	Symbol	I/O	Function Description
1	BP_LIM2	O	Limiter bypass. Connect to one end of the external limiter bypass capacitor.
2	BP_LIM1	O	Limiter bypass. Connect to the other end of the external limiter bypass capacitor.
3	BP_BPF	O	BPF bypass. Connect to external capacitor.
4	VDD_A	I	Analog supply voltage input.
5	RFI	I	RF input.
6	RFO	O	RF output.
7	VDD_VCO	I	VCO supply voltage input.
8	BP_VCO	O	VCO bypass. Connect to external capacitor.
9	VT	I	VCO tuning voltage input. The VCO frequency increases as VT increases.
10	CPO	O	Charge-pump output. This pin charges external capacitor to adjust VCO frequency.
11	VDD_PLL	I	PLL supply voltage input.
12	XI	I	Colpitts crystal oscillator node 1. Connect to external feedback capacitor.
13	XS	I	Colpitts crystal oscillator node 2. Connect to external feedback capacitor.
14	FP_RDY	O	Multi-function pin of FIFO packet R/W complete or ready signal.
15	BB_CLK	O	Clock output.
16 17	MS1 MS0	I	Transceiver operation mode selection inputs. MS [1:0] = x0: Sleep mode. Transceiver circuit is turned off. MS [1:0] = 01: Standby mode. X'TAL oscillator is turned on. MS [1:0] = 11: TRX mode. Use **Mode control register** bit 3 (TRC) to select TX or RX mode.
18	RESETN	I	Digital circuit reset.
19	F_CLK	I	Clock for FIFO data.
20	TXD	I	TX data input.
21	TRXD	I/O	Input: TX data input. Output: RX data output.
22	CD_TXEN	I/O	Input: TX data modulation enable. Output: Carrier is detected.
23	RX_SYN	O	RX sync pulse output.
24	RX_CLK	O	RX data sampling clock output.
25	VDD_D	I	Digital supply voltage input.
26	SPI_RXD	I	SPI data input.
27	SPI_TXD	O	SPI data output.
28	SPI_CLK	I	SPI clock.
29	SPI_CS	I	SPI chip select.
30	BP_LPF	O	LPF bypass. Connect to external capacitor.
31	BP_DS	O	Data slicer reference bypass. Connect to external capacitor.
32	RSSI	O	Analog RSSI output.

Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 5.0	Vdc
Other I/O pins range	GND	-0.3 ~ VDD+0.3	Vdc
Maximum input RF level		0	dBm
Storage Temperature range		-55 ~ 125	°C

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions.
*Device is Moisture Sensitivity Level III (MSL 3).

State Description

1. A7121 State:

The state machine inside the chip controls the A7121 GFSK transceiver operation. During normal operation, the A7121 is in one of five states (i.e., SLEEP, STBY, RADIO, CAL, TEMP). The state diagram is shown in Figure 1 below.

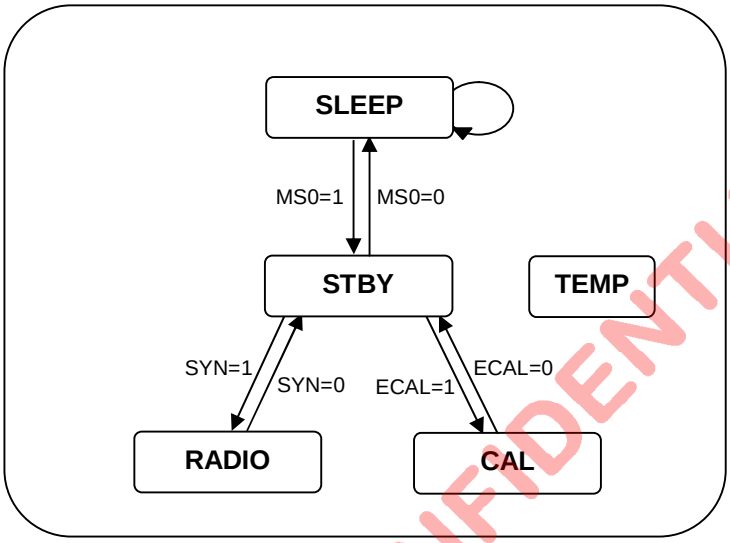


Figure 1: A7121 State Diagram

The A7121 transceiver will enter the SLEEP (Sleep) state when it is powered up or reset and input pin MS0 is "0". The analog circuit power and crystal oscillator clock will be turned off in the SLEEP state. Hence, there is no useable clock output (i.e., BB_CLK output pin) in the SLEEP state. When the input pin MS0 goes to "1" from "0", the state will be changed to the STBY (Standby) state. The crystal oscillator will start in the STBY state and the output clock pin will also be active. But the analog circuit power stays off in the STBY state. When the MS0 goes to "0", the state will go back to the SLEEP state. The A7121 transceiver will return to the SLEEP state if the MS0 is set to "0" at any moment.

2. TEMP State:

The A7121 must be in the TEMP (Temperature measurement) state to do temperature measurement as shown in Figure 1. The TEMP state is an independent state. It may execute temperature measurement in the TEMP state simultaneously when the transceiver is in other state (except the SLEEP state) for doing some thing. For doing temperature measurement, there are some configurations must be set. First, the EXDR bit (**Mode control register** bit 8) must be set to 1. The ET bit (**Calibration control register** (I) bit 0) for enabling temperature measurement must be set to "1" to enter the TEMP state. After the measurement is done, the ET bit will be set to "0" automatically and the transceiver will leave the TEMP state. The state transition to the TEMP state will postpone if the calibration process or RSSI measurement is executing. Similarly, the state transition of the CAL state or the RSSI sub-state will delay until the temperature measurement is done.
The following figure is RSSI measurement timing.

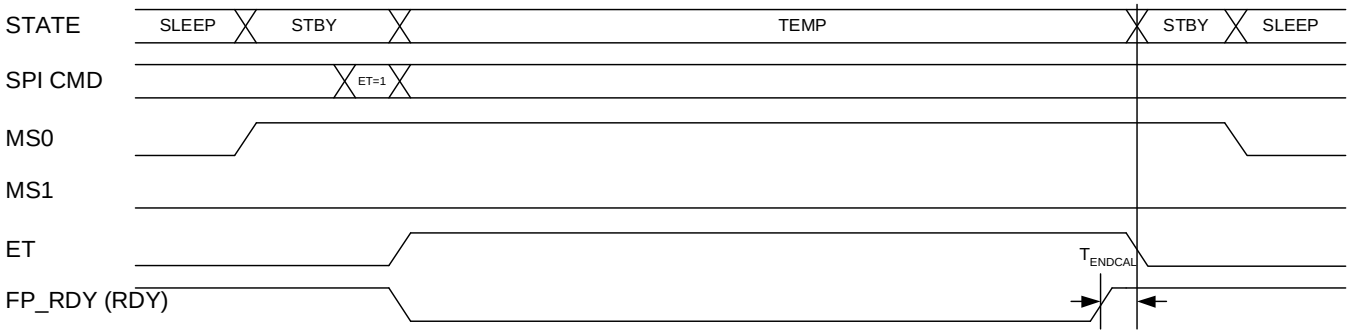


Figure 2: Temperature Measurement State Timing

3. RADIO State:

The RADIO (Radio) state has four sub-states: SYN (Synthesizer), RX (Receiver), TX (Transmitter), and RSSI (RSSI measurement). The entrance and exit sub-state of the RADIO state is the SYN sub-state. The SYN sub-state can be entered only from the STBY state when the SYN bit (**Mode control register** bit 2) is set to "1" and the input pin MS1 is "0". At the same time, the ECAL (**Calibration control register** (II) bit 1) bit must be reset to "0", that is, the calibration process is done or there is no calibration needed. If the ECAL is set to "1", the state transition to the RADIO state by setting the SYN bit will take effect until the ECAL bit reset manually or automatically. The sub-state diagram is shown in Figure 3.

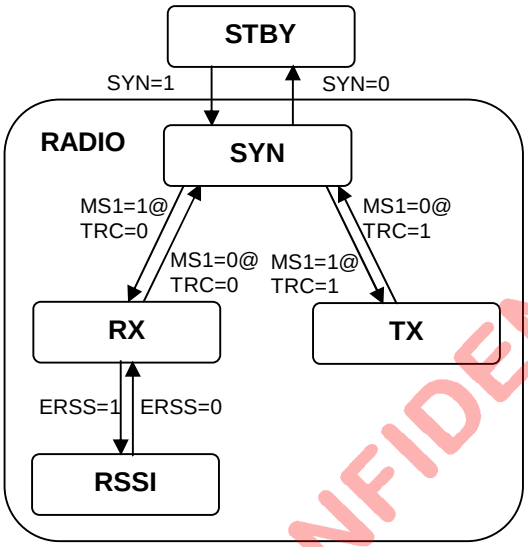


Figure 3: RADIO State Sub-state Diagram

The frequency synthesizer will be powered up in SYN sub-state and stay active until leaving the RADIO state. By pulling the MS1 to "1", The A7121 transceiver will go to RX or TX sub-state according to the TRC bit (**Mode control register** bit 3) status. If the TRC bit is "0", the transceiver will be in RX sub-state. If the TRC bit is "1", the transceiver will be in TX sub-state. In RX sub-state, the power of receiver chain will be turned on and the transmitter will be turned off. The transmitter will be powered up in TX sub-state and the receiver power will be switched off simultaneously. The RX and TX sub-states cannot jump to each other directly. It must pass to SYN sub-state first for RX to TX transition and vice versa. It will return to SYN sub-state from RX or TX sub-state by setting the MS1 to "0".

The following received burst-timing figure shows the relationship between the states and some control signals as an example.

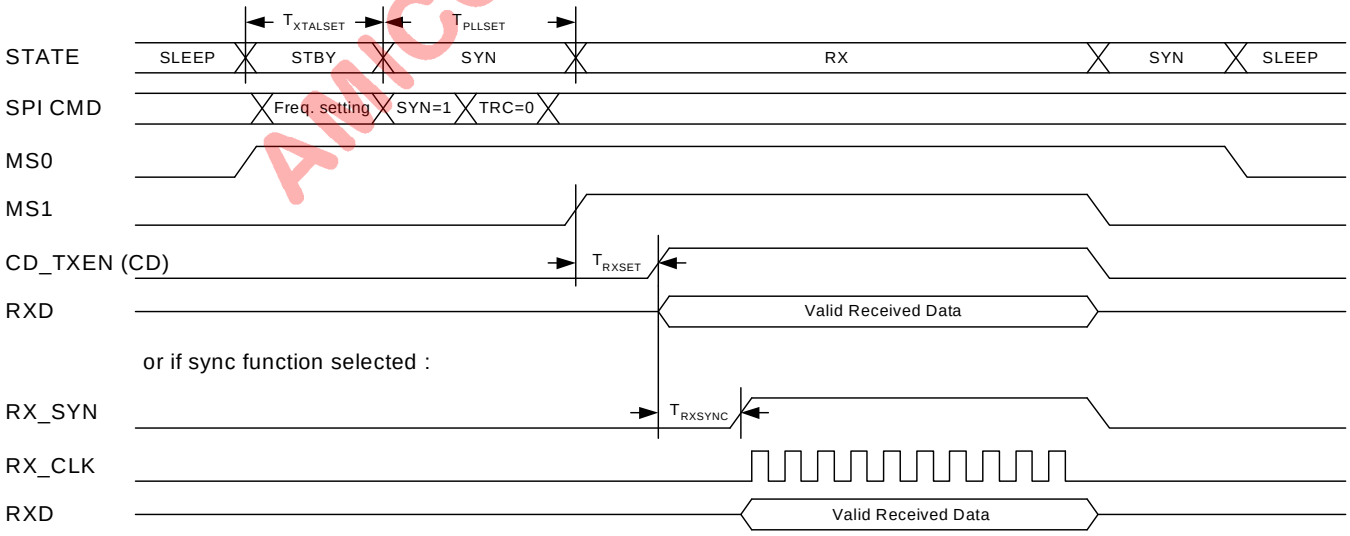


Figure 4: Receive Burst Timing

The following transmitted burst-timing figure shows the relationship between the states and some control signals as an example.

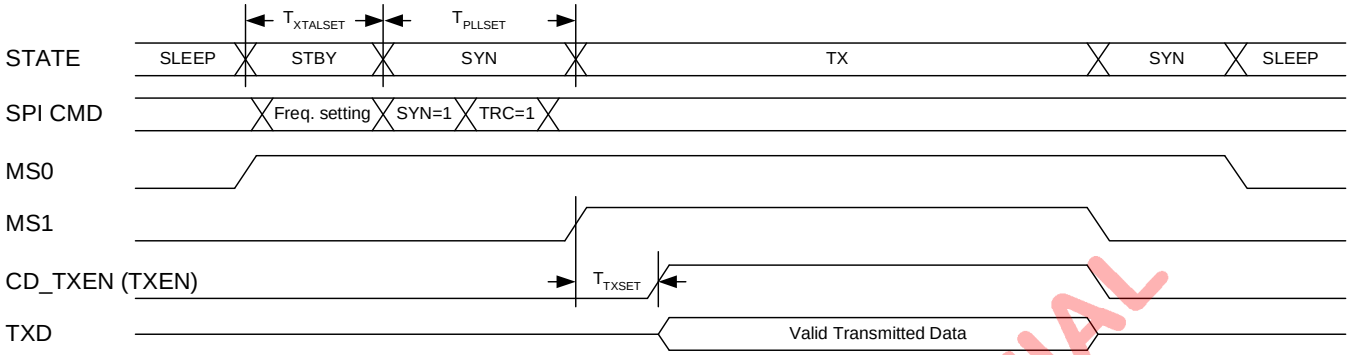


Figure 5: Transmit Burst Timing

The following figure shows the continuous transmitting and receiving data timing.

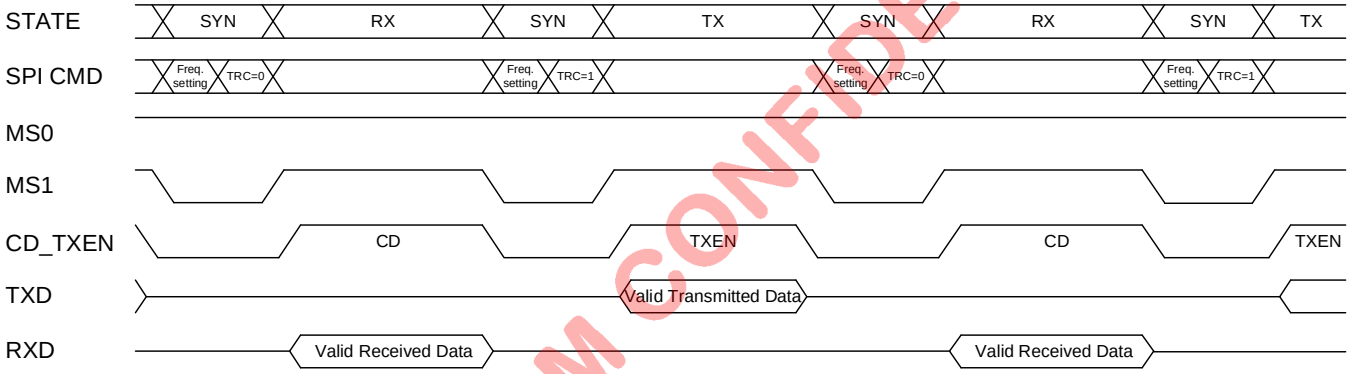


Figure 6: Continuous Bi-directional State Timing

When doing the RSSI measurement, it must be in RX sub-state and some configurations must be set. First, the EXDR bit (**Mode control register** bit 8) must be set to 1. When the RSS1 bit (**Calibration control register** (I) bit 2) is set to "0", the RSSI measurement will be executed automatically according to the RX_SYN or F1P of FP_RDY signals status. If the RSS1 bit is set to "1", the execution of RSSI measurement will depend on the setting of ERSS bit (**Calibration control register** (II) bit 2). If ERSS command's assertion is not in the RX sub-state, the A7121 transceiver will move into the RSSI state when next movement to the RX sub-state takes place unless it is reset first. After finishing the RSSI measurement, it will go back to RX sub-state automatically.
The following figure is RSSI measurement timing.

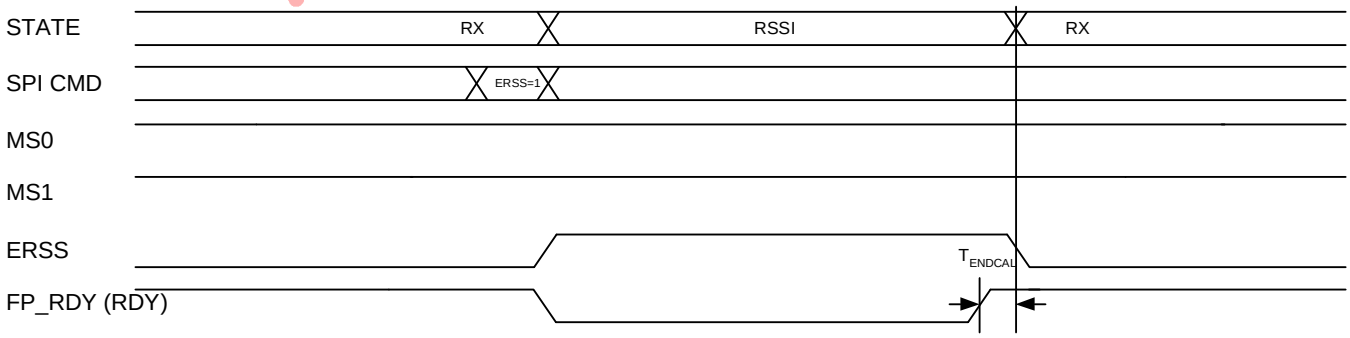


Figure 7: RSSI Measurement State Timing

4. CAL State:

There are five sub-states in the CAL (Calibration) state: IFCAL (IF filter calibration), DFCAL (Data filter calibration), DEMCAL (Demodulator calibration), RHCAL (RSSI slope calibration @RH_{REF}) and RLCAL (RSSI slope calibration @RL_{REF}) where RH_{REF} and RL_{REF} are two internal sources for RSSI slope calibration. The following is the sub-state diagram of the CAL state.

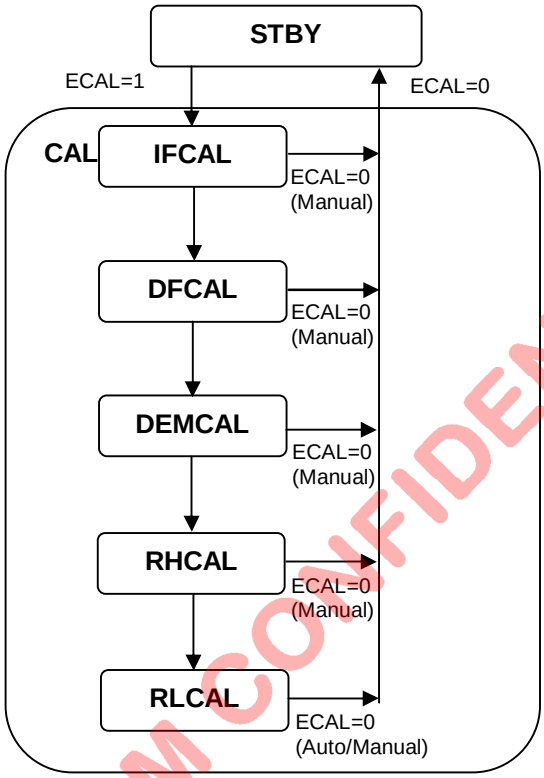


Figure 8: CAL State Sub-state Diagram

Before calibration, the EXIR and EXDR bits (**Mode control register** bit [9:8]) must be set to 1.By setting the ECAL bit to "1" in the STBY state, the A7121 transceiver will move into the CAL state. If ECAL command's assertion is not in the STBY state, the A7121 transceiver will move into the CAL state when next movement to the STBY state takes place unless it is reset first. Two registers must be configured, the **Calibration control register** (I) and (II), for starting the calibration process. The bits 4 to 8 of the **Calibration control register** (I) must be set first. These bits are the selection of which calibrations are going to be executed. They may be set to all "1" to calibrate all five items. Or some of them (one or more) should be set to "1" to calibrate one or more items. Then the command of calibration, the ECAL bit of the **Calibration control register** (II), must be set to "1". The five sub-states will do its specific calibration in turn. The first sub-state is the IFCAL sub-state that does the intermediate frequency filter bandwidth and center frequency calibration. The second is the DFCAL that calibrates the data filter bandwidth and center frequency. The next sub-state is the DEMCAL that calibrates the demodulator center frequency. The RHCAL sub-state calibrates the RSSI slope (@RH_{REF}) and the last one is RLCAL that calibrates the RSSI slope (@RL_{REF}). If some of the bits 4 to 8 of the **Calibration control register** (I) are not issued, the corresponding calibrations will be bypassed. It must be paid attention that the IFCAL and the DFCAL must have been executed correctly before executing the DEMCAL alone and the IFCAL must have been executed correctly before executing the RHCAL or the RLCAL alone.

When finishing the calibration process, the ECAL bit will be reset to "0" automatically in normal case and the state machine will go back to the STBY state. But it may happen that the calibration process halts and the state machine stays in an unknown sub-state. To escape from the halt situation, the ECAL bit should be set to "0" manually and the all sub-states will be reset. At this time, the state machine will also go back to the STBY state.

The following figure shows the calibration state timing as an example

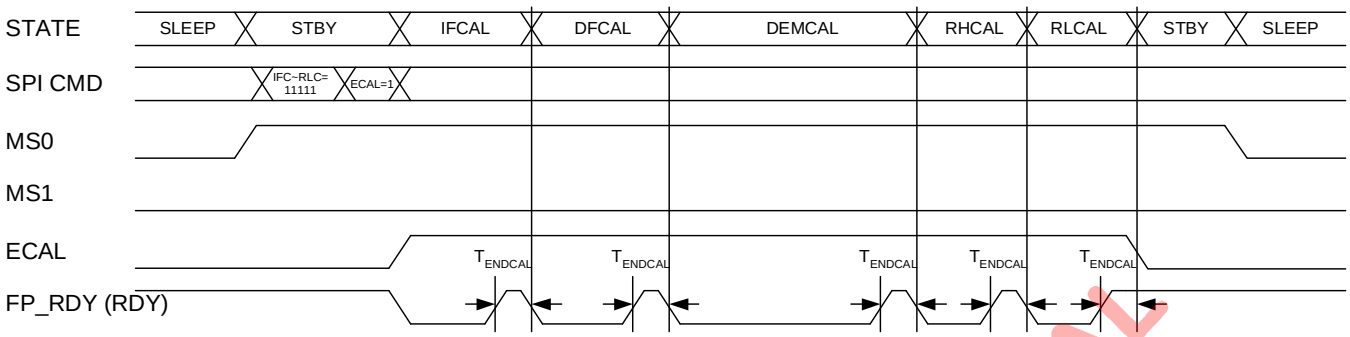


Figure 9: Calibration State Timing

5. Timing specification:

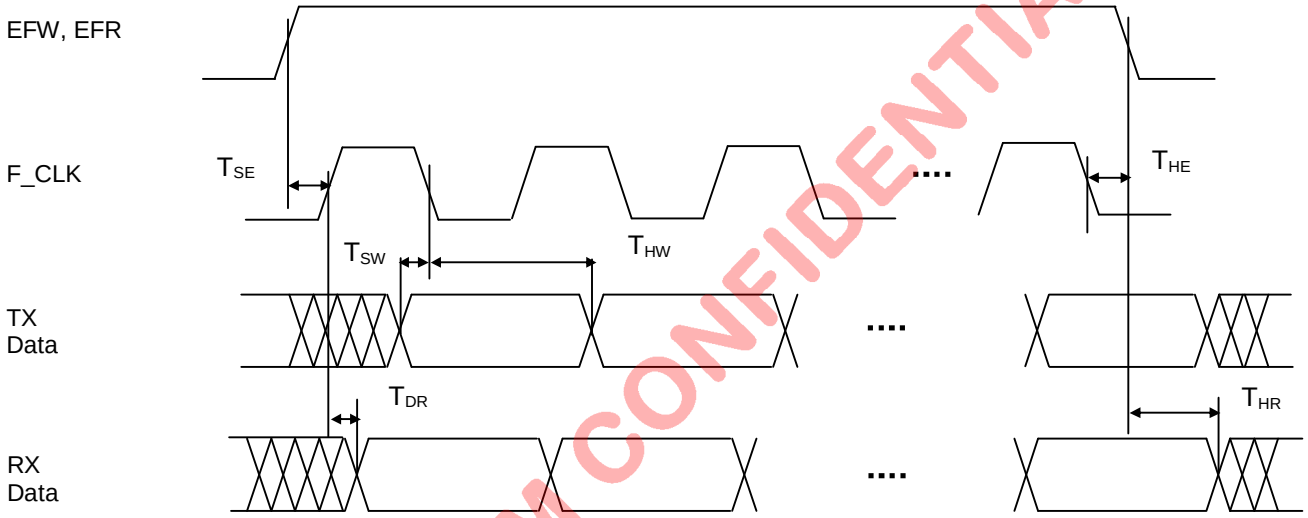
Parameter	Description	Min.	Max.	Unit
$T_{XTALSET}$	Crystal oscillator settling time	5		ms
T_{PLLSET}	PLL settling time	150		μs
T_{RXSET}	RX settling time.	30		μs
T_{RXSYNC}	RX synchronization time.	72		bit
T_{TXSET}	TX settling time.	30		μs
T_{ENDCAL}	Calibration ending time.	12		bit

The bit period differs between 1MHz mode and 3MHz mode. It is 1 μs in 1MHz mode and 1/3 μs in 3MHz.

FIFO Timing

This chip contains two 64 byte FIFO, TX FIFO and RX FIFO, for transmitting data (TX Data) and receiving data (RX Data). One can use **FIFO control register** bit 2 (EFW) and bit 4 (EFR) to enable TX FIFO and RX FIFO respectively. After enabled, TX Data will be written into TX FIFO at the negative edge of F_CLK pin and RX Data will be read out at the positive edge of F_CLK pin.
One can use FIFO byte counter (FBC [5:0]) in **FIFO control register** to set one packet size. When FIFO is disabled or one packet data is written/read to TX/RX FIFO respectively, the FIFO pointer will be reset to FIFO address zero.

1. Timing chart:



2. Timing specification:

Parameter	Description	Min.	Max.	Unit
F_C	FIFO clock frequency.		3	MHz
T_{SE}	Enable setup time.	50		ns
T_{HE}	Enable hold time.	50		ns
T_{SW}	TX Data setup time.	50		ns
T_{HW}	TX Data hold time.	50		ns
T_{DR}	RX Data delay time.	0	100	ns
T_{HR}	RX Data hold time.	0		ns

Note:
1. After EFW/EFR active, the minimum setup time (T_{SE}) is required for the first clock (F_CLK) to be valid.
2. The above timing chart is for the non-inverted case of F_CLK, i.e., FCKI (**FIFO control register** bit 1) = 0. If FCKI = 1, the inverted clock of the input F_CLK pin should meet the above timing.

SPI

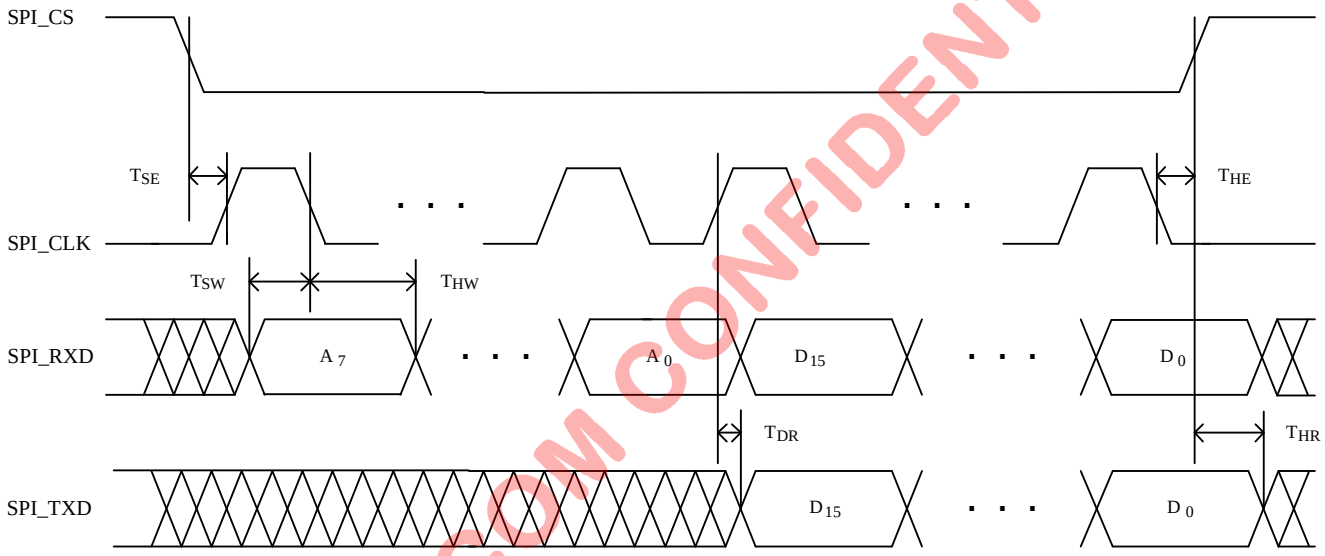
1. SPI format:

When SPI_CS is asserted, it follows one address byte (8 bits) and one data word (16 bits) that are clocked by the SPI_CLK. The format is shown below.

Address byte (8bits)								Data word (16 bits)															
R/W	Address					Reserved		Data															
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The address byte further contains three parts:
Bit 7: R/W command. 0: read from slave register, 1: write to slave register.
Bit [6:2]: Register address. It maps to register address [00000] ~ [11111].
Bit [1:0]: Reserved. Fill [00] for normal operation.

2. Timing chart:



3. Timing specification:

Parameter	Description	Min.	Max.	Unit
F_C	SPI clock frequency.		4	MHz
T_{SE}	SPI_CS setup time.	50		ns
T_{HE}	SPI_CS hold time.	50		ns
T_{SW}	SPI_RXD setup time.	50		ns
T_{HW}	SPI_RXD hold time.	50		ns
T_{DR}	SPI_TXD delay time.	0	100	ns
T_{HR}	SPI_TXD hold time.	0		ns

Note:
1. After SPI_CS active, the minimum setup time (T_{SE}) is required for the first clock (SPI_CLK) to be valid.

Register

Note: If register has reset value, it will be reset when RESETN pin or **Mode control register** bit 0 (RSTN) is low.

Address 00 (00000): Synthesizer register (I)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BNK2	BNK1	BNK0	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0	MA4	MA3	MA2	MA1	MA0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset																

MA [4:0]: Synthesizer A counter.
MB [7:0]: Synthesizer B counter (low byte).
BNK [2:0]: VCO Bank. VCO frequency increases when BNK decreases.

Address 01 (00001): Synthesizer register (II)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVT1	DVT0		CP2	CP1	CP0	VTH2	VTH1	VTH0	R6	R5	R4	R3	R2	R1	R0
R/W	R	R		W	W	W	W	W	W	W	W	W	W	W	W	W
Reset																

R [6:0]: Synthesizer R counter.
Compare frequency = Crystal frequency / R.
RF carrier frequency= (3/2) * (Crystal frequency / R) * (32 * MB + MA).
VTH [2:0]: VT low threshold (VTHL) and high threshold (VTHH) setting for VCO calibration.
[000]: VTHL = 0.3V, VTHH = 1.7V.
[001]: VTHL = 0.5V, VTHH = 1.5V.
[010]: VTHL = 0.6V, VTHH = 1.4V.
[011]: VTHL = 0.5V, VTHH = 1.3V.
[100]: VTHL = 0.3V, VTHH = 1.5V.
[101]: VTHL = 0.3V, VTHH = 1.7V.
[110]: VTHL = 0.6V, VTHH = 1.2V.
[111]: VTHL = 0.3V, VTHH = VDD-0.7.
CP [1:0]: Charge pump current setting. Fill [10] for normal operation. The charge pump current is 500uA under this setting.
CP [2]: Fill 0 for normal operation.
DVT [1:0]: Digital VT output. When VCO calibration is on, the VT of VCO will be compared with VT threshold set by VTH.
[00]: VT< VTHL< VTHH.
[01]: VTHL< VT< VTHH.
[10]: Not used.
[11]: VTHL< VTHH< VT.

Address 02 (00010): System clock register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		XIR4	XIR3	XIR2	XIR1	XIR0	XDR4	XDR3	XDR2	XDR1	XDR0	XBR4	XBR3	XBR2	XBR1	XBR0
R/W		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset												1	1	1	1	1

XBR [4:0]: Crystal frequency to output base band clock frequency ratio (binary format).
Output frequency= Crystal frequency / (XBR+1).
XDR [4:0]: Crystal frequency to data rate ratio (binary format).
Output frequency = Crystal frequency / (XDR+1).
XIR [4:0]: Crystal frequency to IF frequency ratio (binary format).
Output frequency= Crystal frequency / (XIR+1).

Address 03 (00011): Mode control register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							EXIR	EXDR	EXBR	TRD	DR1	DR0	TRC	SYN	CE	RSTN
R/W							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	1	0	0	0	(0)	(0)	1	1

RSTN: Register reset. This bit is masked if RESETN pin is low. 0: reset.
CE: Chip enable. When the chip enters disable state, the reset value with parentheses () will be reset.
This bit is masked if MS0 pin is low. 1: enable.
SYN: Enable synthesizer. 1: enable.
TRC: TRX state command.

The chip will enter TX or RX state according to this command at MS1 pin positive edge and cannot enter TRX state if synthesizer is disabled. 0: RX, 1: TX.

DR [1:0]: Nominal date rate setting.
[00]: Inhibited.
[01]: 1Mbps.
[10]: Inhibited.
[11]: 3Mbps.

TRD: Bi-directional data selector for TRXD pin. 0: RX data only, 1: bi-directional TRX data.
EXBR: Base band clock enables. 1: enable.
EXDR: Internal data rate clock enables for IF calibration and RSSI and Temperature measurement. 1: enable.
EXIR: Internal IF clock enables for IF calibration. 1: enable.

Address 04 (00100): TX control register (I)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QA4	QA3	QA2	QA1	QA0	IA4	IA3	IA2	IA1	IA0	GF	DEV3	DEV2	DEV1	DEV0	TXDI
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset																

TXDI: Transmitter data invert. 1: invert. When TXDI= 1, a binary one TX data is represented by a positive frequency deviation.
DEV [3:0]: Frequency deviation (FDEV).
FDEV= Data rate * {0.5 * 127 * (8 + DEV [2:0]) * $2^{DEV\ [3]}$} / 4096. For example,
DEV [3:0]= [0010]: FDEV=155KHz @1M Mode, FDEV=465KHz @3M Mode.
DEV [3:0]= [0101]: FDEV=201KHz @1M Mode, FDEV=603KHz @3M Mode.
DEV [3:0]= [1000]: FDEV=248KHz @1M Mode, FDEV=744KHz @3M Mode.
GF: Gaussian filter enable. 1: enable.
IA [4:0]: I amplitude fine tuning. Recommend value= [11111].
QA [4:0]: Q amplitude fine tuning. Recommend value= [11111].

Address 05 (00101): TX control register (II)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IQC1	IQC0	QO3	QO2	QO1	QO0	IO3	IO2	IO1	IO0	PC5	PC4	PC3	PC2	PC1	PC0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset																

PC [5:0]: TX power control. Recommend value= [111111].
IO [3:0]: I offset tuning. Recommend value= [1000].
QO [3:0]: Q offset tuning. Recommend value= [1000].
IQC [1:0]: IQ amplitude course tuning. Recommend value= [11].
V_{AC}=6.279m * (33 + XA [4:0]) / $2^{\{2\ *\ (1-\ IQC\ [1])\ +\ (1-\ IQC\ [0])\}}$. X= I or Q. For example,
IA [4:0]= [11111], IQC [1:0]= [11], then V_{AC}=401.84mVpp.
QA [4:0]= [11111], IQC [1:0]= [10], then V_{AC}=200.92mVpp.
V_{DC}=3.164m * {7*(XO [3]-1) + XO [2:0]} / $2^{\{2\ *\ (1-IQC\ [1])\ +\ (1-IQC\ [0])\}}$. X= I or Q. For example,
IO [3:0]= [1000], IQC [1:0]= [11], then V_{DC} =0mV.
QO [3:0]= [1111], IQC [1:0]= [10], then V_{DC} =11.07mV.

Address 06 (00110): RX control register (I)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SYNI	DS2	DS1	DS0	RCP2	RCP1	RCP0	ETH2	ETH1	ETH0	DPC1	DPC0	RXDI
R/W				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	1	1	1	1	0	0	0	0

RXDI: Receiver data invert. 1: invert. When RXDI= 1, a positive frequency deviation is demodulated to a binary one RX data.
DPC [1:0]: Data process control.
[00]: Disable frame sync and FIFO. No data process.
[01]: Enable frame sync. RX output data is inactive (high) before sync.
[10]: Enable frame sync. No data process.
[11]: Enable frame sync and FIFO.
ETH [2:0]: Sync word error bit number threshold. Recommend value= [110].
RCP [2:0]: Shift RX data sampling clock position. The shift resolution is 1/8 data bit. Recommend value= [011].
DS [0]: Fill 0 for normal operation.

DS [2:1]: Data slicer reference voltage mode.
[00]: Inhibited.
[01]: Average mode before RX sync, off after RX sync.

[10]: Average mode.
[11]: Fix reference voltage mode.
SYNI: Sync signal invert. 1: invert.

Address 07 (00111): RX control register (II)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DFG2	DFG1	DFG0	VGA2	VGA1	VGA0
R/W											W	W	W	W	W	W
Reset											1	1	1	1	1	1

VGA [2:0]: IF VGA Gain.
[0xx]: 0 dB.
[10x]: 5 dB.
[110]: 15 dB.
[111]: 20 dB.
DFG [2:0]: Data filter Gain. Magnification = DFG + 1.

Address 08 (01000): FIFO control register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				FT	FBC5	FBC4	FBC3	FBC2	FBC1	FBC0	FRC	EFR	FWC	EFW	FCKI	FDS
R/W				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0							0	0	0	0	0	0

FDS: TX FIFO data select. 0: TXD pin, 1: SPI_RXD pin.
FCKI: FIFO clock invert. 1: invert.
EFW: Enable TX FIFO write. 1: enable.
FWC: Write TX FIFO packet control. 0: write one packet (FBC+1 byte). 1: write continuously.
EFR: Enable RX FIFO read. 1: enable.
FRC: Read RX FIFO packet control. 0: read one packet (FBC+1 byte). 1: read continuously.
FBC [5:0]: FIFO byte counter. Byte number= FBC + 1.
FT: FIFO test mode. TX FIFO data will be written to RX FIFO in test mode. 1: test mode.

Address 09 (01001): Access code register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TAC7	TAC6	TAC5	TAC4	TAC3	TAC2	TAC1	TAC0	RAC7	RAC6	RAC5	RAC4	RAC3	RAC2	RAC1	RAC0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset																

RAC [7:0]: Access code for RX.
TAC [7:0]: Access code for TX.
The access code is 9 bytes (72 bits) containing 4 bits preamble in LSB, 64 bits sync word and 4 bits trailer in MSB. After reset, the access code (from LSB to MSB) is written to internal table (address from 0 to 8) by this register cyclically. In FIFO mode, the LSB (bit TAC7 of internal table address 0) of TX access code will be transmitted first.

Address 0A (01010): Thermometer register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	T7	T6	T5	T4	T3	T2	T1	T0								
R/W	R	R	R	R	R	R	R	R								
Reset																

T [7:0]: 8-bit thermometer output. This value increases when temperature increases.
The temperature slope is around 2 ℃ / LSB.

Address 0B (01011): RSSI register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSSI7	RSSI6	RSSI5	RSSI4	RSSI3	RSSI2	RSSI1	RSSI0								
R/W	R	R	R	R	R	R	R	R								
Reset																

RSSI [7:0]: Digital RSSI output. This value increases when input power decreases.
V_{RSSI}= 0.2 + 1.6 * RSSI [7:0] / 256.

Address 0C (01100): Calibration control register (I)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TR	RSSR	IFR	DFR	DEMR	RHR	RLR	RLC	RHC	DEMC	DFC	IFC	MCAL	RSS1	RSS0	ET

R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	(1)	(1)	(1)	(1)	(1)	(1)	(1)	0	0	0	0	0	0	0	0	(0)

ET: Enable temperature measurement. After set, it will be reset automatically when temperature measurement is done.
RSS [1:0]: Start signal selector of RSSI measurement.
[00]: after RX FIFO receives one packet data.
[01]: after RX sync is active.
[1X]: after **Calibration control register** (II) bit 2 (ERSS) is set.
MCAL: Manual setting of Calibration registers (**IF filter, Data filter, Demodulator, RH and RL register**).
0: auto setting, 1: manual setting.
IFC: IF filter calibration command. 1: set calibration.
DFC: Data filter calibration command. 1: set calibration.
DEMC: Demodulator calibration command. 1: set calibration.
RHC: RSSI slope calibration (@RH_{REF}) command. 1: set calibration.
RLC: RSSI slope calibration (@RL_{REF}) command. 1: set calibration.
IFC ~ RLC commands will be executed when set and **Calibration control register** (II) bit 1 (ECAL)= 1.
RLR: RSSI slope calibration (@RL_{REF}) ready. 1: ready.
RHR: RSSI slope calibration (@RH_{REF}) ready. 1: ready.
DEMR: Demodulator calibration ready. 1: ready.
DFR: Data filter calibration ready. 1: ready.
IFR: IF filter calibration ready. 1: ready.
RLR ~ IFR will be pulled low when associated calibration is set and **Calibration control register** (II) bit 1 (ECAL)= 1 and pulled high when associated calibration is done.
RSSR: RSSI measurement ready. It will be pulled low when **Calibration control register** (II) bit 2 (ERSS)= 1 and pulled high when RSSI measurement is done. 1: ready.
TR: Temperature measurement ready. It will be pulled low when ET= 1 and pulled high when temperature measurement is done. 1: ready.

Address 0D (01101): Calibration control register (II)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TAD2	TAD1	TAD0							RR0	TADB	FPRI	FPRS	ERSS	ECAL	ETR
R/W	R	R	R							RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	(0)	(0)	(1)

ETR: Enable TRX state. This bit is masked if MS1 pin is low. 1: enable.
ECAL: Enable calibration. After set, it will be reset automatically when all calibration process is finished. 1: enable.
ERSS: Enable RSSI measurement. After set, it will be reset automatically when RSSI measurement is done. 1: enable.
FPRS: Selector of FIFO packet/ready multi-function pin. 0: packet indictor output, 1: ready indictor output.
FPRI: FIFO packet/ready signal invert. 1: invert.
TADB: Fill 0 for normal operation.
RR0: Reserved. Fill 0 for normal operation.
TAD [2:0]: Reserved.

Address 0E (01110): ADC sampling clock register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	ADC3	ADC2	ADC1	ADC0
R/W				W	W	W	W	W	W	W	W	W	W	W	W	W
Reset																

ADC [1:0]: ADC sampling clock setting for demodulator calibration. Recommend value= [11].
F_S= IF frequency / $2^{(ADC\ [1:0]\ +\ 1)}$.
ADC [3:2]: Fill [00] for normal operation.
AD [8:0]: ADC sampling clock delay time. Where
AD [2:0]: Temperature and RSSI measurement clock delay. Recommend value= [000]. Delay time=4us * $2^{AD\ [2:0]}$.
AD [5:3]: BPF, LPF and demodulator calibration clock delay. Recommend value= [011]. Delay time=30us * $2^{AD\ [5:3]}$.
AD [8:6]: RH and RL calibration clock delay. Recommend value= [011]. Delay time=32us * $2^{AD\ [8:6]}$.

Address 0F (01111): IF filter register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IFF7	IFF6	IFF5	IFF4	IFF3	IFF2	IFF1		IFF7	IFF6	IFF5	IFF4	IFF3	IFF2	IFF1	
R/W	R	R	R	R	R	R	R		W	W	W	W	W	W	W	
Reset																

IFF [7:1]: IF filter register.

Address 10 (10000): Data filter register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DF7	DF6	DF5	DF4	DF3	DF2	DF1		DF7	DF6	DF5	DF4	DF3	DF2	DF1	
R/W	R	R	R	R	R	R	R		W	W	W	W	W	W	W	
Reset																

DF [7:1]: Data filter register.

Address 11 (10001): Demodulator register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEM7	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0	DEM7	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W
Reset																

DEM [7:0]: Demodulator register.

Address 12 (10010): RH register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RH15	RH14	RH13	RH12	RH11	RH10	RH9	RH8	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W
Reset																

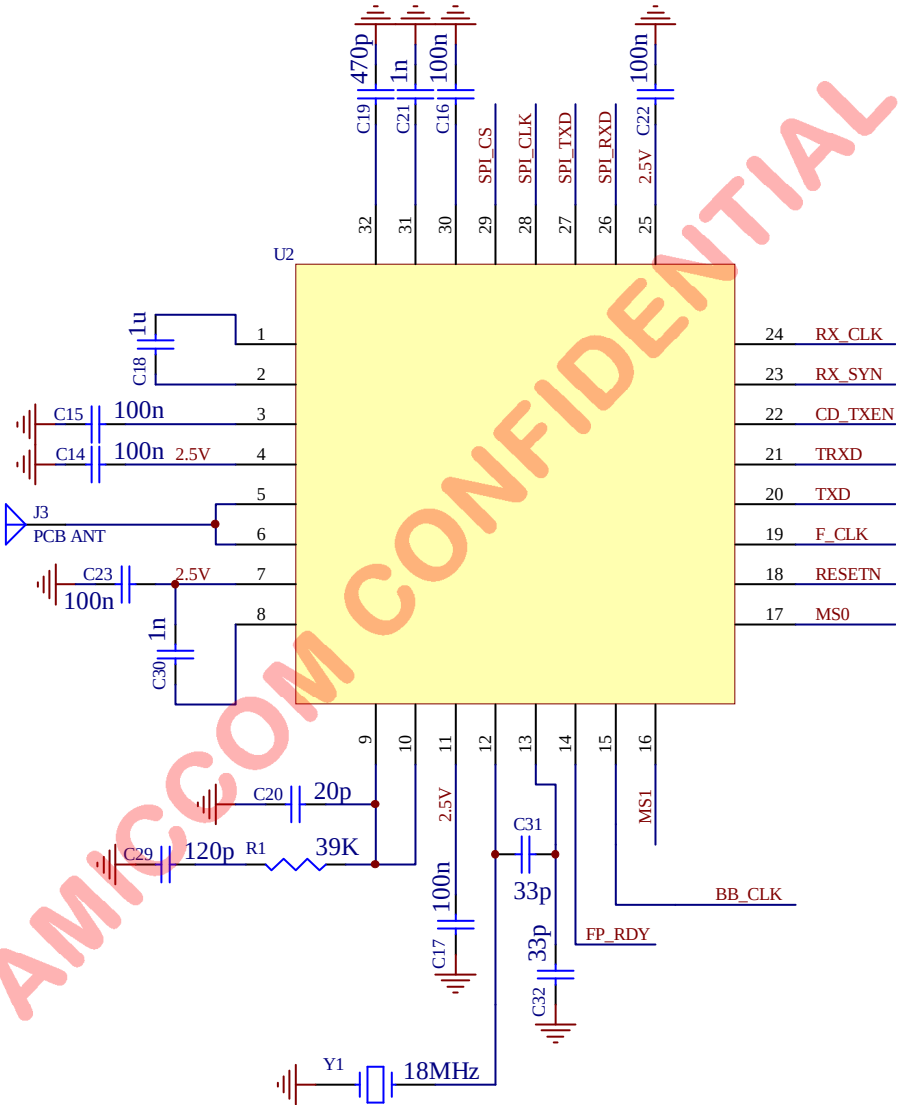
RH [7:0]: RSSI high threshold register. It will be overwritten by RH [15:8] during RSSI slope calibration (@RH_{REF}).
RH [15:8]: RSSI slope calibration register (@RH_{REF}).

Address 13 (10011): RL register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RL15	RL14	RL13	RL12	RL11	RL10	RL9	RL8	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W
Reset																

RL [7:0]: RSSI low threshold register. It will be overwritten by RL [15:8] during RSSI slope calibration (@RL_{REF}).
RL [15:8]: RSSI slope calibration register (@RL_{REF}).

Application Circuit



A7121 application circuit

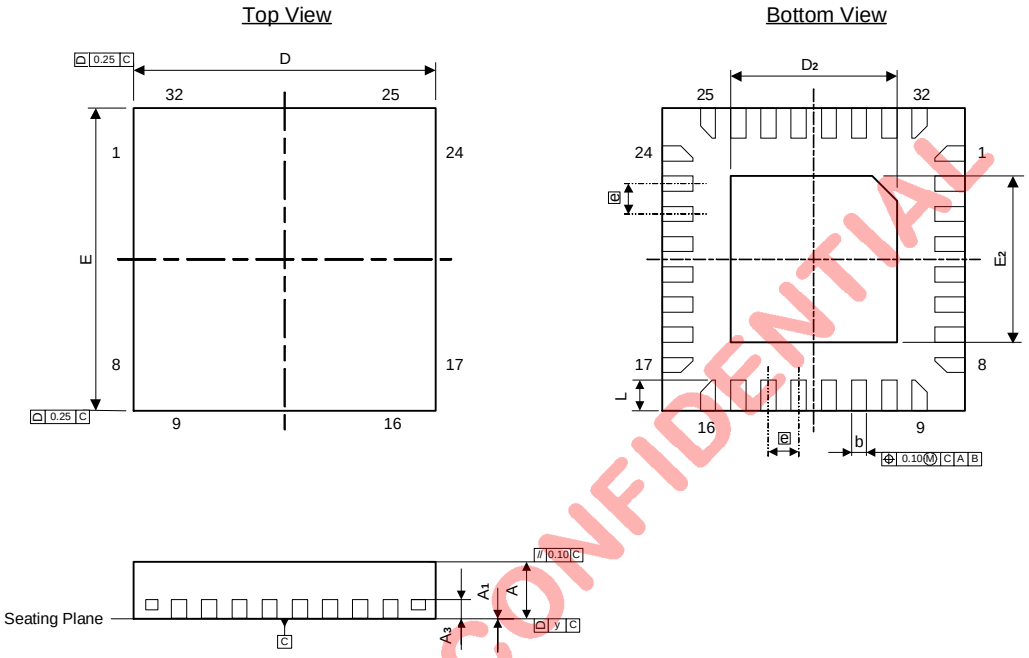
Ordering Information

Part No.	Package	Units Per Reel / Tray
A71C21AQF/Q	QFN32L, Tape & Reel, PB free, -40℃～85℃	3K
A71C21AQF	QFN32L, Tray, PB free, -40℃～85℃	490EA
A71C21AH	Die form, -40℃～85℃	100EA

Package Information

QFN 32L Outline Dimensions

unit: inches/mm

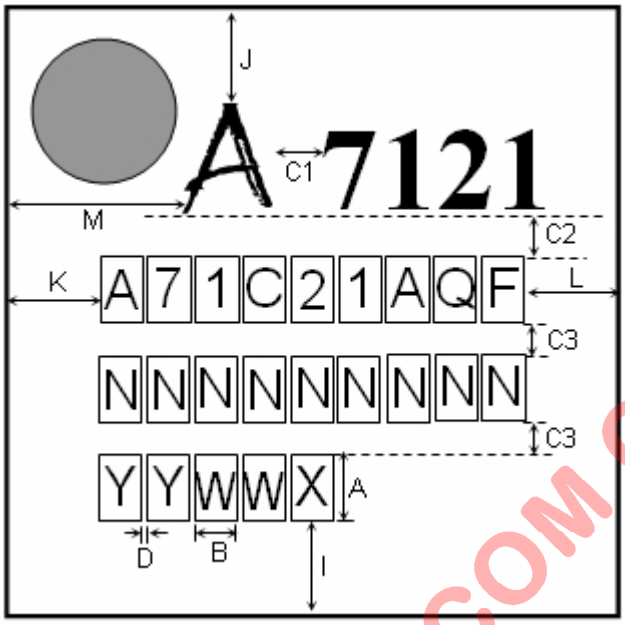


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.036	0.70	0.75	0.90
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3	0.010 REF			0.20 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.193	0.197	0.200	4.90	5.00	5.10
D_2	0.049	0.106	0.141	1.25	2.70	3.60
E	0.193	0.197	0.200	4.90	5.00	5.10
E_2	0.049	0.106	0.141	1.25	2.70	3.60
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50
y	0 - 0.004			0 - 0.10		

Top Marking Information

A71C21AQF

- Part No. : **A71C21AQF**
- Pin Count : **32**
- Package Type : **QFN**
- Dimension : **5*5 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**
- Remark : **Pb Free Type**



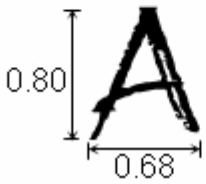
A : 0.55
B : 0.36
C1 : 0.25 **C2 : 0.3** **C3 : 0.2**
D : 0.03
M : 1.5

I=J
K=L

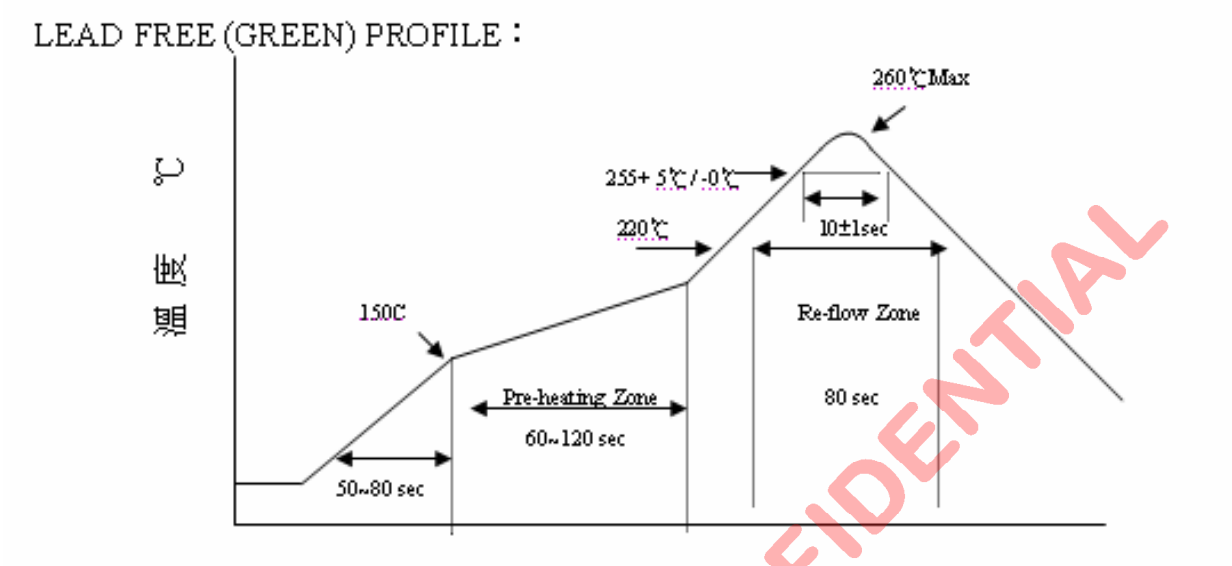
YYWW : DATECODE

X : PKG HOUSE ID

NNNNNNNNN : LOT NO.
(max. 9 characters)

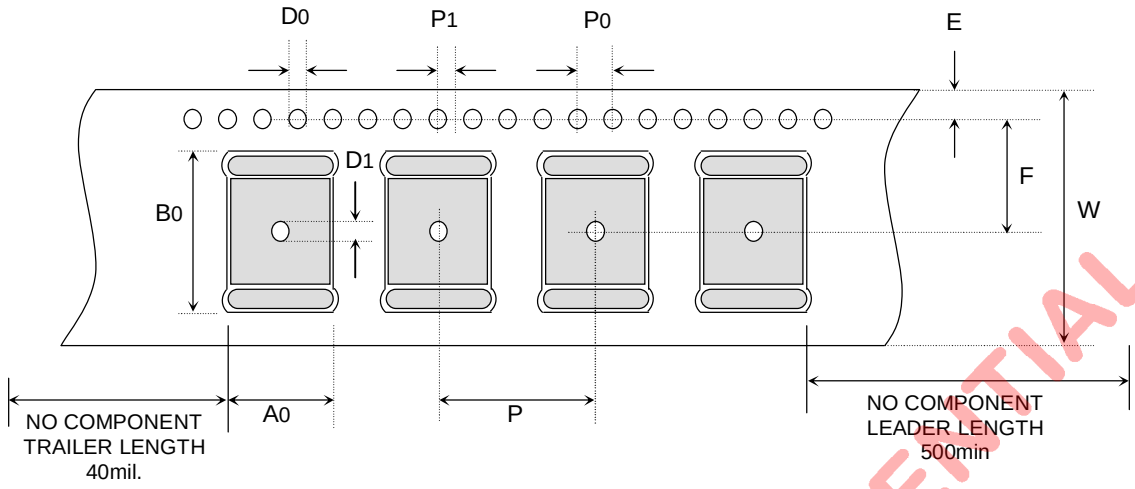


Reflow Profile



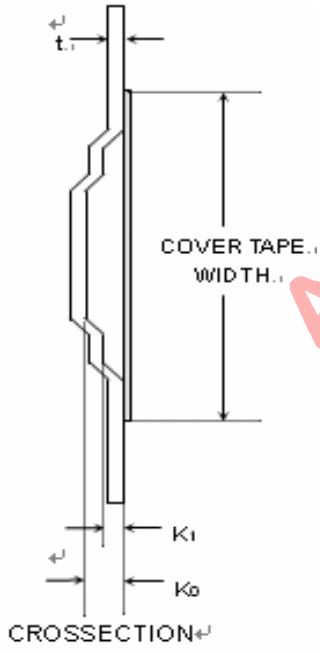
Actual Measurement Graph

Cover / Carrier Tape Dimension



11 EA IC **60cm±4cm**

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W
20 QFN 4*4	8	4.35	4.35	4.0	2.0	1.5	1.5	1.75	5.5	12
24 QFN 4*4	8	4.4	4.4	4.0	2.0	1.5	1.5	1.75	5.5	12
32 QFN 5*5	8	5.25	5.25	4.0	2.0	1.5	1.5	1.75	5.5	12
48 QFN 7*7	12	7.25	7.25	4.0	2.0	1.5	1.5	1.75	7.5	16
DFN-10	4	3.2	3.2	4.0	2.0	1.5	-	1.75	1.9	8
20 SSOP	12	8.2	7.5	4.0	2.0	1.5	1.5	1.75	7.5	16
24 SSOP	12	8.2	8.8	4.0	2.0	1.5	1.5	1.75	7.5	16
28 SSOP (150mil)	8	6	10	4.0	2.0	1.5	1.5	1.75	7.5	16



TYPE	K0	K1	t
20 QFN (4X4)	1.1	-	0.3
24 QFN (4X4)	1.4	-	0.3
32 QFN (5X5)	1.1	-	0.3
48 QFN (7X7)	1.1	-	0.3
DFN-10	0.75	-	0.25
20 SSOP	2.5	-	0.3
24 SSOP	2.1	-	0.3
28 SSOP (150mil)	2.5	-	0.3

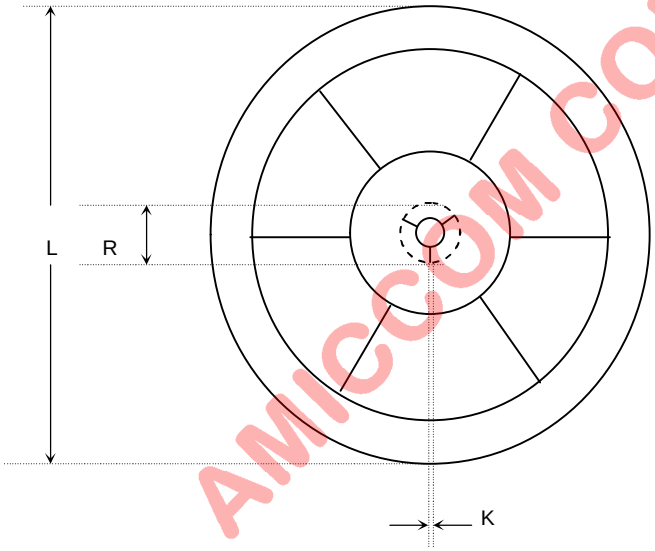
COVER TAPE WIDTH
9.2
9.2
9.2
13.3
8
13.3
13.3
12.5

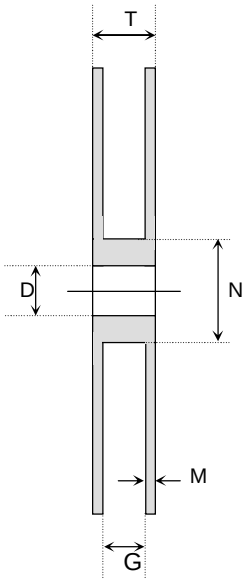
Unit : mm

REEL DIMENSIONS

UNIT IN mm

TYPE	G	N	T	M	D	K	L	R
20 QFN(4X4) 24 QFN(4X4) 32 QFN(5X5) DFN-10	12.8+0.6/-0.4	100 REF	18.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+0.00/-1.0	20.2
48 QFN(7X7)	16.8+0.6/-0.4	100 REF	22.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+0.00/-1.0	20.2
28 SSOP (150mil)	20.4+0.6/-0.4	100 REF	25(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+0.00/-1.0	20.2
20 SSOP 24 SSOP	16.4+2.0/-0.0	100 REF	22.4(MAX)	1.75±0.25	13.0+0.2/-0.2	1.9±0.4	330+0.00/-1.0	20.2





Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

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