44557 TX block diagram

2411.2-2465.2MHz

ANT

2.4G MODUIE

CON1

X1
16MHz

MCU

U1

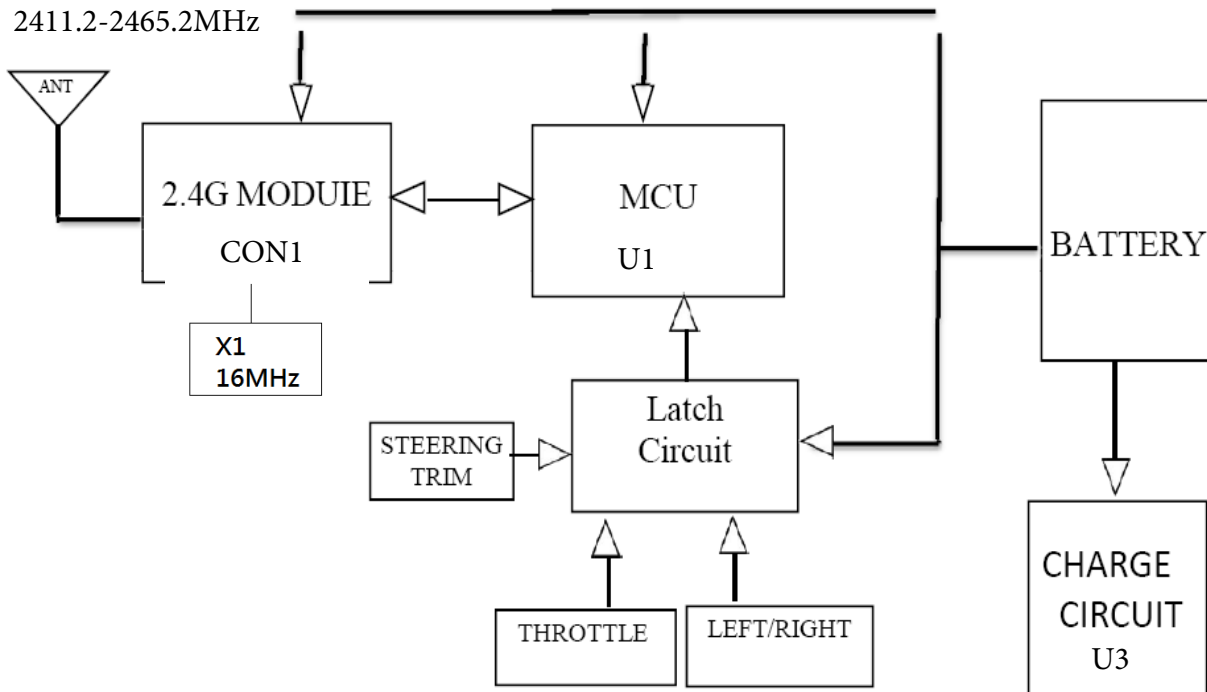STEERING
TRIM

Latch
Circuit

THROTTLE

LEFT/RIGHT

BATTERY

CHARGE
CIRCUIT

U3

A transmitter and a receiver must be programmed with the same RF channel frequency to be able to communicate with each other.

The output power of XN297 is set by the RF_PWR bits in the RF_SETUP register.

Demodulation is done with embedded data slicer and bit recovery logic. The air data rate can be programmed to 1Mbps or 2Mbps by RF_DR_HIGH and RF_DR_LOW register. A transmitter and a receiver must be programmed with the same setting.

In the following chapters, all registers are in register bank 0 except with explicit claim.
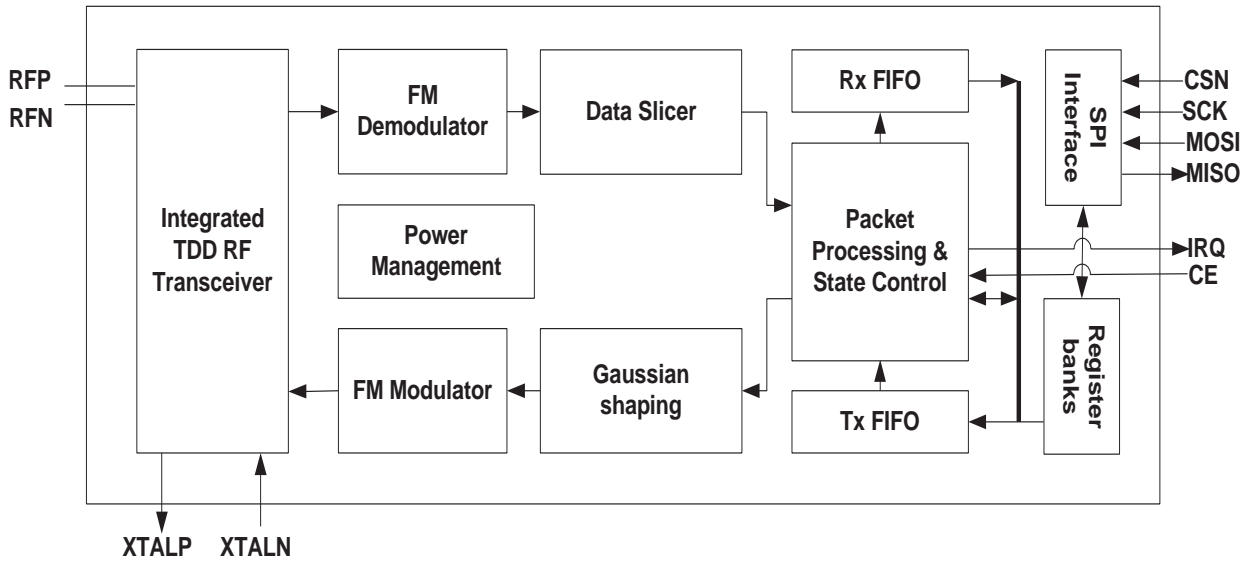

Figure 1 XN297 Chip Block Diagram

3   State Control

3.1   State Control Diagram

Pin signal: VDD, CE

SPI register: PWR_UP, PRIM_RX, EN_AA, NO_ACK, ARC, ARD

System information: Time out, ACK received, ARD elapsed, ARC_CNT, TX FIFO empty, ACK packet transmitted, Packet received

XN297 has built-in state machines that control the state transition between different modes.

When auto acknowledge feature is disabled, state transition will be fully controlled by MCU.