Technical Description:

The brief circuit description is listed as follows:

U1 acts as Decoder and MCU
U2 acts as Voltage Regulator
U3 and associated circuit act as 2.4GHz RF transceiver module
    -U7 acts as 2.4G FSK/GFSK Transceiver
U4 acts as Charge MCU
U5 acts as Coil Driver
U6 acts as Gyro Control

Antenna Used:

An internal, integral antenna has been used.
Antenna Gain: 0dBi
Nominal rated field strength: 90.2dBμV/m at 3m
Maximum allowed field strength of production tolerance: +/- 3dB

Version Note:
V1.0 ---- Add M06E-D-W-SI type Module.

1. General Description

The M06E module is designed for 2.4GHz ISM band with 0dBm output power wireless applications using A7106 FSK/GFSK tr ansceiver IC. This module features a fully programmable frequency synthesizer by SPI. The data rate is 500Kbps. Also the module is included the PCB Antenna.

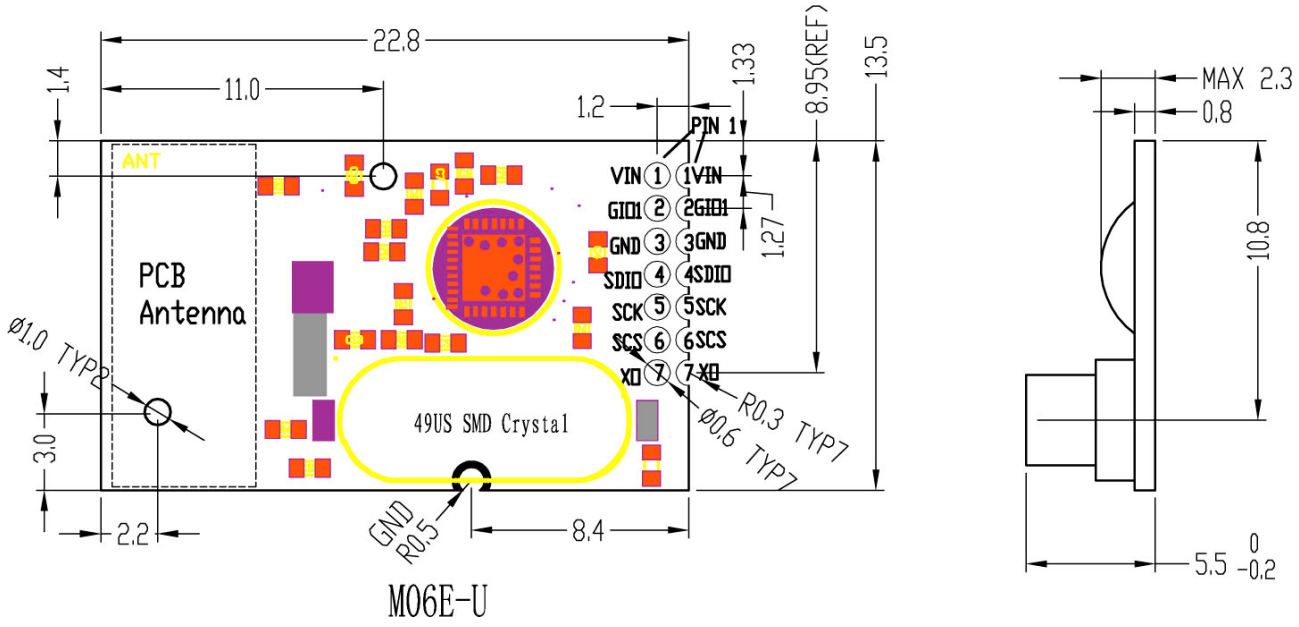
It has four different type models with different type crystal connected

M06E-U (with SMD49 crystal)
M06E-U-N (with C14,C15; without crystal, need to solder 20PF,10PPM SMD49 crystal)
M06E-D (with 49S crystal)
M06E-D-SI (with C14,C15; without R3,R4 and crystal; need to solder ANT and 20PF, 10PPM 49S crystal)
M06E-D-W-SI (with 49S crystal, But without R3,R4; need to solder ANT)
M06E-A (with AT26 crystal)
M06E-3 (with SMD 3225 crystal)
M06E-N (no crystal, without C14,C15, using external clock source,)

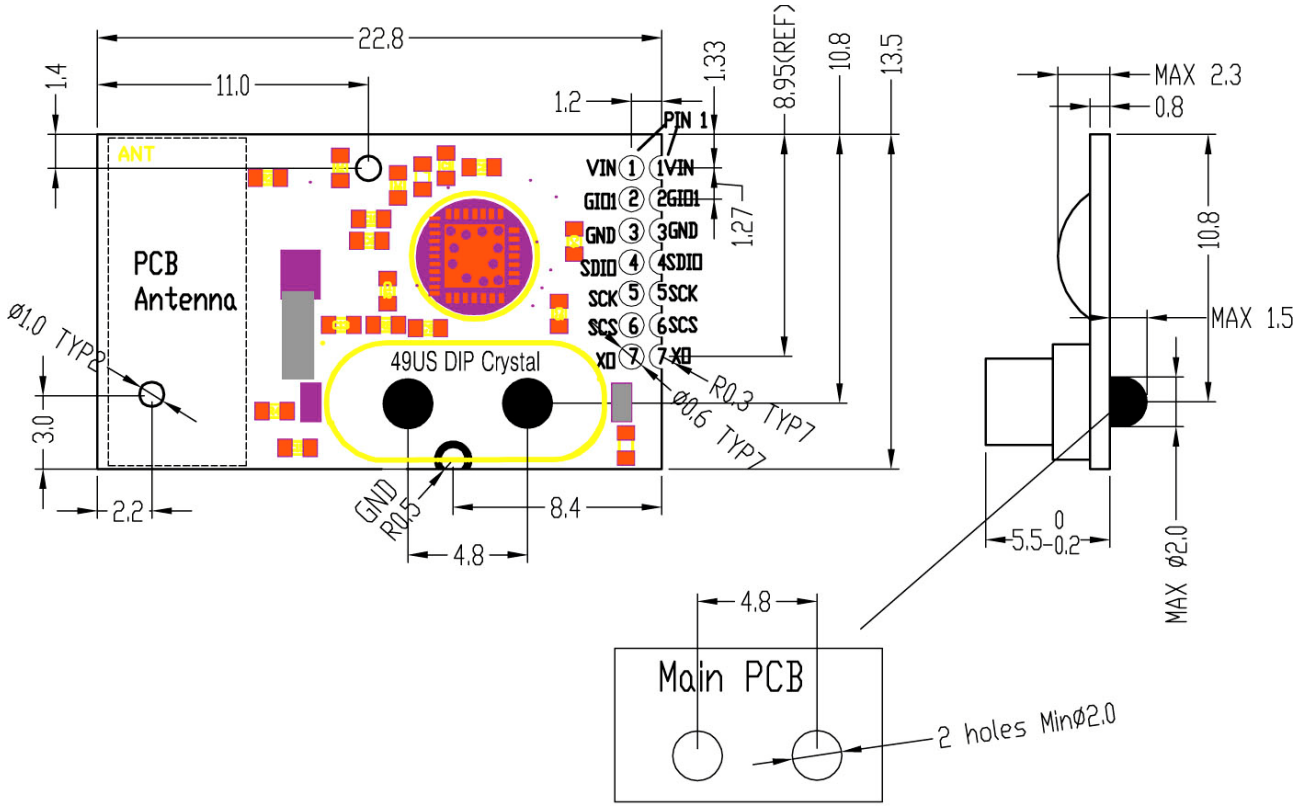
2. Electrical specification

Item	**Specification**	**Remark**
Supply voltage	2.0V-3.6V	Unit : Volt
Current consumption	1.5uA @Sleep mode (RC OCS off) 0.3mA @Idle mode (Regulator on) 1.9mA @Stand-by Mode (XOCS on, clock generator on) 9mA @ PLL mode 16mA @ RX mode 20mA@TX mode (0 dBm output) 12.5mA@TX mode (-20 dBm output)	Typical
Frequency	2400 – 2483.5 MHz	ISM band
Transmit output power	0 dBm @ room temperature 3.3V -5 dBm @ room temperature 3V0	Typical +/- 2dBm
Rx sensitivity	-95 dBm @ Data rate 500K mode	Typical, BER≦1E-3, With Gaussian filter.
Modulation	FSK or GFSK	
Interface	7 pin 1.27 mm header	
PCB Dimension	22.8(L) x 13.5(W) x 0.8(H)	Unit : mm
Operating temperature	0 ~ 50 ℃	

3. Dimension and Interface Pin Out

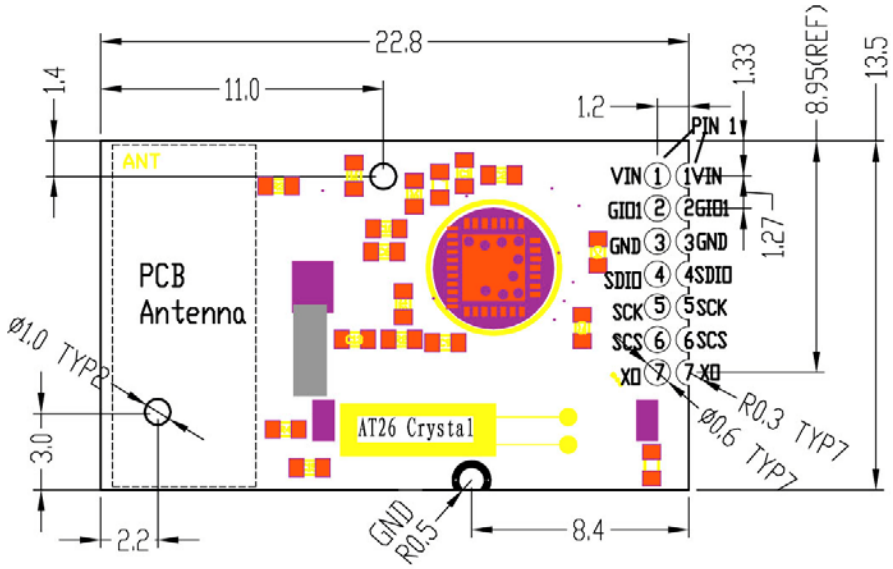


M06E-U

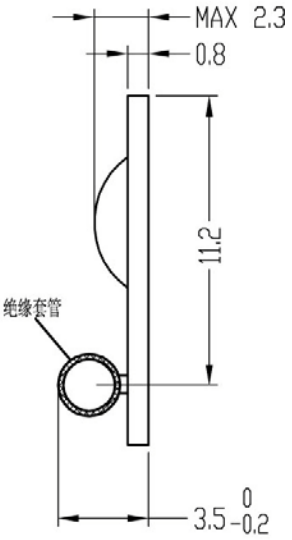


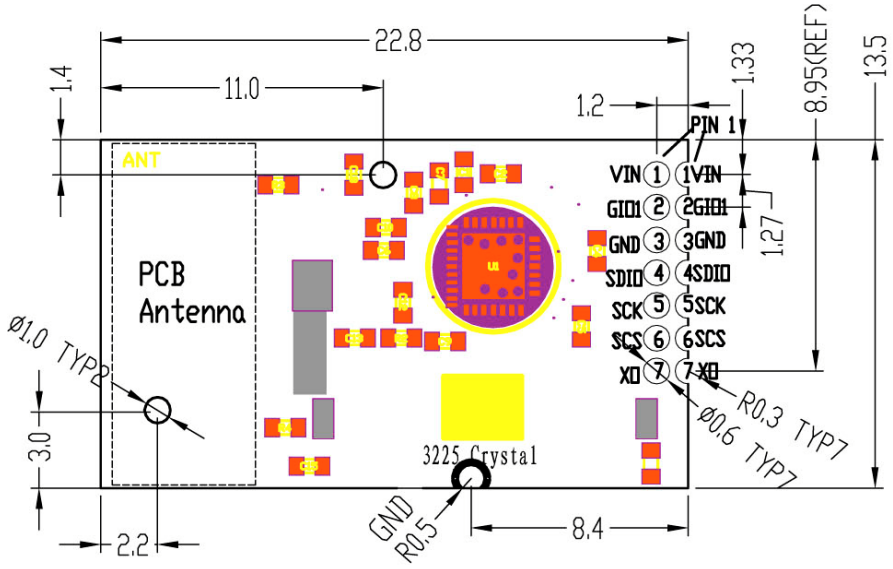
Notice: please make 2 holes in main PCB avoid the welding spots.

M06E-D

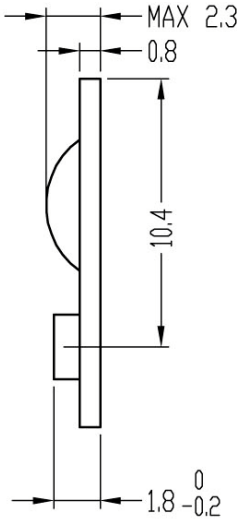


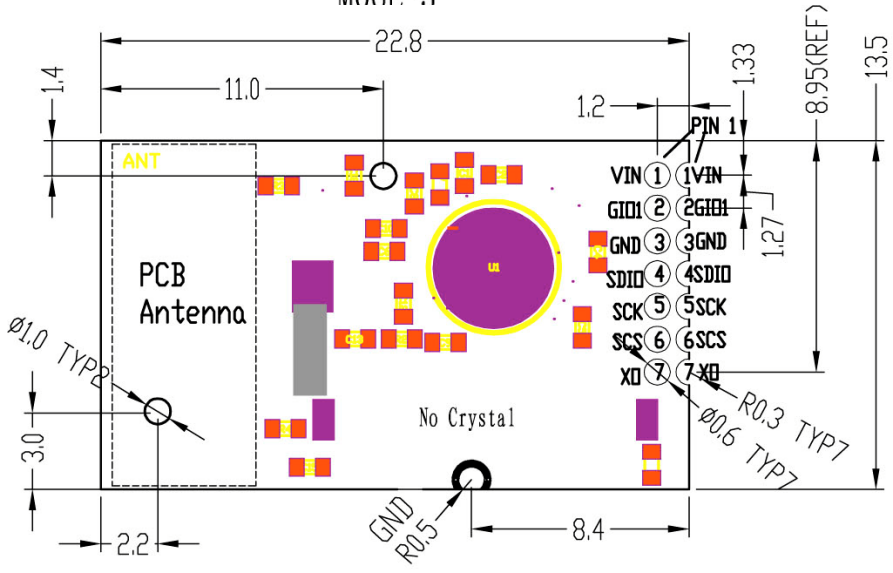
M06E-A



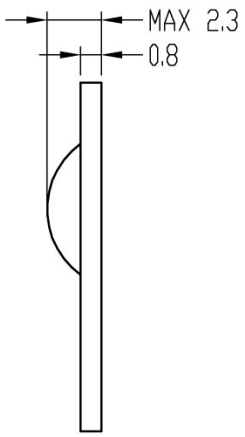


M06E-3





M06E-N



Pin No.	Pin name	Description	Type
1	VIN	RF module supply voltage input	PWR
2	GIO1	Data transfer over or ready	O
3	GND	Ground	PWR
4	SDIO	SPI data input/output	I/O
5	SCK	SPI Clock	I
6	SCS	SPI Chip Selection	I
7	X O	External Clock input	I

4. Module photograph

M06E-U

M06E-U-N

M06E-D

M06E-D-SI

M06E-A

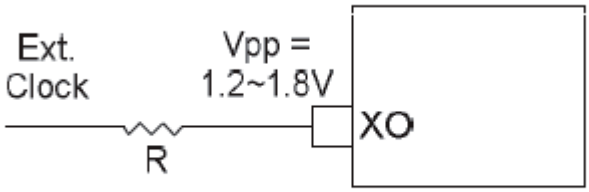
M06E-3

M06E-N

M06E-D-W-SI

5. Use External Clock (For M06E-N)

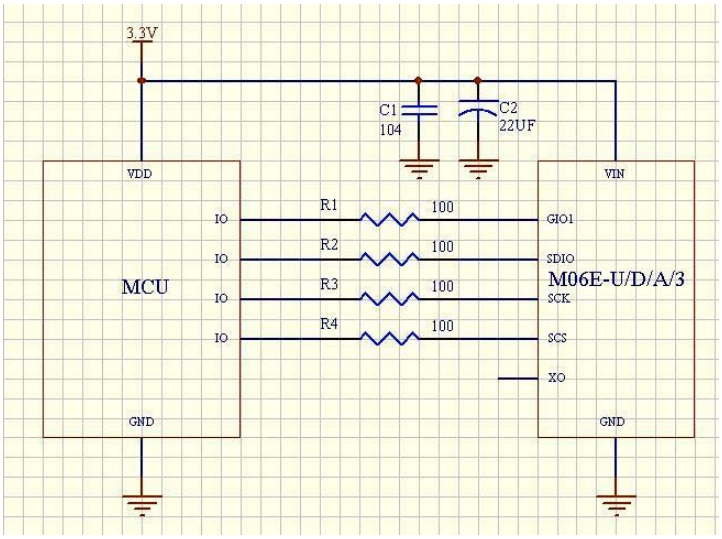
The M06E have build-in AC couple capacitor to support external clock input, The below figure shows how to connect. The frequency accuracy of external clock shall be controlled within +/- 20 ppm, and the amplitude of external clock shall be within 1.2 ~ 1.8 V peak-to-peak.



External clock source. R is used to tune Vpp = 1.2~1.8V

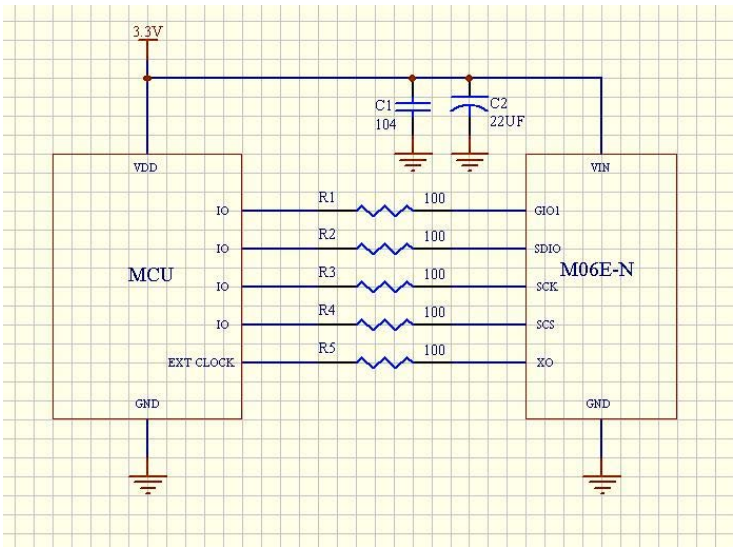
6. Application Circuit

a) M06E-U/D/A/3 application.



Using internal clock

b) M06E-N application.



Using external clock

7. Ordering Information.

Part Number	Size(W*L*H)	Description
M06E-U	22.8*13.5*5.5mm	Use SMD49 crystal.
M06E-U-N	22.8*13.5*2.3mm	With C14,C15; without crystal; need to solder 20PF, 10PPM 49US SMD crystal
M06E-D	22.8*13.5*5mm	Use 49S crystal.
M06E-D-SI	22.8*13.5*2.3mm	with C14,C15; without R3,R4 and crystal; need to solder ANT and 20PF,10PPM 49S DIP crystal
M06E-D-W-SI	22.8*13.5*5mm	Use 49S crystal; But without R3,R4; need to solder ANT
M06E-A	22.8*13.5*3.5mm	Use AT26 type crystal.
M06E-3	22.8*13.5*2.3mm	Use SMD3225 type crystal.
M06E-N	22.8*13.5*2.3mm	No crystal inside; without C14, C15; use external clock, 16MHz, 12MHz or 8MHz, consult with JESS or HJT.

1. General Description

A7106 is a high performance and low cost 2.4GHz ISM band wireless transceiver. This device integrates both high sensitivity receiver (- 95dBm @ 500Kbps) and high efficiency power amplifier (up to 1dBm). In low data rate application, A7106 has special strength for long LOS (line-of-sight) distance because of its ultra high sensitivity (-107 dBm @ 2Kbps, - 104 dBm @ 25Kbps) with no requirement of external LNA or PA. Based on Data Rate Register (0x0E), user can configure on-air data rates from 2Kbps to 500Kbps.

A7106 supports fast settling time (130 us) for frequency hopping system. For packet handling, A7106 has built-in separated 64-bytes TX/RX FIFO (could be extended to 256 bytes) for data buffering and burst transmission, CRC for error detection, FEC for 1-bit data correction per code word, RSSI for clear channel assessment, data whitening for data encryption / decryption, the internal RC oscillator for WOR (Wake-On-RX) to support periodically wake up from sleep and listen (auto-enter RX mode) for incoming packets without MCU interaction. Those functions are very easy to use while developing a wireless system. All features are integrated in a small QFN 4X4 20 pins package.

A7106's control registers can be easily accessed via 3-wire or 4-wire SPI bus. For power saving, A7106 supports sleep mode, idle mode, standby mode. For easy-to-use, A7106 has an unique SPI command set called **Strobe command** that are used to control internal state machine. Based on Strobe commands via SPI bus, MCU can control everything from power saving, TX delivery, RX receiving, channel monitoring, frequency hopping to auto calibrations. In addition, A7106 supports two general purpose I/O pins, GIO1 and GIO2, to inform MCU its status so that MCU could use either polling or interrupt scheme to do radio control. Hence, it is very easy to monitor radio transmission between MCU and A7106 because of its digital interface.

2. Typical Applications

- Wireless keyboard and mice
- Remote control
- Helicopter and airplane radio controller
- 2400 ~ 2483.5 MHz ISM system
- Wireless metering and building automation
- Wireless toys and game controllers

3. Feature

- Small size (QFN4 X4, 20 pins).
- Frequency band: 2400 ~ 2483.5MHz.
- FSK or GFSK modulation
- Low current consumption: RX 16mA, TX 20mA (at 0dBm output power).
- Low sleep current (1.5 uA).
- On chip regulator, support input voltage 2.0 ~ 3.6 V.
- Programmable data rate from 2Kbps to 500Kbps.
- Programmable TX power level from – 20 dBm to 1 dBm.
- Ultra High sensitivity:
  - -95dBm at 500Kbps on-air data rate.
  - -97dBm at 250Kbps on-air data rate
  - -104dBm at 25Kbps on-air data rate
  - -107dBm at 2Kbps on-air data rate
- Fast settling time (130 us) synthesizer for frequency hopping system.
- Built-in Battery Detector.
- Support low cost crystal (6 / 8 /12 / 16 / 20 / 24MHz).
- Support crystal sharing, (1 / 2 / 4 / 8MHz) to MCU.
- Auto Frequency Compensation
- Easy to use.
  - Support 3-wire or 4-wire SPI.
  - Unique Strobe command via SPI.
  - ONE register setting for new channel frequency.
  - 8-bits Digital RSSI for clear channel indication.
  - Fast exchange mode during TRX role switching.
  - Auto RSSI measurement.
  - Auto Calibrations.

- Auto IF function.
- Auto CRC Check.
- Auto FEC by (7, 4) Hamming code (1 bit error correction / code word).
- Data Whitening for encryption and decryption.
- Separated 64 bytes RX and TX FIFO.
- Easy FIFO / Segment FIFO / FIFO Extension (up to 256 bytes).
- Support direct mode with recovery clock output to MCU.
- Support direct mode with frame sync signal to MCU.
- Support WOR (Wake-On-RX) to periodically wake up from sleep to RX mode.

4. Pin Configurations

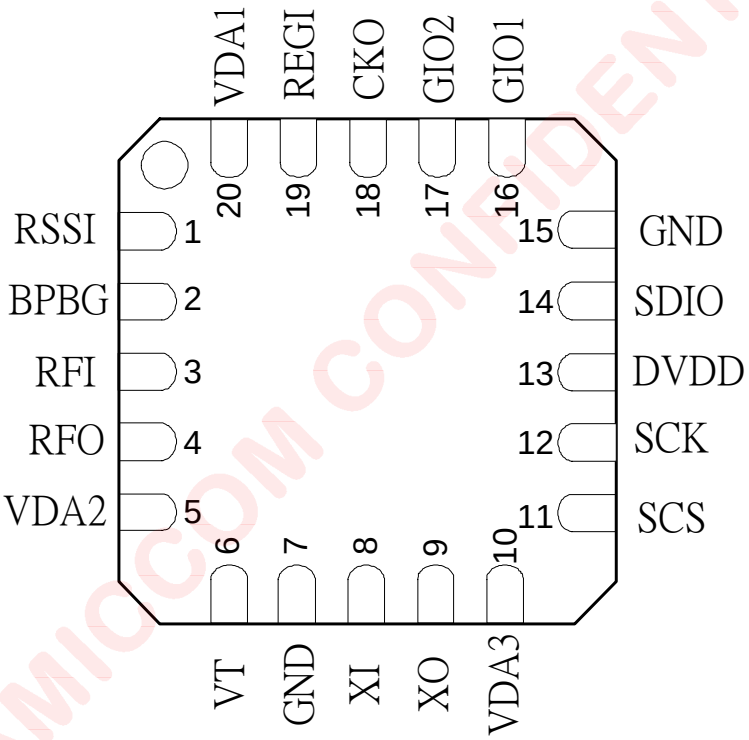


Fig 4-1. A7106 QFN 4x4 Package Top View

5. Pin Description (I: input; O: output, I/O: input or output)

Pin No.	Symbol	I/O	Function Description
1	RSSI	O	Connected to a bypass capacitor for RSSI reading.
2	BPBG	O	Connected to a bypass capacitor for internal Regulator bias point
3	RFI	I	Low noise amplifier input.
4	RFO	O	Power amplifier output.
5	VDA2	I/O	Voltage supply **(from VDA1, pin 20)** for RX & TX analog part.
6	VT	I	VCO frequency control input, internal connected to PLL charge pump.
7	GND	G	Ground
8	XI	I	Crystal oscillator input node
9	XO	O	Crystal oscillator output node
10	VDA3	I	Voltage supply **(from VDA1, pin 20)** for PLL part
11	SCS	I	3 wire SPI chip select.
12	SCK	I	3 wire SPI clock input pin.
13	DVDD	I	Connected to a bypass capacitor to supply voltage for digital part.
14	SDIO	I/O	3 wire SPI read/write data pin.
15	GND	G	Ground
16	GIO1	I/O	Multi-function GIO1 / 4-wire SPI data output.
17	GIO2	I/O	Multi-function GIO2 / 4-wire SPI data output.
18	CKO	O	Multi-function clock output.
19	REGI	I	Internal Regulator input **(External Power Input)**
20	VDA1	I/O	Internal Regulator output to supply **VDA2 (pin 5), VDA2 (pin 10) and RFO (pin 4).**
	Back side plate	G	Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.

6. Chip Block Diagram

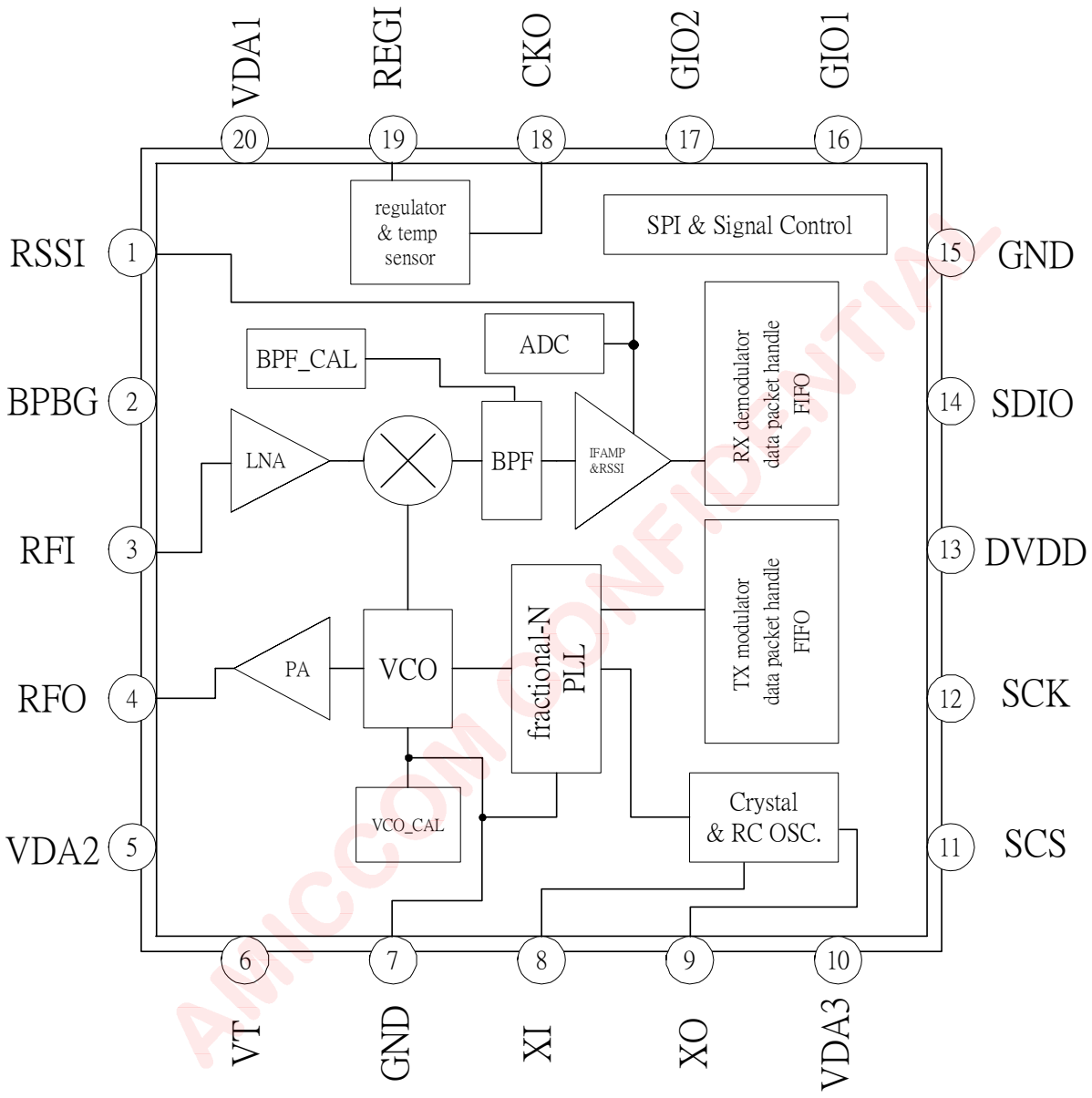


Fig 6-1. A7106 Block Diagram

7. Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 2.1	V
Input RF level		5	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	± 2K	V
	MM	± 100	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).

8. Electrical Specification

(Ta=25℃, VDD=3.0V, data rate= 500Kbps, IF bandwidth = 500KHz, F_{XTAL} =16MHz, with Match Networking and low pass filter, On Chip Regulator = 2.1V, unless otherwise noted.)

Parameter	Description	Min.	Type	Max.	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage (VDD)	with internal regulator	2.0		3.6	V
Current Consumption	Sleep mode (RC OSC off)		1.5*[1]		μA
	Idle Mode (Regulator on)		0.3*[1]		mA
	Standby Mode (XOSC on,clock generator on)		1.9		mA
	PLL mode		9		mA
	RX Mode		16		mA
	TX Mode (@0dBm output)		20		mA
	TX Mode (@-3dBm output)		16		mA
	TX Mode (@-6dBm output)		14.5		mA
	TX Mode (@-11dBm output)		13.9		mA
	TX Mode (@-20dBm output)		12.5		mA
PLL block					
Crystal start up time*[2]			0.6		ms
Crystal frequency		6, 8, 12, **16**, 20, 24			MHz
Crystal tolerance	without FW FC	±10			ppm
	with FW FC	±20			ppm
Crystal ESR				80	ohm
VCO Operation Frequency		2400		2483.5	MHz
PLL phase noise	Offset 10k Offset 100K Offset 1M		80 85 90		dBc
PLL settling time *[3]	@Loop BW = 500Khz		70		μS
Transmitter					
Output power range		-20	0		dBm
Out Band Spurious Emission *[4]	30MHz~1GHz			-36	dBm
	1GHz~12.75GHz			-30	dBm
	1.8GHz~ 1.9GHz			-47	dBm
	5.15GHz~ 5.3GHz			-47	dBm
Frequency deviation*[5]	Data rate > 50Kbps		186K		Hz
	Date rate <=50Kbps		124K		Hz
Data rate		2K		500K	Bps
TX ready time*[6] (PLL to WPLL + WPLL to TX)	@Loop BW = 500 KHz, LO fixed		10+60		μS
	@Loop BW = 500 KHz, Hopping		70+60		μS
Receiver					
Receiver sensitivity @ BER = 0.1%	Data rate 500K (F_{IF} = 500KHz)		-95		dBm
	Data rate 250K (F_{IF} = 500KHz)		-97		dBm
	Data rate 25K (F_{IF} = 500KHz)		-104		dBm

	Data rate 2K (F_{IF} = 500KHz)		-107		dBm
IF frequency bandwidth			250/500		KHz
IF center frequency			250/500		KHz
Interference *7	Co-Channel (C/I_0)		11		dB
	±1MHz Adjacent Channel		- 20		dB
	±2MHz Adjacent Channel		- 30		dB
	> ±5MHz Adjacent Channel		- 40		dB
	Image (C/I_{IM})		- 12		dB
Maximum Operating Input Power	@RF input (BER=0.1%)			0	dBm
Spurious Emission *4	30MHz~1GHz			-57	dBm
	1GHz~12.75GHz			-47	
RSSI Range	@RF input	-105		-50	dBm
RX Ready Time*8 (PLL to WPLL + WPLL to RX)	LO fixed, Data rate < = 125 Kbps		10+40		µs
	LO fixed, Data rate = 250 Kbps		10+100		µs
	LO fixed, Data rate = 500 Kbps		10+60		µs
	Hopping, Data rate < = 125 Kbps		70+40		µs
	Hopping, Data rate = 250 Kbps		70+100		µs
	Hopping, Data rate = 500 Kbps		70+60		µs
RX Spurious Emission	above 1GHz			-47	dBm
Regulator					
Regulator settling time	Pin 2 connected to 1.5 nF		500		µs
Band-gap reference voltage			1.23		V
Regulator output voltage		1.8	2.1	2.3	V
Line regulation	Load current 30mA	35	40		dBc
Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V

Note 1: When digital I/O pins are configured as input, those pins shall NOT be floating but pull either high or low (SCS shall be pulled high only); otherwise, leakage current will be induced.
Note 2: Refer to Delay Register II (17h) to set up crystal settling delay.
Note 3: Refer to Delay Register I (17h) to set up PDL (PLL settling delay).
Note 4: With external RF filter that provides minimum 17dB of attenuation in the band: 30MHz ~ 2GHz and 3GHz ~12.75GHz.
Note 5: Refer to TX Register II (15h) to set up FD [4:0].
Note 6: Refer to Delay Register I (17h) to set up PDL and TDL delay.
Note 7: The power level of wanted signal is set at sensitivity level +3dB. The modulation data for wanted signal and interferer are PN9 and PN15, respectively. Channel spacing is 500KHz.
Note 8: For 250K/500Kbps, set DCM[1:0]= [10b] by ID, (29h). For <= 125Kbps, set DCM[1:0]= [01b] by Preamble, (29h).