Technical Description:

The brief circuit description is listed as follows:

Module 1 act as 2.4GHz RF transceiver module
- U3 (SR1N001F) is 2.4GHz radio transceiver
- Y1 (12MHz) crystal providing clock for U3

U1 act as 3.3V power regulator
U2 acts as encoder control

Antenna Used:

An internal, integral antenna has been used.
Antenna Gain: 0dBi
Production tolerance: +4dBm (Minimum) to +8dBm (Maximum)

2.4GHz Digital wireless module (channel table)

Channel	Frequency
1	2.404GHz
2	2.405GHz
3	2.406GHz
4	2.407GHz
5	2.408GHz
6	2.409GHz
7	2.410GHz
8	2.411GHz
9	2.412GHz
10	2.413GHz
11	2.414GHz
12	2.415GHz
13	2.416GHz
14	2.417GHz
15	2.418GHz
16	2.419GHz
17	2.420GHz
18	2.421GHz
19	2.422GHz
20	2.423GHz
21	2.424GHz
22	2.425GHz
23	2.426GHz
24	2.427GHz
25	2.428GHz
26	2.429GHz
27	2.430GHz
28	2.431GHz
29	2.432GHz
30	2.433GHz
31	2.434GHz
32	2.435GHz
33	2.436GHz
34	2.437GHz
35	2.438GHz
36	2.439GHz
37	2.440GHz
38	2.441GHz
39	2.442GHz
40	2.443GHz
41	2.444GHz
42	2.445GHz
43	2.446GHz
44	2.447GHz
45	2.448GHz
46	2.449GHz
47	2.450GHz
48	2.451GHz
49	2.452GHz

Channel	Frequency
50	2.453GHz
51	2.454GHz
52	2.455GHz
53	2.456GHz
54	2.457GHz
55	2.458GHz
56	2.459GHz
57	2.460GHz
58	2.461GHz
59	2.462GHz
60	2.463GHz
61	2.464GHz
62	2.465GHz
63	2.466GHz
64	2.467GHz
65	2.468GHz
66	2.469GHz
67	2.470GHz
68	2.471GHz
69	2.472GHz
70	2.473GHz
71	2.474GHz
72	2.475GHz
73	2.476GHz
74	2.477GHz
75	2.478GHz
76	2.479GHz

WAILLY 2.4GHz RF Module Datasheet

WT24S00V03

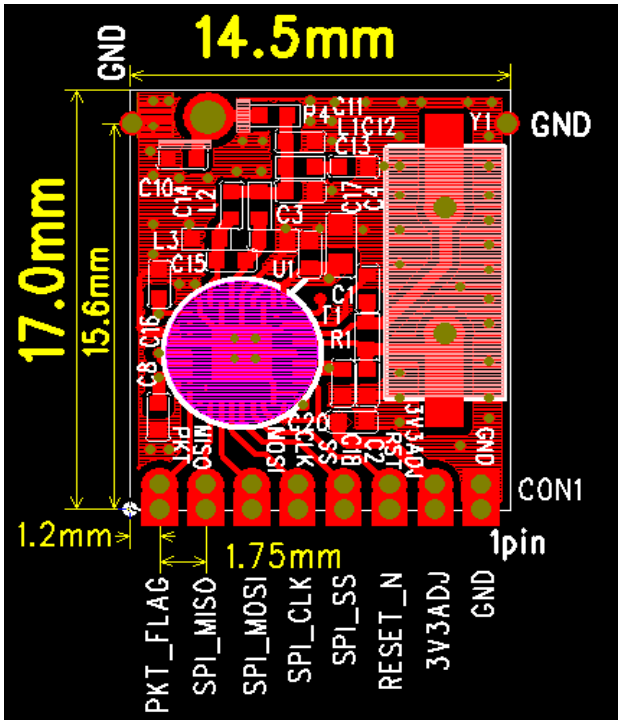
RF characteristic:

- 2.4Ghz ISM Band, Multi-channels.
- Up to 1M bps data rate.
- TX: Up to 4 dBm output power
- RX: -92 dBm sensitivity.
- GFSK modulation
- 64 bytes FIFO
- RSSI indicator
- No Need External SAW Filter
- Open field distance(Antenna in meander type, 1 meter from ground, BER < 0.1%):
  0 dBm/30 m, 4 dBm/45 m

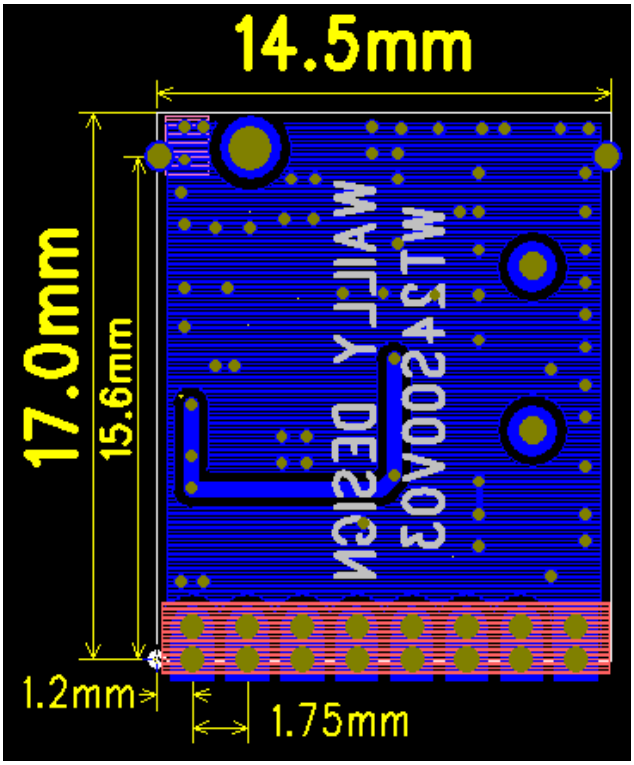
Electrical specification

Item	Parameters	Min	Typ	Max	Unit	Condition
1	**Supply**					
1.1	Supply voltage	1.6		3.6	V	
2	**Current Consumption**					
2.1	sleep mode		2.69		uA	
2.2	Rx states		18		mA	
2.3	Tx states		21.7		mA	
3	**Transmitter Part**					
3.1	Frequency range	2402		2480	MHz	
3.2	Output power	-16	0	4	dBm	

Module Dimension Drawing (Top view)



Module Dimension Drawing (Botton view)



Pin Configuration

Pin	Symbol	Function
1	GND	Ground
2	3V3ADJ	RF module supply voltage
3	RESET_N	Reset input,active Low
4	SPI_SS	SPI slave Select input
5	SPI_CLK	SPI Clock input
6	SPI_MOSI	SPI Data Input
7	SPI_MISO	SPI Data Output
8	PKT_FLAG	Packet TX/ RX flag

Application:

- Remote control
- Wireless keyboard/mice
- Home application
- Toys/Game control

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SR1N001F

Product Datasheet

Rev 1.0e

Revision History

Version	Date	Description
0.9a	2011/05/30	Modify chapter "10.Reference Design" figure.
	2011/06/01	Modify chapter "3.Electrical Characteristic" Table2: TX High typical value and notes & TX Low notes.
	2011/06/02	Modify chapter "7.Register" REG09 bit4-3 description & REG17 bit15-9 description.
	2011/06/15	Modify chapter "7.Register" REG2A bit7-0 description.
	2011/06/23	Modify chapter "7.Register" REG28 description.
		Modify "8.4 FIFO Pointer Clear" description. Original "*FIFO write pointer must be cleared*" → Modified "*FIFO write & read pointer must be cleared*"
		Modify chapter "7.Register" REG20 description.
		Modify chapter "7.Register" REG2A description. Original "*reg0x29*" → Modified "*reg29*".
	2011/07/07	Modify chapter "7.Register" REG20 description.
		Modify "8.4 FIFO Pointer Clear" description.
	2011/08/24	Modify chapter "7.Register" REG09 bit15-13 description.
1.0a	2011/12/01	chapter1, figure 1 add LDO_OUT chapter4, add LDO_OUT,LDO_IN, update all relative diagram chapter7, add REG1B Description chapter 10, change reference design Product name change to SR1n001F
1.0b	2011/12/13	chapter 3, RF output power under 0dBm, reg0x09 setting fix to 0x8570
1.0c	2011/12/15	Figure and Table number. Chapter 5.1, 5.2 and 8.12 refer information.
1.0d	2011/12/16	7.2.12. REG20 SYNCWORD_LEN define change.
1.0e	2012/04/12	Revise chapter 10 reference design

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1. Overview

1.1 Key Features

- Complete 2.4 GHz radio transceiver with fully integrated PLL and channel filtering.
- Supports Frequency-Hopping Spread Spectrum.
- Supports SPI bus interfaces to communicate with external MCU.
- Built-in smart auto-acknowledge TX/RX protocol to simplify the chip usage.
- 1 Mbps GFSK on air data rate.
- Programmable output power.
- With FIFO flag signaling to help the streaming of data to/from external MCU.
- With power management mechanism to minimizing the current consumption.
- Support RSSI.readout.
- Lead-free 4x4 mm QFN24 is available.

1.2 Application

- Remote control.
- Wireless keyboard and mice.
- Proprietary wireless network.
- Home automation.
- Commercial and industrial shot-range wireless communication.
- Wireless voice, VoIP or cordless headsets.
- Robotics and machine connectivity.

1.3 Bloc Diagram

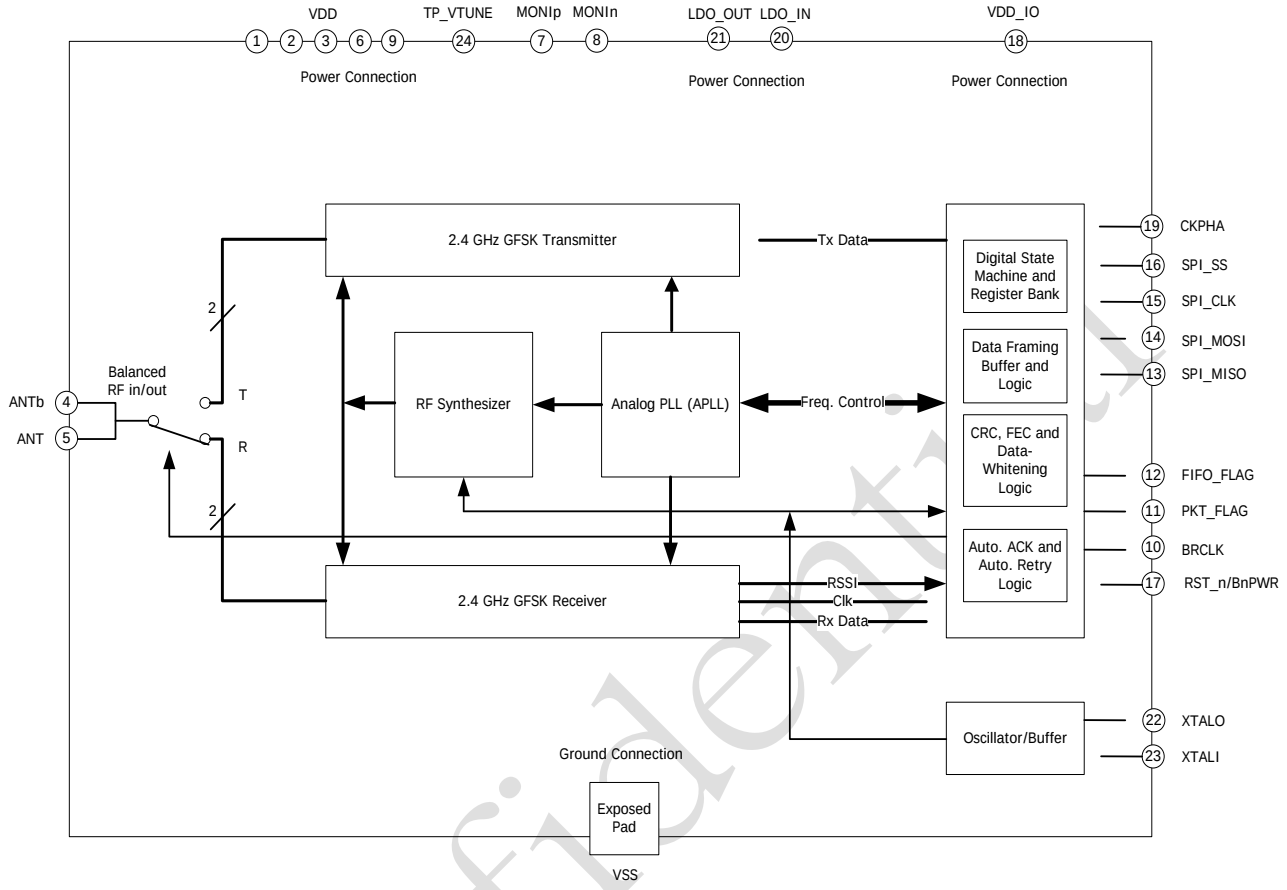


Figure 1-1 SR1N001F Block Diagram (QFN24 Package)

2. Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Unit
Operating Temp.	TOP			°C
Storage Temp.	TSTORAGE			°C
VDD_IO Voltage	VIN			VDC
VDD Pins	VDD_IN			VDC
Applied Voltage to Other Pins	VOTHER			VDC
Input RF Level	PIN			dBm
Output Load Mismatch (Z0=50Ω)	VSWROUT			VSWR

Table 2-1 Absolute Maximum Rating

Notes:

1. Absolute Maximum Rating indicates the limit that beyond which may damage the device. Recommended operation conditions indicates condition for which the device is intended to be functional, but without guarantee to specific performance level. For guaranteed specifications and test conditions, please refer to 'Electrical Characteristics' section below.
2. These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover workbenches with grounded conductive mats.

3. Electrical Characteristics

Note: The following specifications are guaranteed for TA = 25°C, VDD_IO = 3.3 VDC, unless other noted.

Parameter	Symbol	MIN	TYP	MAX	Unit	Test Conditions and Notes
Supply Voltage						
DC Power Supply Voltage Range	V_{IN}	1.6		3.6	VDC	Input to VDD_IO pins
External Power Input	PLL_VDD, IF_VDD, VCO_VDD, RF_VDD, AMS_AVDD	1.62		1.98	VDC	Input to the power pins
Current Consumption						
TX High	I_{DD_TXH}		21.7		mA	POUT= high power (0dBm)
TX Low	I_{DD_TXL}		14.7		mA	POUT= low power (-14dBm)
RX	I_{DD_RX}		18		mA	
IDLE State 1	I_{DD_IDLE1}		1.69		mA	Configure for BRCLK output on
IDLE State 2	I_{DD_IDLE2}		1.66		mA	Configure for BRCLK output off
SLEEP State	I_{DD_SLP}		2.69		uA	
Digital Inputs						
Logic Input High	V_{IH}	0.8 V_{DD_IN}		1.2 V_{DD_IN}	V	
Logic Input Low	V_{IL}	0		0.8	V	
Input Capacitance	$C_{\_IN}$			10	pF	
Input Leakage Current	$I_{\_LEAK\_IN}$			10	uA	SoC
Digital Outputs						
Logic Output High	V_{OH}	0.8 V_{DD_IN}		1.0 V_{DD_IN}	V	
Logic Output Low	V_{OL}			0.4	V	
Output Capacitance	$C_{\_OUT}$			10	pF	
Output Leakage Current	$I_{\_LEAK\_OUT}$			10	uA	
Rise/Fall Time (SPI)	$T_{\_RISE\_SOUT}$			5	ns	
Clock Signals						
CLK Rise/Fail Time (SPI)	T_{R_SPI}			25	ns	Requirement for error free read/write
CLK Frequency	F_{SPI}	0	12		MHz	

Range (SPI)						
Overall Transceiver						
Operating Frequency Range	$F_{\_OP}$	2402		2480	MHz	
Antenna Port Mismatch (ZO=50Ω)	$VSWR_{\_I}$		<1.2		VSWR	Receive mode
	$VSWR_{O}$		<1.2		VSWR	Transmit mode

Parameter	Symbol	MIN	TYP	MAX	Unit	Test Conditions and Notes
Receive Section						Measured using 50Ω balun. For BER<=0.1%
Receiver Sensitivity			-87		dBm	FEC off
Maximum Usable Signal			-7		dBm	
Data(Symbol) Rate	T_S		1		us	
Min. Carrier/Interference Ratio						For BER <=0.1%
Co-Channel Interference	$CI_{Cochannel}$		8		dB	-60 dBm desired signal
Adj. Channel Interference (1MHz Offset)	$CI_{\_1}$		4		dB	-60 dBm desired signal
Adj. Ch. Interference (2MHz Offset)	$CI_{\_2}$		-14		dB	-60 dBm desired signal
Adj. Ch. Interference (3MHz Offset)	$CI_{\_3}$		-23		dB	-67 dBm desired signal
Out-of-Band Blocking	$OBB_{\_1}$	-24			dBm	30MHz to 2000MHz (3)
For additional test conditions, check Note 3.	$OBB_{\_2}$	-27			dBm	2000MHz to 2400MHz (3)
	$OBB_{\_3}$	-24			dBm	2500MHz to 3000MHz (3)
	$OBB_{\_4}$	-10			dBm	2000MHz to 5000MHz (3)
Transmit Section						Measured using 50Ω balun.
RF Output Power	P_{AV}		4		dBm	POUT= Maximum output power. REG09=0x8070
			0		dBm	POUT= Nominal output power. REG09=0x8570
			-14		dBm	POUT= Minimum output power. REG09=0x8F70
Second Harmonic			<-50		dBm	Conduct to ANT pin
Third Harmonic			<-50		dBm	Conduct to ANTb pin
Modulation Characteristics						
Peak FM Deviation (0Fh Pattern)	$\Delta f1_{avg}$		320		kHz	
Peak FM Deviation (55h Pattern)	$\Delta f2_{max}$		256		kHz	
In-Band Spurious Emission						
2MHz Offset	IBS_2			-40	dBm	
>3MHz Offset	IBS_3			-60	dBm	
	OBS_O_1		<-60	-36	dBm	30MHz~1GHz
	OBS_O_2		-45	-30	dBm	1GHz~12.75GHz, exclude desired

						signal and harmonic
	OBS_O_3		<-60	-47	dBm	1.8GHz~1.9GHz
	OBS_O_4		<-65	-47	dBm	5.15GHz~5.3GHz

Note

1. The test is run at one mid-band frequency, typically 2441MHz. With blocking frequency swept in 1MHz steps, up to 24 exception frequencies are allowed. Of these, no more than 5 shall persist with blocking signal reduced to -50dBm. For blocking frequencies below desired received frequency, in-band harmonics of the out-of-band blocking signal are the most frequent cause of failure. Please make sure the blocking signal is embedded with adequate harmonic filter.
2. In some applications, this filter may be incorporated into the antenna, or be approximated by the effective antenna bandwidth.
3. These conditions are measured on ANT pin with additional LC circuit as referenced in corresponding application note. Desired signal is -67 dBm, BER <=0.1%. The poor $OBB_{\_1}$ is caused by the interference of half operating frequency.

Parameter	Symbol	MIN	TYP	MAX	Unit	Test Conditions and Notes
RF VCO and PLL Section						
Typical PLL Lock Range	F_{LOCK}	2400		2483	MHz	
TX/RX Frequency/Tolerance					ppm	Same as XTALI pin frequency tolerance
Channel (Step) Size			1		MHz	
SSB Phase Noise			≤-95		dBc/Hz	550kHz offset
			≤-115		dBc/Hz	2MHz offset
Crystal Oscillator Freq. Range			12		MHz	Designed for 12MHz crystal reference frequency
RF PLL Setting Time	T_{HOP}		75	150	us	Settle to within 30kHz of final value
Spurious Emissions	$OBS_{\_1}$		<-75		dBm	30MHz~1GHz(1)
	$OBS_{\_2}$		-68		dBm	1GHz~5GHz(1)

Note

1. Test conditions: chip is at IDLE state and VCO is on.

4. Chip Pins Description

4.1 Chip Top View

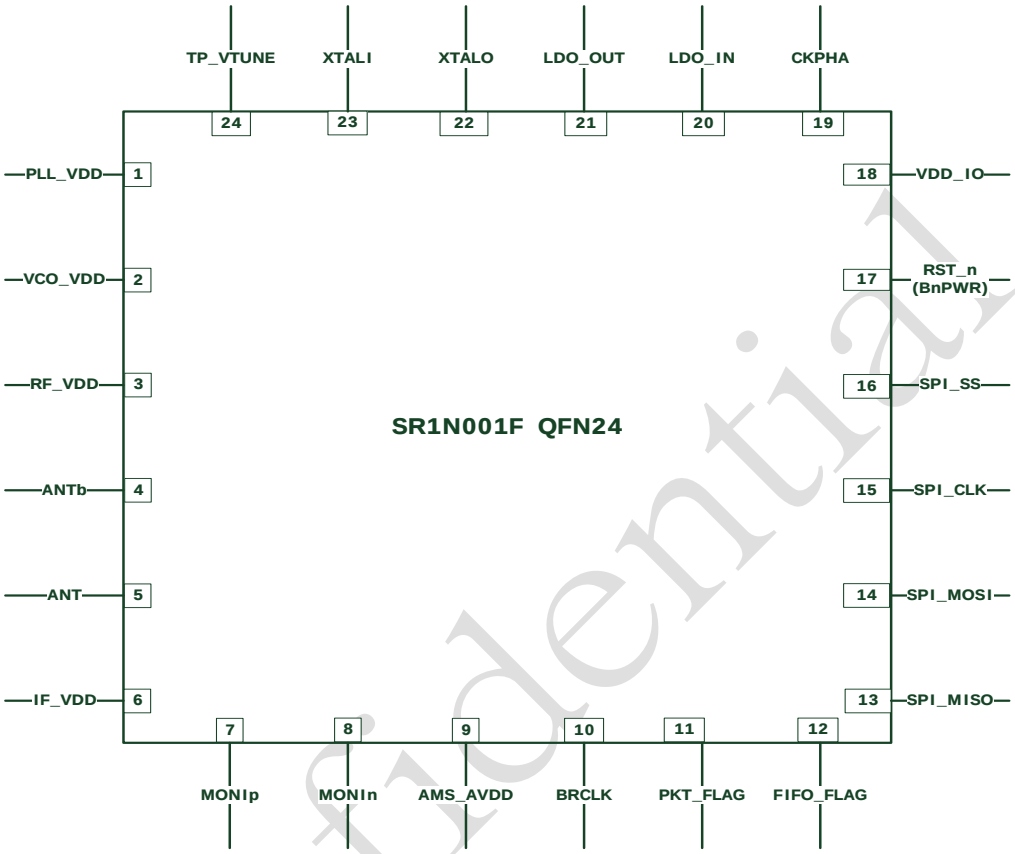


Figure 4-1 The QFN24 Package Pin Location

4.2 Pin Description

Pin Number	Pin Name	Pin Type	Description
1	PLL_VDD	Power	The power pin for internal PLL
2	VCO_VDD	Power	The power pin for internal VCO
3	RF_VDD	Power	The power pin for internal radio frequency components
4	ANTb	RF Port	RF IO port
5	ANT	RF Port	RF IO port
6	IF_VDD	Power	The power for internal inter-media frequency components
7	MONIp	AO	The monitor pins for the differential input signals to internal BPF
8	MONIn	AO	
9	AMS_AVDD	Power	The power pin for the chip.
10	BRCLK	O	Clock output pin
11	PKT_FLAG	O	Packet transmit/receive status pin
12	FIFO_FLAG	O	Internal FIFO status indication pin
13	SPI_MISO	I/O	SPI: Master input/slave output
14	SPI_MOSI	I	SPI: The master output/slave input
15	SPI_CLK	I	SPI: The clock input
16	SPI_SS	I	SPI bus enable pin, active low. Toggles this pin can make the chip to exit the SLEEP state
17	RST_n(BnPWR)	I	Pull down this pin will make this chip to enter the power saving state. The content of all internal registers will lose. 1. Raise up this pin will reset all the internal registers to their initial value.
18	VDD_IO	Power	Power for IO ring
19	CKPHA	I	Select default/optional SPI transfer format to communicate 1: Support optional SPI transfer format
20	LDO_IN		LDO input(3.3V)
21	LDO_OUT		LDO output(default 1.8V, adjustable)
22	XTALO	AO	The output of crystal oscillator gain block
23	XTALI	AI	The input of crystal oscillator gain block
24	TP_VTUNE	Power	The monitor and control pin for VCO voltage

Table 4-1 The QFN24 Pin Description Table

5. Communication Interface

External MCU can communicate with SR1N001F by 2 communication bus interfaces: SPI, and SR1N001F plays the slave role.

SR1N001F supports two SPI data transfer formats. Please check the following sections.

5.1 Default Format

Figure 5-1 shows the default SPI transfer format. (CKPHA=1)

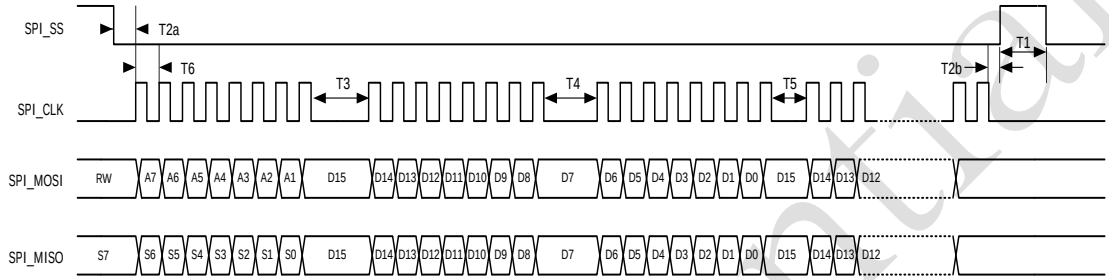


Figure 5-1 Default SPI Transfer Format.

5.2 Optional Format

Figure 5-2 shows the optional SPI transfer format. (CKPHA=0)

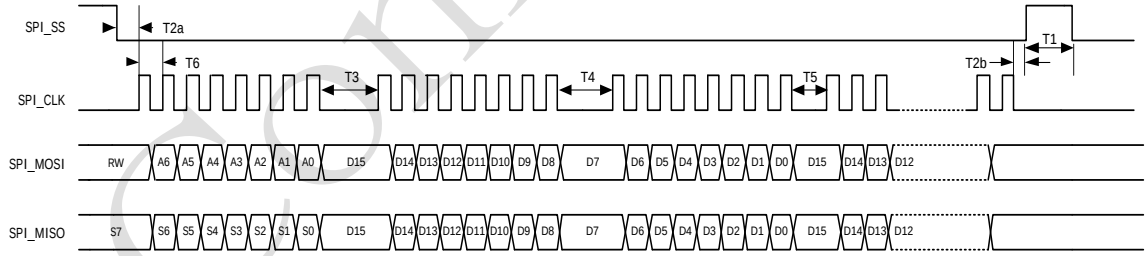


Figure 5-2 Optional SPI Transfer Format

SPI Operation highlights:

1. Polarity of SPI transfer R/W bit: 0, write; 1, read.
2. Access to the FIFO register is byte-to-byte (always integer multiples of 8-bytes). The transferring bit sequence is most significant bit first (bit 15 for word transfer, bit 7 for byte transfer). Accessing to multiple FIFO bytes may be combined into one or more SPI_SS cycles if desired.
3. Except the FIFO register, all register is always accessed by word length (16-bit).
4. Access to multiple registers may be combined into one SPI_SS cycle. If combined, address is written only once at the beginning of the SPI cycle, then each 16-bit register value follows. The SR1N001F will automatically increase the register access address each time a word is read or written. In case of doubting or confusing about the operation, just use separate SPI_SS cycles to access the registers.
5. MISO return status byte will be the same as the top byte of REG30. (Contains the result of CRC and FEC error check, and the status of framer state)

5.3 SPI Timing Requirements

Name	Min	Typ	Max	Description
T1	250 ns			Interval between two SPI access
T2a, T2b	41.5 ns			Related timing intervals between SPI_SS and SPI_CLK
T3	Note 1			Interval between address and data
T4	Note 1			Interval between high byte and low byte
T5	Note 1			Interval between two register data
T6	83 ns			SPI_CLK period

Table 5-1 The SPI Timing Requirement

Note:

When MCU/Application reads FIFO register, at least 450 ns wait time is required for the framer to get correct FIFO read pointer.

Except the FIFO register, the register access time (T3) is 41.5 ns.

6. Operation State Diagram

Figure 6-1 shows the abstract state transition for SR1N001F operation.

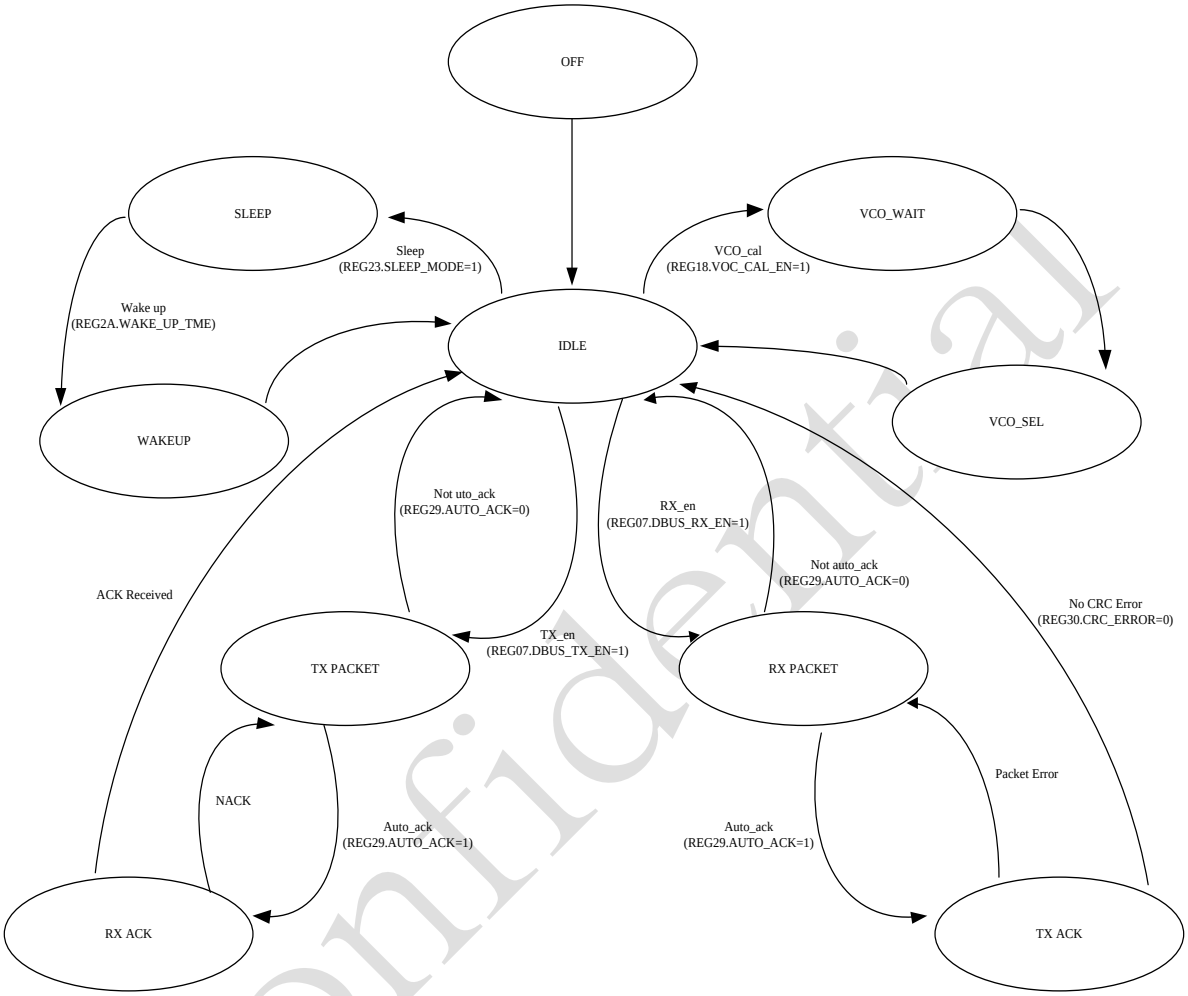


Figure 6-1 The State Transition Diagram

7. Registers

7.1 Register Summary

Table 7-1 shows the basic registers information for SR1N001F.

Address	Name	Value After Reset	RW	Note
8'h00:8'h05	Reserved			
8'h06	REG03[7:0]		R	TX/RX status register
8'h07	REG03[15:8]		R	
8'h08:8'h0B	Reserved			
8'h0C	REG06[7:0]		R	RSSI value register
8'h0D	REG06[15:8]		R	
8'h0E	REG07[7:0]		R	Synthesizer TX RX control register
8'h0F	REG07[15:8]		R	
8'h10:8'h11	Reserved			
8'h12	REG09[7:0]	8'h50	RW	PA control register
8'h13	REG09[15:8]	8'h23	RW	
8'h14	REG0A[7:0]	8'hF5	RW	AMS test control register 1
8'h15	REG0A[15:8]	8'h7F	RW	
8'h16	REG0B[7:0]	8'h08	RW	AMS test control register 2
8'h17	REG0B[15:8]	8'h40	RW	
8'h18:8'h2D	Reserved			
8'h2E	REG17[7:0]	8'h05	RW	TX/RX VCO_CAL control register
8'h2F	REG17[15:8]	8'h00	RW	
8'h30:8'h39	Reserved			
8'h3A	REG1D[7:0]		R	Manufacturer revision code register
8'h3B	REG1D[15:8]		R	
8'h3C	REG1E[7:0]		R	Manufacturer ID code register (LSB)
8'h3D	REG1E[15:8]		R	
8'h3E	REG1F[7:0]		R	Manufacturer ID code register (MSB)
8'h3F	REG1F[15:8]		R	
8'h40	REG20[7:0]	8'h06	RW	Packet configuration register
8'h41	REG20[15:8]	8'h18	RW	
8'h42:8'h45	Reserved			

8'h46	REG23[7:0]	8'h80	RW	Miscellaneous control register 1
8'h47	REG23[15:8]	8'h03	RW	
8'h48	REG24[7:0]	8'h00	RW	SYNCWORD register 1
8'h49	REG24[15:8]	8'h00	RW	
8'h4A	REG25[7:0]	8'h00	RW	SYNCWORD register 2
8'h4B	REG25[15:8]	8'h00	RW	
8'h4C	REG26[7:0]	8'h00	RW	SYNCWORD register 3
8'h4D	REG26[15:8]	8'h00	RW	
8'h4E	REG27[7:0]	8'h00	RW	SYNCWORD register 4
8'h4F	REG27[15:8]	8'h00	RW	
8'h50	REG28[7:0]	8'h07	RW	FIFO/SYNCWORD threshold value configuration register
8'h51	REG28[15:8]	8'h21	RW	
8'h52	REG29[7:0]	8'h00	RW	Miscellaneous register 2
8'h53	REG29[15:8]	8'h00	RW	
8'h54	REG2A[7:0]	8'h6B	RW	Miscellaneous register 3
8'h55	REG2A[15:8]	8'hFD	RW	
8'h56	REG2B[7:0]	8'h0F	RW	Miscellaneous register 4
8'h57	REG2B[15:8]	8'h00	RW	
8'h58:8'h5F	Reserved			
8'h60	REG30[7:0]		R	Operating status register
8'h61	REG30[15:8]		R	
8'h62:8'h63	Reserved			
8'h64	FIFO_OUT	8'h00	RW	FIFO read/write port
8'h65				
8'h66:8'h67	Reserved			
8'h68	FIFO_W_PTR	8'h00	RW	FIFO pointers configuration register
8'h69	FIFO_R_PTR	8'h00	RW	

Table 7-1 Registers Summary

7.2 Register Description

7.2.1 REG03

Address: 8'h06				
Bit	Symbol	Value After Reset	RW	Description
15	VPON	xb	R	VCO curve selection indicators. If the correct VCO value is selected, the value of {VPON, VTFREQ} should be 2'b11.
14	VTFREQ	xb	R	
13	APLL_LOCK	xb	R	1: The APLL is locked. 0: Otherwise
12	RF_SYNTH_LOCK	xb	R	1: The RF synthesizer is locked 0: Otherwise
11-10		00b	R	Reserved bits
9	RF_FIN	xb	R	1: The RC CALC circuit has finished the RC calculation. 0: Otherwise
8	CAL_ERR_SEL	xb	R	1: Indicates no proper VCO curve has been found. Refer REG17. 0: Otherwise
7-4	RAW_VCO_SEL	xxxxb	R	Indicates the current VCO frequency band setting after automatic calibration. Refer to REG17.
3-0	TEMP	xxxxb	R	Indicates the current temperature range from analog circuit.

7.2.2 REG06

Address: 8'h0C				
Bit	Symbol	Value After Reset	RW	Description
15-10	RAW_RSSI	xxxxb	R	The raw RSSI value from analog circuit. For debugging only.
9	AGC	xb	R	Indicates the current I-bit AGC value.
9-6		xxxb	R	Reserved bits.
5-0	RSSI_LATCH	xxxxxxb	R	Latched RSSI value.

7.2.3 REG07

Address: 8'h0E				
Bit	Symbol	Value After Reset	RW	Description
15-14		00b	RW	Reserved
13-9	SWALLOW	00000b	RW	Synthesizer Swallow counter.
8	DBUS_TX_EN	0b	RW	1: Trigger the TX operation sequence. 0: Otherwise This field and DBUS_RX_EN field should be mutually exclusive.
7	DBUS_RX_EN	0b	RW	1: Trigger the RX operation sequence. 0: Otherwise. This field and DBUS_TX_EN field should be mutually exclusive. Otherwise, the configuration to Thunder will not work.
6-0	RF_PLL_CH_NO/ RF_PLL	110000b	RW	The RF channel frequency selector.

7.2.4 REG09

Address: 8'h12				
Bit	Symbol	Value After Reset	RW	Description
15-13	PAB	001b	RW	PA bias current control. The value of PAB [2] is complemented. 3'b000: Level 4 (middle) 3'b011: Level 7 (Lowest) 3'b100: Level 0 (Highest) 3'b111: Level 3
12		0	RW	Reserved
11-8	PA_PWR1_REG	0011b	RW	PA power level control. 4'h0: x → Highest power 4'hF: x → Lowest power
7-5	PAGV	010b	RW	PA gate voltage control. PAGV use 2's complement.. 3'b000: Level 4 (middle) 3'b011: Level 7 (Highest) 3'b100: Level 0 (Lowest) 3'b111: Level 3.
4-3	PA_PWR1_RAMP_CTL	10b	RW	2'b0x: No ramp up/down 2'b10: Adjust two levels per ramp-up or ramp-down. Every level stands for 1 us. 2'b11: Adjust two levels per ramp-up or ramp-down. Every level stands for 0.5 us.
2-0			RW	Reserved

7.2.5 REG0A

Address: 8'h14				
Bit	Symbol	Value After Reset	RW	Description
15	AMS_TST_ENB	0	RW	1: Enable AMS test mode and bypass the BlueRF FSM 0: Otherwise
14	APLL_TST_PD	1	RW	1: Power down the APLL.
13	RF_VCO_TST_PD	1	RW	1: Power down the RF VCO circuit.
12	SYNTH_TST_PD	1	RW	1: Power down the synthesizer circuit.
11	TX_DAC_TST_PD	1	RW	1: Power down the TX DAC.
10	TX_PA_TST_PD	1	RW	1: Power down the PA module.
9	LNA_TST_PD	1	RW	1: Power down the LNA module.
8	MIXER_TST_PD	1	RW	1: Power down the Mixer module.
7	BPF_TST_PD	1	RW	1: Power douwn the BPF.
6	RC_TST_PD	1	RW	1: Power down the RC circuit.
5	ADC_TST_PD	1	RW	1: Power down the ADC.
4	RC_TST_START	1	RW	1: Activate the RC circuit. Only valid when AMS_TST_ENB is set to 1. 0: Otherwise
3	ADC_TST_CLKEN	0	RW	1: Enable the ADC clock. Only valid when AMS_TST_ENB is set to 1. 0: Otherwise
2	TR_TST_SW	1	RW	RF switch selector when AMS_TST_ENB is set to 1. 1: RF switches to transmitting circuit. 0: RF switches to receiving path.
1	TXDAC_MOD_MON	0	RW	1: Enable DAC output monitor 0: Otherwise
0	IXTAL_OSC_EN	1	RW	1: Otherwise. 0: Force the internal oscillator off.

7.2.6 REG0B

Address: 8'h16				
Bit	Symbol	Value After Reset	RW	Description
15	CW_MODE	0	RW	1: CW mode 0: Normal mode
14	TEMP_SENS_EN	1	RW	1: The sensor is off when Band Gate is off 0: The sensor is always off.
13	BG_TST_PDN	0	RW	1: The BG power off, Valid when AMS_TST_ENB is set to 1. 0: Otherwise.
12	XTAL_TST_PDN	0	RW	1: Analog crystal buffer power off. Valid when AMS_TST_ENB is set to 1 0: Otherwise

11-10		00b	RW	Reserved bits
9	RSSI_DIS	0	RW	1: Disable the RSSI features. 0: Otherwise.
8	IRSSI_PD	0	RW	Power off RSSI.
7	TEST1_OUT_EN	0	RW	1: Select TEST1 pin as SYNTH_SIGOUT output for monitor purpose. It is redirected to BRCLK pin. 0: Otherwise
6	TEST_DIV	0	RW	1: Route the DIV signal of PFD to SYNTH_SIGOUT. (digital-analog interface pin) 0: Otherwise
5	TEST_FREF	0	RW	1: Route the FREF to SYNTH_SIGOUT. (digital-analog interface pin) 0: Otherwise
4	TEST_NA	0	RW	1: Route the CLK of N/A counter to SYNTH_SIGOUT. (digital-analog interface pin) 0: Otherwise
3	AMS_BUF_PD	1	RW	Power down control for testing buffer in mixed mode region. 1: Power down. 0: Otherwise.
2	AMS_BUF_LS	0	RW	Signal level shift control for testing buffer in mixed mode region. 1: The signal level is shifted to 0.6V. 0: No signal level shifting.
1	AMS_BUF_GN	0	RW	Gain control for testing buffer in mixed-mode region. 1: 2V/V 0: 1V/V
0	AMS_BUF_SIN	0	RW	Single end/Differential mode selector for buffer testing in mixed mode region. 1: Single end. 0: Differential mode

7.2.7 REG17

Address: 8'h2E

Bit	Symbol	Value After Reset	RW	Description
15-9		xxxhb	R	Reserved
8-4	DIT_SEED	00000b	RW	Dither seed
3	VT_COMP_PORI	0b	RW	1: Swap VPON and VTFREQ. 0: Otherwise
2	TXRX_VCO_CAL_EN	1b	RW	1: Enable VCO calibration for every TX/RX transaction 0: Otherwise
1-0	TXRX_VCO_TIM	01b	RW	The TXRX_VCO calibration waiting time. Base is 5 us. The total wait time is: Wait Time = (TXRX_VCO_TIM * 4 + 5) us

7.2.8 REG1B

Address: 8'h36				
Bit	Symbol	Value After Reset	RW	Description
15-13	SLVSEL	000b	RW	sleep mode voltage setting, default 1.5V 3'b000:1.5V, 3'b001:1.6V, 3'b010:1.7V, 3'b011:1.8V 3'b100:1.9V, 3'b101:2.0V, 3'b110:2.1V, 3'b111:2.2V
12-11	reserve	10b	RW	Don't change
10-8	NRVSEL	011b	RW	normal mode voltage setting, default 1.8V 3'b000:1.5V, 3'b001:1.6V, 3'b010:1.7V, 3'b011:1.8V 3'b100:1.9V, 3'b101:2.0V, 3'b110:2.1V, 3'b111:2.2V
7-0	reserve	00h	RW	Don't change

7.2.9 REG1D

Address: 8'h3A				
Bit	Symbol	Value After Reset	RW	Description
15-8		xxh	R	Reserved
7-4	RF_VER_ID	xh	R	This field identifies the sub version of this chip. Different metal option and different site will have different reversion ID. 0000b: No reversion letter 0001b: Reversion A 0010b: Reversion B 0011b: Reversion C
3		xb	R	Reserved
2-0	DIG_VER_ID	xh	R	Digital version specification.

7.2.10 REG1E

Address: 8'h3C				
Bit	Symbol	Value After Reset	RW	Description
15-0	ID_CODE_L	F413h	R	Least significant 16-bit of JEDEC JEP106-K Manufacture's ID code. Containing the manufacturer, part number and the revision. The LSB bit is always '1'.

7.2.11 REG1F

Address: 8'h3E				
Bit	Symbol	Value After Reset	RW	Description
15-12	RF_CODE_ID	1h	R	The number represents the tape-out times
11-0	ID_CODE_M	002h	R	The most significant portion Manufacturer's ID code.

7.2.12 REG20

Address: 8'h40				
Bit	Symbol	Value After Reset	RW	Description
15-13	PREAMBLE_LEN	000b	RW	The number of bytes in the Preamble field of RF packet. 3'h0: 1 byte 3'h1: 2 bytes 3'h2: 3 bytes 3'h3: 4 bytes 3'h4: 5 bytes 3'h5: 6 bytes 3'h6: 7 byte 3'h7: 8 bytes. Note: in transmit mode, always keep 8 bit '1010…' before BPKTCTL as sync data
12-11	SYNCWORD_LEN	11b	RW	SYNC word length in bit 2'b11: 64-bit ({REG27, REG26, REG25, REG24}) 2'b10: 48-bit ({REG26, REG25, REG24}) 2'b01: 32-bit ({REG25, REG24}) 2'00: 16-bit ({REG24})
10-8	TRAILER_LEN	000b	RW	The length of Trailer field of RF packet in bit. 3'h0: 4-bit 3'h1: 6-bit 3'h2: 8-bit 3'h3: 10-bit 3'h4: 12-bit 3'h5: 14-bit 3'h6: 16-bit 3'h7: 18-bit
7-6	DATA_PACKET_TYPE	00b	RW	The selection of data type. 2'b00: NRZ data type 2'b01: Manchester data type 2'b10: 8/10 line code 2'b11: Interleave data type
5-4	FEC_TYPE	00b	RW	FEC field type selection 2'b00: No FEC 2'b01: FEC13

				2'b10: FEC23 2'b11: Reserved.
3-1	BRCLK_SEL	011b	RW	BRCLK output selection 3'b000: Reserved 3'b001: 12 MHz 3'b010: 6 MHz 3'b011: 3 MHz 3'b100: 1 MHz 3'b101: TXCLK1M 3'b110: APLL_CLK 3'b111: Reserved
0	DIRECT_MODE	0	RW	1: TX/RX data from/to pin, off framer packet

7.2.13 REG23

Address: 8'h46

Bit	Symbol	Value After Reset	RW	Description
15	POWER_DOWN	0	W	1: Set the crystal off then enter power down mode 0: Otherwise
14	SLEEP_MODE	0	W	1: Set crystal off and then enter sleep mode 0: Otherwise
13	AUTO_RX_ACK_TIME	0	RW	Automatic receive acknowledge timing control.
12	BRCLK_ON_ SLEEP	0	RW	1: Set crystal to run under SLEEP mode or POWER DOWN mode 0: Otherwise
11-8	RE_TX_TIMES	3h	RW	The maximum retransmitting times for packet under auto-acknowledge function is enabling.
7	MISO_TRI_OPT	1	RW	1: Otherwise 0: Set SPI_MISO to tri-state when SPI_SS = 1.
6-0	SCRAMBLE_DATA	00h	RW	Whitening seed for data scramble

7.2.14 REG24

Address: 8'h48

Bit	Symbol	Value After Reset	RW	Description
15-0	SYNC_WORD [15:0]	0000h	RW	The least significant word of SYNC field in packet

7.2.15 REG25

Address: 8'h4A				
Bit	Symbol	Value After Reset	RW	Description
15-0	SYNC_WORD [31:16]	0000h	RW	The sub-least significant word of SYNC field in packet

7.2.16 REG26

Address: 8'h4C				
Bit	Symbol	Value After Reset	RW	Description
15-0	SYNC_WORD [47:32]	0000h	RW	The sub-most significant word of SYNC field in packet

7.2.17 REG27

Address: 8'h4E				
Bit	Symbol	Value After Reset	RW	Description
15-0	SYNC_WORD [63:48]	0000h	RW	The most significant word of SYNC field in packet

7.2.18 REG28

Address: 8'h50				
Bit	Symbol	Value After Reset	RW	Description
15	Reserve	0	RW	
14-11	FIFO_EMPTY_THRES	0100b	RW	The FIFO empty threshold value. When non-empty entries of FIFO is smaller than this number, FIFO_FLAG will active. Don't use 0000 value
10	Reserve	0	RW	
9-6	FIFO_FULL_THRES	0100b	RW	The FIFO full threshold value. When empty entries of FIFO is smaller than this number, FIFO_FLAG will active. Don't use 0000b value
5-0	SYNCWORD_THRES	000111b	RW	The maximum allow bit number for SYNC word in receive packet.

7.2.19 REG29

Address: 8'h52				
Bit	Symbol	Value After Reset	RW	Description
15	CRC_ON	1	RW	1: CRC on 0: CRC off
14	SCRAMBLE_ON	0	RW	1: Scramble on 0: Scramble off
13	PACK_LENTH_EN	1	RW	1: SR1N001F will take the first byte of payload as the packet length 0: Otherwise Refer to Table 7-5
12	FW_TERM_TX	1	RW	1: FW handles the packet length and HW will terminate the packet TX when FIFO write pointer is equal to FIFO read pointer. 0: FW takes care of the packet length and TX termination. Refer to Table 7-5
11	AUTO_ACK	0	RW	1: After received a packet, HW will send the ACK frame automatically. 0: Otherwise
10	PKT_HINT_PRIORIY	0	RW	1: PKT_FLAG/FIFO_FLAG output pin is active low 0: PKT_FLAG/FIFO_FLAG output pin is active high
9-8	PIN_MUX	00b	RW	'FIFO_FLAG', 'PKT_FLAG' and 'BRCLK' pin will be affected by this setting. Refer to Table 7-2, Table 7-3 and Table 7-4
7-0	CRC_INIT_DATA	00h	RW	The initial value for CRC field calculation

PIN_MUX	REG20.DIRECT_MODE	RX_EN_SYNTH (chip internal signal)	FIFO_FLAG
2'bxx	0	X	Original output
2'b00	1	X	Original output
2'b01 or 2'b10	1	0	bdata1_out(internal)
2'b01 or 2'b10	1	1	rxdata(internal)
2'b11	1	X	VTFREQ(internal)

Table 7-2 Pin MUX Table for FIFO_FLAG

PIN_MUX	REG20.DIRECT_MODE	PKT_FLAG
2'b11	1	VPON (internal)
2'b11	0	Original output
Others	X	Original output

Table 7-3 Pin MUX Table for PKT_FLAG

PIN_MUX	REG0B.TEST1_OUT_EN	REG20.BRCLK_SEL	BRCLK
2'b01	Xb	xxxb	RXCLK(internal)
2'b10	Xb	xxxb	BPKTCTL(normal)
2'b11	Xb	xxxb	Reserved
2'b00	1	xxxb	SYNTH_SIGOUT(internal)
2'b00	0	000b	0
2'b00	0	001b	XTAL_CORE(internal)
2'b00	0	010b	DIV_CLK_6M(internal)
2'b00	0	011b	DIV_CLK_3M(internal)
2'b00	0	100b	DIV_CLK_1M(internal)
2'b00	0	101b	TXCLK_1M
2'b00	0	110b	APLL_CLK
2'b00	0	111b	0

Table 7-4 Pin MUX Table for BRCLK

7.2.20 REG2A

Address: 8'h54				
Bit	Symbol	Value After Reset	RW	Description
15-10	SCAN_CHL_NO	111111b	RW	Scan RSSI channel number. Only can be read before RSSI scan done.
9-8	WAKE_UP_TIME	01b	RW	Wake up timer. The time = (1 + WAKE_UP_TIME) *4 us
7-0	RX_ACK_TIME	6Bh	RW	Time interval (us) between RX packet and AUTO ACK packet when reg29[11] =1.

7.2.21 REG2B

Address: 8'h56				
Bit	Symbol	Value After Reset	RW	Description
15	SCAN_RSSI_EN	0	RW	1: Start to scan the RSSI value for certain channel 0: Otherwise
14-8	SCAN_START_CHANNEL_OFFSET	0000000b	RW	The offset of channel to start the RSSI value scanning.
7		0	RW	Reserved
6-0	WAIT_RSSI_SCAN_TIME	0001111b	RW	The VCO & synthesizer setup time when scan the RSSI value for different channel.

7.2.22 REG30

Address: 8'h60				
Bit	Symbol	Value After Reset	RW	Description
15	CRC_ERROR	xb	R	1: CRC error is detected. 0: Otherwise
14	FEC23_ERROR	xb	R	1: FEC23 error is detected 0: Otherwise
13-8	FRAMER_ST	XXXXXXb	R	State of internal framer FSM
7	SYNCWORD_REV	xb	R	1: The SYNC word is received. Only valid on RX mode 0: Otherwise
6	PKT_FLAG	xb	R	The PKT_FLAG pin out value.
5	FIFO_FLAG	xb	R	The FIFO_FLAG pin out value
4-1	CH_NO	xxsxb	R	The least significant 4-bit of channel number that operating currently.
0	POR	xb	R	Reserved

7.2.23 FIFO_OUT

Address: 8'h64				
Bit	Symbol	Value After Reset	RW	Description
15-0	TXRX_FIFO	xxxxh	RW	The FIFO port for external MCU to transmit/receive the packet data

7.2.24 FIFO_CTRL

Address: 8'h68				
Bit	Symbol	Value After Reset	RW	Description
15	CLR_W_PTR	0	W	Write 1 to clear the TX FIFO_W_PTR to 0. Only valid in TX operation
14		0		Reserved
13-8	FIFO_W_PTR	00h	R	The FIFO pointer for write.
7	CLR_R_PTR	0	W	Write 1 to clear the RX FIFO_R_PTR to 0. Only valid in RX operation
6		0		Reserved
5-0	FIFO_R_PTR	00h	R	The FIFO pointer for read.

REG29.PACK_LENGTH_EN	REG29.FW_TERM_TX	Description
MCU handles the packet length)	0	Transmit will stop only when REG07.DBUS_TX_EN is set to 0. Receive will stop when REG07.DBUS_RX_EN is set to 0
	1	Transmit will stop automatically when the FIFO runs empty. Receive will stop only when REG07.DBUS_RX_EN is set to 0
1 (Internal Framer handle the packet length)	x	The 1st byte of payload will be taken as the packet length by hardware. The range of length is 0 to 255 bytes Transmit will stop automatically when the designated packet bytes are transmitted.

Table 7-5 The Packet Payload Length Determination

8. Usage Notes

SR1N001F RF Transceiver is developed to be an easy-to-attached wireless communication component for various systems. By simple SPI bus interface, the external MCU can transmit/receive data through SR1N001F without much effort. The following sections will provide the guidelines and some answers of frequently asking questions to help users to understand and use this chip.

8.1 Power On and Register Initialization Sequence

Figure 8-1 shows the power on, reset and register configuration sequence when external power (VDD) is applied.

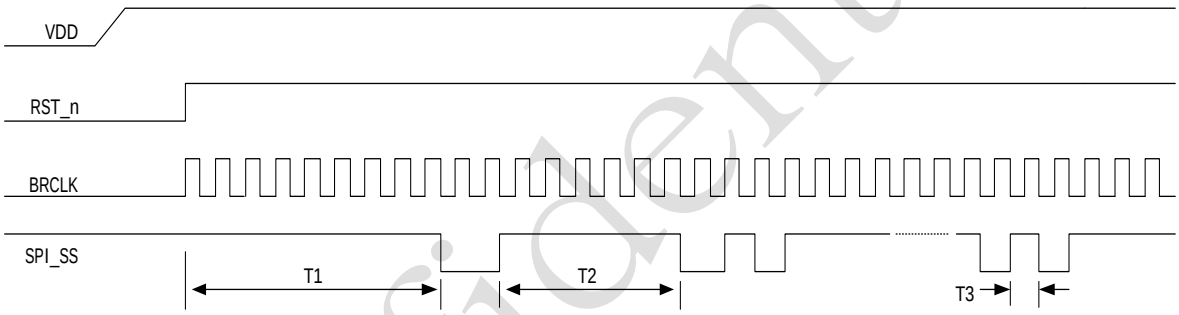


Figure 8-1 The Power On and Register Configuration Sequence

1. After VDD power is ready, make sure the RST_n pin stays low.
2. After RST_n pin is released (pull high), the BRCLK pin will output a clock which frequency is 12MHz.
3. Host must wait T1 (1 to 5 ms) for crystal oscillator stabilization, then external MCU/Application can start to configure the control registers of SR1N001F.
4. After the registers configuration is done, SR1N001F will be ready to work.

Figure 8-2 shows the initialization flowchart for SR1N001F.

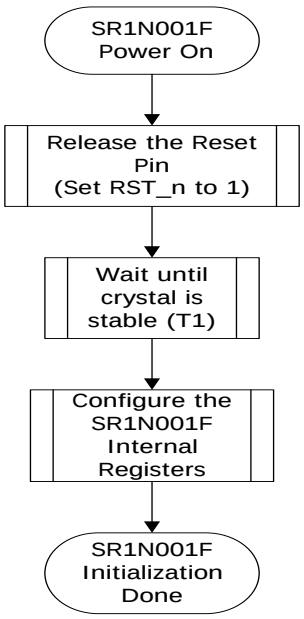


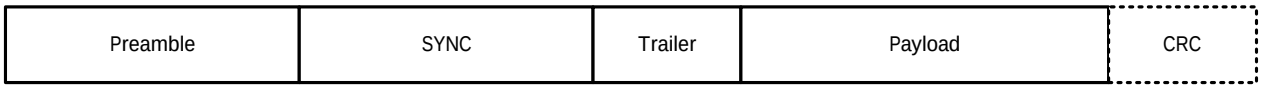
Figure 8-2 The SR1N001F Initialization Flowchart

8.2 Enter Sleep State and Wakeup

To reduce the power consumption, external MCU can configure the SR1N001F to enter the SLEEP state. SR1N001F will enter the SLEEP state once upon the SPI_SS is pulled up at the transaction that external MCU set the REG23.SLEEP_MODE to 1. When the chip is at the SLEEP state, if the SPI_SS is pulled low by the external MCU, the chip will wake up automatically. But be careful that MCU have to wait for a certain period (the time period that RFIC crystal requires for the stabilization) before toggles the SPI_CLK and SPI_MISO/SPI_MOSI pins.

8.3 Packet Data Structure

The basic packet format to be RX/TX is shown on the following diagram.



- Preamble: 1 ~ 8 bytes, programmable.
- SYNC: 16/32/48/64 bits, programmable as device syncword.
- Trailer: 4 ~ 18bits, programmable.
- Payload: TX/RX data. There 4 data types:
  1. Raw data
  2. 8b/10b line code
  3. Manchester
  4. Interleave with FEC option
- CRC: 16 bits. This field is optional.

Figure 8-3 The Packet Structure

8.4 FIFO Pointer Clear

The FIFO read pointer can be cleared manually by writing 1 to the FIFO_CTRL.CLR_R_PTR.

The FIFO writer pointer can be cleared manually by writing 1 to the FIFO_CTRL.CLR_W_PTR.

To transmit the data, the FIFO write & read pointer must be cleared before the transmitted data is written into the FIFO port. The FIFO write pointer can be cleared automatically when the SYNC word is received too.(But read pointer cannot be cleaned automatically)

To receive the data, after SYNC word received, read/write pointer will be cleaned to 0 automatically.

8.5 Packet Payload Length

There are two ways to handle the length of TX/RX packet in SR1N001F. If the value of REG29.FW_TERM_TX is set to 1, SR1N001F will take the first byte of payload to be the packet length. If the value of REG29.FW_TERM_TX is 0, the TX/RX packet length is determined by either TX FIFO is running empty, or DBUS_TX_EN bit is cleared. Table 7-5 shows the detail.

8.6 Framer Handles Packet Length

When REG29.PACK_LENGTH_EN is set to 1, the internal framer of SR1N001F will handle the packet length and take care of the TX/RX start and stop automatically. The first byte of payload on TX/RX transaction will be regarded to contain the packet length information. (Note, the first byte is excluded from the real payload byte count). Hence, the range of payload length is from 0 byte to 255 bytes. The following sections give more detail information about the TX and RX respectively.

8.6.1 Transmit Timing

The packet TX diagram is shown on Figure 8-4. After external MCU selects a proper channel and sets REG07.DBUS_TX_EN to 1, the framer will generate the packet using payload data from FIFO automatically. External MCU has to write the transmit data to FIFO before the internal framer sends the 'Trailer' bits.

If the desired TX data length exceeds the capacity of FIFO, multiple data writes to FIFO is necessary. The FIFO_FLAG pin out indicates whether the FIFO is empty or not during the TX condition.

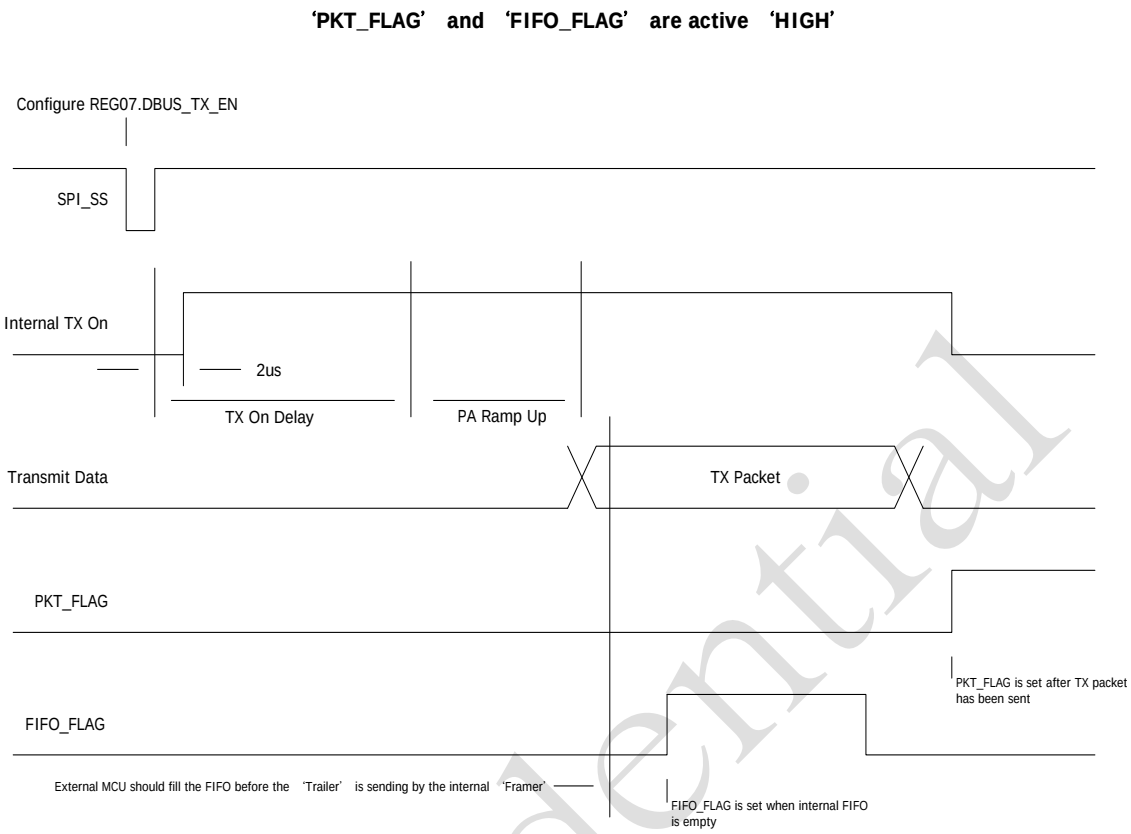


Figure 8-4 The TX Timing Diagram for Framer Handles the Packet Length

Figure 8-5 shows the configuration and interrupt handling sequence flowchart.

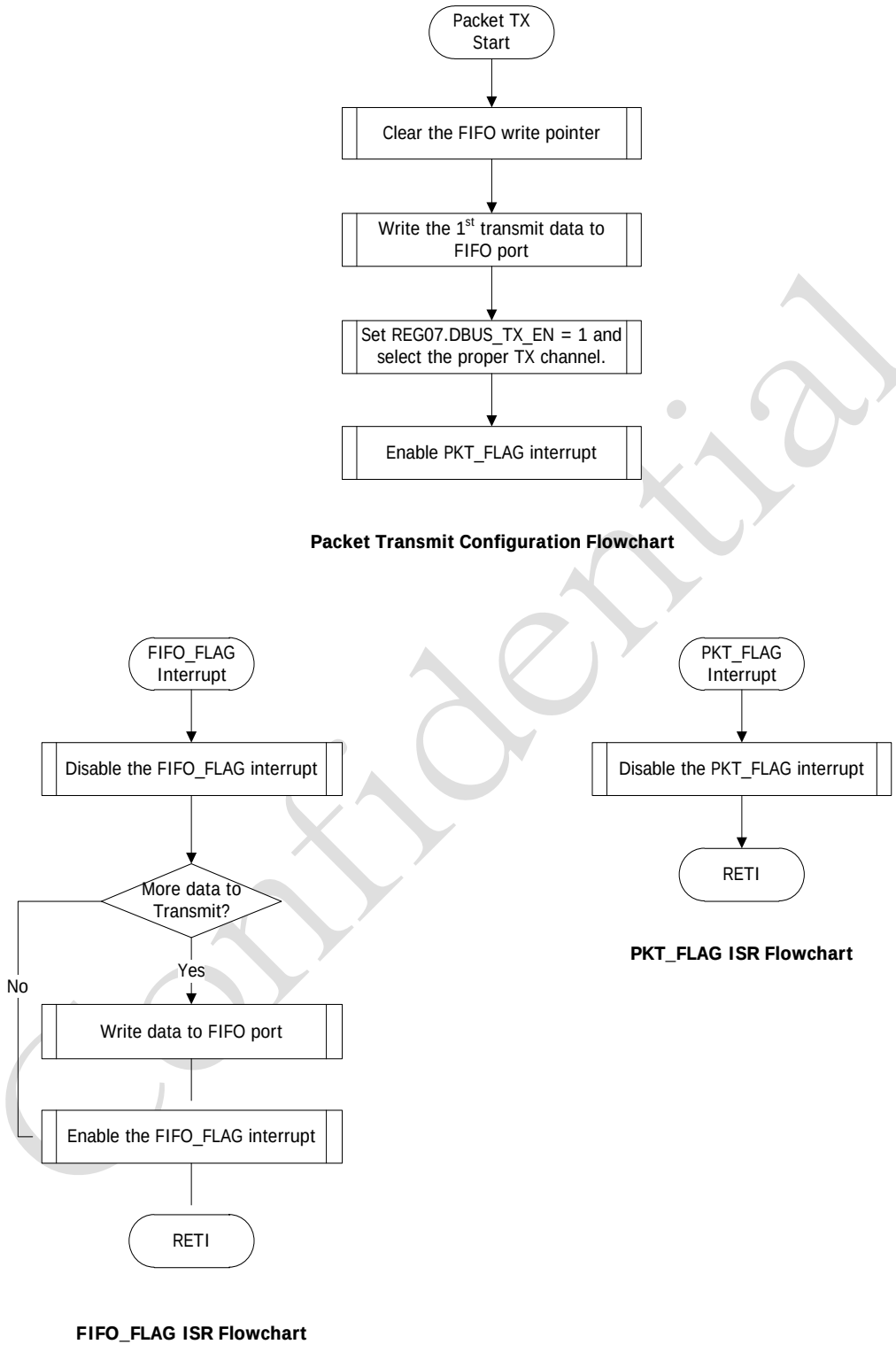


Figure 8-5 The Flowcharts for TX Operation Configuration and ISR

8.6.2 Receive Timing

The RX timing diagram is shown on Figure 8-6. When external MCU set the REG07.DBUS_RX_EN to 1 and selects the desired receiving channel, SR1N001F framer will turn on the receiver and starts to detect the valid SYNCWORD.

If valid SYNCWORD is found, the internal framer will process packet automatically. When the packet is received completely, framer will return to IDLE state.

If the length of received packet exceeds the capacity of FIFO memory (63 bytes), FIFO_FLAG will go active to inform the external MCU to read out the data from FIFO.

Since the real world environment is not perfect, the weak signal, multipath signal cancelation, device out of range, etc., the valid SYNCWORD is not always available. To accommodate these situations and prevent the lockup, external MCU should use a timer to generate timeout signaling to avoid the infinite waiting. In most application, receive packet are expected to arrive within a defined 'timing window'. If the packet is not received during the pre-defined 'timing window', the system can use either polling or timer-base interrupt to correct it.

Figure 8-6 shows the timing diagram for RX packet.

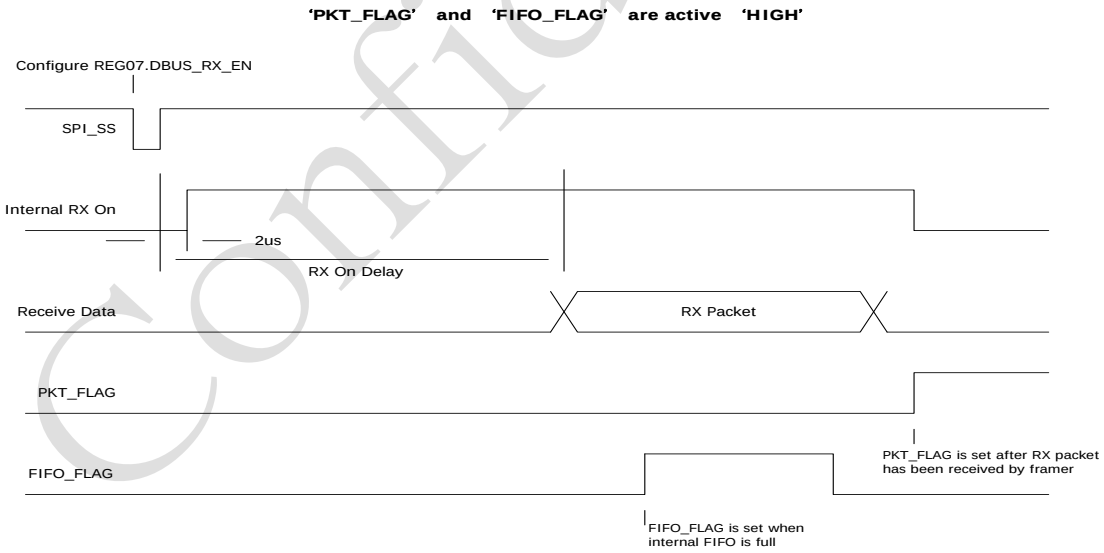


Figure 8-6 The RX Timing Diagram for Internal Framer Handles the Packet Length

Figure 8-7 shows the configuration and interrupt handling sequences.

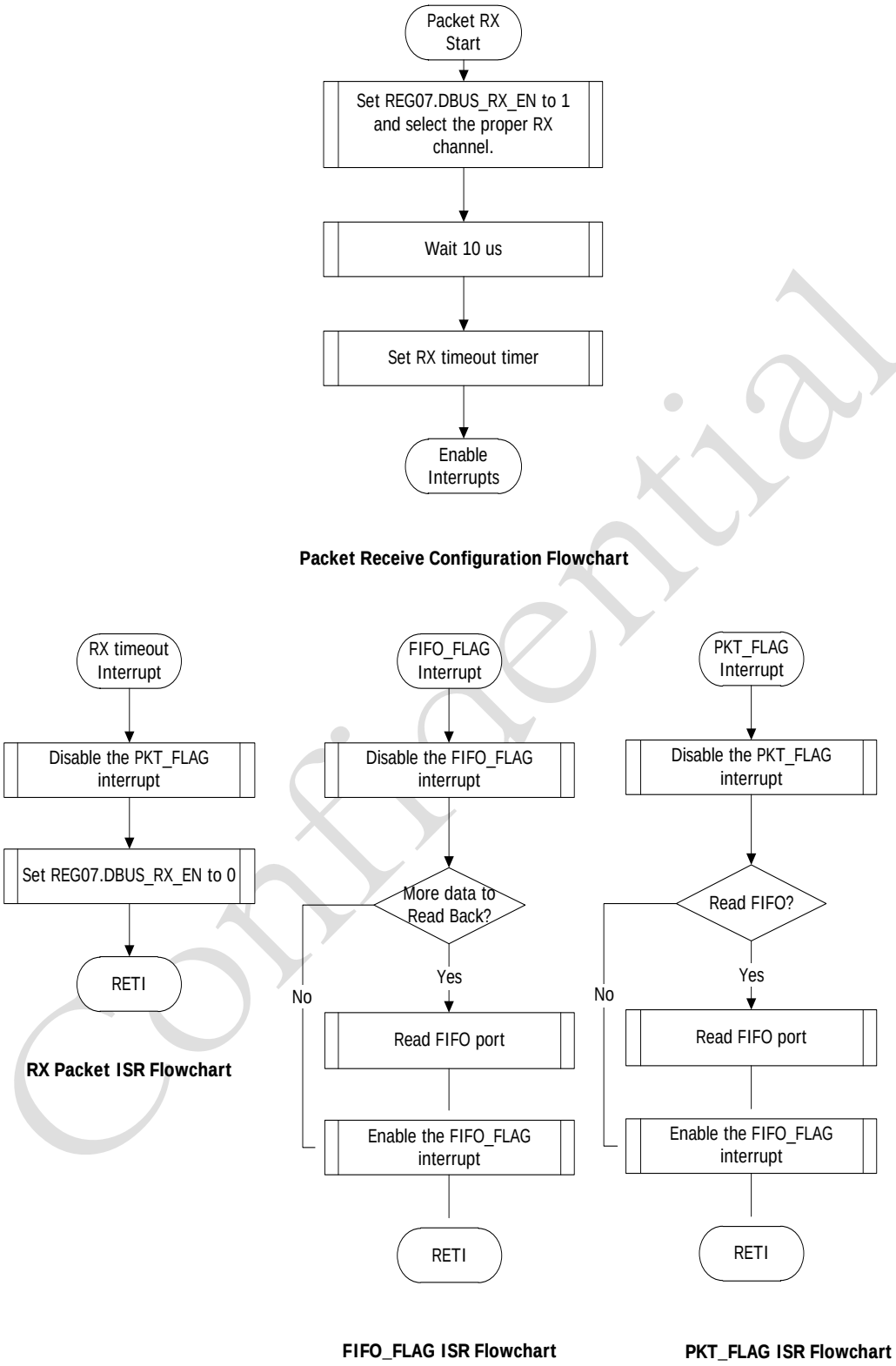


Figure 8-7 The Flowcharts for RX Operation Configuration and ISR

8.7 MCU/Application Handles Packet Length

IF REG29.PACK_LENGTH_EN is set to 0, the external MCU should take care of the TX/RX packet length handling. Depending on the value of REG29.FW_TERM_TX, the handling sequences are different. Please check the following sections for detail information.

8.7.1 REG29.FW_TERM_TX = 1 for Packet TX

If REG29.FW_TERM_TX is set to 1, SR1N001F will compare the FIFO write pointer and FIFO read pointer continuously during the packet TX process. If external MCU stops writing data to FIFO, the framer will detect the FIFO empty eventually. Upon the FIFO empty condition is detected, the framer will cease the packet transmission automatically. The timing diagram is show on Figure 8-8.

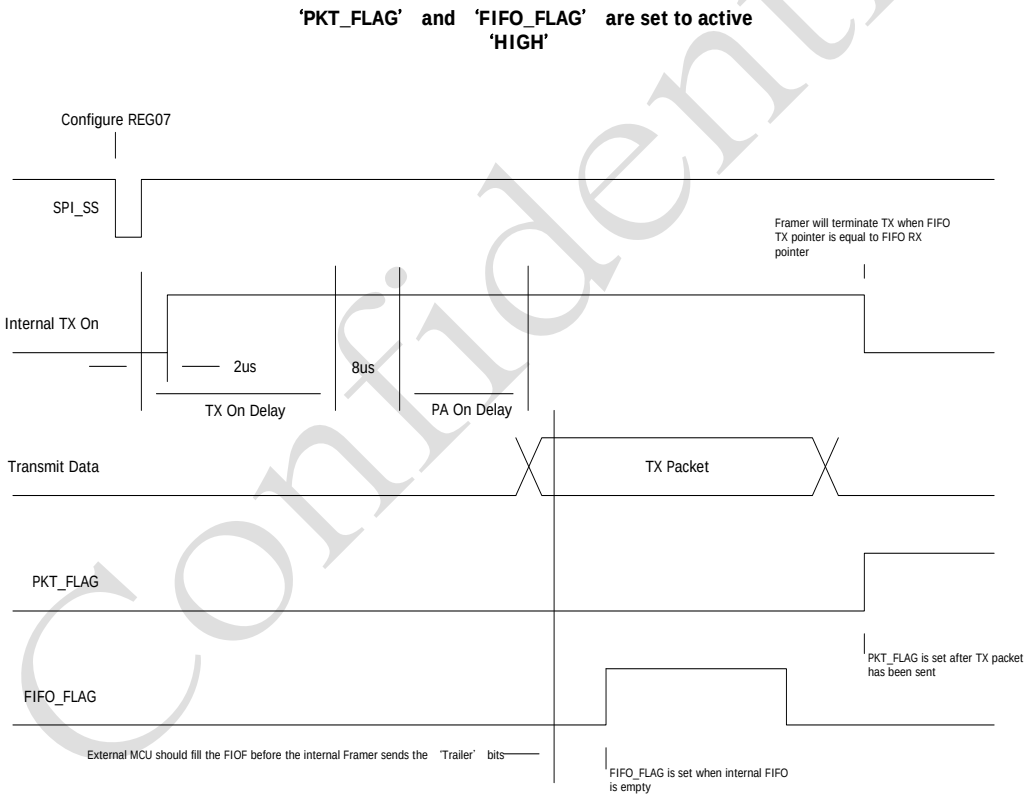
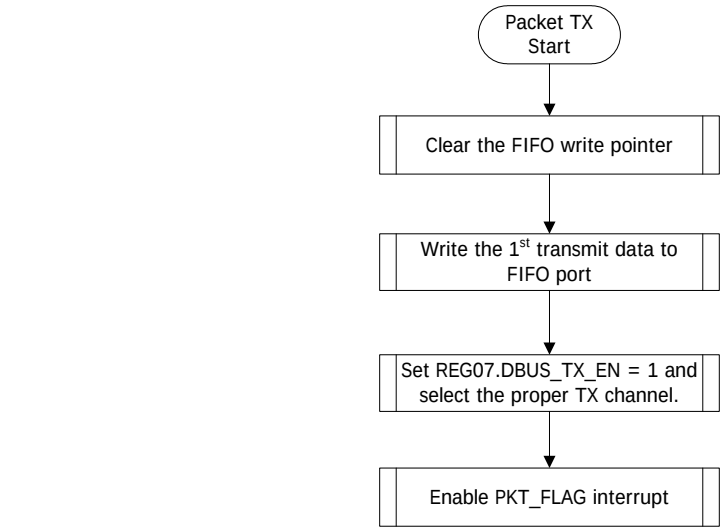


Figure 8-8 Packet TX Timing Diagram for TX Stopped When FIFO is Empty

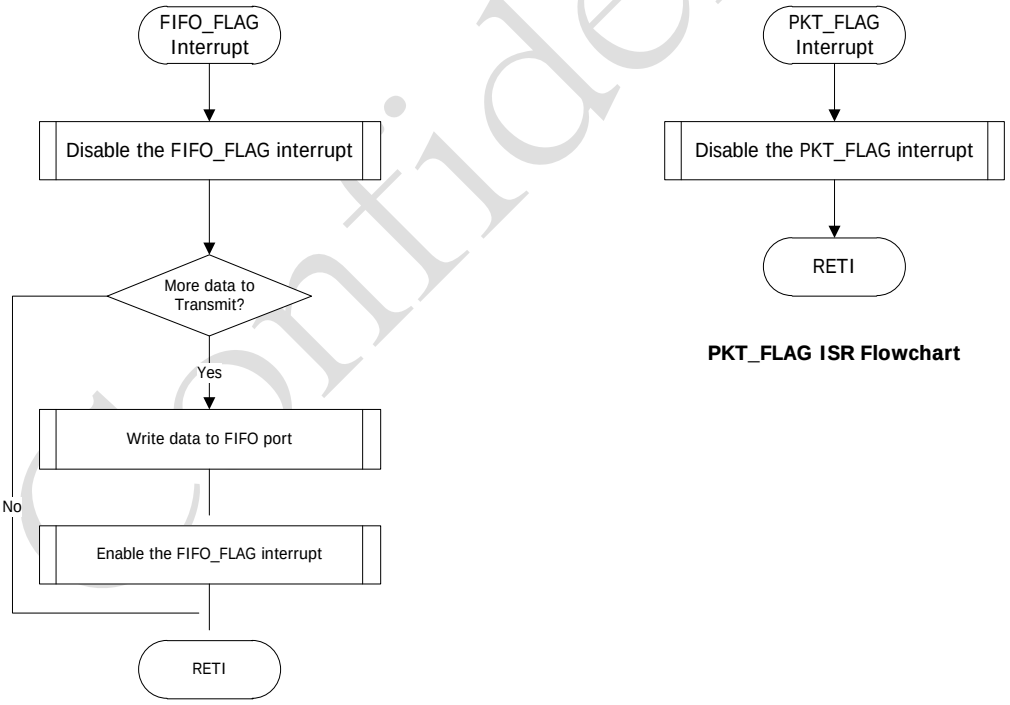
Note:

When REG29.PACK_LENGTH_EN = 0, external MCU should never allow the FIFO underflow or FIFO overflow to happen. The REG28.FIFO_EMTPY_THRES and REG28.FIFO_FULL_THRES should be set properly to make the alert to MCU. The best value to set is depends on the SPI transmission speed and the MCU processing capability.

Figure 8-9 shows the flowcharts for TX operation configuration and interrupts processing sequence.



Packet Transmit Configuration Flowchart



PKT_FLAG ISR Flowchart

FIFO_FLAG ISR Flowchart

Figure 8-9 The Flowchart of Packet TX Configuration and ISR

8.7.2 FW_TERM_TX = 0 for Packet TX

If the value of REG29.FW_TERM_TX is set to 0, SR01T framer will not stop the packet transmission until the external MCU write 0 to REG07.DBUS_TX_EN. Packet transmission continues even the FIFO empty occurred. Figure 8-10 shows the related timing sequence.

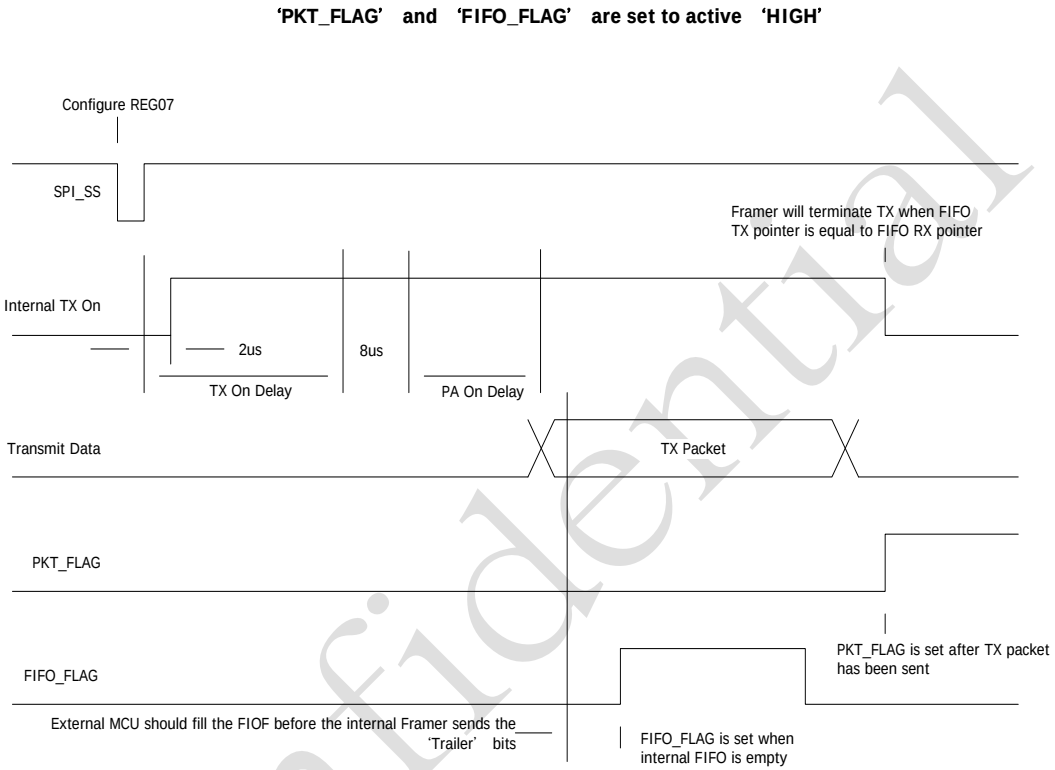


Figure 8-10 The Timing Diagram for TX Framer Stopped when TX Enable Is Cleared

Note:

When REG29.PACK_LENGTH_EN = 0, external MCU should never allow the FIFO underflow or FIFO overflow to happen. The REG28.FIFO_EMTPY_THRES and REG28.FIFO_FULL_THRES should be set properly to make the alert to MCU. The best value to set is depends on the SPI transmission speed and the MCU processing capability.

Figure 8-11 shows the TX operation flowchart.

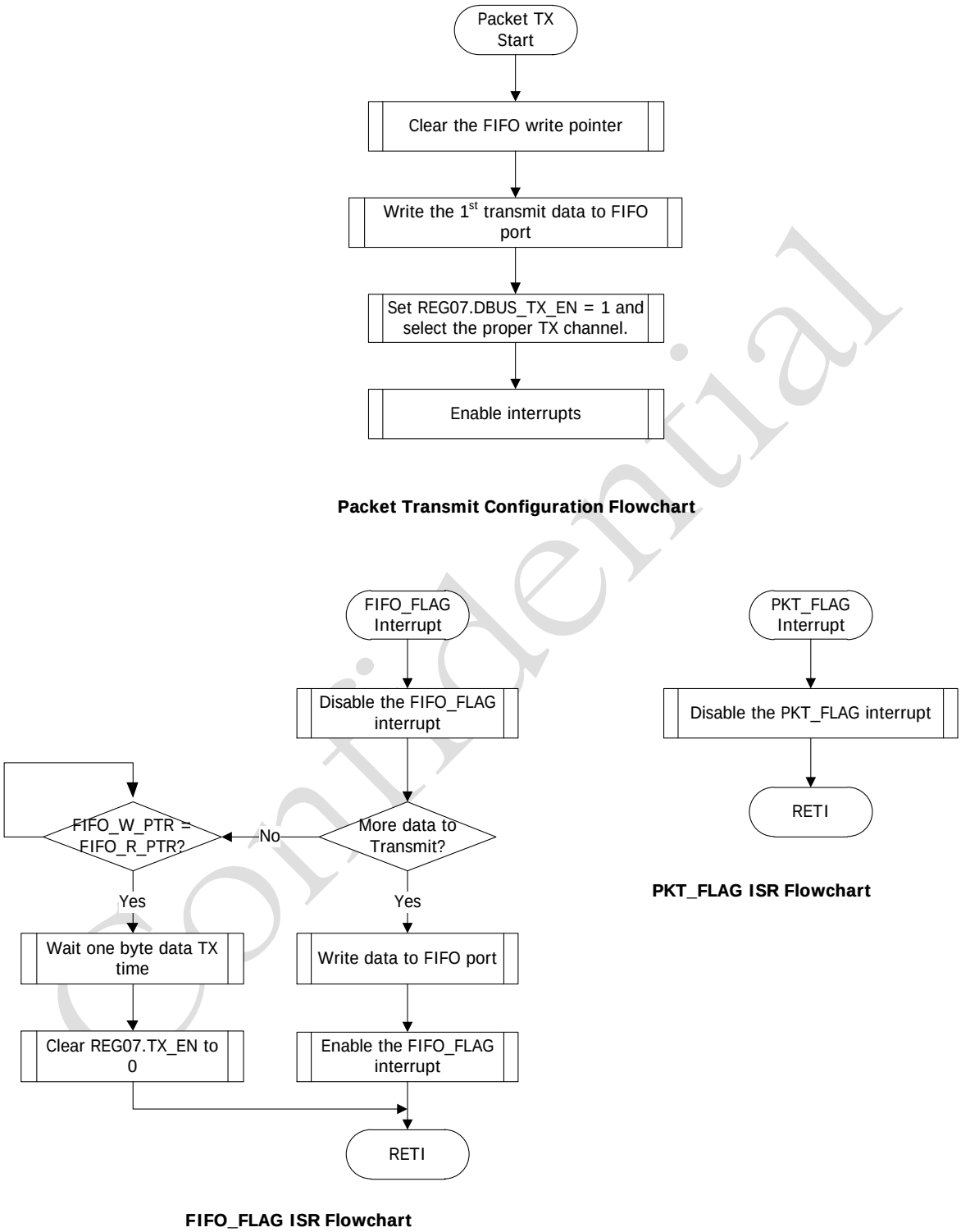


Figure 8-11 The Flowchart to Configure and ISR

8.7.3 FW_TERM_TX = 0 or FW_TERM_TX =1 for Packet RX

When the value of REG29.PACK_LENGTH_EN is set to 0, packet reception starts when external MCU sets the REG07.DBUS_RX_EN to 1. At this time, the framer will automatically turn on the receiver to frequency channel specified by the fields in REG07. After waiting for the designated timing period for ready of internal synthesizer and receiver, the framer will start to detect the SYNCWORD from the receiving signal. After a completed SYNCWORD is detected, the PKT_FLAG is active to inform the external MCU, and the received data will be written into the FIFO. After MCU read the 1st byte from the FIFO, the PKT_FLAG will be inactive.

The packet RX will be stopped after external MCU write 0 to REG07.DBUS_RX_EN.

Figure 8-12 shows the packet RX operation sequence.

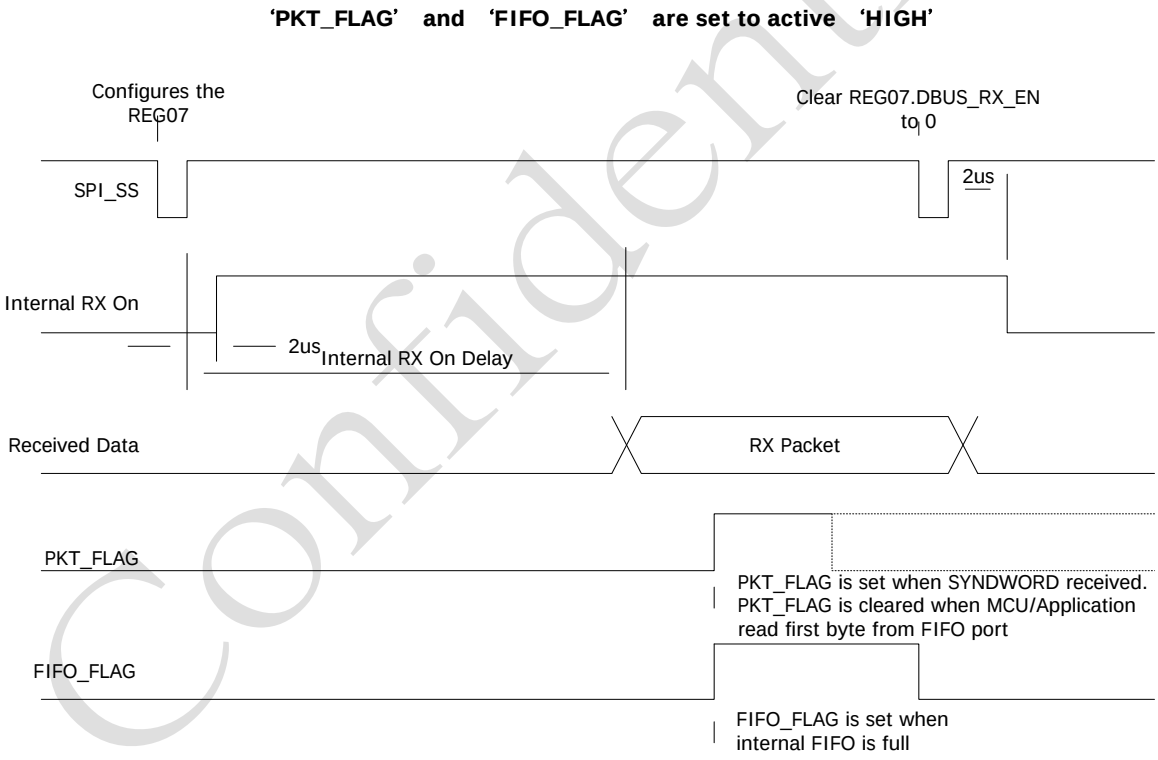
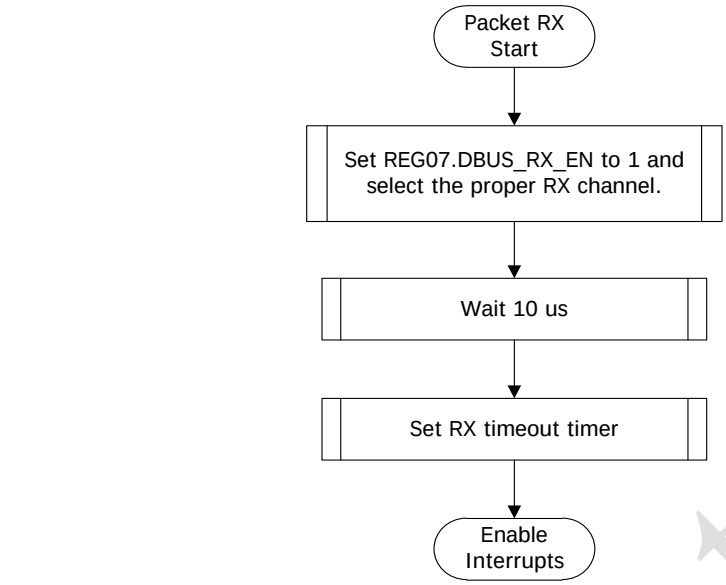
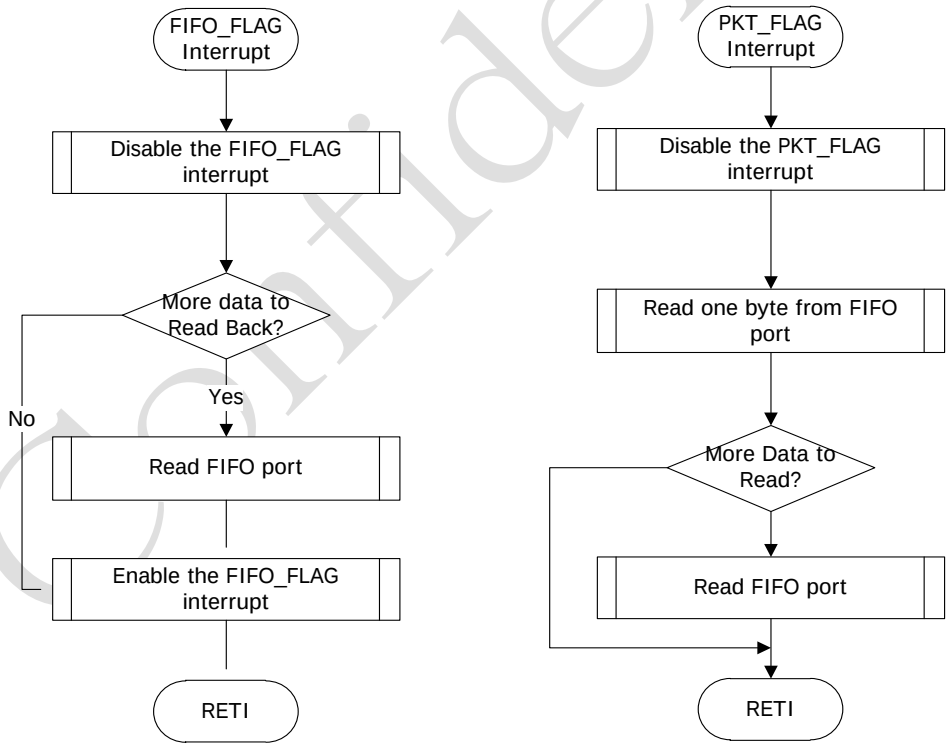


Figure 8-12 The Timing Diagram for RX Stopped when RX Enable Is Cleared

Figure 8-13 shows the packet RX configuration and interrupt handling flowchart.



Packet Receive Configuration Flowchart



FIFO_FLAG ISR Flowchart **PKT_FLAG ISR Flowchart**

Figure 8-13 The Flowchart for Packet RX Configuration and ISR

8.8 Crystal Oscillator

SR1N001F supports the quartz crystal, or external clock input. The following sections show some detail about the usage.

8.8.1 Quartz Crystal Application

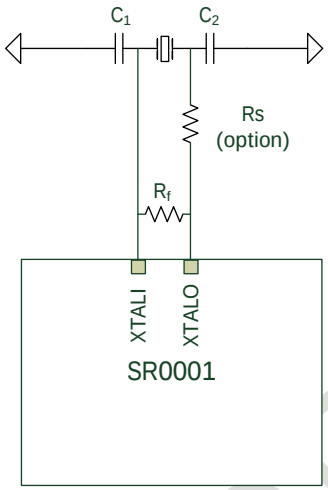


Figure 8-14 The Quartz Crystal Connection

Series resister R_s limits the power to the crystal, and contributes to the phase shift necessary for oscillation. Crystal loading capacitances C_1 and C_2 determines the load seen by the crystal, which should match the vendor's specification. Self-bias resister R_f, from buffer output to input, serves the self-bias the on-chip buffer to the center of the linear region for maximum gain.

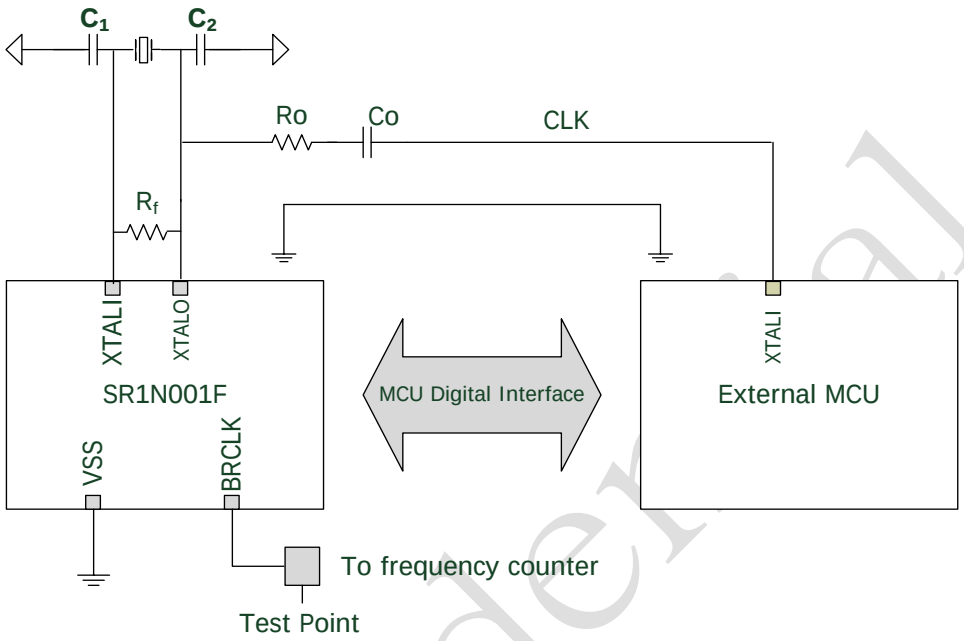
8.8.2 External Clock Application

Please refer to Figure 8-15. The self-bias resister R_f should still be used, but the external clock may be coupled to the XTALO pin via a series DC blocking capacitors.

Output resister R_o is used to sample a small amount of power from an existing oscillator or clock circuit. The best value of Ro may need to be determined experimentally, but around 3k Ohms is a good starting point. In the extreme case of R_o being too large, the RFIC will fail to initialize to the IDLE state properly.

Regarding to PCB layout, the clock trace should be kept short and direct. The trace should be relatively narrow (high impedance), and must route away from other traces on the PCB

that may inject or couple noise onto the clock trace. SR1N001F will receive the clock signal relative to ground; therefore, the ground between chips should be a good low-noise, low-inductance ground. Ideally, this ground return should be a single ground plane on the PCB layout.



Notes
1. Clock duty cycle should be 50%. If not, some additional drive voltage may be required. (i.e. reduce Ro)
2. If received Bit Error Rate is high, it may be caused by insufficient clock drive to the RFIC. (i.e., reduce Ro)
3. Another possible reason for high BER is phase noise on the clock signal. Try putting 0.1 and 2.2 uF ceramic bypass capacitor across the baseband chip VDD/VSS pins that power the oscillator.

Figure 8-15 The Example of External Clock Application

8.9 Minimum Pin Count

SR1N001F provides a great flexibility for external MCU to TX/RX packet over-the-air with limited pin connection. The following statements provide the system architect some ideas to reduce the BOM cost.

FIFO_FLAG pin: This pin is only necessary when the TX/RX payload length is larger than 63 bytes. For the application which transfers short packet only, this pin can be ignored.

PKT_FLAG pin: This pin is used to identify the packet received. If the multi-tasking is not a critical point for the application, this pin can be ignored by taking advantage of polling to status register of SR1N001F.

RST_n pin: This pin is sometimes connected through an RC filter to the VDD_IN, which makes the chip self-reset when power is applied. Thus, external MCU does not need to connect this pin in this case.

8.10 CKPHA

This input pin is used to select the SPI communication format between SR1N001F and external MCU. When this pin is tied to 1, only the default SPI transfer format is selected. If this pin is tied to 0, the optional SPI transfer format is chosen. Please refer to section 5.1 and section 5.2 for more detail information.

8.11 Antenna Type and Location

Probably, the key factor that affects the RF performance of SR1N001F is the antenna-bar just the antenna type, but also placement and orientation. Antenna again is normally measured with respect to isotropic, that is, an ideal radiator that sends/receives power equally from/to any direction. This ideal antenna would be described as 0dBi, or zero dB's above/below isotropic. Unfortunately, they do not exist in real world. A simple dipole with a theoretical gain of +2 dBi is usually a good choice, but the designer should exercise care when placing the antenna, since dipole antennas have a radiation pattern described as a donut, whereby the null can be very deep.

For most wireless applications, the printed full-wave loop antenna shown on the schematic should perform well, provided that the antenna is placed in the clear, away from other circuitry and wires, hands, etc. In particular, the antenna must be kept away from human tissue, the sensitive spots like the heart, brain and eyes. Violating this design principle will not only make the end product perform poorly, but also can be a danger fact to users in the long term. The violation of principles may cause the disapproval of FCC or other regulatory agencies.

So, for better performance, make the antenna away from the human body, or at least, not proximity loaded by the human body, or dielectric objects within the product.

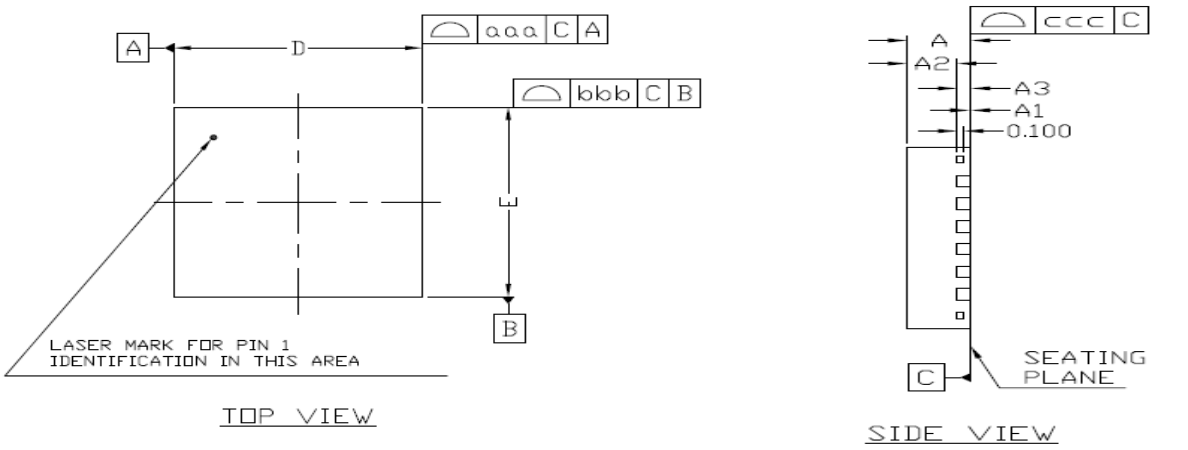
The last, be sure to keep the antenna away from the clock lines and digital bus signals; otherwise, harmonics of these signals will jam certain receive frequencies. It is just good to keep the antenna away from all wires and metal object.

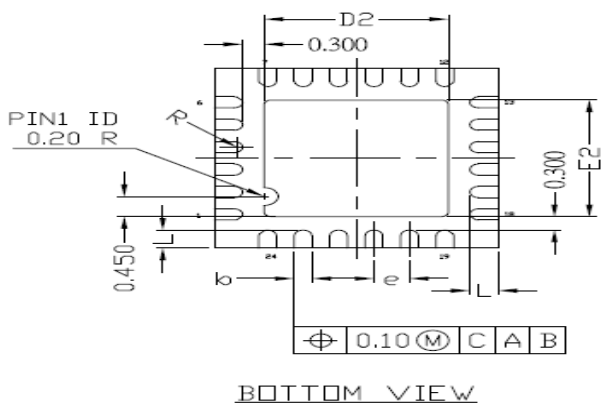
8.12 PCB Layout

Guideline for PCB layout

- RF path: Since the SR1N001F uses 2-conductor balanced transmission lines at the RF port, ground plane is not necessary along the balanced line length. Be sure to keep the length of the two conductor is equal.
- Clock trace: It is best to keep the clock trace simple and direct. The self-bias resistor should be close to the XTALI and XTALO pins. The oscillation loop, consisting of the series resistor and crystal, should be a simple and small loop. The crystal loading capacitance should be near the crystal. The ground connection to these capacitors must be a good, clean, and quiet ground. This keeps noise from becoming injected into the oscillator. It is a good reason to have one ground plane for the entire RF section.
- Power distribution and decoupling: Capacitors should be located near the VDD pins, as shown in the schematic. (Refer to section 10)
- Antenna placement: If using an antenna manufactured by a particular vendor, be sure to follow the manufacturer's recommendation regarding to layout.
- Digital interface: In order to provide a good ground return for digital lines, it is a good idea to provide at least 2 pins for ground, not just one. Good grounding between RF and MCU can help to reduce the noise 'seen' at antenna, thus improving the performance.

9. Package Outline





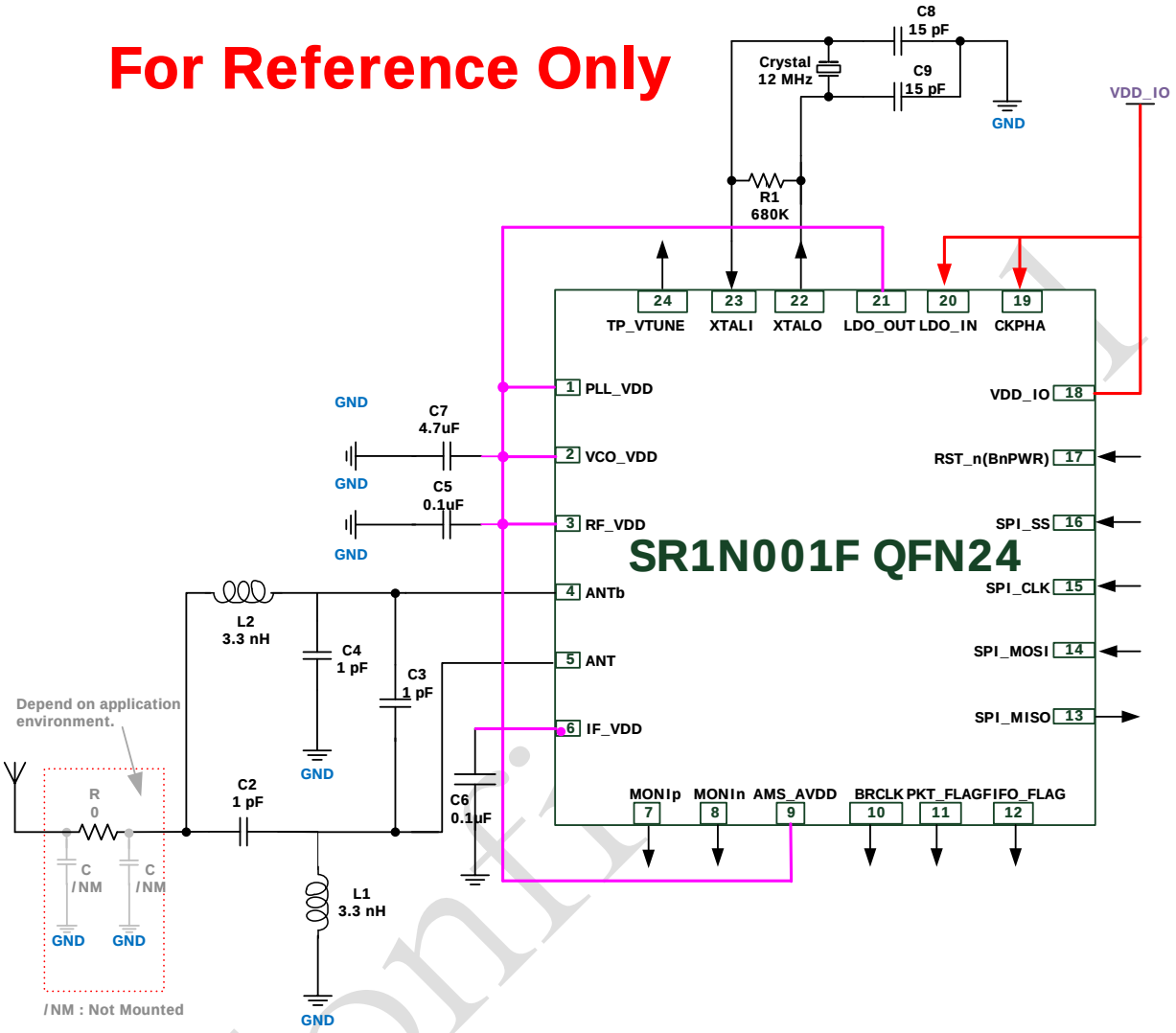
* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	0.90	–	–	0.035
A1	–	–	0.05	–	–	0.002
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	4.0 BSC			0.157 BSC		
D2	2.50	2.60	2.70	0.098	0.102	0.106
E	4.0 BSC			0.157 BSC		
E2	2.50	2.60	2.70	0.098	0.102	0.106
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 BSC			0.020 BSC		
R	0.09	–	–	0.004	–	–
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

Figure 9-1 Outline for QFN24 Package

10. Reference Design



11. IR Reflow Standard

The Following figure shows the information about IR Reflow.

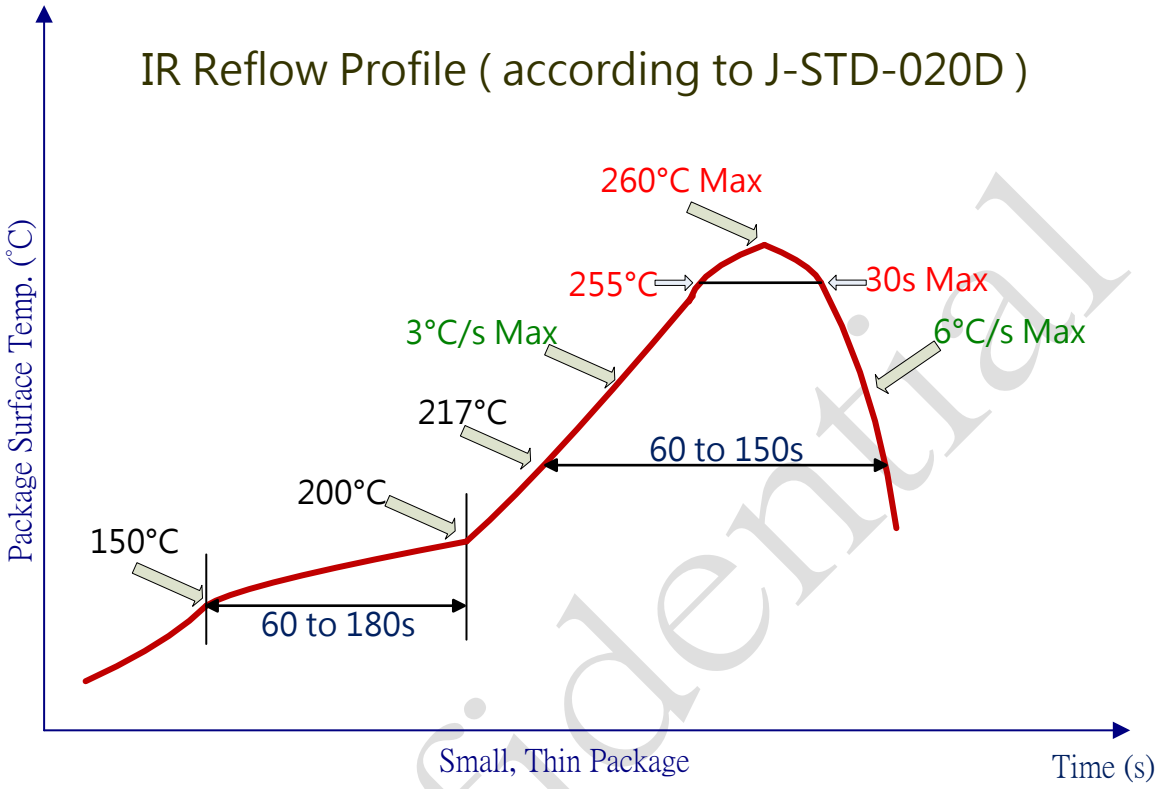


Figure 11-1 IR Reflow Temperature