USER MANUAL

Wi-Fi HaLow 802.11ah Module

Model Name: WSG300NRC

Brand: LITEON

FCC Statement

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna. Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- -Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For product available in the USA/Canada market, only channel 1~11 can be operated. Selection of other channels is not possible. This device and its antenna(s) must not be co-located with any other transmitters except in accordance with FCC multi transmitter product procedures. Referring to the multi transmitter policy, multiple transmitter(s) and module(s) can be operated simultaneously without C2PC.

IMPORTANT NOTE: FCC Radiation Exposure Statement: This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IMPORTANT NOTE: This module is intended for OEM integrator. The OEM integrator is responsible for the compliance to all the rules that apply to the product into which this certified RF module is integrated. Additional testing and certification may be necessary when multiple modules are used.

20 cm minimum distance has to be able to be maintained between the antenna and the users for the host this module is integrated into. Under such configuration, the FCC radiation exposure limits set forth for an population/uncontrolled environment can be satisfied.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:

In the user's manual of the end product, the end user has to be informed to keep at least 20 cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio frequency exposure guidelines for an uncontrolled environment can be satisfied. The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment. If the size of the end product is smaller than 8x10cm, then additional FCC part 15.19 statement is required to be available in the user's manual: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following "Contains FCC ID: PPQ-WSG300NRC". If the size of the end product is larger than 8x10cm, then the following FCC part 15.19 statement has to also be available on the label: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

OEM Integrator Checklist

The party below will implement the LITE-ON Module in host systems in accordance with the instructions specified in this document and the documents referenced herein.

- 1. The OEM integrator will ensure the Module is integrated in a host systems using only the approved antenna model(s) described in this document.
- 2.The OEM integrator will ensure the antenna placement inside the host system willmaintain the required spacing to end user for RF Exposure compliance, as specified in this document. 3.If other radios are integrated inside the host with the LITE-ON Module, the OEM integrator will contact its test lab, TCB or LITE-ON to determine if additional FCC compliance evaluation is required to meet FCC collocation rules.
- 4.The OEM integrator will ensure end user documentation will contain the specified regulatory wording and ensure the host system and the Module itself are labeled as specified in this

document.

5. The OEM integrator will ensure the Module is programmed in the factory with compliant transmit power not exceeding the levels specified in this document. LITE-ON requests that the OEM integrator acknowledge its receipt of this document and the above instructions. You may contact LITE-ON with any questions concerning this document or the responsibilities of the OEM integrator

Overview

IEEE 802.11ah is a new Wi-Fi standard operating in the Sub 1GHz license-exempt band, offering longer range and lower power connectivity necessary for internet of things (IoT) applications. WSG300NRC contains external RF front end module (FEM) which can increase transmission power up to 23 dBm. Onboard serial flash can be used for OTA software development and with internal 32KB cache memory, it can support execution in place (XIP) feature.

1.1 Module features

The main features are represented as follows:

- Standard
- IEEE Std 802.11ahTM-2016 compliant
- 1/2/4 MHz channel bandwidth support
- WPA2 PSK support
- 150 kbps ~ 15 Mbps data rate
- AP and STA role support
- Radio frequency
- -109 dBm minimum receive sensitivity
- +23 dBm transmit power
- 920.5~924.5 MHz frequency band

(By replacing RF SAW filter, other frequency band can be supported within 750~950 MHz)

- CPU
- ARM Cortex-M3 for application
- ARM Cortex-M0 for IEEE 802.11ah WLAN
- Clock frequencies for both processor

(32/48 MHz) • Host interface

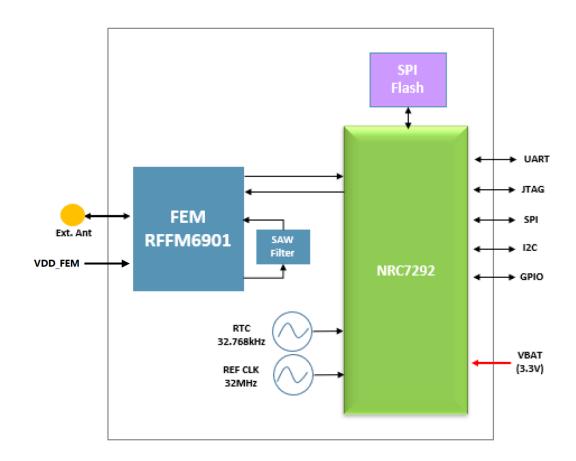
- UART and SPI support for host interface
- Peripherals
- GPIO, ADC, PWM and timers
- I2C, SPI and UART
- Temperature range
- -40°C to +125°C

1.2 Applications

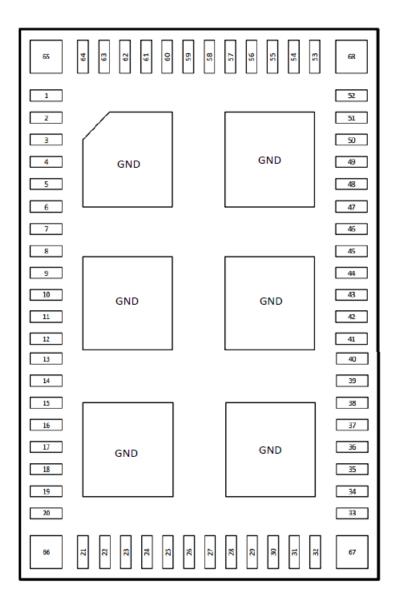
Low to high data rate can be applied in various IoT applications like: • Wearable

- Home automation
- Healthcare
- Industrial automation
- Safety and security
- Smart grid
- Multimedia streaming

2. Block Diagram



3. Pin Description



Pad no.	Name	Direction	Volt	Description
1	GROUND	GND		
2	GROUND	GND		
3	GROUND	GND		
4	GROUND	GND		
5	VDD_FEM	Р		Module power input for FEM
6	VBAT_3.3V	Р		Module power input for SYS
7	GROUND	GND		
8	GROUND	GND		
9	MODE_00	- 1		SW define (When ROM BOOT)
10	MODE_01	1		11: Internal SRAM BOOT
11	MODE_02	I		0: ROM BOOT 1: XIP BOOT
12	MODE_03	I		0: Cortex-M0 Mater 1: Cortex-M3 Mater
13	MODE_04	I		0: Two CPU 1: One CPU
14	GROUND	GND		
15	HSPI_nCS	I		Host SPI-Chip Select (active low)
16	HSPI_CLK	I		Host SPI-Clock
17	HSPI_MISO	0		Host SPI-Mater in Slave out
18	HSPI_MOSI	I		Host SPI-Mater out Slave in
19	HSPI_EIRQ	0		Host SPI-Interrupt
20	GROUND	GND		
21	GROUND	GND		
22	NC	-		
23	NC	-		
24	NC	-		
25	GP_00_UART2_TX	I/O		UART Channel2 Tx
26	GP_01_UART2_RX	I/O		UART Channel2 Rx
27	GP_02_UART2_RTS	I/O		UART Channel2 RTS
28	GP_03_UART2_CTS	I/O		UART Channel2 CTS
29	GP_04_UART0_TX	I/O		UART Channel0 Tx
30	GP_05_UART0_RX	I/O		UART Channel0 Rx
31	GP_06_UART3_TX	I/O		UART Channel3 Tx
32	GP_07_UART3_RX	1/0		UART Channel3 Rx
33	GP_08_UART1_RX	I/O		UART Channel1 Rx
34	GP_11_UART1_TX	I/O		UART Channel1 Tx
35	GP_10_GPIO	I/O		Multiple purpose
36	GP_09_GPIO	I/O		(GPIO, I2C, PWM, SPI, Ext-INT)
37	GP_17_I2C_SDA	1/0		I2C_SDA

41 PD_13_SSP0_MOSI O SPI0_Mater out Slave in 42 PD_12_SSP0_MISO I SPI0_Mater in Slave out 43 RESET I Reset (active high) 44 GROUND GND 45 JTAG_TRSTN I JTAG reset 46 JTAG_TMS I JTAG mode selection 47 JTAG_TCK I JTAG clock 48 JTAG_TDI O JTAG data input 49 JTAG_TDO I JTAG data output 50 GROUND GND 51 VDDIO P Module I/O supply input 52 GROUND GND 53 GROUND GND 54 AUXADCIN3 I AUXADC input 3 55 AUXADCIN2 I AUXADC input 2 56 AUXADC input 1 I AUXADC input 1 57 GROUND GND I 58 NC - I 59 NC - <th>38</th> <th>GP_16_I2C_SCL</th> <th>I/O</th> <th>I2C_SCL</th>	38	GP_16_I2C_SCL	I/O	I2C_SCL
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62 RF_ANT I/O RF IN/OUT 63 GROUND GND 64 GROUND GND 65 GROUND GND	60	GROUND	GND	
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	64	GROUND	GND	
66 GROUND GND	65	GROUND	GND	
	66	GROUND	GND	
67 GROUND GND	67	GROUND	GND	
68 GROUND GND	68	GROUND	GND	

4. Absolute Maximum Rating

Symbol	Rating	Min	Max	Units
Storage Temperatur	-40	+125	°C	
Cumply Voltage	VBAT	-0.5	3.8	V
Supply Voltage	VDDIO	-0.5	3.8	V

NOTE: Stresses above those listed in Absolute Maximum Rating may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

5. Operating Condition

5.1 Operating condition

Symbol	Rating	Min	Тур	Max	Units
Operating Temperature	Operating Temperature Range		-	+85	°C
Operating Voltage	VBAT	2.8	3.3	3.6	V
Operating Voltage	VDDIO	1.8	3.3	VBAT	V

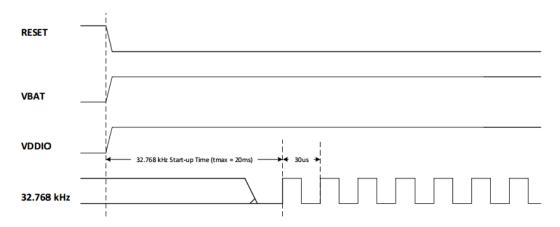
NOTE: To ensure WLAN performance, ripple on the 2.1- to 3.3-V supply must be less than ± 300 mV and ripple on the 1.8-V supply must be less than 2% (± 40 mV).

5.2 Current consumption

Mode	DUT Status	Band (MHz)	VBAT=3.3V, Ta=27°C
002 44 ab (484ba BW)	TX@18dBm	022	200
802.11ah (1Mhz BW)	Continuous RX@-80dBm	922	41
002 44 - h (204h - DW)	TX@18dBm	022	200
802.11ah (2Mhz BW)	Continuous RX@-80dBm	922	41
902 44 ab /4N4b= BN/)	TX@18dBm	022	200
802.11ah (4Mhz BW)	Continuous RX@-80dBm	922	42

Note: Unless otherwise specified, TA=27°C, VBAT=3.6V, using internal PMU. Measurements are done at antenna port, which is directly connect to the device.

5.3 Power on sequence

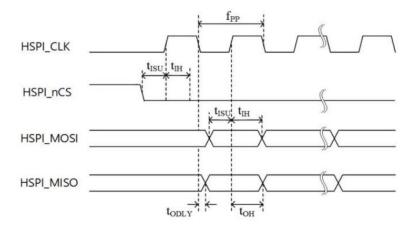


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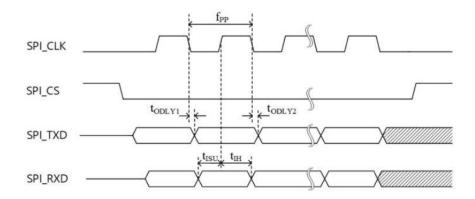
6. AC Specifications

6.1 HSPI timing



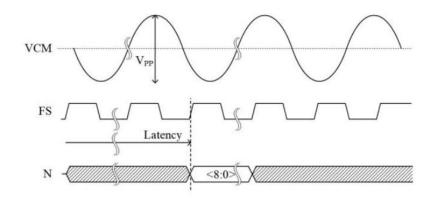
Symbol	Parameter	Min	Тур	Max	Unit
fpp	Frequency	-	-	25	MHz
todly	Output delay time	6	-	-	ns
tон	Output hold time	2	-	-	ns
t _{ISU}	Input setup time	-	-	14	ns
t _{iH}	Input hold time	2.5	-		ns

6.2 SPI Timing



Symbol	Pai	rameter	Min	Тур	Max	Unit
	Francisco	master	-	-	24	MHz
fpp	Frequency	slave	-	-	4	MHz
todLY1	Output delay	time1	0	-	10	ns
t _{ODLY2}	Output delay	time2	0	(-)	10	ns
tisu	Input setup tii	me	18	·-	-	ns
tıн	Input hold tim	ie	20	-	-	ns

6.3 AUXADC Timing



Symbol	Parameter	Min	Тур	Max	Unit
VCM	Input common-mode voltage	0.25	0.28	0.31	V
V _{PP}	Input Swing	•	0.5	-	Vpp
FS	Sampling Clock		32	[MHz
Latency	Conversion latency(1 cycle = 31.25 ns)	•	11	0.0	cycle
N	Resolution		9	122	Bit
RIN	Input impedance		1	-	Mohms
I_active	Current consumption (1.2V supply)	•		300	uA
I_down	Power-down current (1.2V supply)	-		1	uA

7. 11ah WLAN RF Specifications and Performance

7.1 Transmitter Specifications

Parameter	Conditions	Min	Тур	Max	Unit
RF Output Frequency Range (1)		920.5		924.5	MHz
EVM compliant Output Power	13.5 Mbps (MCS7, 4 MHz BW)		18		dBm
EVM at 0 dBm output power			33		dB
Transmitter Spurious Signal	< 700 MHz		<-36		dBm/
Emissions	> 1 GHz		<-45		MHz
RF Output Return Loss	Single ended output port		-10		dB
Output 1dB Gain Compression	0.4 MHz CW signal input		25		dBm
Gain Control Range		30			dB
Gain Control Step			1		dB
Unwanted Sideband	Over RF channel, RF frequency, and baseband frequency at 0 dBm output power		<-40		dBc

Note: Unless otherwise specified, TA=27°C, VBAT=3.6V, RF input/output specifications are referenced not device pins and do not include 1dB loss from EV kit OCB and SMA connector.

(1) RF output frequency range depends on RF SAW filter on the module. The NRC7292 chipset by itself can support frequency range from 750 to 950 MHz.

7.2 Receiver Specifications

Parameter	Conditions	Min	Тур	Max	Unit
RF Input Frequency Range (1)		920.5		924.5	MHz
RF Input Return Loss	For LNA high/mid/low gain modes	-10	-12	-15	dB
Total Voltage Gain Range	Analog + Digital Gain	-10		92	dB
RF Gain Step	From high gain mode to medium gain mode		6		dB
RX Gain Step	From RF to Analog		1		dB
DSB Noise Figure	LNA max gain mode		3.5		dB
IIP3	LNA with high gain mode		-17		
	LNA with low gain mode		24		dBm

Baseband Filters for Receiver (Analog + Digital Filter)					
Baseband -3dB Low-pass	1 MHz channel	0.5	MHz		
Corner Frequency	2 MHz channel	1.0	MHz		
(Controllable)	4 MHz channel	2.0	MHz		

Note: Unless otherwise specified, TA=27°C, VBAT=3.6V, RF input/output specifications are referenced not device pins and do not include 1dB loss from EV kit OCB and SMA connector.

⁽¹⁾ RF output frequency range depends on RF SAW filter on the module. The NRC7292 chipset by itself can support frequency range from 750 to 950 MHz.

7.3 Transmitter Performance

DR/MCS/BW (Mbps//MHz)	constellation error (dB)	EVM (%) (IEEE)	EVM (%) (NRM7292A)	Comments
0.15/MCS10/1	-4	63.1	3.1	BPSK Peak
0.30/MCS0/1	-5	56.2	3.1	BPSK Peak
0.60/MCS1/1	-10	31.6	3.1	18 dBm OFDM, RMS
0.90/MCS2/1	-13	22.4	3.1	18 dBm OFDM, RMS
1.20/MCS3/1	-16	15.8	3.1	18 dBm OFDM, RMS
1.80/MCS4/1	-19	11.2	3.1	18 dBm OFDM, RMS
2.40/MCS5/1	-22	7.9	3.1	18 dBm OFDM, RMS
2.70/MCS6/1	-25	5.6	3.1	18 dBm OFDM, RMS
3.00/MCS7/1	-27	4.5	3.1	18 dBm OFDM, RMS
0.65/MCS0/2	-5	56.2	2.9	BPSK Peak
1.30/MCS1/2	-10	31.6	2.9	18 dBm OFDM, RMS
1.95/MCS2/2	-13	22.4	2.9	18 dBm OFDM, RMS
2.60/MCS3/2	-16	15.8	2.9	18 dBm OFDM, RMS
3.90/MCS4/2	-19	11.2	2.9	18 dBm OFDM, RMS
5.20/MCS5/2	-22	7.9	2.9	18 dBm OFDM, RMS
5.85/MCS6/2	-25	5.6	2.9	18 dBm OFDM, RMS
6.50/MCS7/2	-27	4.5	2.9	18 dBm OFDM, RMS
1.35/MCS0/4	-5	56.2	3.0	BPSK Peak
2.70/MCS1/4	-10	31.6	3.0	18 dBm OFDM, RMS
4.05/MCS2/4	-13	22.4	3.0	18 dBm OFDM, RMS
5.40/MCS3/4	-16	15.8	3.0	18 dBm OFDM, RMS
8.10/MCS4/4	-19	11.2	3.0	18 dBm OFDM, RMS
10.80/MCS5/4	-22	7.9	3.0	18 dBm OFDM, RMS
12.15/MCS6/4	-25	5.6	3.0	18 dBm OFDM, RMS
13.50/MCS7/4	-27	4.5	3.0	18 dBm OFDM, RMS

Note: <Conditions> supply voltage VBAT 2.6~3.6V, TA=25°C, Signal within spectrum mask.

7.4 Receiver Performance

7.4.1 Receiver Sensitivity

Band	BW	Rate	Modulation/Coding Rate	Conditions/Conditions	Chip Port Specification [dBm]		
					Min	Тур	Max
920.5~ 924.5M Hz	1 MHz	300	BPSK 1/2	@ PER<10%, 256 bytes Full Operating Temperature; Full Battery Voltage Range; Load Z: 50 Ohms;		-105	
		600	QPSK 1/2			-103	
		900	QPSK 3/4			-100	
		1200	16QAM 1/2			-97	
		1800	16QAM 3/4			-94	
		2400	64QAM 2/3			-90	
		2700	64QAM 3/4			-88	
		3000	64QAM 5/6			-87	
		150	BPSK 1/2 rep. 2x			-108	
	2 MHz	650	BPSK 1/2	@ PER<10%, 256 bytes Full Operating Temperature; Full Battery Voltage Range; Load Z:50 Ohms;		-101	
		1300	QPSK 1/2			-98	
		1950	QPSK 3/4			-95	
		2600	16QAM 1/2			-92	
		3900	16QAM 3/4			-89	
		5200	64QAM 2/3			-85	
		5850	64QAM 3/4			-83	
		6500	64QAM 5/6			-82	
	4 MHz	1350	BPSK 1/2	@ PER<10%, 256 bytes Full Operating Temperature; Full Battery Voltage Range; Load Z: 50 Ohms;		-98	
		2700	QPSK 1/2			-95	
		4050	QPSK 3/4			-92	
		5400	16QAM 1/2			-89	
		8100	16QAM 3/4			-86	
		10800	64QAM 2/3			-82	
		12150	64QAM 3/4			-80	
		13500	64QAM 5/6			-79	

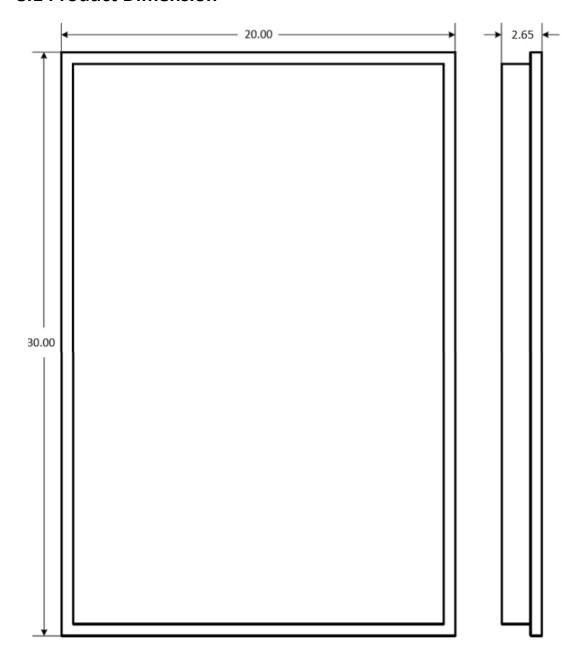
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7.4.2 Adjacent Channel Rejection (ACR)

Band	BW	Rate	Modulation/Coding Rate	Conditions/Conditions	ACR [dB]		
					Min	Тур	Max
920.5~ 924.5M Hz	1 MHz	300	BPSK 1/2	@ PER<10%, Pdesired=Psensitivty + 3dB, Pinterfere]@ N+1 channel		32	
		600	QPSK 1/2			30	
		900	QPSK 3/4			29	
		1200	16QAM 1/2			28	
		1800	16QAM 3/4			25	
		2400	64QAM 2/3			24	
		2700	64QAM 3/4			23	
		3000	64QAM 5/6			22	
		150	BPSK 1/2 rep. 2x			35	
	2 MHz	650	BPSK 1/2	@ PER<10%, Pdesired=Psensitivty + 3dB, Pinterfere]@ N+1 channel		30	
		1300	QPSK 1/2			28	
		1950	QPSK 3/4			27	
		2600	16QAM 1/2			26	
		3900	16QAM 3/4			23	
		5200	64QAM 2/3			21	
		5850	64QAM 3/4			19	
		6500	64QAM 5/6			17	
	4 MHz	1350	BPSK 1/2	@ PER<10%, Pdesired=Psensitivty + 3dB, Pinterfere]@ N+1 channel		28	
		2700	QPSK 1/2			26	
		4050	QPSK 3/4			25	
		5400	16QAM 1/2			23	
		8100	16QAM 3/4			20	
		10800	64QAM 2/3			18	
		12150	64QAM 3/4			15	
		13500	64QAM 5/6			12	

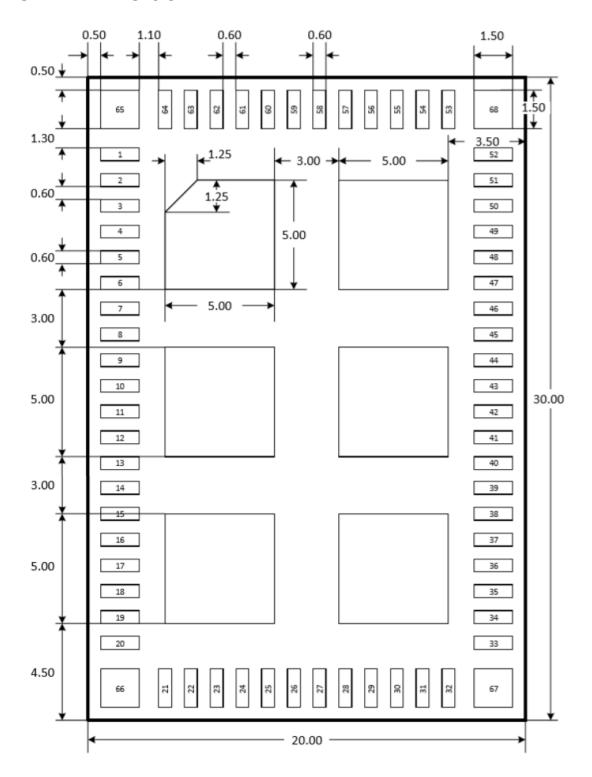
8. Product Characteristic

8.1 Product Dimension



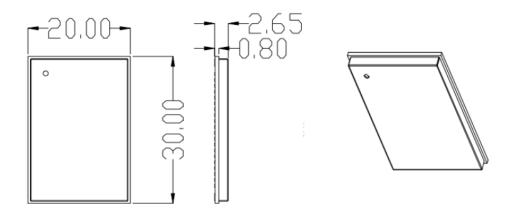
Physical dimension (top view) Unit: mm

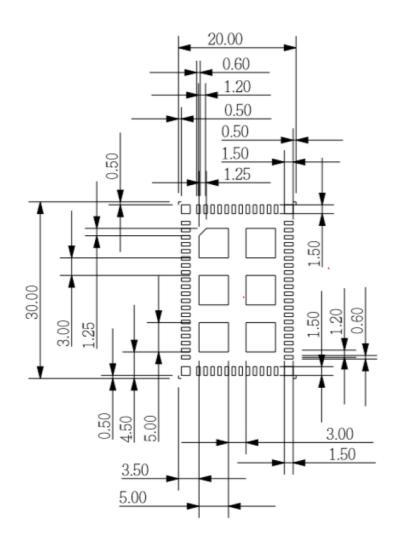
8.2 PAD Dimension



Physical dimension (top view) Unit: mm

8.3 Recommend footprint





9. SMT Temperature Sequence (Pb-free)

