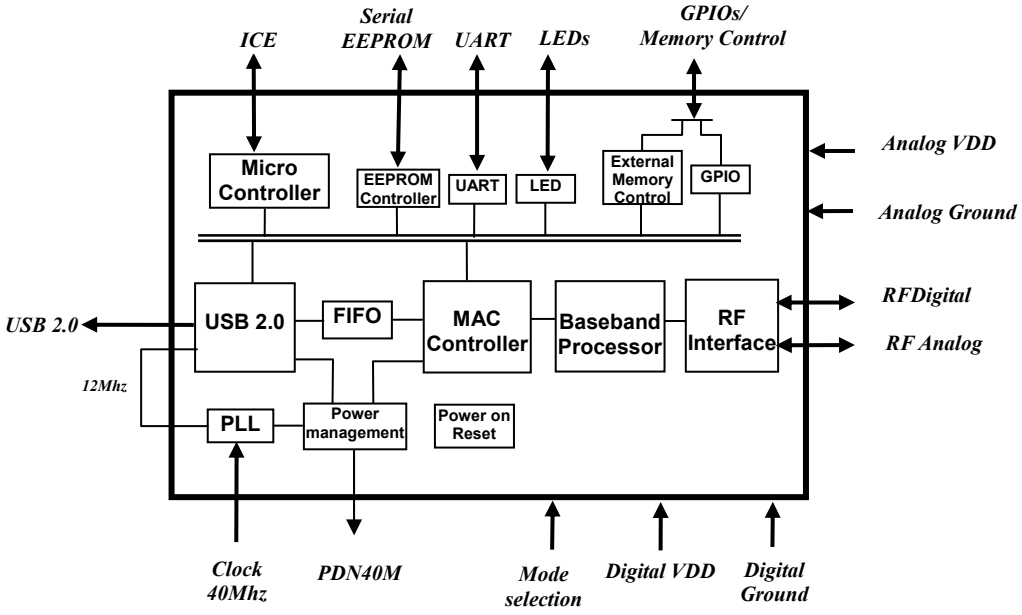
Function Diagram



Function Description

Reset

ZD1211 provides build-in power on reset circuit generates stable reset signal for the whole chip that was derived from external supply power in power on time. The voltage threshold detection and ripple counter circuit are designed to eliminate un-stable state in power on stage.

Power Control

The ZD1211 considers the power state in WLAN application and USB specification requirement. The different power states are defined as followings:

Normal Operation state: While WLAN operates, all chip function is active. MAC controller is in operating all the time. To save the current consumption in this state, transmission function of baseband processor is gated during receiving, and the receiving function is gated during transmission.

Power Saving State: When ZD1211 operates in 802.11 power saving mode, the chip will gated the clock to Microcontroller, MAC and baseband processor. The 40Mhz OSC still working to keep USB alive. In the state, only a timer circuit in the chip still operates. After the timer timeout, the chip is wakeup for protocol handling.

USB suspend State: When the host system slept or enter hibernate mode, ZD1211will enter USB suspend mode. ZD1211 asserts the pin *PDN40M* to shutdown 40Mhz OSC. In this power state, all the circuit in ZD1211 is in the clock gated state and only static current is consumed. After receive resume signal from USB host, the pin *PDN40M* will be de-alert automatically. Then the 40Mhz OSC starts beating and enter normal operation mode.

Power mode

Power State	Clock 40M	Micro controller	MAC	Baseband	USB State	State Enter Condition	State Leave Condition
Normal operation	*On*	*40M*	*40M*	*40M*	*Connect*	*NA*	*NA*
Power saving	*On*	*Gated*	*Gated*	*Gated*	*Connect*	*Power saving*	*ATIM timer timeout*
USB suspend	*Shutdown*	*Gated*	*Gated*	*Gated*	*Suspend*	*USB Suspend*	*USB Resume*

Clock

ZD1211 MAC and baseband operates in 40Mhz clock. The pin *40MCLKI* connects to 40Mhz OSC which provides the clock. The USB clock pin *XSCI* may come from external 12M OSC or use the pin *12MCLKO* that derived from internal PLL.

Mode Selection

There are configurable pins may be set as external memory control signals or GPIO pins. Mode selection pins *mode 0* and *mode 1* decide the options. The mode selection pins are detected on power on stage.

Mode1/Mode0	Low/Low	Low/High
Pin Number	External Memory	GPIO
85,86,87,88,89,90,91,92	MD[7:0]	Reserved
97	MA0	SGPIO0
98	MA1	SGPIO1
99	MA2	SGPIO2
100	MA3	SGPIO3
101	MA4	SGPIO4
102	MA5	SGPIO5
103	MA6	Reserved
104	MA7	Reserved
79	MA8	Reserved
80	MA9	Reserved
83	MA10	Reserved
81	MA11	Reserved
105	MA12	Reserved
78	MA13	Reserved
106	MA14	Reserved
82	MOE_N	Reserved
84	MCE_N	Reserved
77	MWE_N	Reserved

USB 2.0 Interface

USB 2.0 interface is fully compatible to 480M USB high speed mode and 12M full speed mode. It integrates USB 2.0 physical layer transceiver and controller in chip. The embedded microcontroller and serial EEPROM provide flexibility for customization of card identification in USB enumeration.

ICE

These pins are used for debug purpose only.

Serial EEPROM Interface

ZD1211 needs a 32K bit serial EEPROM to provide the card identification on booting stage and RF information on operation. The interface also provides software interface to read and write EEPROM.

UART

The UART may operate in 115200, 57600, 38400, 19200, 9600 baud rate. The interface can be provided for debug purpose or for specific feature.

LED

Two LED pins are provided for indication of WLAN operation. The behavior of LED may be programmable by software on host system.

GPIO

There are 6 general purpose IO pins provided for specific application. All these pins are configurable and software programmable to input or output. In input mode, it may generate interrupt to micro controller for event handling. These pin are default in input state when power on reset. These pins are pin MUX with external memory control pins. The mode selection pins decide the option.

More GPIO pins may be derived from RF interface pins. If used RFMD RF2959 then some pins may used as general purpose output.

RF GPIO pins

Pin	Name
34	B6
42	B1
35	B5
41	B2
29	SHDNB

External Memory Control

The external memory control pins may connect to 8 bit SRAM or Flash memory. The memory access range may up to 32K byte. These pins are pin MUX with GPIO pins. The mode selection pins decide the option. If more external memory is required, it may use RF GPIO to connect more address lines.

RF Interface

There are kinds of RF interface allowed to connect to ZD1211. ZD1211 provides programmable interface flexibility to hook lots of RF transceivers.

RXIQ interface

The common mode voltage for the RXIQ is 1.6V typically (Maximum 1.7, Minimum 1.4). If the RXIQ common mode voltage from RF transceiver is greater than 1.4V and less than 1.7V, then DC couple is recommended. Otherwise, AC couple will be used. When AC couple is used, 0.1uF is recommended.

The I,Q ADC input resistance (single) is 25 kΩ typically (maximum 28kΩ, minimum 21kΩ). The I,Q ADC input capacitance (single) is 3.3 pF typically (maximum 2.54pF, minimum 3.06 pF).

RX AGC interface

ZD1211 supports 2 RX AGC interface: digital RX AGC (B1-B7) and analog RX AGC (RX_VGC). For Maxim MAX2825, B1-B7 and RXHP are used to support digital RX AGC. B7 and B6 control the LNA gain([B7,B6]=[1,1] high gain; [B7,B6]=[1,0] middle gain; [B7,B6]=[0,x] low gain); B5-B1 control baseband VGA gain; RXHP controls HPF (High Pass Filter for DC cancellation) bandwidth. Please refer to Maxim datasheet for detail. For RFMD RF2959, analog RX AGC is used. RX_VGC is provided by ZD1211 to control transceiver RX VGA gain. The dynamic range for RX_VGA is 0V to 2V.

TXIQ interface

TXIQ DAC is current type DAC, full scale current is 2mA if the resistance from EXTRES (pin4) to ground is 26.7 kΩ. Resistor network is needed to convert current to voltage (Please refer to schematics in reference design). TXIQ is DC coupled to RF transceiver.

TX power control interface

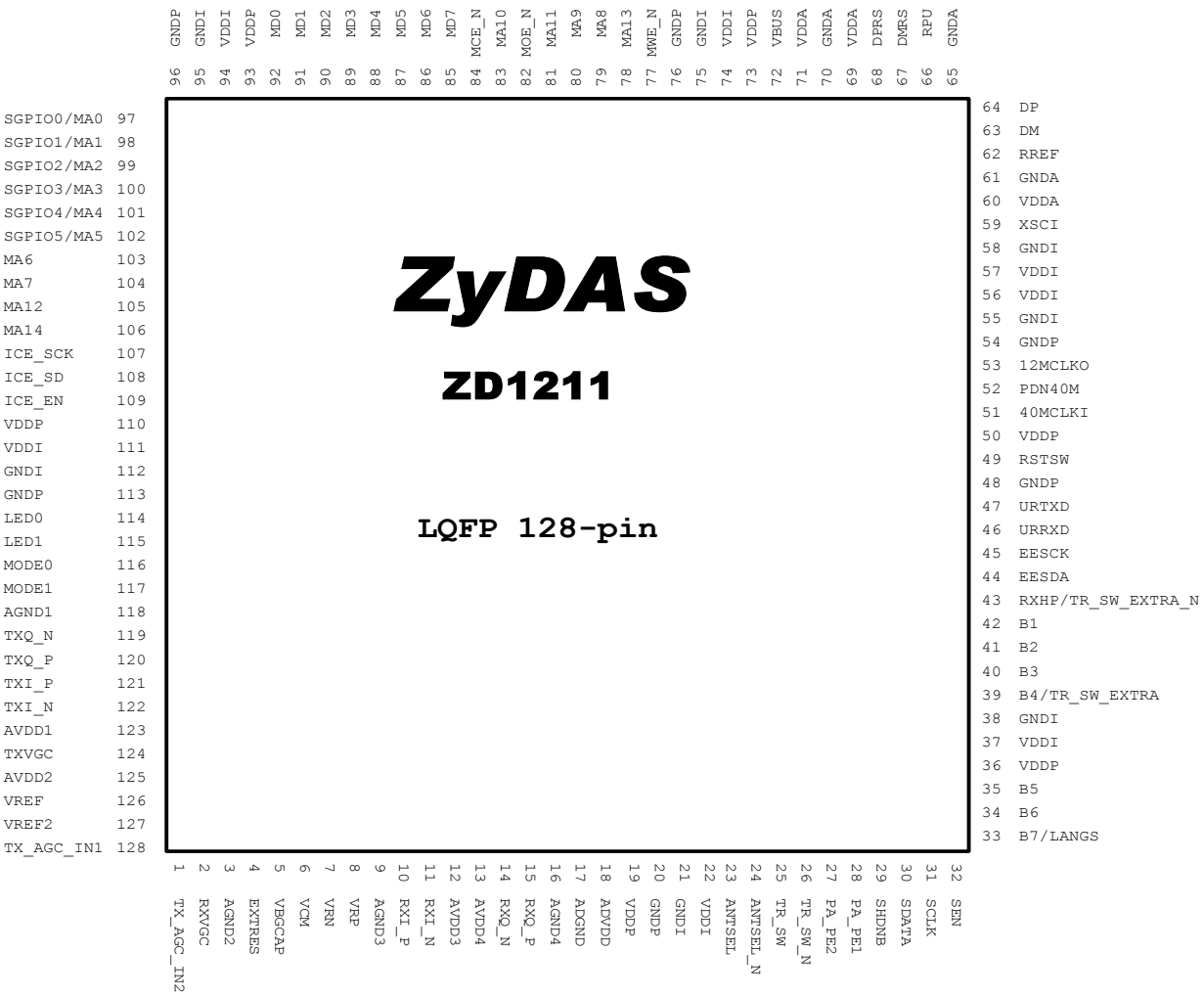
To perform TX close loop power control, power detector from PA is needed. Besides, baseband has to control transceiver TX gain based on power detector measurement from PA. ZD1211 is designed for a/b/g, so two separate pins are used to receive PA power detector from 802.11g and 802.11a. TX_AGC_IN1(pin128) is for 802.11g PA power detector; TX_AGC_In2(pin1) is for 802.11a PA power detector.

ZD1211 support two TX gain control interface: digital TX gain control interface (B1-B5) and analog TX gain control interface (TX_VGC). For Maxim Max2825, B1-B5 are used to support digital TX gain control. For RFMD RF2959, analog RX AGC is used. TX_VGC is provided by ZD1211 to control transceiver TX gain. The dynamic range for TX_VGA is 0V to 2V.

Baseband to RF interconnection Table

Pin	ZD1211 Pin Name	RFMD(RF2959)	MAX2825 /Airoha (AL2230)
34	**B6**	NC	B6
32	**SEN**	SSB	CSB
31	**SCLK**	SCLK	SCLK
30	**SDATA**	SDATA	SDATA
42	**B1**	NC	B1
35	**B5**	NC	B5
41	**B2**	NC	B2
29	**SHDNB**	NC	SHDNB
40	**B3**	NC	B3
39	**B4 (TR_SW_EXTRA)**	TR_SW_EXTRA (connect to TR switch, does not connect to RF2959)	B4
43	**RXHP(TR_SW_EXTRA_N)**	Connect to TR switch, does not connect to RF2959	RXHP
33	**B7(LNAGS)**	LNAGS (LNA H/L gain control)	B7
25	**TR_SW#**	RF2959-MODE0 (does not connect to TR switch)	RXENA (also connect to TR switch)
26	**TR_SW**	RF2959-MODE1 (does not connect to TR switch)	TXENA (also connect to TR switch)
23	**ANT_SEL**	ANT_SEL (antenna switch)	ANT_SEL (antenna switch)
24	**ANT_SEL#**	ANT_SEL#	ANT_SEL#
28	**PA_PE1**	To 802.11g PA	To 802.11g PA
27	**PA_PE2**	To 802.11a PA	To 802.11a PA
128	**TXAGC_IN1**	Power detector (from 802.11g PA)	Power detector (from 802.11g PA)
1	**TXAGC_IN2**	Power detector (from 802.11a PA)	Power detector (from 802.11a PA)
121	**TXI+**	TXI+	TXI+
122	**TXI-**	TXI-	TXI-
120	**TXQ+**	TXQ+	TXQ+
119	**TXQ-**	TXQ-	TXQ-
124	**TXVGC**	TX VGC (TX power control)	NC (MAX2825 use B1-B5 for TX power control)
10	**RXI+**	RXI+	RXI+
11	**RXI-**	RXI-	RXI-
15	**RXQ+**	RXQ+	RXQ+
14	**RXQ-**	RXQ-	RXQ-
2	**RXVGC**	RX VGC	NC (MAX2825 use B1-B7 for RX AGC)

PIN Assignment



PIN Description – Functional grouping

Mode Selection pins

Pin	Name	Type	Description
116	**MODE0**	I	Operation mode selections; MODE[1:0]: 00: Configurable pins set as External RAM interface 01: Configurable pins set as GPIO functions 10: Reserved 11: Reserved.
117	**MODE1**	I	See description of *MODE0*

LED pins

Pin	Name	Type	Description
114	**LED0**	I/O/Z, 4mA	LED0, output 0: LED ON, 1: LED OFF. (note: external LED, one end is connected to power, another is connected to this pin; for internal pad, the input end of output buffer is connected to ground, and LED on/off signal is used to control the output enable of the buffer.) Default: 0, LED ON.
115	**LED1**	I/O/Z,4mA	LED1, output 0: LED ON, 1: LED OFF. (note: external LED, one end is connected to power, another is connected to this pin; for internal pad, the input end of output buffer is connected to ground, and LED on/off signal is used to control the output enable of the buffer.) Default: 0, LED ON

GPIO pins *(For Mode[1:0]=01)*

Pin	Name	Type	Description
97	**SGPIO0**	I/O/Z,4mA,	bi-direction, general purpose IO port.
98	**SGPIO1**	I/O/Z,4mA	bi-direction, general purpose IO port.
99	**SGPIO2**	I/O/Z,4mA,	bi-direction, general purpose IO port.
100	**SGPIO3**	I/O/Z,4mA,	bi-direction, general purpose IO port.
101	**SGPIO4**	I/O/Z,4mA,	bi-direction, general purpose IO port.
102	**SGPIO5**	I/O/Z,4mA,	bi-direction, general purpose IO port.

External Memory Control Pins *(For Mode[1:0]=00)*

Pin	Name	Type	Description
85,86, 87,88, 89,90, 91,92	**MD[7:0]**	I/O/Z, 4mA	MD[7:0], bi-direction; Data in and out to external SRAM.
97	**MA0**	I/O/Z,4mA	MA0, output; bit 0 of 15-bit address out to external SRAM.
98	**MA1**	I/O/Z,4mA	MA1, output; bit 1 of 15-bit address out to external SRAM.
99	**MA2**	I/O/Z,4mA	MA2, output; bit 2 of 15-bit address out to external SRAM.
100	**MA3**	I/O/Z,4mA	MA3, output; bit 3 of 15-bit address out to external SRAM.
101	**MA4**	I/O/Z,4mA	MA4, output; bit 4 of 15-bit address out to external SRAM.
102	**MA5**	I/O/Z,4mA	MA5, output; bit 5 of 15-bit address out to external SRAM.
103	**MA6**	I/O/Z,4mA	MA6, output; bit 6 of 15-bit address out to external SRAM.
104	**MA7**	I/O/Z,4mA	MA7, output; bit 7 of 15-bit address out to external SRAM.
79	**MA8**	I/O/Z,4mA	MA8, output; bit 8 of 15-bit address out to external SRAM.
80	**MA9**	I/O/Z,4mA	MA9, output; bit 9 of 15-bit address out to external SRAM.
83	**MA10**	I/O/Z,4mA	MA10, output; bit 10 of 15-bit address out to external SRAM.
81	**MA11**	I/O/Z,4mA	MA11, output; bit 11 of 15-bit address out to external SRAM.
105	**MA12**	O,4mA	MA12, output; bit 12 of 15-bit address out to external SRAM.
78	**MA13**	O/Z,4mA	MA13, output; bit 13 of 15-bit address out to external SRAM.
106	**MA14**	I/O/Z,4mA	MA14, output; bit 14 of 15-bit address out to external SRAM.
82	**MOE_N**	I/O/Z,4mA	MOE_N, output; data output enable to external SRAM, low active.
84	**MCE_N**	I/O/Z,4mA	MCE_N, output; chip enable to external SRAM, low active.
77	**MWE_N**	I/O/Z,4mA	MWE_N, output; data write enable to external SRAM, low active.

Power management pins

Pin	Name	Type	Description
52	PDN40M	I/O/Z,4mA, Schimitt input	PDN40M, output; this pin acts as a PDN44M. To power down external 40MHz Oscillator, active low.
49	RSTSW	I	Reserved, connect to GND.

Clock pins

Pin	Name	Type	Description
51	40MCLKI	I	3.3V 40MHz chip master clock input.
53	12MCLKO	O,4mA	12MHz clock from internal PLL can used as USB 12MHz clock input.

ICE pins

Pin	Name	Type	Description
107	ICE_SCK	I,pull-low internal	3.3V ICE clock input. ICE command transmission CLK pin for programmable controller.
108	ICE_SD	I/O/Z,4mA, pull-low internal	ICE command transmission data pin for programmable controller. Default: input
109	ICE_EN	I, Pull-low internal	For programmable controller. 0:Micro-controller free run 1:enable ICE function

UART Pins

Pin	Name	Type	Description
47	URTXD	O, 4mA.	UART serial data out
46	URRXD	I, Pull-high internal	UART serial data in.

Serial EEPROM pins

Pin	Name	Type	Description
45	EESCK	O/Z, 4mA	Clock output to external sequential EEPROM. Clock speed 78.125KHz (40MHz/512, for 40MHz chip clock). This signal will active, only while data is transferring, otherwise this signal will keep at high. Default: high.
44	EESDA	I/O/Z,4mA Open-Drain	Data in/out to external sequential EEPROM. This pin needs external pull-up. And data will be clocked out after falling edge of EESCK, and will be clocked in after rising edge of EESCK. Default: output High-Z, input.

Digital VDD/GND pins

Pin	Name	Type	Description
22,37, 56,74, 94,111	VDDI	PWR	1.8V digital power for core.
21,38, 55,75, 95,112	GNDI	GND	Digital ground for core.
19,36, 50,73, 93,110	VDDP	PWR	3.3V digital power for IO pad.
20,48, 54,76, 96,113	GNDP	GND	Digital ground for IO pad.
17	ADGND	GND	Digital ground for RF analog interface
18	ADVDD	PWR	3.3V digital power for RF analog interface

RF digital interface (18 pins)

Pin	Name	Type	Description
34	**B6**	I/O/Z,4mA	For MAX2825, it is B6(RX base band gain control bit 6). For RF2959, it may used as general purpose output.
32	**SEN**	I/O/Z, 4mA	Normally, it is Serial interface enable signal of 3-wire RF interface.
31	**SCLK**	I/O/Z, 4mA	Normally, it is Serial interface enable signal of 3-wire RF interface.
30	**SDATA**	I/O/Z, 4mA	Normally, it is Serial interface enable signal of 3-wire RF interface.
42	**B1**	I/O/Z, 4mA	For MAX2825, it is B1(RX/TX base band gain control bit 1). For RF2959, it may used as general purpose output.
35	**B5**	I/O/Z, 4mA	For MAX2825, it is B5(RX/TX base band gain control bit 5). For RF2959, it may used as general purpose output.
41	**B2**	I/O/Z, 4mA	For MAX2825, it is B2(RX/TX base band gain control bit 2). For RF2959, it may used as general purpose output.
29	**SHDNB**	I/O/Z, 4mA	For MAX2825, it is SHDNB(Shutdown, low shutdown).Default: output, 0. For RF2959, it may used as general purpose output.
40	**B3**	O, 4mA	For MAX2825, it is B3(RX/TX base band gain control bit3). For other RF, it indicates packet arrival. Default: 1
39	**B4 (TR_SW_EXTRA)**	O, 4mA	For MAX2825, it is B4(RX/TX base band gain control bit4). For RF2959, it is TR_SW_EXTRA. TR_SW_EXTRA will connect to TR switch. Even RF2959 has only 2-step LNA gain control. With TR_SW_EXTRA, we can achieve 3-step LNA gain step to get better RX performance (refer to application note of RF2959) Default: 0
43	**RXHP (TR_SW_EXTRA_N)**	O, 4mA	For MAX2825, it is RXHP (RX DC cancellation bandwidth control). For RF2959, it is TR_SW_EXTRA_N. TR_SW_EXTRA_N will connect to TR switch. Even RF2959 has only 2-step LNA gain control. With TR_SW_EXTRA_N, we can achieve 3-step LNA gain step to get better RX performance (refer to application note of RF2959) Default: 0
33	**B7(LNAGS)**	O, 4mA	For RF2959, it is LNA High/Low gain control. For MAX2825, it is B7. In combination with B7 and B6, MAX2825 can achieve 3-step LNA gain control (B7B6=11→High gain; B7B6=10→Mid gain; B7B6=0x→Low gain) Default: 1.
25	**TR_SW**	O, 4mA	TX/RX switch. Normally this signal will connect to TR-switch and Transceiver mode control except RF2959. For RF2959, this signal will connect only to transceiver mode control; TR-switch of RF2959 solution will connect to TR_SW_EXTRA(pin39) Default: 0, RX.
26	**TR_SW_N**	O, 4mA	Inversion of pin-TR_SW. Normally this signal will connect to TR-switch and Transceiver mode control except RF2959. For RF2959, this signal will connect only to transceiver mode control; TR-switch of RF2959 solution will connect to TR_SW_EXTRA_N (pin43) Default: 1.
23	**ANTSEL**	O, 4mA	Antenna diversity Selection Default: 0
24	**ANTSEL_N**	O, 4mA	Antenna switch differential drive, it is an inversion of pin-ANTSEL. Default: 1.
28	**PA_PE1**	O, 8mA	802.11g Power amplifier enable. 0: disable, 1: enable. Default: 0, disable.
27	**PA_PE2**	O,8mA	802.11a Power amplifier enable. 0: disable, 1: enable. Default: 0, disable.

RF analog interface

Pin	Name	Type	Description
119	**TXQ_N**	O	Transmit Quadrature channel negative terminal. Current output, full scale current is controlled by resistor value of EXTRES(pin4), 26.7k ohm corresponds to 2mA.
120	**TXQ_P**	O	Transmit Quadrature channel positive terminal. Current output, full scale current is controlled by resistor value of EXTRES(pin4), 26.7k ohm corresponds to 2mA.
121	**TXI_P**	O	Transmit In-phase channel positive terminal. Current output, full scale current is controlled by resistor value of EXTRES(pin4), 26.7k ohm corresponds to 2mA.
122	**TXI_N**	O	Transmit In-phase channel negative terminal. Current output, full scale current is controlled by resistor value of EXTRES(pin4), 26.7k ohm corresponds to 2mA.
124	**TX_VGC**	O	TX gain control to transceiver, analog output 0-2V.
128	**TX_AGC_IN1**	I	802.11g Power-amplifier power detector.

1	**TX_AGC_IN2**	I	802.11a Power-amplifier power detector.
2	**RX_VGC**	O	Drive to RF chip RX AGC/VGA control, analog output 0~2V.
10	**RXI_P**	I	Receive In-phase channel positive terminal. Common mode voltage is 1.65V-1.45V.
11	**RXI_N**	I	Receive In-phase channel negative terminal. Common mode voltage is 1.65V-1.45V.
14	**RXQ_N**	I	Receive Quadrature channel negative terminal. Common mode voltage is 1.65V-1.45V.
15	**RXQ_P**	I	Receive Quadrature channel positive terminal. Common mode voltage is 1.65V-1.45V.
126	**VREF**	I	Full scale voltage reference (Normally 2V).
127	**VREF2**	I	Half Vref (Normally 1V).
4	**EXTRES**	I	Current limit resistor. Connect with 26.7K/1% external resistor.
5	**VBGCAP**	I	Noise immunity low pass filter. Connect with 1uF filter capacitor.
6	**VCM**	O	1.65 Volt common reference voltage. Need to connect with 1uF filter capacitor.
7	**VRN**	O	1.15 Volt negative reference voltage. Need to connect with 1uF filter capacitor.
8	**VRP**	O	2.15 Volt positive reference voltage. Need to connect with 1uF filter capacitor.

Analog VDD/GND pins

No	Name	Type	Description
118	**AGND1**	**GND**	Analog ground
123	**AVDD1**	**PWR**	3.3V analog power
125	**AVDD2**	**PWR**	3.3V analog power
3	**AGND2**	**GND**	Analog ground
9	**AGND3**	**GND**	Analog ground
12	**AVDD3**	**PWR**	3.3V analog power
13	**AVDD4**	**PWR**	3.3V analog power
16	**AGND4**	**GND**	Analog ground

USB pins

No	Name	Type	Description
72	**VBUS**	I, 5V tolerant	A 5V digital signal. To indicate this device has been attached on an USB connector.
57	**VDDI**	PWR	1.8V digital supply
58	**GNDI**	GND	Digtal ground supply
59	**XSCI**	**I**	12MHz crystal input, clock input.
60	**VDDA**	**PWR**	3.3V analog supply
61	**GNDA**	**GND**	Analog ground supply
62	**RREF**	**I**	Connect to analog ground (GNDA) through an external resistor (12.1K Ohm+/-1%)
63	**DM**	**I/O**	USB2.0 data in/out, data negative pin terminal
64	**DP**	I/O	USB2.0 data in/out, data positive pin terminal
65	**GNDA**	**GND**	Analog ground supply
66	**RPU**	**I**	Connect to analog power (VDDA) through an external resistor (1.5K Ohm+/-1%)
67	**DMRS**	**I/O**	Connect to DM through an external resistor (39 Ohm+/-1%)
68	**DPRS**	**I/O**	Connect to DP through an external resistor (39 Ohm+/-1%)
69	**VDDA**	**PWR**	3.3V analog power for USB
70	**GNDA**	**GND**	Analog ground for USB
71	**VDDA**	**PWR**	3.3V analog power for USB