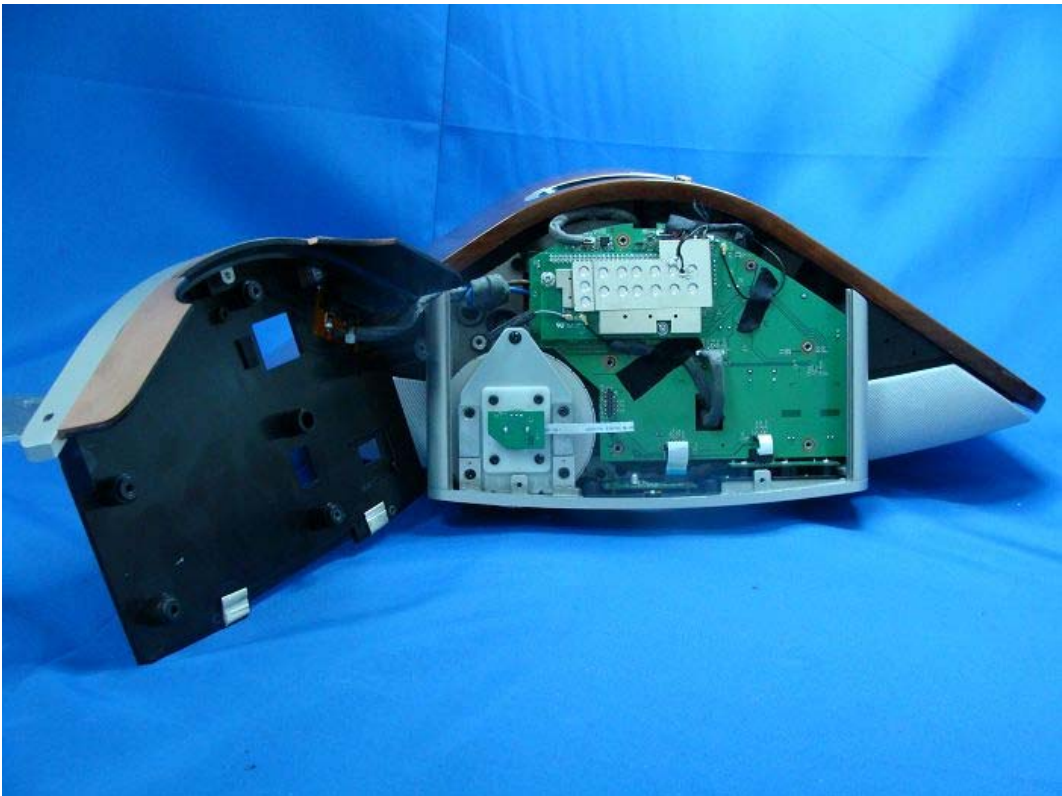


(7) EUT Photo



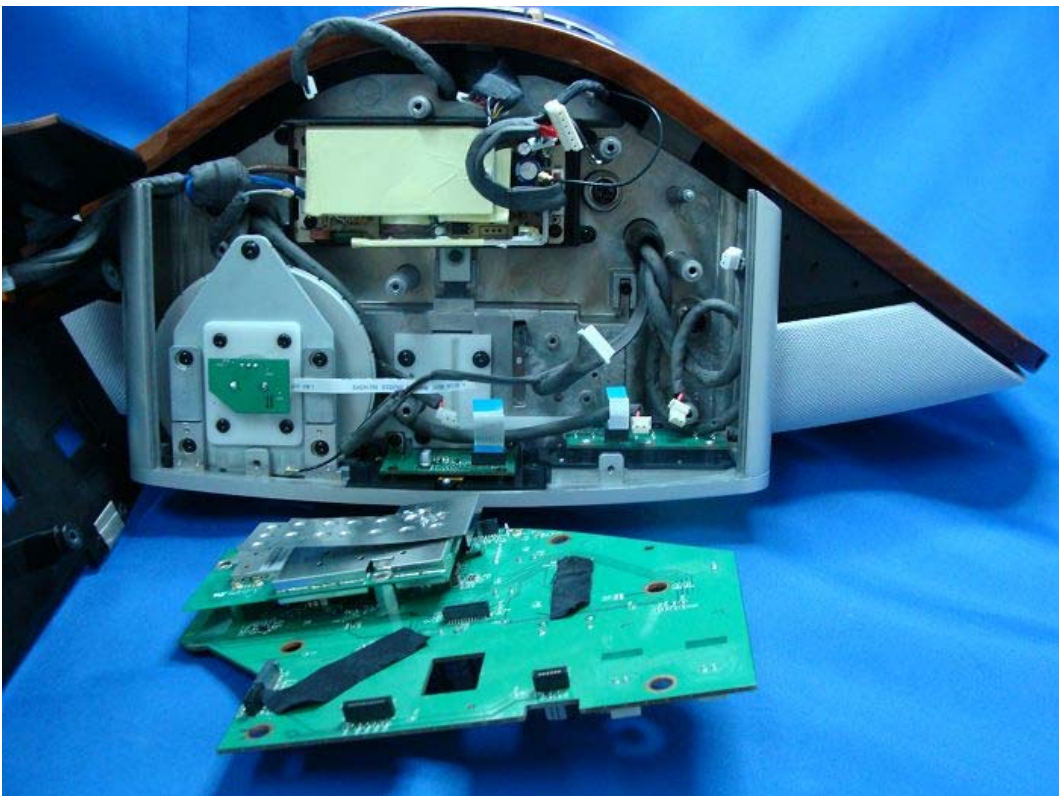
(8) EUT Photo



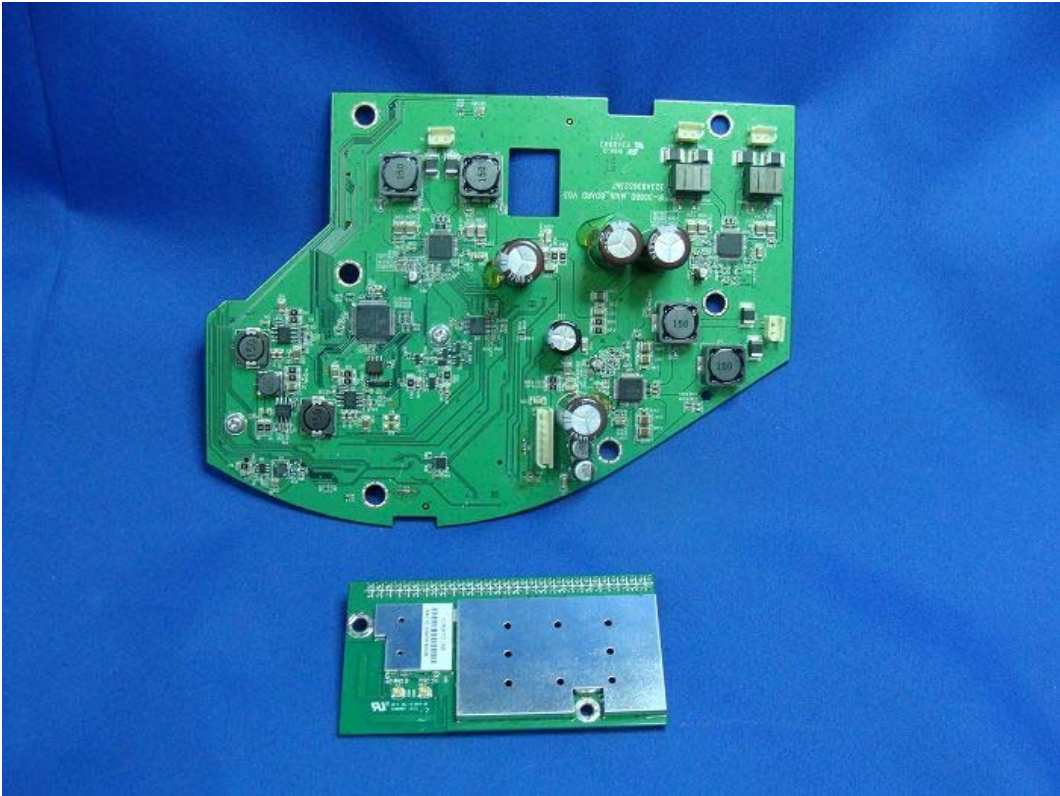
(9) EUT Photo



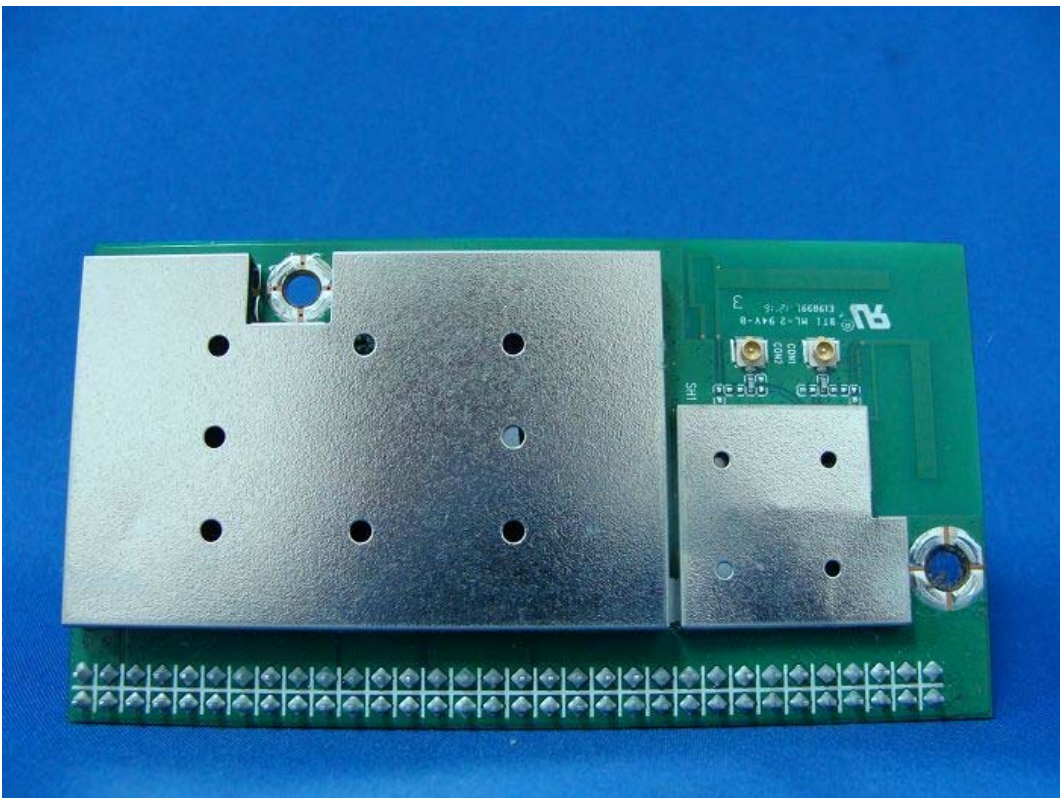
(10) EUT Photo



(11) EUT Photo



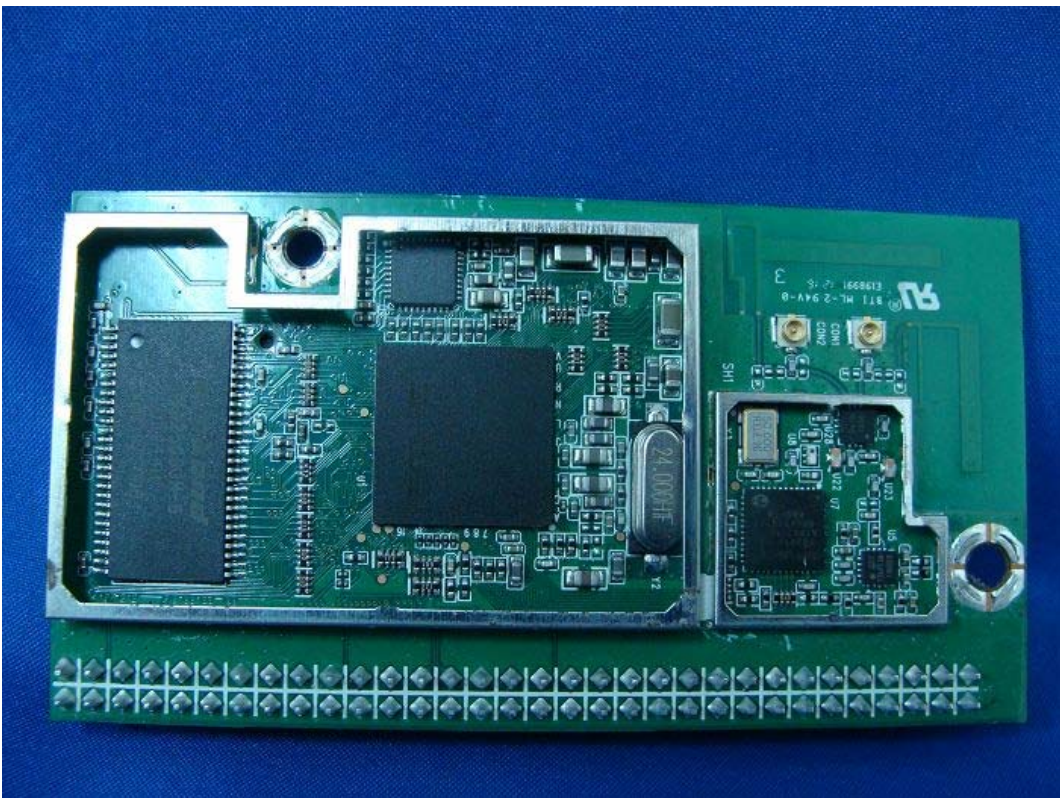
(12) EUT Photo



(13) EUT Photo



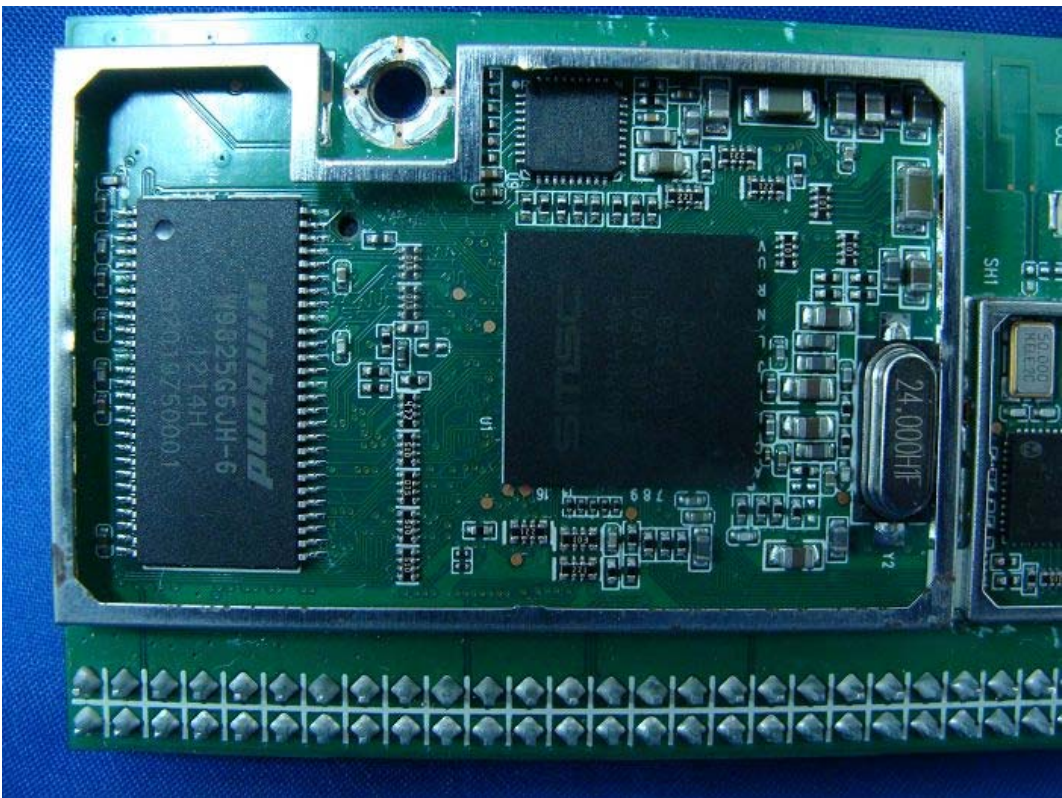
(14) EUT Photo



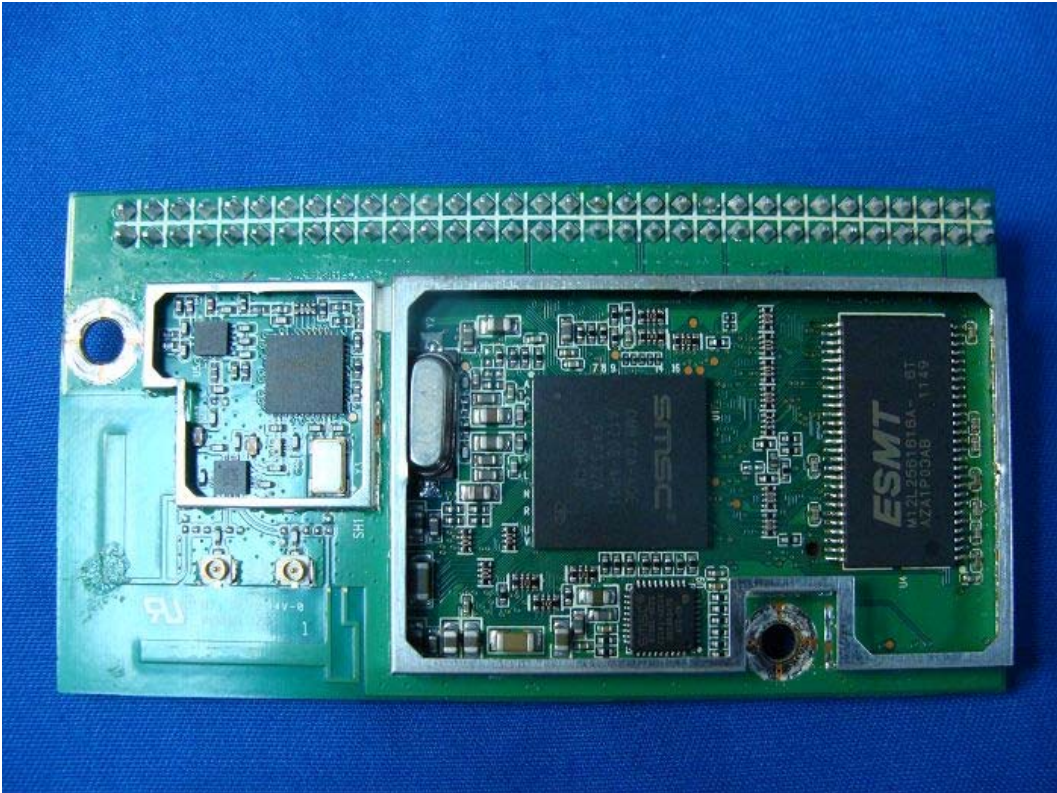
(15) EUT Photo



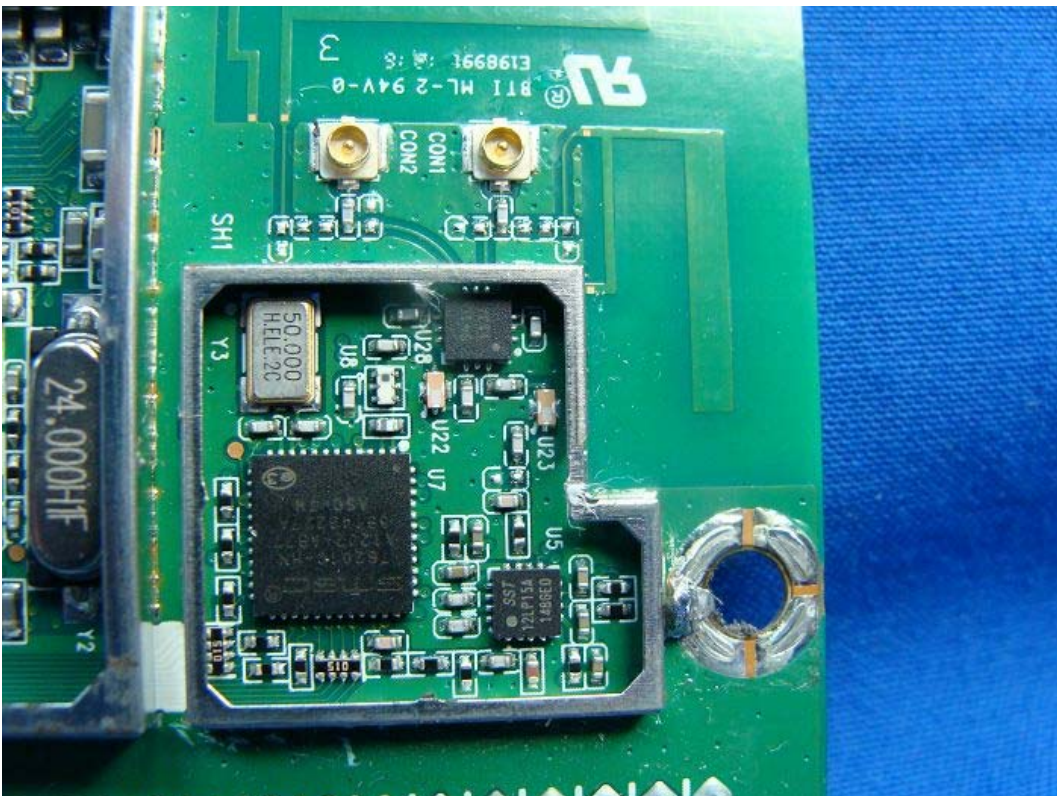
(16) EUT Photo (SDRAM_Winbond)



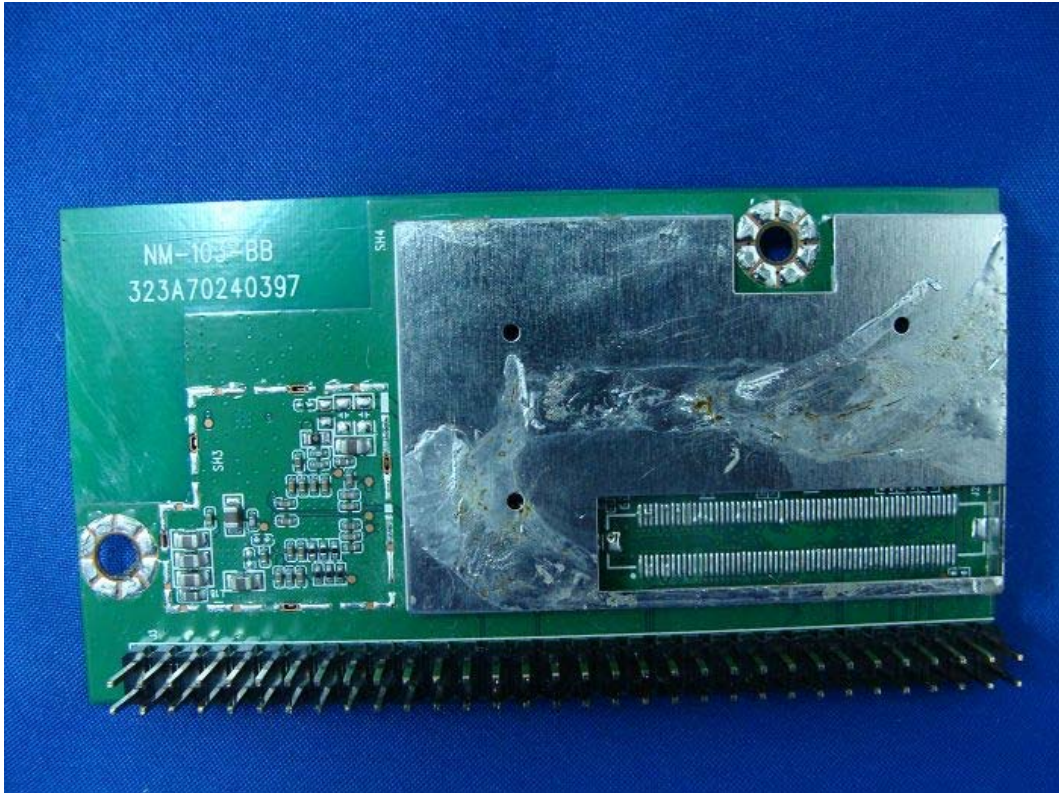
(17) EUT Photo (SDRAM_ESMT)



(18) EUT Photo



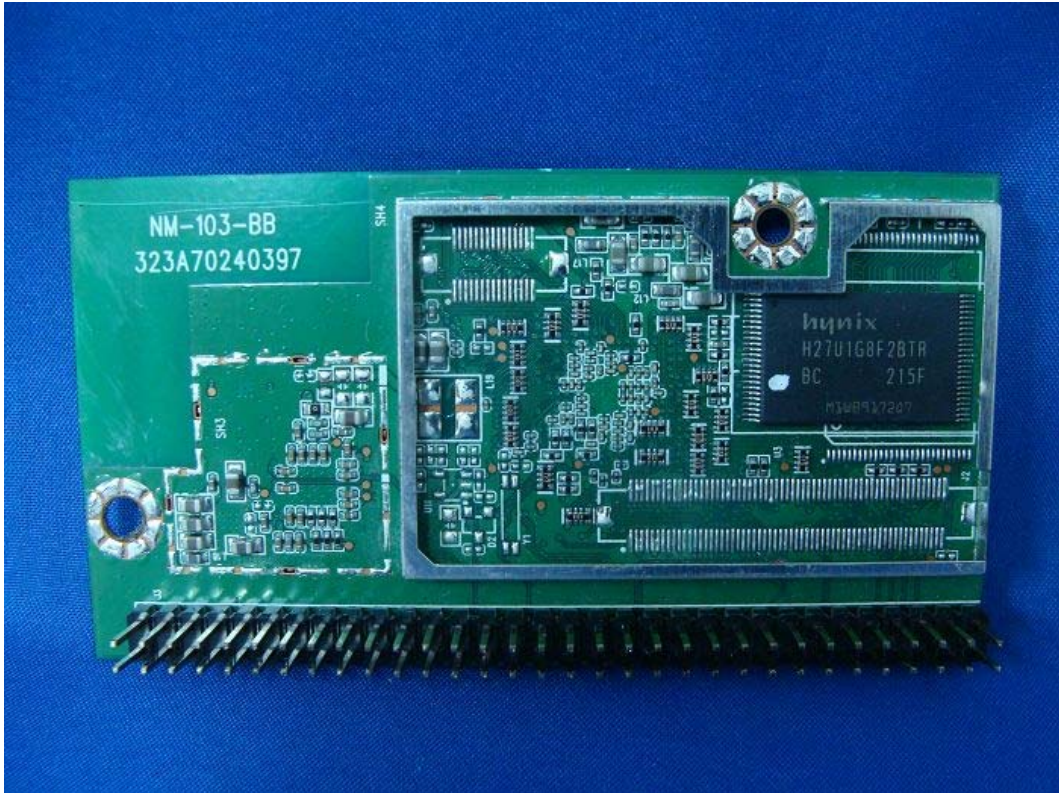
(19) EUT Photo



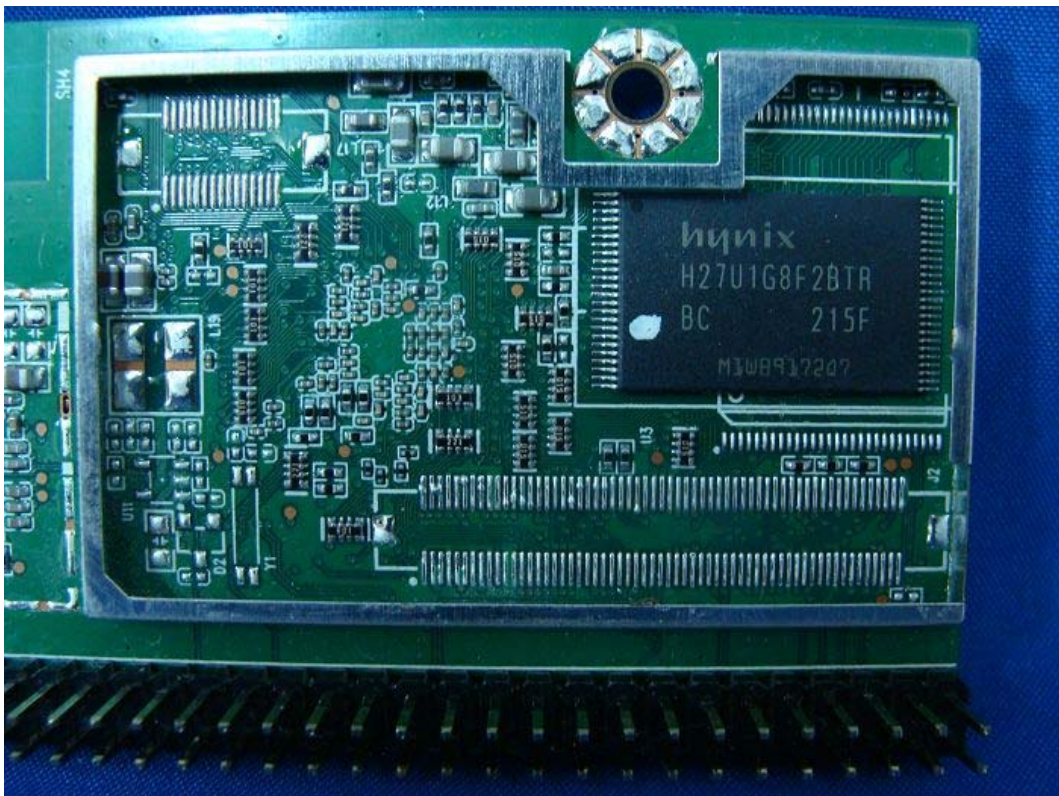
(20) EUT Photo



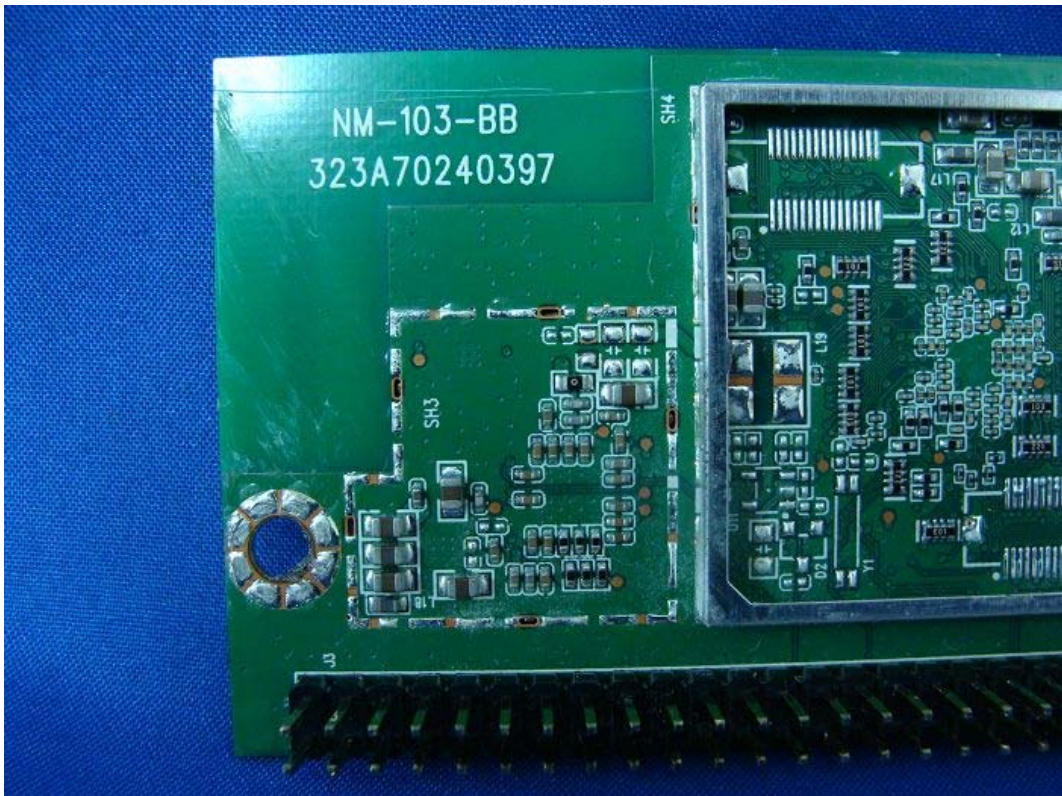
(21) EUT Photo



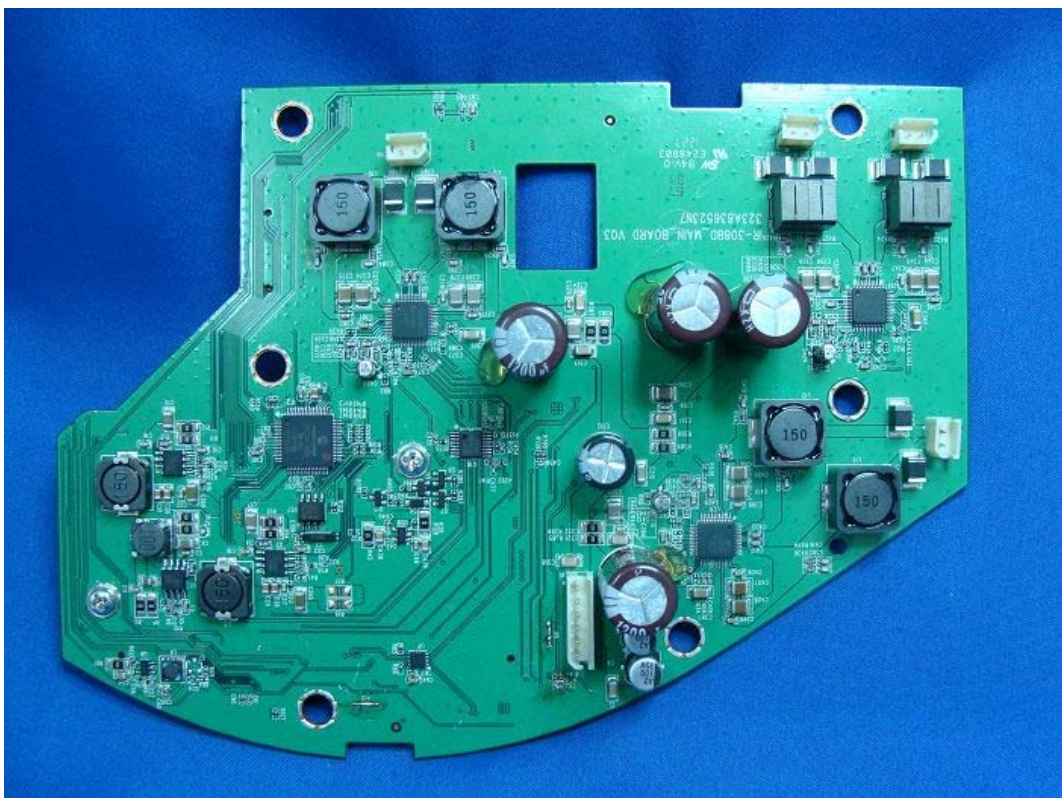
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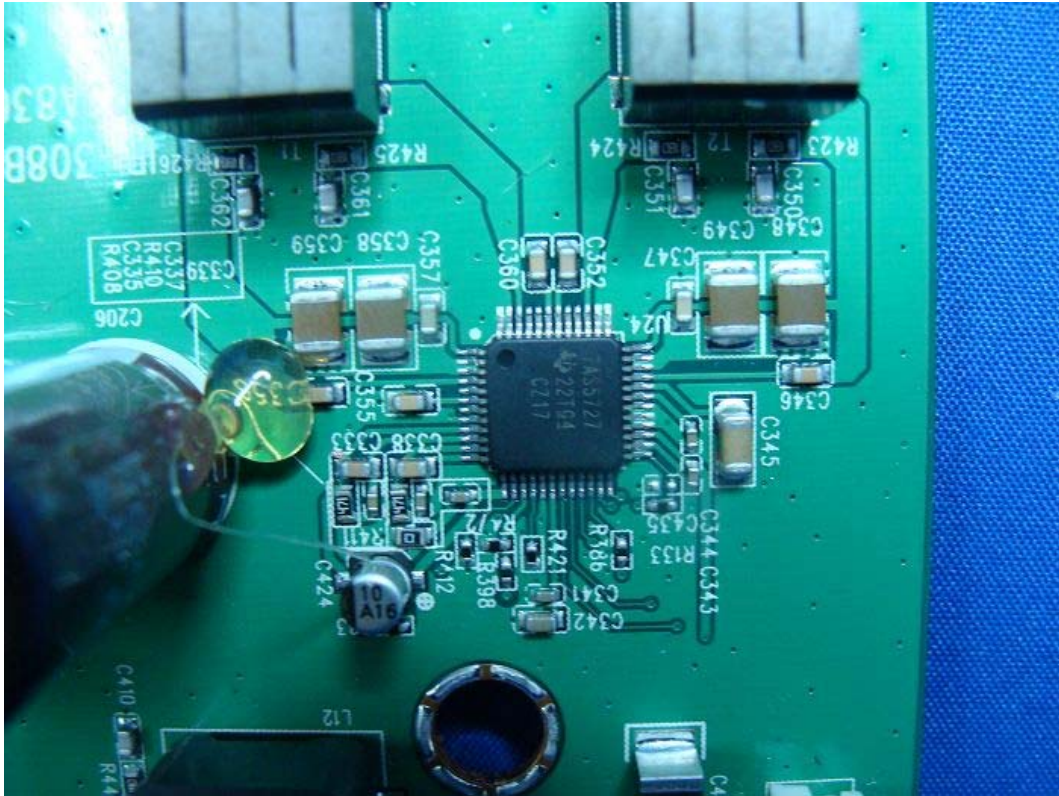
(23) EUT Photo



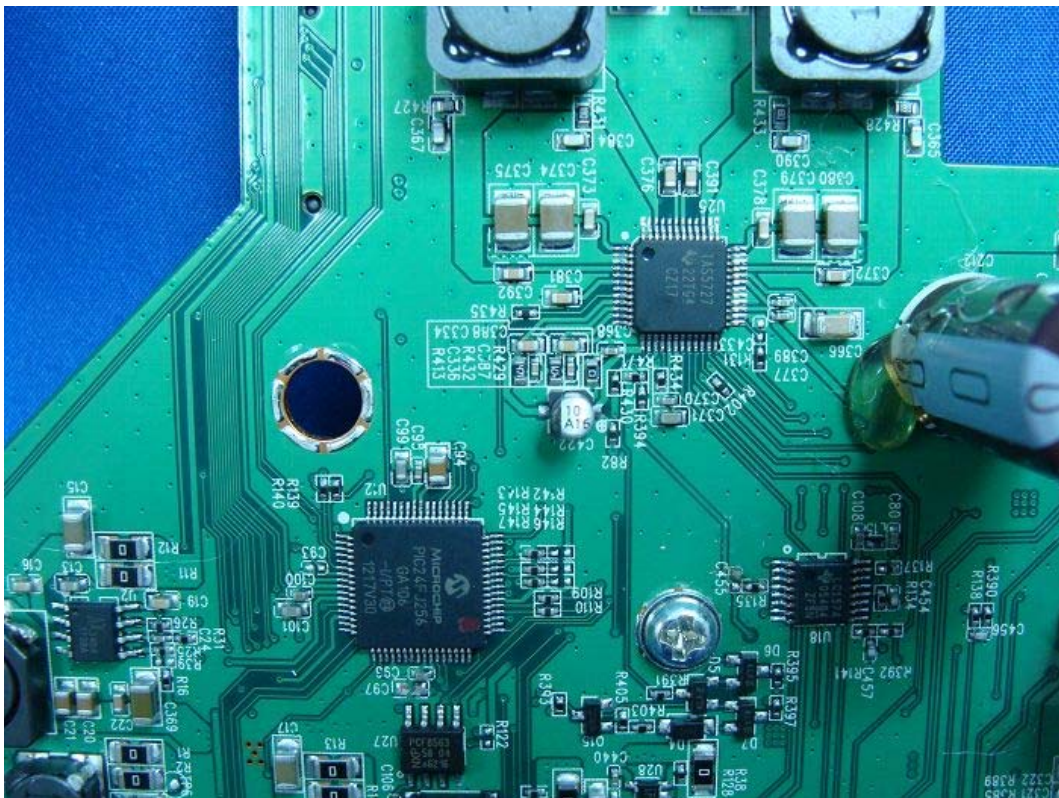
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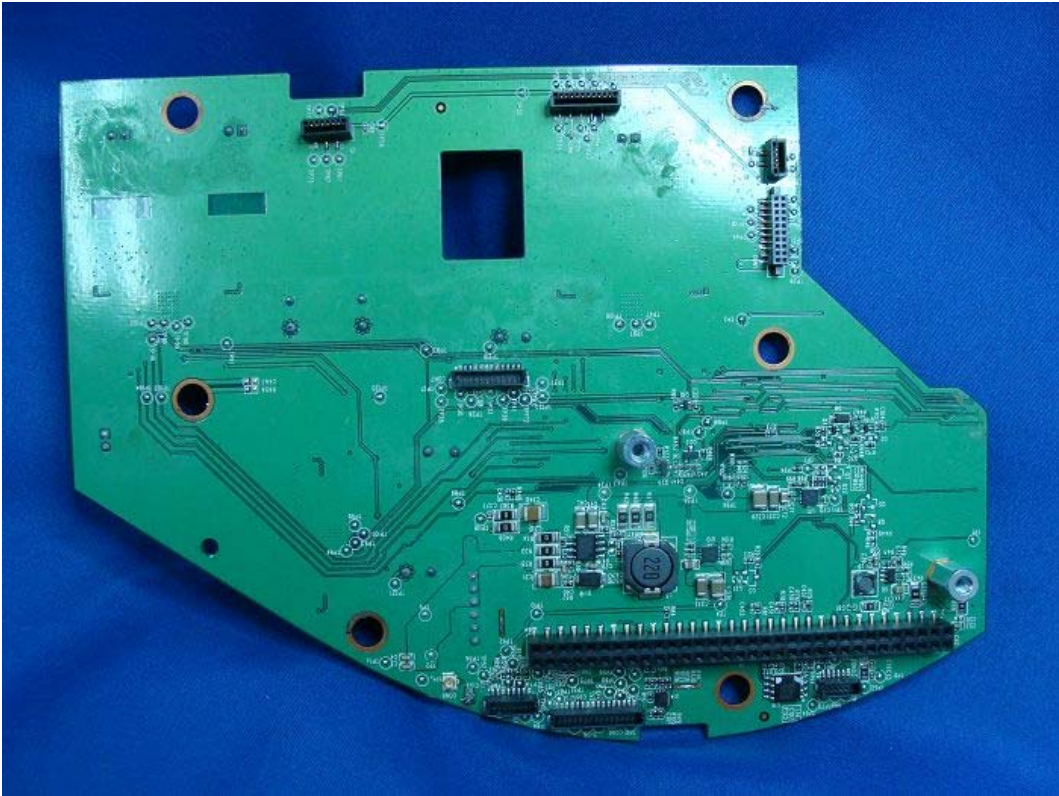
(25) EUT Photo



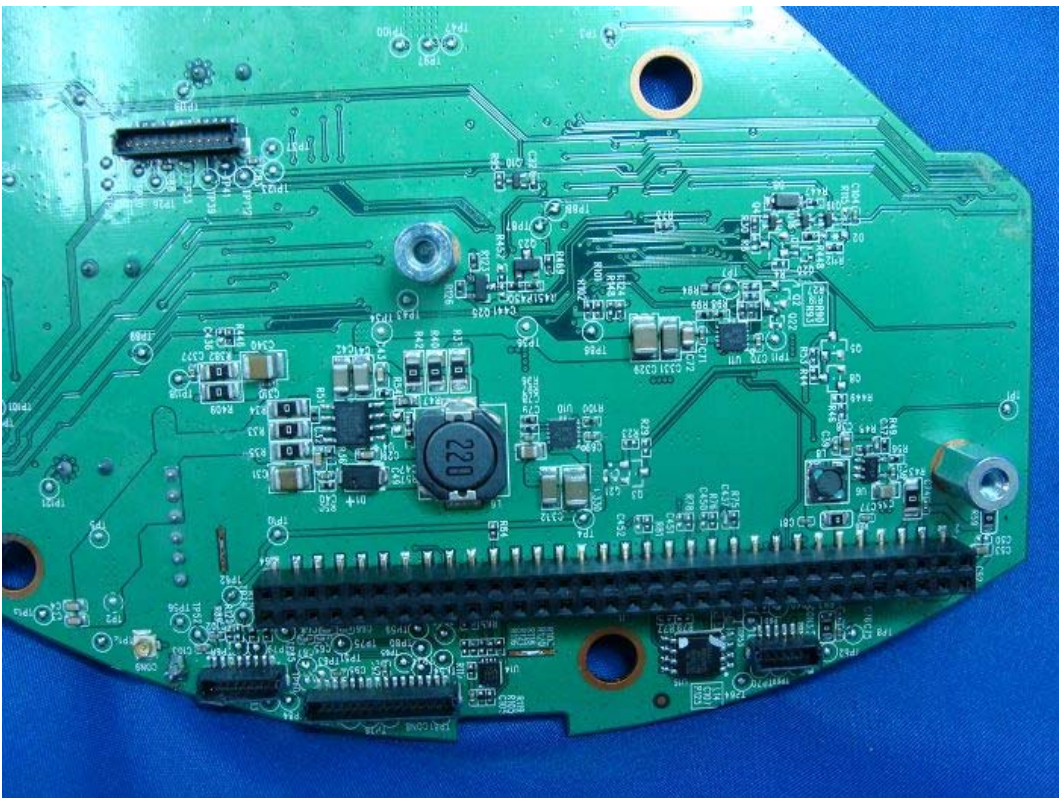
(26) EUT Photo



(27) EUT Photo



(28) EUT Photo



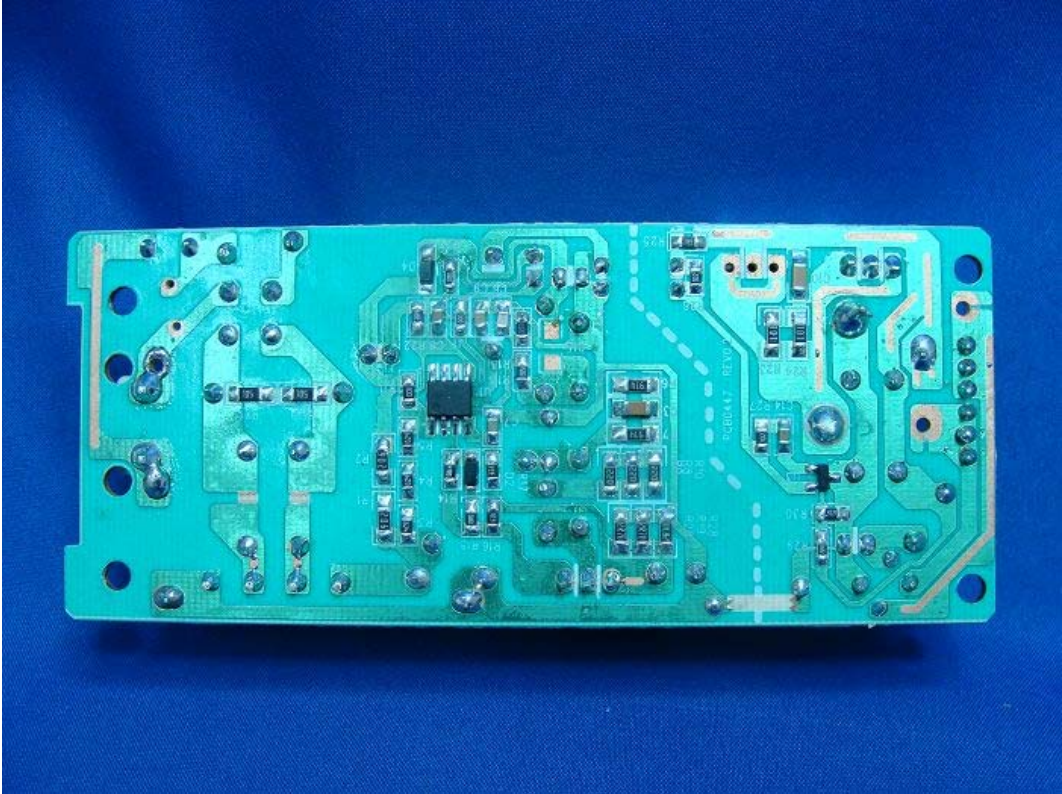
(29) EUT Photo



(30) EUT Photo



(31) EUT Photo



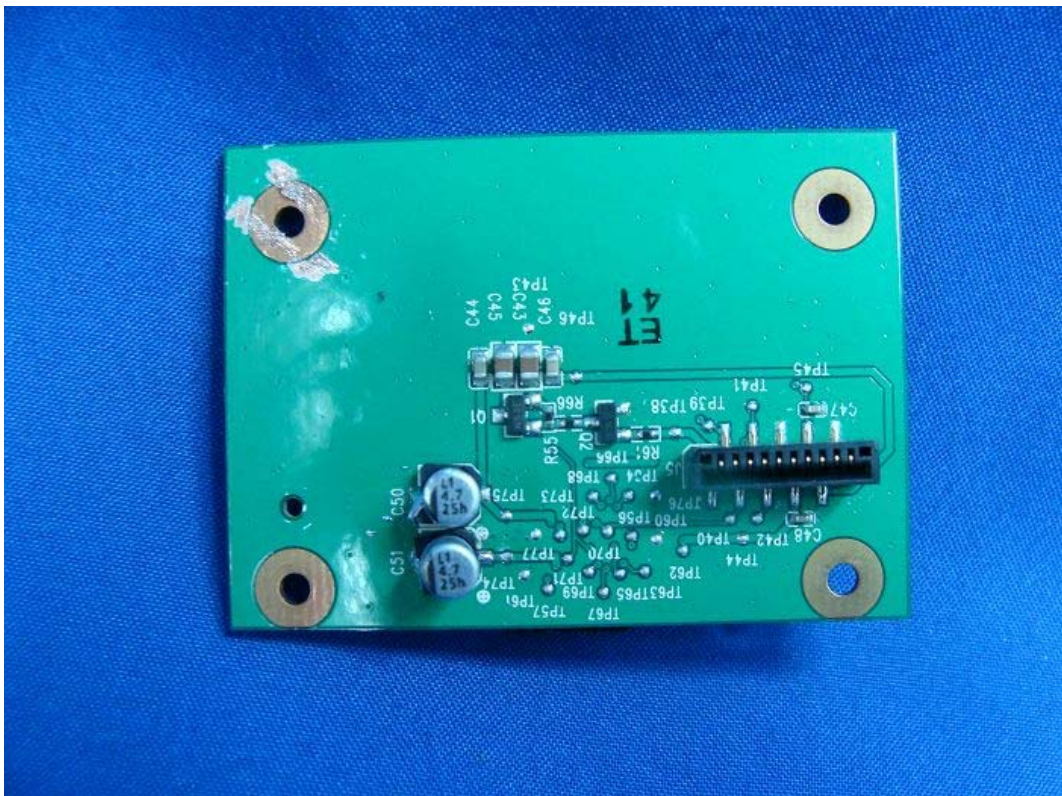
(32) EUT Photo



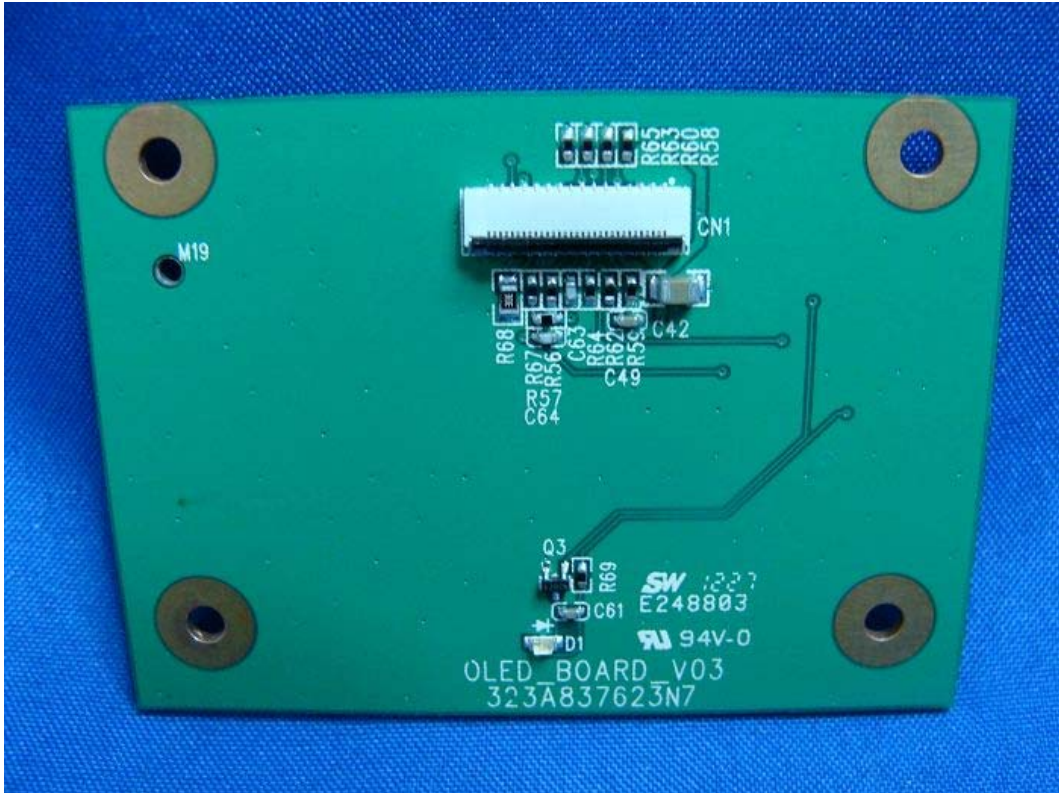
(33) EUT Photo



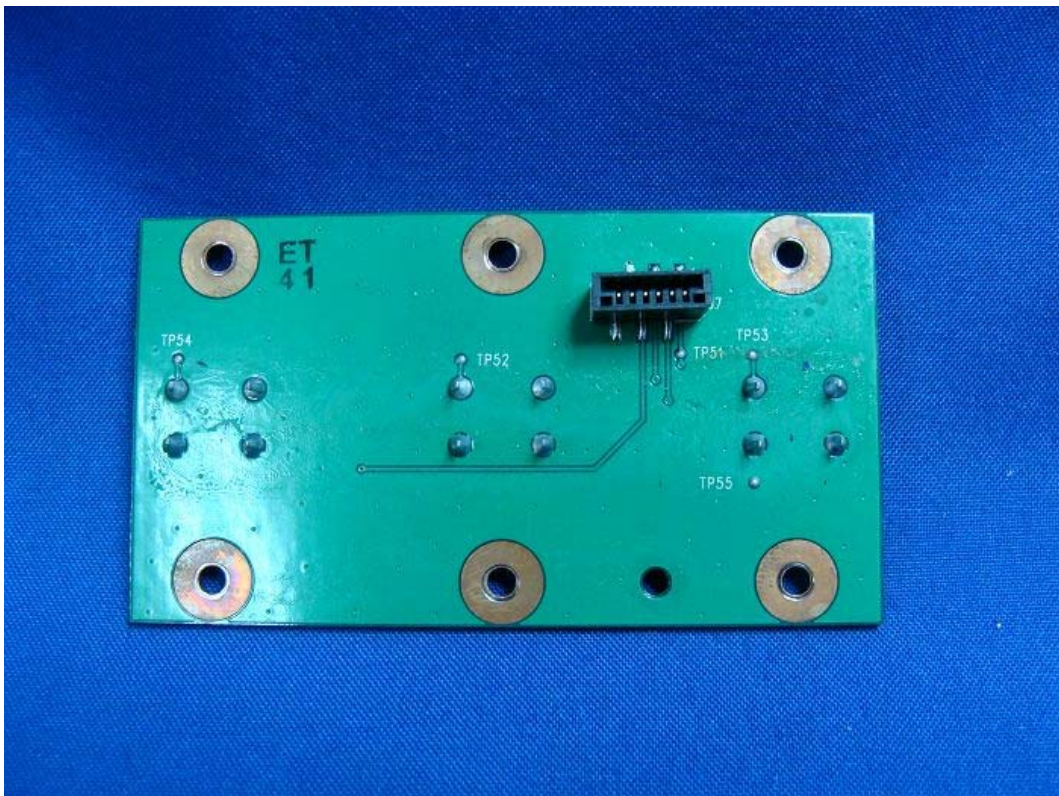
(34) EUT Photo



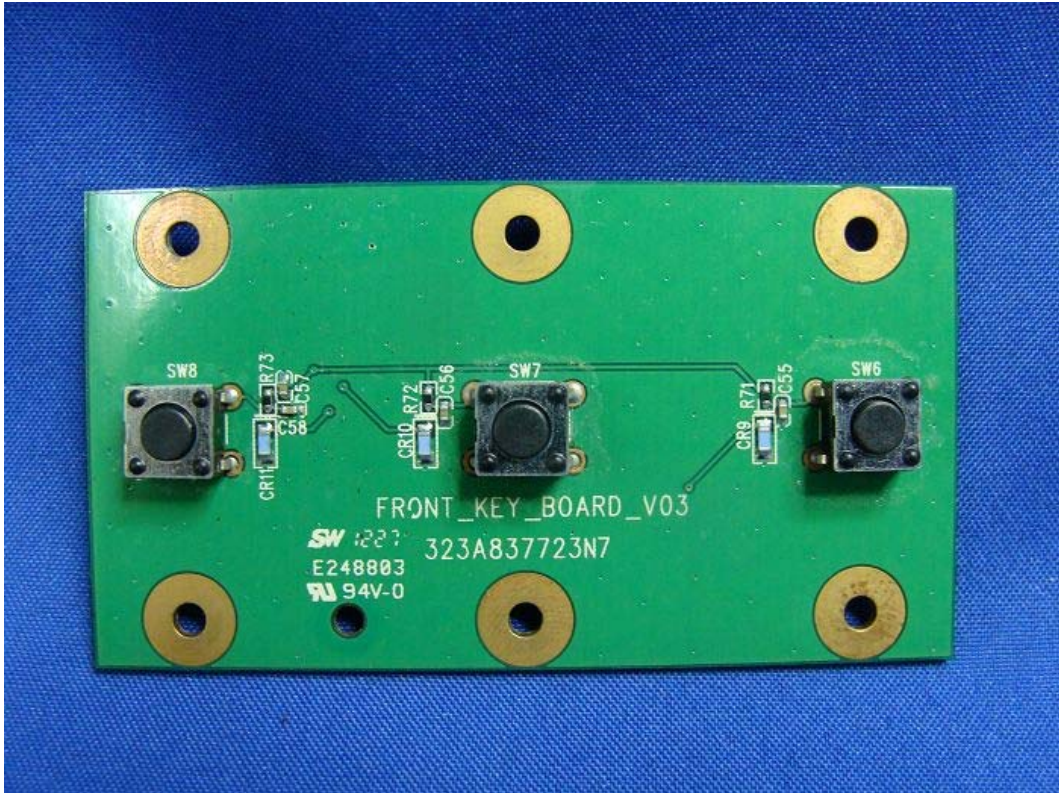
(35) EUT Photo



(36) EUT Photo



(37) EUT Photo



(38) EUT Photo



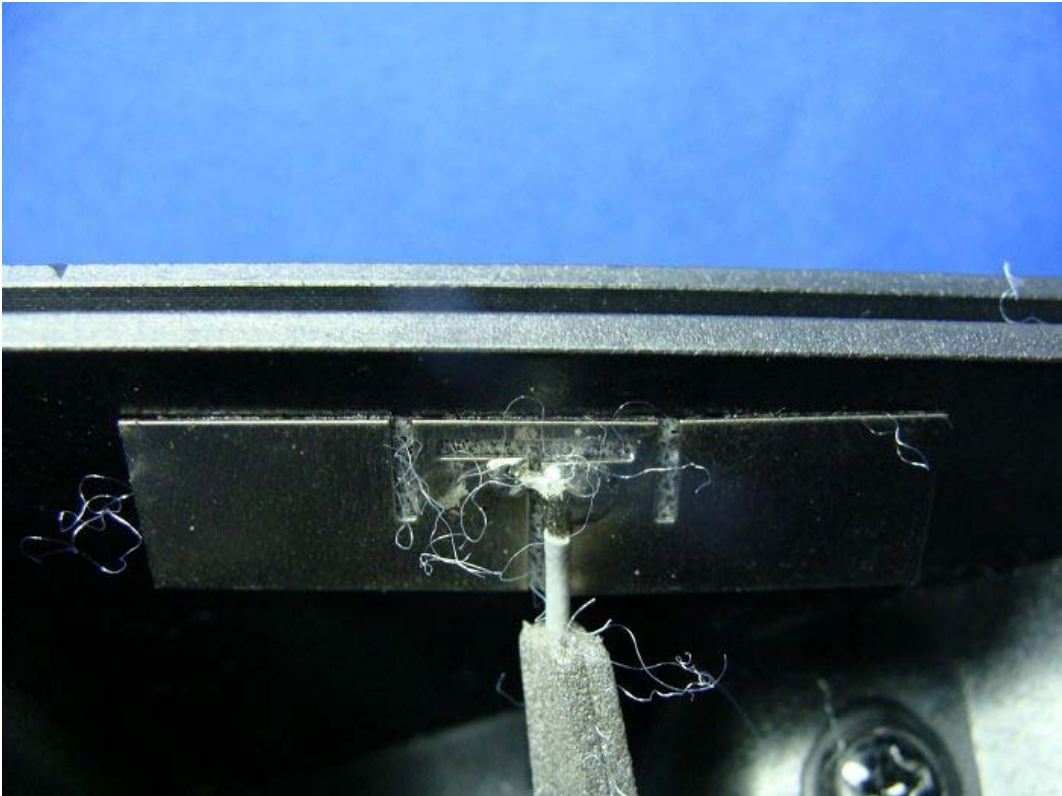
(39) EUT Photo



(40) EUT Photo



(41) EUT Photo



(42) EUT Photo



(43) EUT Photo



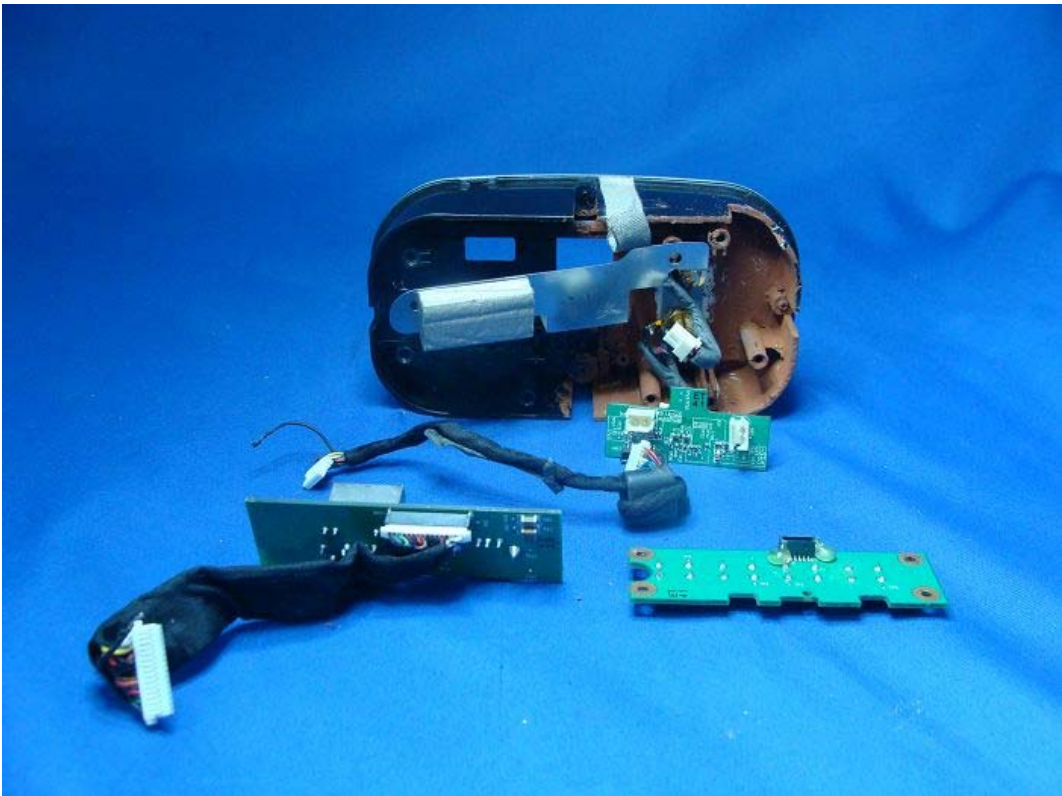
(44) EUT Photo



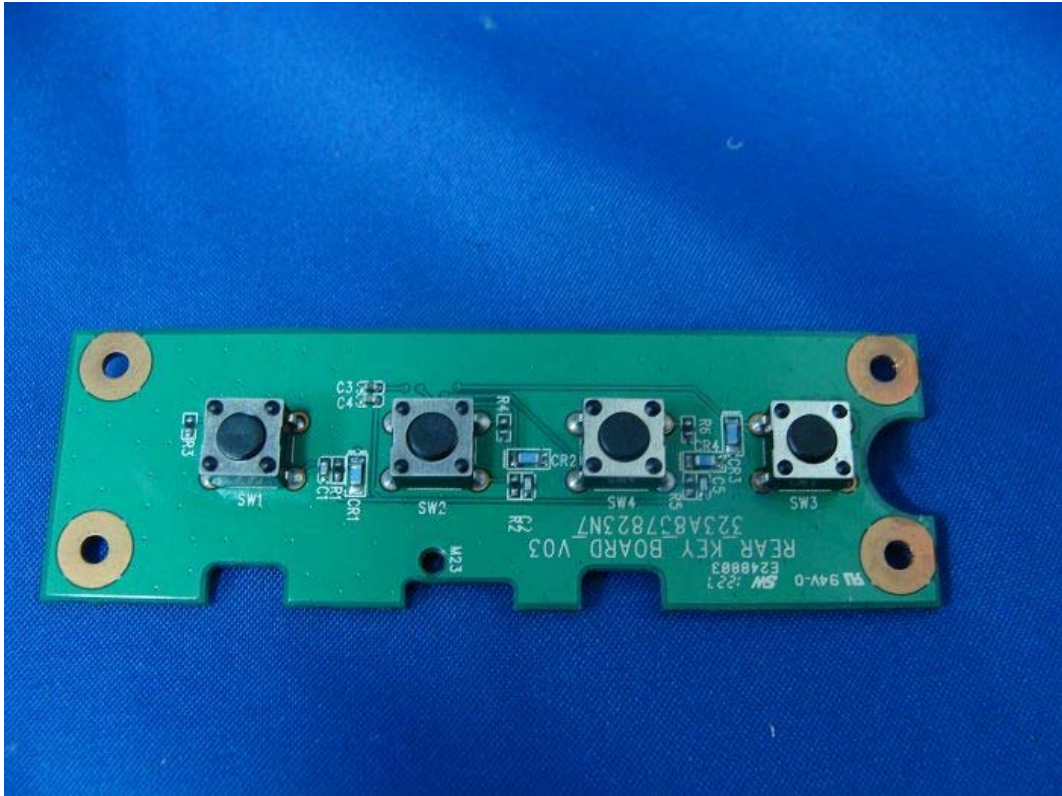
(45) EUT Photo



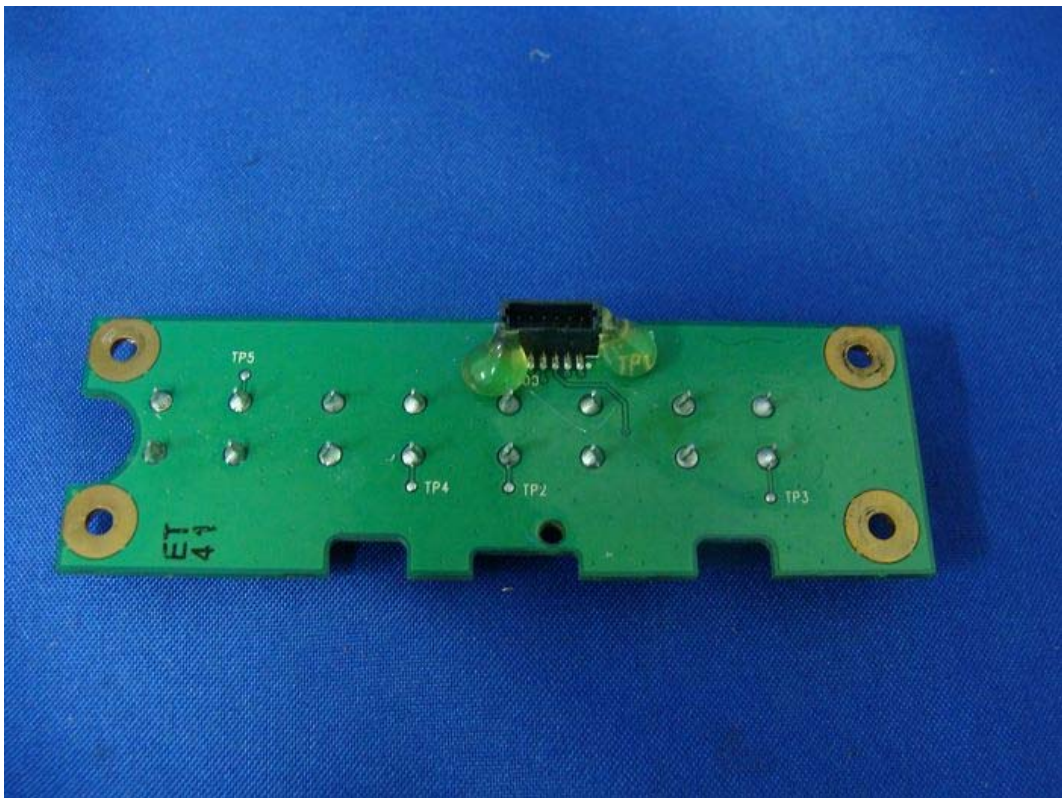
(46) EUT Photo



(47) EUT Photo



(48) EUT Photo



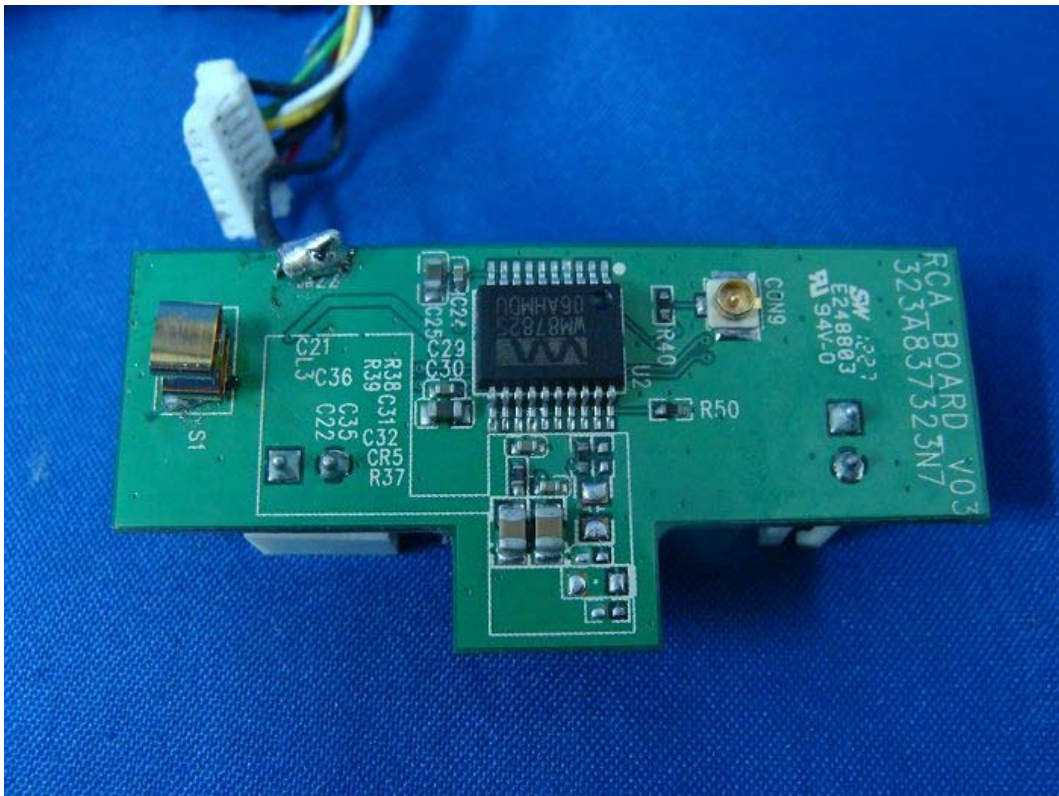
(49) EUT Photo



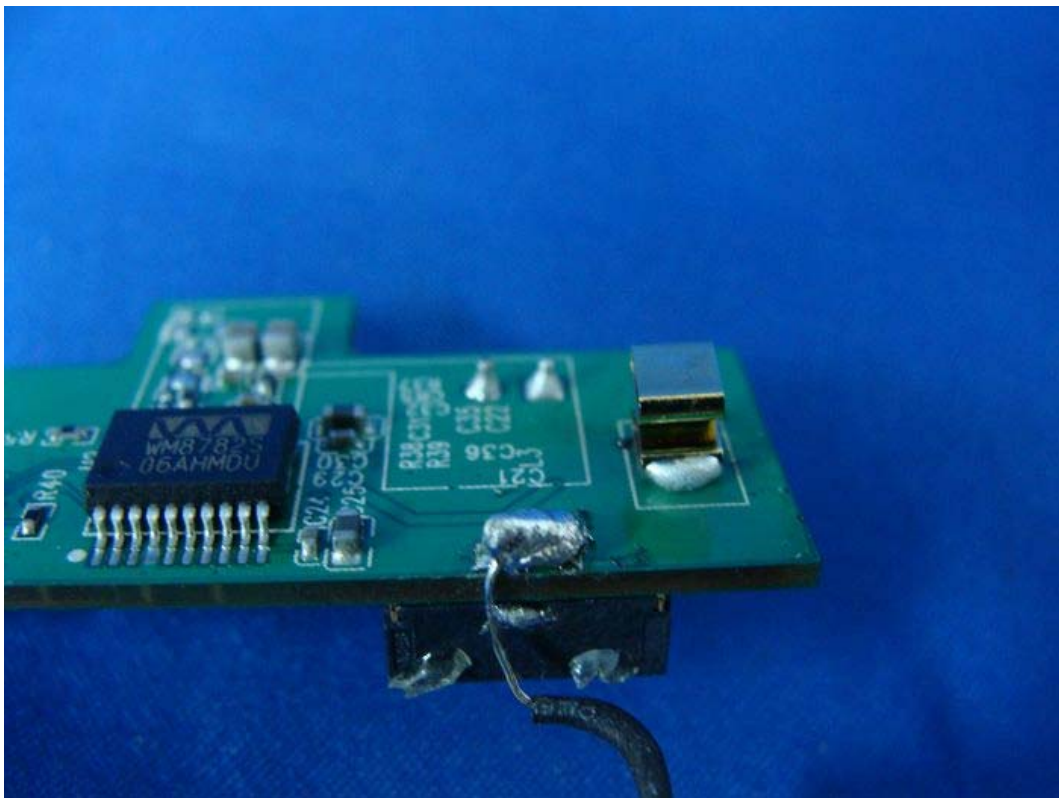
(50) EUT Photo



(51) EUT Photo



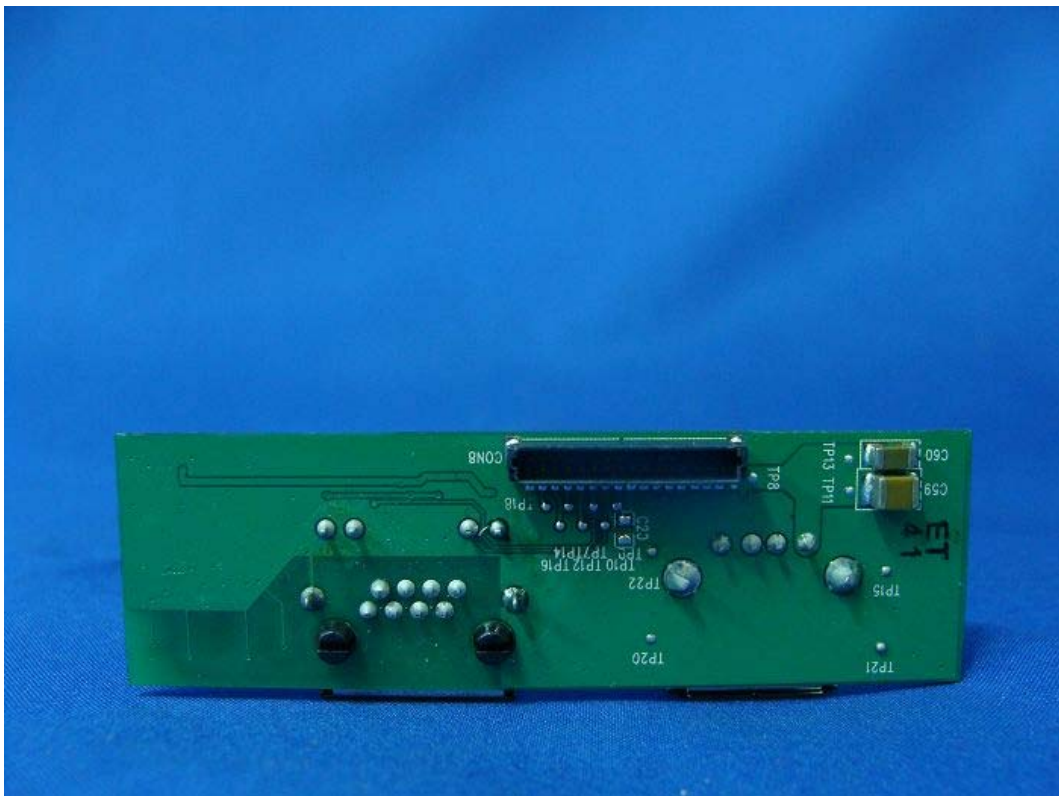
(52) EUT Photo



(53) EUT Photo



(54) EUT Photo



(60) EUT Photo



(61) EUT Photo



(62) EUT Photo



(63) EUT Photo

