1. Section 2.983 (d)(3). Range of operating power levels and description of means for variation of operating power

1. Range of operating power levels

The operating power levels is divided into 16 steps in CDMA mode

1-1PCS mode : -53.4 dBm ~ 24.6 dBm $\pm$ 0.2 dB

Level 0 : 24.6 dBm $\pm$ 0.2 dB	Level 8 : -16.3 dBm $\pm$ 0.2 dB
Level 1 : 20.8 dBm $\pm$ 0.2 dB	Level 9 : -21.6 dBm $\pm$ 0.2 dB
Level 2 : 15.5 dBm $\pm$ 0.2 dB	Level 10 : -26.9 dBm $\pm$ 0.2 dB
Level 3 : 10.2 dBm $\pm$ 0.2 dB	Level 11 : -32.2 dBm $\pm$ 0.2 dB
Level 4 : 4.9 dBm $\pm$ 0.2 dB	Level 12 : -37.5 dBm $\pm$ 0.2 dB
Level 5 : -0.4 dBm $\pm$ 0.2 dB	Level 13 : -42.8 dBm $\pm$ 0.2 dB
Level 6 : -5.7 dBm $\pm$ 0.2 dB	Level 14 : -48.1 dBm $\pm$ 0.2 dB
Level 7 : -11.0 dBm $\pm$ 0.2 dB	Level 15 : -53.4 dBm $\pm$ 0.2 dB

2. Means for variation of operating power

The RF interface of MSM communicates with the RF analog circuitry. This RF interface performs gain controls of Power amplifier(PA) and AGC(automatic gain control) amplifier using digital control signals.

The circuit functions of the IFR300 include the Rx AGC amplifier with 90dB dynamic range, quadrature IF mixer, down-conversion from IF to analog baseband, low-pass filters, and analog-to-digital converters(ADC) for converting to digital baseband.

The RF power output level is detected and then this information is sent to the MSM. The software controlled power management in MSM controls the Tx-AGC adjust signal.

2. Section 2.983 (d)(5) : The DC voltages supplied to and DC currents into the final RF amplifying device.

The final RF amplifier circuitry is consisted of RF amplifier module and DC voltage control transistor. The PCS Amplifier Module DC voltage and current supplied into the power amp module (PAM) is typical 3.4V and 300mA. In this hand-held device, power amp is directly activated using the battery cell

3. Section 2.983 (d)(6) : Function of each electron tube, semiconductor or other active device

The function of main component is as follows. The other active device is described in the attached material, part list.

1. RF part

RF part consists of power part, synthesizing part, transmission and reception part.

1-1. Frequency synthesizing Part

Frequency synthesizing part called Dual Digital PLL Synthesizer consists of two synthesizer circuit which is first local synthesizer, Dual Tx IF synthesizer and Rx IF synthesizer. Case of PCS Part, The first local synthesizer generates the primary local system oscillation frequency, operating over 2113.6 ~ 2173.6 MHz frequency range. Tx IF and Rx IF synthesizer generate the second local oscillation frequency, 527.2 MHz and 367.2 MHz respectively.

1-2. Receiving Part

- PCS Duplexer(U502) : The duplexer filters the RF signal transmitted through ANT (frequency range:1850~1910MHz) and sends the signals to LNA (frequency range:1930~1990MHz)
- RF2489(U601): The RF2489 is a high performance CDMA dual-band /tri-mode integrated LNA/mixer. The operating voltage is 2.7V and is compatible with 1.8V logic for control lines. The RF2489 integrates the dual-band LNA/downconverters with 30dB of gain control and TX LO buffers. Additionally, a divide-by-2 prescaler is integrated to allows the use single-band VCO.
- IFR3000(U661): This part is designed to control the gain of the dynamic range of midrange frequency produced in down converter according 90 dB dynamic range.

1-3. Transmission Part

- RFT3100 (U731) : This part includes an IF mixer for upconverting analog baseband to IF to RF, a programmable PLL for generating Tx IF frequency, single sideband up conversion from IF to RF, two Cellular and two PCS driver amplifiers, and Tx power control through an 85dB VGA.
- PCS Power AMP module (U811) : This part is designed to work in 1850 MHz ~ 1910 MHz frequency range in the CDMA mode and can generate the proper power
- PCS Up converter (FIL721): This part mixes the mid-range transmission frequency 130.38 MHz and the first local 2113.6 ~ 2173.6MHz to generate transmission frequency of 1850 ~ 1910 MHz.

2. Logic Part

Logic part consists of power supply part, digital and audio part, LCD module part. The Fig 1-2 is the block diagram of logic part.

2-1. Power supply Part

Power is supplied by battery, operating over 3.2V to 4.2V range, or external source. And also battery power is input about 4 low-dropout voltage regulators.

- U101 : voltage regulator for digital and analog circuit (2.7V DC)
- U151 : voltage regulator for TCXO part(3.0V DC)
- U161 : voltage regulator for RF Rx part (3.0V DC)
- U171 : voltage regulator for RF Tx part (3.0V DC)

2-2. Digital and Audio Part

- MSM 5105 (U102) : ASIC is a chip responsible for CDMA/FM mobile station's base-band digital signal processing. For this chip to function, CHIPx8(9.8304MHz) and TCXO(19.2MHz) are required as basic clocks.
- And sleep crystal(32.768KHz) is used as clock source of SBI.
- MSM consists of a CDMA processor, a Digital FM(DFM) processor, a multi-standard Vocoder, an integrated CODEC with earpiece and microphone amplifiers, general-purpose ADC for system monitoring, an ARM7TDMI microprocessor.
- The integrated Codec contains all of the required conversion stages for the audio front end
- The Codec interface includes the amplification stages for both the microphone and earphone. The interface support two differential microphone inputs and a differential auxiliary input, each of which can be configured as single-ended if desired. In addition, the interface supports one differential earphone output, one single ended earphone output, and one differential auxiliary output.

4. Section 2.983 (d)(9). Tune-up procedure over the power range.

Cellular Telephone Adjustment and Test Procedure

1. Overview

With ordinary use in clean, dry environments, no periodical alignment should be necessary for PX-25B.

2. Test equipment

The equipment listed below are required for proper test and maintenance.

No.	Equipment	Specifications
1	DC Power supply	Capable of 6V/2A Max. and has built-in Amphere meter

2	Radio Test	● HP 8924C CDMA Mobile Test Station
		● MARCONI 2957, 2960
		● Replacement equipment for HP 8924C
		  1) RF Signal generator
		  2) FM Linear detector
		  3) RF Power meter
		  4) Frequency Counter
		  5) AF Generator

		6) SINAD Meter
		7) Modulation Analyzer
3	DC Voltage meter	20V range
4	Spectrum Analyzer	HP 8595E
5	Oscilloscope	Maximum freq. 50MHz
6	Test Jig.	Interface port for UART communication

3. Test Configuration

The test configuration for adjustment and test is shown in Figure 1.

4. Test Mode

Test commands can be used after switching to test mode when adjusting and diagnosing the telephone. Test mode uses a separate command structure. Built-in antenna shall not be connected in test mode and shall be connected only to the test instrument. If other telephone begins operation within the radius of several meters where telephone is tested in the test mode, it will cause a bit noise or other failure.

Also, a telephone is affected by interference from local stations at places where strong field signal exists causing undesirable effects when measuring reception sensitivity or diagnosing in test mode

* Caution

− When inputting adjustment data in the semi-permanent memory by pressing [SEND] key, phone set shall not be turned off the power or power supply shall not be interrupted after pressing [SEND] key. Until storing is completed in the memory, at least one minute shall pass before turning off the power.

− Wrong operation will cause CPU to stop, or cause phone set to fail to operate or not to operate.

5. Key Functions of Test Mode

Code	Test Item	Remark
[#][#][2][7] [2][6][END]	1: VER VIEW	Display S/W version
[#][#][2][7] [7][3][END]	3: DEBUG SCREEN	Display debug information
[#][#][2][7] [6][8][END]	4: VIEW BATT VAL	Display battery ADC value
[#][#][0][5] [1][5][END]	5: VIEW THERM VAL	Display thermister value
[#][#][2][2] [2][2][END]	6: VIEW LNA STAT	Display LNA state
[#][#][2][2] [4][0][END]	7: TEST mode	Test mode
[2][5][3][9] [*][*]	A-KEY INPUT	

6. PCS test mode

Perform the following procedures to switch to test mode.

TEST ITEMS	REMARK
1	Press [PWR] key to turn on the telephone.
2	Press the following 7 keys in sequence. [#][#][2][7][7][4][2][END]
3	Telephone is currently switched to test mode. To exit test mode, press [END] key, then turn it on again to switch to standby mode.

6-1. Test program proceeding method

| TEST ITEMS	REMARK
1:RX_AGC_ADJ [9][0][0][STO]	.RX AGC Extract Channel Setting. .Set Asec Pwr to –107.4 ~ -22.6 dBm (+ loss) .Asec Pwr is divided into 16 stages in 5.3 dBm intervals .Delayed for 0.5 seconds until the value is stabilized .Press [STO] Key
2:TX_AGC_ADJ [9][0][1][STO]	.TX AGC Extract Channel Setting .Setting Asec Pwr to the level of –65 dBm (+ loss) .Press the Up and Down Keys to adjust until Avg .Pwr Become 20.8 dBm to –42.8 dBm. .Intervals of Avg Pwr are 14 stages with 5.3 dBm.
3:CDMA_PWR_LIMI	.Adjust 500 Channels Power Limit
4:TX_CHAN_PWR [9][0][2][STO]	.Set Asec Pwr to –104 dBm (+ loss) .Press Up and Down Keys to Adjust Pwr to maintain over 24.5 dBm
5:FCC_PWR_TEST	.TX PWR Carrier On .Press # and keys to Adjust Pwr to maintain at 24.8 dBm
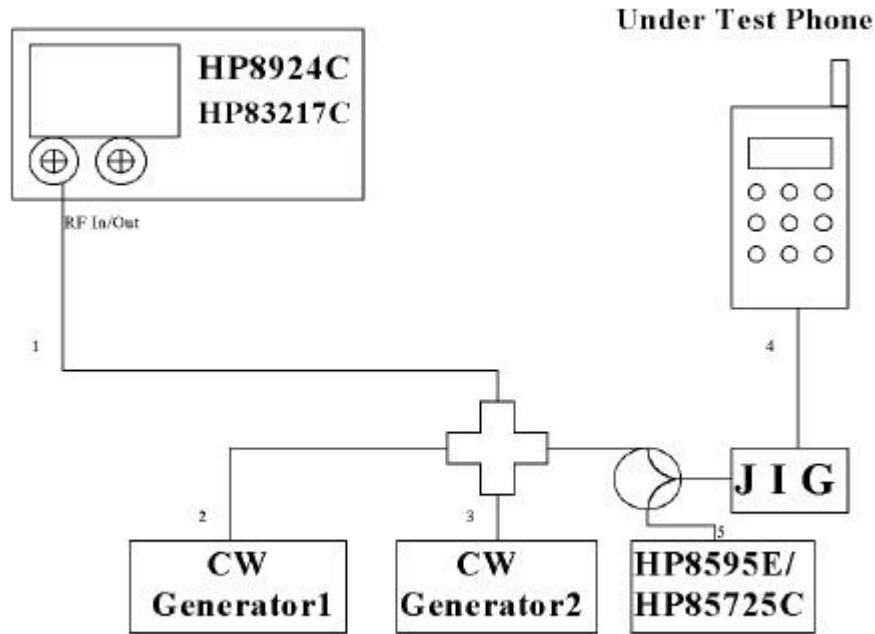
Figure 1. Equipment Configuration for Adjustment and Test

5. Section 2.983 (d)(10). Description of frequency determining and stabilizing circuitry

Frequency synthesizing part is composed of the first local RX IF synthesizer which is single mode PLL synthesizer and the internal Tx IF and Rx IF synthesizer which are in IFT and IFR chip. This part generates the first local oscillation frequency, Rx IF frequency and Tx IF frequency.

- PCS Mode First local frequency synthesizer : 2113.6MHz ~ 2173.6 MHz
  PLL loop is composed of single PLL synthesizer, Loop filter, VCO and VC-TCXO. It generates transmission and receive frequency of 2113.6MHz ~2173.6 MHz.
- PCS Mode Rx IF synthesizer : 367.2 MHz
  PX-25B is use the common Receive Intermediate Frequency structure.
  So, Cellular and PCS mode Rx IF is same.
  Rx IF PLL loop is consisted of PLL synthesizer in the PLL module, VCO installed in IFR IC, loop filter and VC-TCXO(Crystal oscillator 19.2 MHz). It oscillates twice the intermediate receiving frequency of 367.2 MHz and then generates 183.6 MHz, Rx IF frequency.

■ PCS mode Tx IF Synthesizer : 527.2MHz

The configuration of PLL loop is composed of PLL Synthesizer, VCO which is internally installed, loop filter and VC-TCXO(standard clock). It oscillates twice of the transmission intermediate frequency of 527.2MHz and then generates Tx IF frequency of 263.6 MHz through the PLL loop.

The frequency of 19.2 MHz generated from the VC-TCXO is the standard clock of those each the frequency synthesizer part. PLL frequency stability is determined by the stability of oscillator sage of VC-TCXO. This prevents maximum frequency variation from exceeding **2.0P**PM.

6. Section 2.983 (d)(11). Description of circuit employed for suppression of spurious radiation

In the CDMA transmit signal path, the frequency spectrum at the output of the CDMA DACs contains unwanted frequency components due to the DAC output transition edges and transients. The transmit clock frequency and harmonics are found in the spectrum.

■ Each CDMA DAC is followed by an anti-aliasing low-pass filter with a bandwidth of 630 KHz that reduces unwanted frequency components installed in RFT.

The Tx RF output of the Tx Mixer and the drive amp is filtered again by the SAW band pass filter. The nominal specification of the filter is as follows.

< PCS Mode >
■ Pass band   : 1850 MHz ~ 1910 MHz
■ Attenuation : DC ~ 1500MHz   : 20 dB min.
        1500 MHz ~ 1800 MHz : 23 dB min.
        1930 MHz ~ 1990 MHz : 7 dB min.
        3700 MHz ~ 3820 MHz : 25 dB min.

7. Section 2.983 (d)(12). Description of modulation system used

The PCS Only phone PX-25B uses digital signal processing. To design the digital signal processing, Qualcomm Mobile Station Modem(MSM), RFT and IFR(Rx IF-Baseband converter) performs all of the signal processing. The MSM integrates functions of a CDMA processing, a digital FM(DFM) processing, Vocoder, Codec, RF interface, and ARM microprocessor.   CDMA subsystem in the MSM performs CDMA
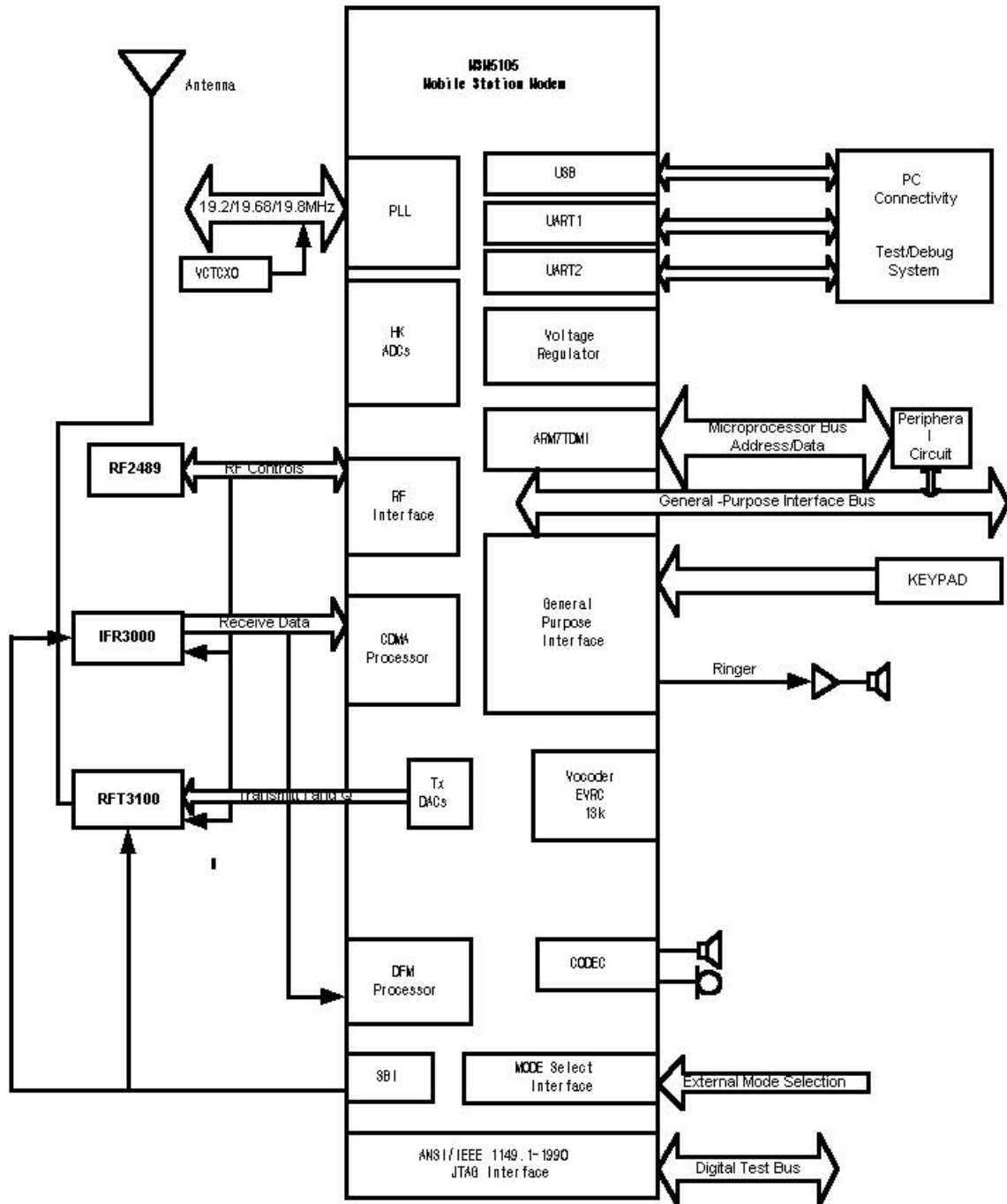
Figure 3-1. MSM5105 Functional Block Diagram

The Vocoder encodes and decodes packets using Qualcomm's QCELP and EVRC encoding to compress the speech samples. The encoding rate is determined by the Vocoder which formats the encoded speech samples as data packets. The encoded signal is transferred to the DFM subsystem.

The Vocoder interpolates incoming Tx PCM from the CODEC to a higher sample rate for the DFM subsystem. In DFM mode, the Vocoder acts as a digital signal processor(filtering, gain control, limiting), processing digital audio samples during operation. The following figure shows the DFM signal processing blocks and DFM signal flow from the internal CODEC of MSM through to VOCODER and to the IFR and the RFT.
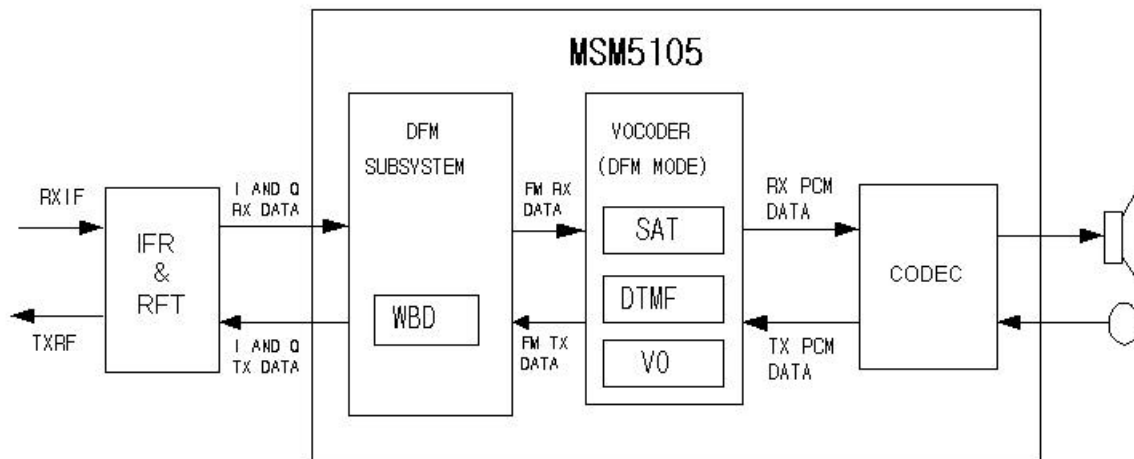
Figure 3-2. Signal Flow Between CODEC and RFT/IFR

The vocoder's Tx path also includes a SAT transponder, DTMF generation circuits and pre-emphasis filter. The CDMA baseband processor performs forward-link demodulation, time tracking and reverse-link modulation for CDMA digital signals. The following figure shows a CDMA digital baseband processor block diagram.
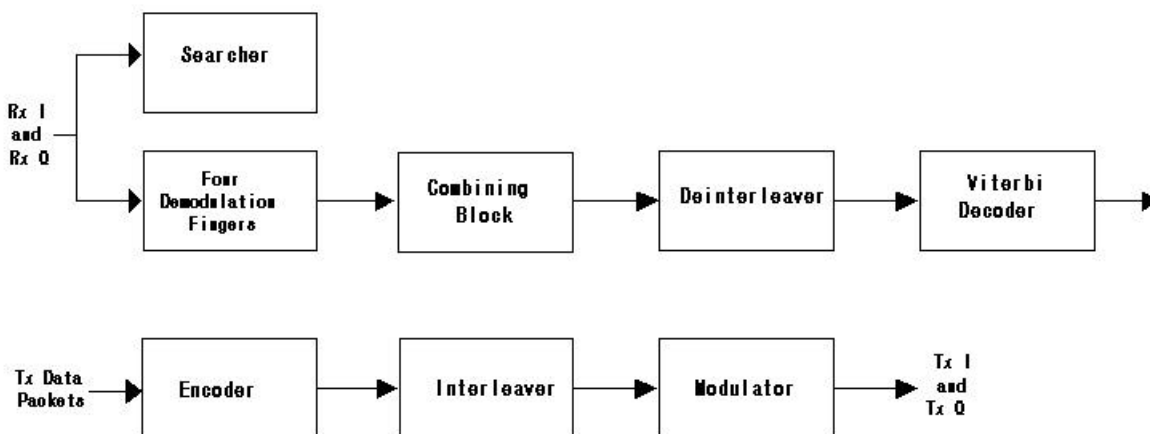

Figure 3-3. CDMA digital Baseband Block Diagram

The modulator performs the orthogonal modulation, long code PN spreading and quadrature spreading. The resulting data stream is then band limited with FIR filters and sent to the analog baseband processor.

The RFT3100 Baseband-to-RF Transmit Processor performs all transmit(Tx) signal processing functions required between digital baseband and Power Amplifier(PA) for JSTD-018 PCS.b The baseband quadrature signals are upconverted to PCS frequency bands and amplified to provide signal drive capability to the PA. The RFT3100 includes an IF mixer for upconverting analog baseband to IF , a programable PLL for generating Tx IF frequency, signal sideband upconversion from IF to RF, two Cellular and two PCS driver amplifiers, and Tx power control through an 85dB VGA. RFT3100 operating modes are controlled by the MSM5105 and include selective power-down, gain control, and punctured CDMA transmission(gated Tx power), for optimal power savings and talk-time improvement.
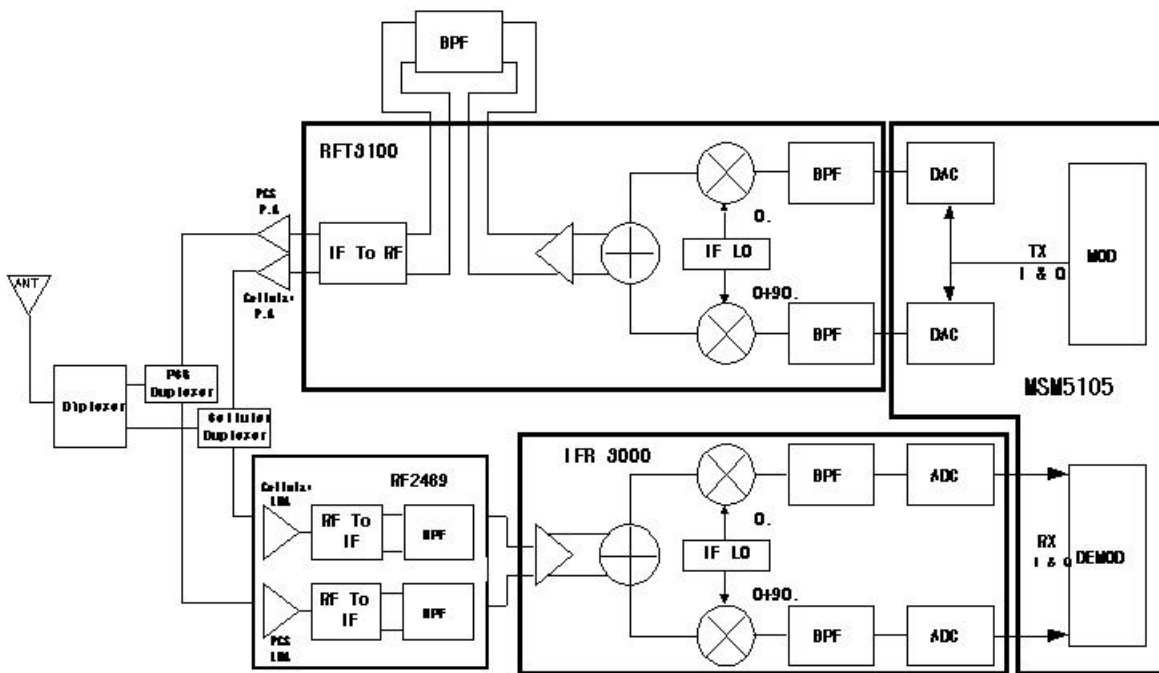
Figure 3-4. RFT 3100 and IFR3000 Funtional Block Diagram