3. Technical Description

3.1 Receiver

Refer Figure 3-1

3.1.1 Front End Filters and RF Amplifier

The receiver input signal from the antenna passes through the antenna filter comprising L10, L11, L12 and associated tuning capacitors. With the mobile in receive mode, diodes D3, D4 and D5 in the antenna switch are reverse biased allowing the receiver input signal to be coupled through to the front end with minimal loss. The overall insertion loss of the antenna filter and switch is approximately 0.8dB. Front end selectivity is provided by varactor tuned bandpass filters at the input and output of the RF amplifier.

Front end tuning voltages are derived from the alignment data stored in the radio. The DSP processes this data to optimise front end tuning relative to the programmed channel frequencies which may be changed at any time without re-aligning the radio.

To achieve the required varactor tuning range an arrangement of positive and negative bias power supplies is used to provide a total bias across the varactors of up to 14.0VDC. A fixed 2.5V positive bias derived from the 5.0V supply and voltage divider R425/426 is applied to the cathodes of the varactor diodes. The negative bias supply originates at the DSP/FPGA as a composite digital tuning signal (FE TUNE) containing the data for the four front end tuning values TUNE 1 to 4 for the particular channel frequency selected. The level is dependent on channel frequency and tuning and varies between +0.1 and +3.0V. This signal then passes through buffer U901A and level translator Q900 to Q903 where it is converted to a high level (-0.5 to -11.5V) negative equivalent of the original signal. The -12.0V rail of the level translator is generated by U300B/C with D304 to D306 providing the required voltage multiplier effect. The high level negative signal is then split into the four individual front end negative DC values under software control by multiplexer U902 and associated storage capacitors C904 to C907 before being applied to the anodes of the front end tuning varactors.

The RF amplifier stage comprises a low noise transistor amplifier (Q400) which is compensated to maintain good linearity across the required frequency bands and temperature range. This provides excellent intermodulation and blocking performance across the full operating range. The gain of this stage is typically 17dB for both UHF and VHF versions.

3.1.2 First Mixer and IF Section

The output of the last front end bandpass filter is coupled into single balanced mixer T400/D413 which converts the RF signal to an IF frequency of 45MHz. The local oscillator injection level is typically +8dBm at T400 pin 1 with low side injection used for UHF and high side for VHF.

Following the mixer is IF amplifier Q401 which provides approximately 15dB of gain and in association with its output circuitry presents the required load conditions to the 4 pole 45MHz crystal filter Z401/402.

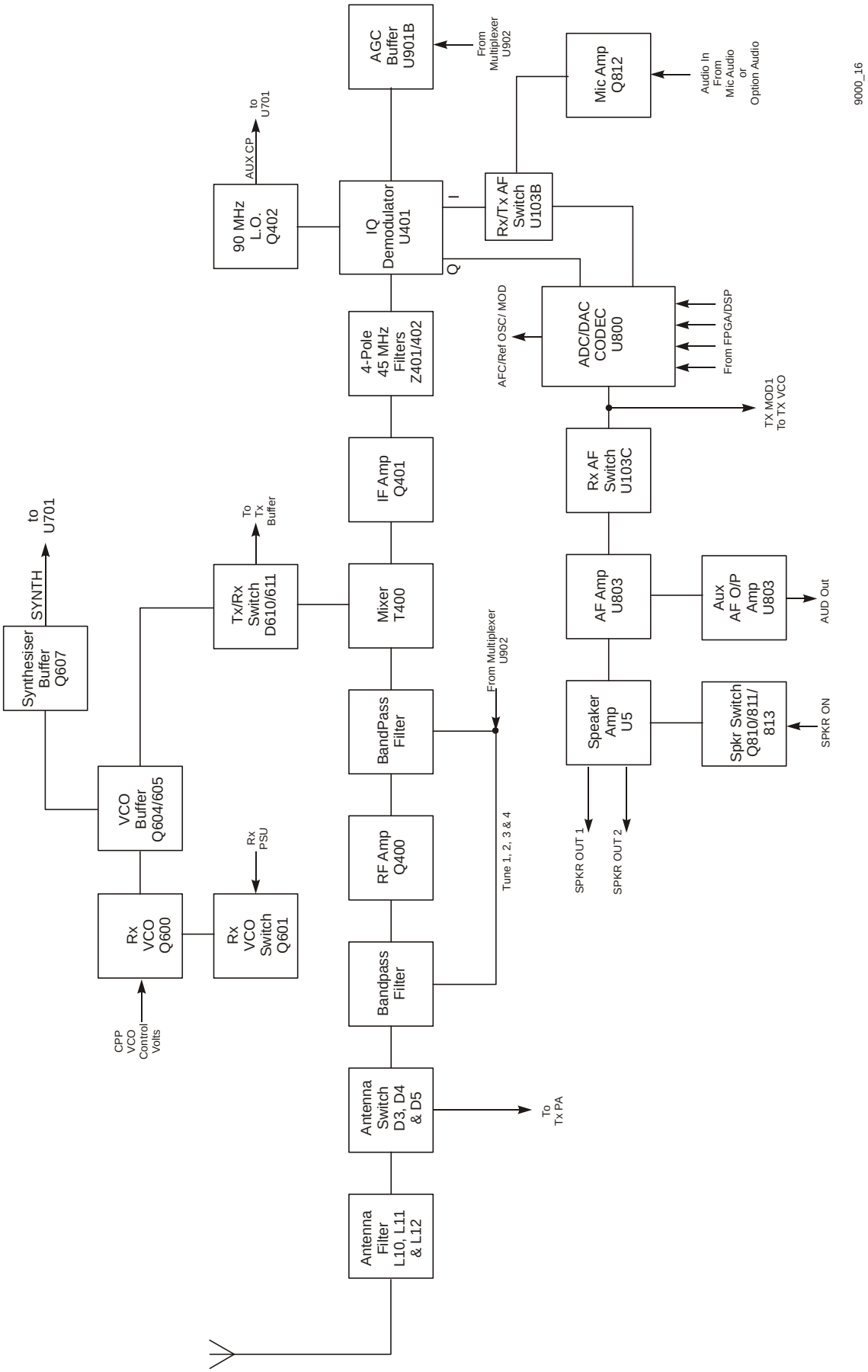

Figure 3-1 VHF/UHF Receiver Block Diagram

3.1.3 Quadrature Demodulator

Additional IF gain of approximately 30dB occurs at U401 which is a dedicated IF AGC amplifier/Quadrature Demodulator configured for single ended input and output operation. The AGC voltage for U401 is derived from the RSSI function of the DSP via AUX CTL and multiplexer U902. The onset of AGC operation occurs when RF input signal levels at the antenna exceed -90dBm.

Conversion of the 45MHz IF signal to I and Q baseband signals is carried out by the demodulator section of U401. The 90MHz local oscillator signal is generated by VCO Q402 which is phase locked by the auxiliary PLL output of U701 via feedback signal AUX LO2.

3.1.4 Receiver Audio Processing

All receiver audio processing and filtering functions are performed by the CODEC U800 under the control of the DSP. The receiver I and Q analog baseband signals are converted to digital signals by the CODEC ADC before being applied to a series of digital filters which provide the final stage of adjacent channel filtering, high pass and low pass filtering and mute noise processing for narrow and wideband operation. The processed signals are then converted to analog audio signals by the CODEC DAC and are applied to conventional audio amplifiers U803A/B and the speaker amplifier U5.

There are two speaker options available. A half bridged configuration using a speaker across balanced output SPKR OUT1 and 2 which provides an audio output level of up to 4 watts into 4 ohms. The other option is a full bridge configuration using a high power speaker across SPKR OUT1 and 2 and providing an audio output level of up to 10 watts into 8 ohms. The carrier and signalling mute functions are performed by Q810/811/813 under DSP control with additional receiver muting to U803B being applied by U103C when the mobile is in transmit mode. De-emphasis to the audio PA U5 is performed by R43 and capacitors C42 to C58. Flat audio is provided to S1-6 via amplifier U803A.

3.2 Transmitter

Refer Figure 3-2.

3.2.1 Drivers and PA Stages

The RF output level from the VCO buffer Q604 is typically +5dBm (UHF) and +8dBm (VHF). TX buffer Q606 increases this level by approximately 3dB (UHF) and 11dB (VHF) and also provides additional VCO isolation. The following section of the TX buffer Q612 is controlled by the transmitter power control loop and Q609. Q609 is normally saturated in transmit mode so there is no minimum gain control applied to this stage. The gain of Q612 is typically 10dB (UHF) and 15dB (VHF) but the output level is reduced by input and output resistive attenuators to limit the PA driver input level to typically +20dBm. The gain of PA driver Q12 is controlled by the power control loop to ensure that transmitter output power remains within defined limits. The PA driver output level is typically +25dBm. PA module U2 utilises three stages (UHF) and two stages (VHF) to achieve the required final RF output power level of +44dBm (25 watts). Power output settings are derived from alignment data stored in flash memory during the initial factory alignment. The DSP processes this data to optimise the power output level relative to the programmed channel frequencies which may be changed at any time without retuning the radio.
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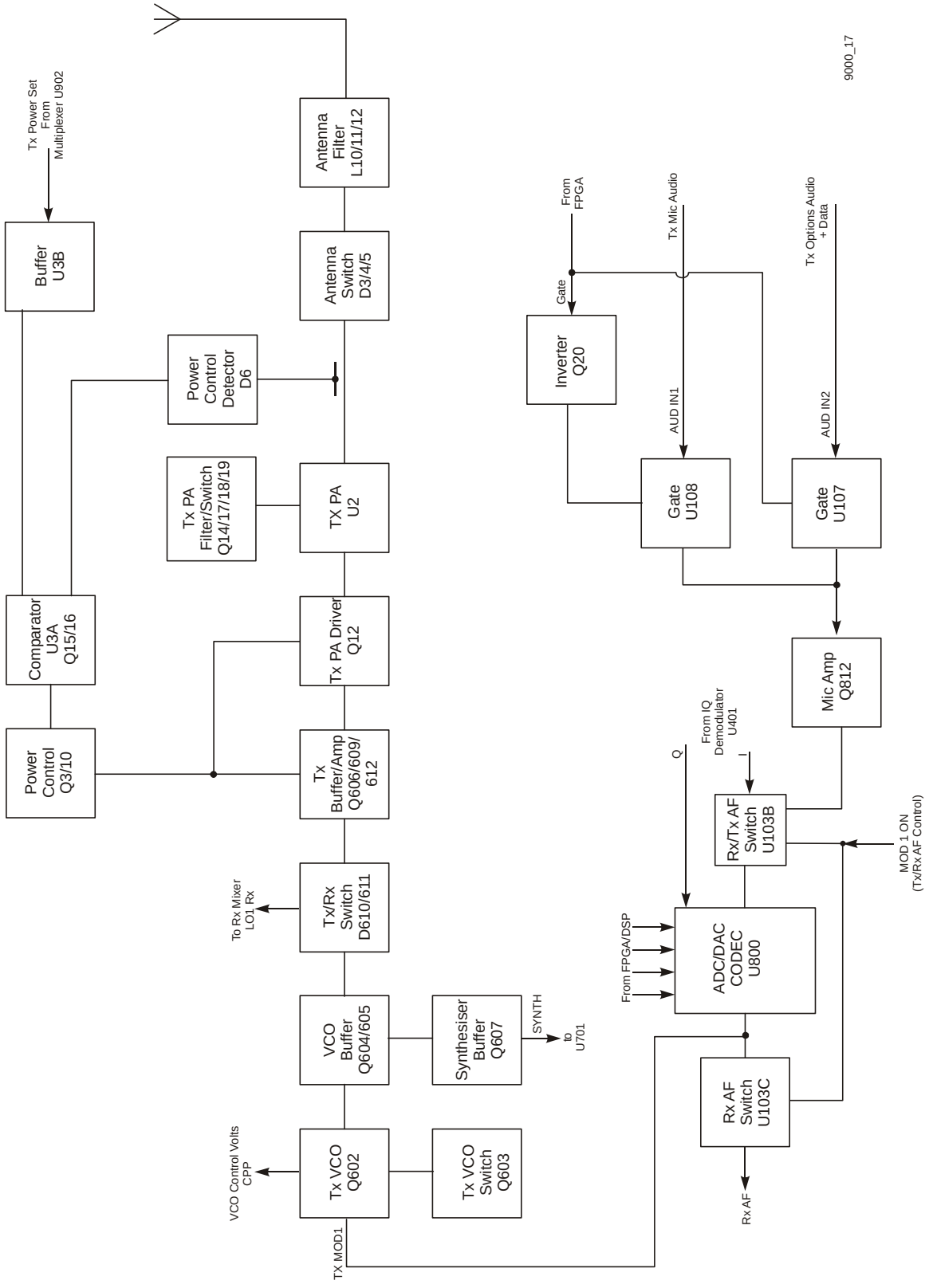

Figure 3-2 VHF/UHF Transmitter Block Diagram

An active filter comprising Q14, 17,18 and 19 provides isolation to minimise power supply noise at the PA. This is achieved by maintaining a voltage differential of approximately 1V across Q14 and indirectly filtering its gate voltage. Q14 is switched on only during transmit via R523 to minimise receiver power requirements.

3.2.2 Power Control

Output power is stabilised by a power control feedback loop. L1, R54, a printed circuit transmission line, D6 and associated components comprise the power detector with Q3/10, U3 and associated components providing the power setting and control sections. Forward and reverse power is sampled by the power detector and applied as a DC voltage to the inverting input of comparator U3A. The TX PWR SET voltage which is a DC voltage proportional to the programmed TX power setting is applied to the non-inverting input of the comparator. PA module output level changes due to supply voltage, load or temperature variations are detected and applied to the comparator which proportionally adjusts the PA driver (Q12) supply, and therefore the PA drive level, via Q10/Q3. High temperature protection is provided by thermistor R452 which progressively reduces the power level if the PA module temperature becomes excessive. Q15 and Q16 provide for dual power control time constants necessary for good power ramp and decay characteristics.

3.2.3 Antenna Changeover and Harmonic Filter

The antenna changeover circuit consisting of pin diodes D3/D4/D5 is switched by Q4/Q8/Q11 and associated circuitry allowing the transmitter output to be coupled to the antenna while providing isolation for the receiver input. With the transmitter switched on, the diodes are forward biased allowing power to be coupled through to the antenna and isolating the receiver by grounding its input at C28. The short circuit at the receiver input is transformed to an effective open circuit at D3 by L13, which minimises transmitter loading. With the transmitter switched off the diodes are reverse biased allowing the receiver input signal to reach the receiver front end with minimal loading and loss.

The harmonic rejection low pass filter comprises L10/11/12 and associated capacitors.

3.2.4 Transmitter Audio Processing

Microphone audio input signals of 40mV RMS with a source impedance of 470 ohms are provided at the microphone input (AUD IN1) by an external microphone unit comprising an electret microphone insert and a preamplifier with a gain of 18dB. U108 is a control gate for the microphone audio signals.

AUD IN2 is the external audio options and data input which is controlled by gate U107. Inverter Q20 ensures that the data or audio options signals are muted when the mic. audio gate is active. The AUD IN2 input level and source impedance is the same as the microphone input.

Q812 is a unity gain amplifier which provides buffering of the audio and data signals. U103B provides CODEC input switching which selects either the receiver I signal or transmitter audio/data signals depending on the TX/RX mode. All pre-emphasis, filtering, compression and limiting processes for narrow and wideband operation are carried out in the CODEC (U800) under the control of the DSP. The processed transmitter audio/data from the CODEC output at VOUTL is applied to the VCO as a modulation signal with a level of approximately 200mV P/P.

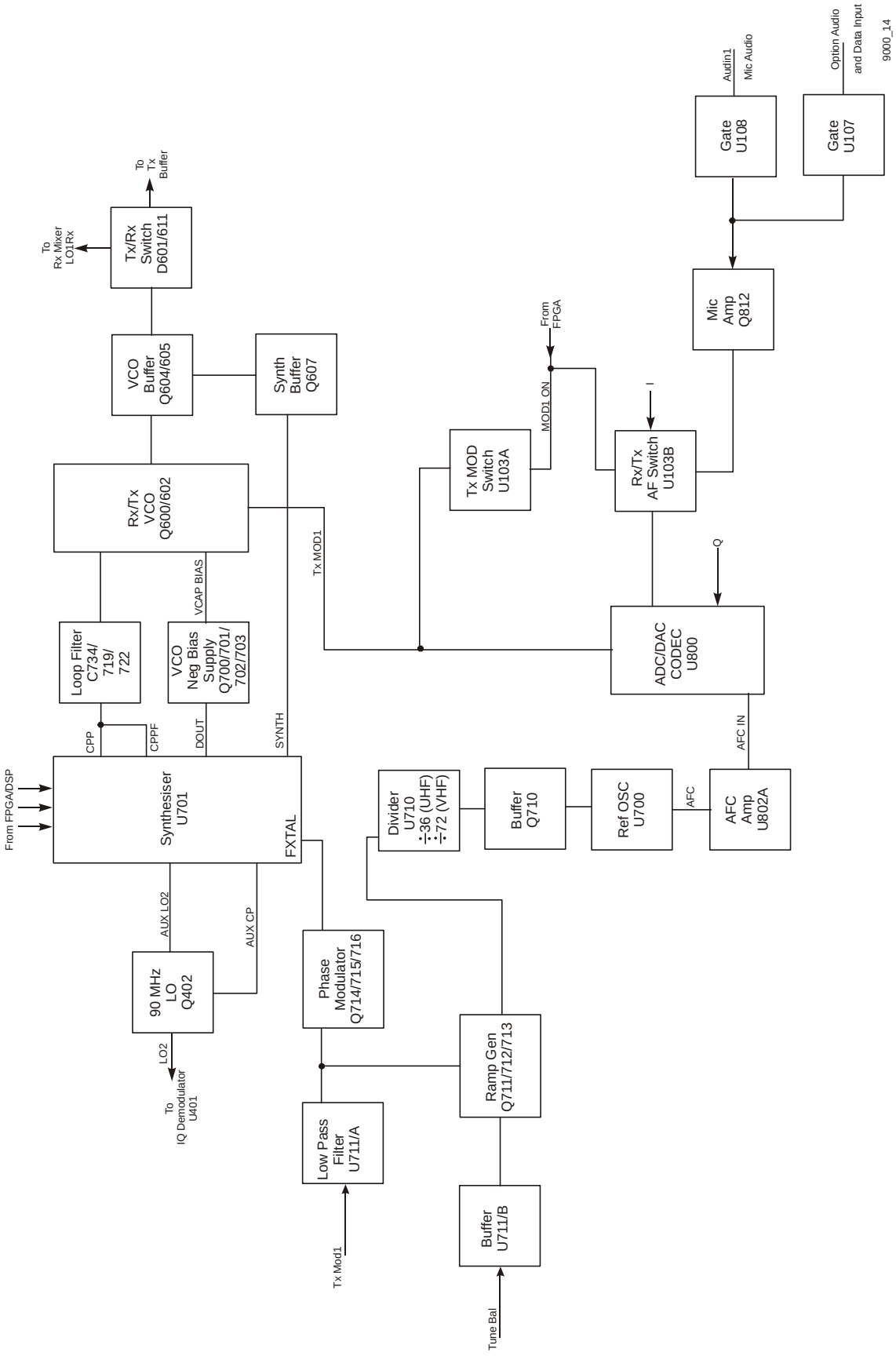

Figure 3-3 VHF/UHF Synthesiser, Block Diagram

3.3 Frequency Synthesiser

3.3.1 General

Refer Figure 3-3

The SRM9000 frequency synthesiser consists of individual transmitter and receiver (local oscillator) voltage controlled oscillators, loop filter, varactor negative bias generator, reference oscillator and an integrated, dual phase locked loop device U701.

3.3.2 PLL

The PLL device contains two prescalers, programmable dividers and phase comparators to provide a main and auxiliary PLL. The main PLL of U701 controls the frequency of the TX/RX VCOs via Control Voltage outputs at pins 2 and 3 and VCO Feedback to pin 6. The auxiliary PLL is used to control the receiver 90MHz second local oscillator via the Control Voltage output at pin 17 and VCO Feedback to pin 15. The PLL operation involves the division of the 14.4MHz reference oscillator frequency by divider U710 and the internal divider of U701 down to a lower frequency which corresponds to a sub-multiple of the radio channel spacing ie. 6.25kHz for 12.5/25kHz channel spacing or 5kHz for 20kHz channel spacing. The VCO frequency is sampled and divided down to the same frequency after which it is phase compared to the reference. Any error produces an offset to the Control Voltage output which is used to correct the VCO frequency. A valid lock detect output is derived from pin 20 and is sampled by the FPGA during transmit. If an unlocked signal is detected the radio will switch back to receive mode.

3.3.3 VCO

The transmitter and receiver VCOs use low noise JFET transistors (Q600 RX, Q602 TX) and inductors L602 (RX), L608 (TX) to generate the signals for the required band coverage. Electronic tuning is provided by varactor diodes D600 to D608 with their control voltages derived from the Loop Filter, PLL and Negative Bias Generator.

VCO selection and timing is controlled by the DSP via the RX and TX power supplies and applied through switches Q601 (RX) and Q603 (TX). VCO buffer Q604/605 isolates the VCO from load variations and active power supply filter Q615 minimises supply related noise. A PLL feedback signal is sampled from the VCO buffer output via buffer Q607.

3.3.4 Negative Bias Generator and Loop Filter

A positive and negative varactor bias supply similar to the front-end varactor arrangement has been used to achieve the required broadband tuning range of the VCOs. PLL device U701 is programmed to deliver a fixed nominal +2.5V output from phase detector/charge pump CPPF or CPP (selection depends on radio setup) regardless of the channel frequency selected. This voltage is filtered to remove synthesiser noise and reference products by loop filter C719/722/734 and R721/724/734. The resulting low noise voltage is applied to the cathode side of the VCO varactor tuning diodes as a positive bias voltage. The negative bias supply originates as a positive DC voltage (0.1V to 3.0V) at the DAC output of U701 (DOUT) with a level relative to the programmed state of the radio (eg. channel frequency, TX/RX state). The voltage is converted to a high level negative supply by VCO Varicap Negative Supply Q700 to Q703. The -17V rail of this supply is generated by U300B/C with D304 to D307 providing the voltage multiplying effect needed to achieve -17V. The output of the negative supply is applied directly to the VCO varactor anodes as the negative tuning voltage VCAP BIAS.

3.3.5 Phase Modulator

The modulation path for audio, data and higher frequency CTCSS signals is via D609 and its associated components in the TX VCO. The reference input to the PLL (FXTAL) provides the low frequency modulation path in conjunction with phase modulator Q714 to Q716. U711A is a low pass filter which provides 6dB per octave attenuation to frequencies above approximately 180Hz. Modulation balance adjustment is carried out using a CODEC generated 100Hz square wave applied to TX MOD1. A DAC output from the Alignment Tool is applied to buffer U711B and ramp generator Q711 to Q713 via the TUNE BAL line to adjust the low frequency modulation level.

3.3.6 Reference Oscillator

TCXO U700 determines the overall frequency stability and frequency setting of the radio. The frequency setting is achieved by adjusting its ADJ voltage with the Alignment Tool. In addition, the ADJ input is used in a frequency control loop with the receiver I and Q signals to provide receiver AFC. U700 operates at 14.4MHz and is specified at ±2.5ppm frequency stability over the temperature range -25° to +75°C.

3.4 Control

Refer Figure 3-4

3.4.1 DSP and FPGA

The SRM9000 transceiver operates under the control of a DSP (U102) and FPGA (U106) combination which together with a number of other dedicated devices perform all the operational and processing functions required by the radio. The FPGA is configured by the DSP under software control to provide the following functions:

- Channel set-up of all operating frequencies
- Modulation processing and filtering
- De-modulation processing and filtering
- TX power output reference
- Receiver front end tuning
- Serial communications with alignment tool, microphone and control head
- Modem functionality for data modulation
- All signalling / CTCSS generation and decoding
- CO control
- Receiver muting control
- TX / RX switching
- PLL detect

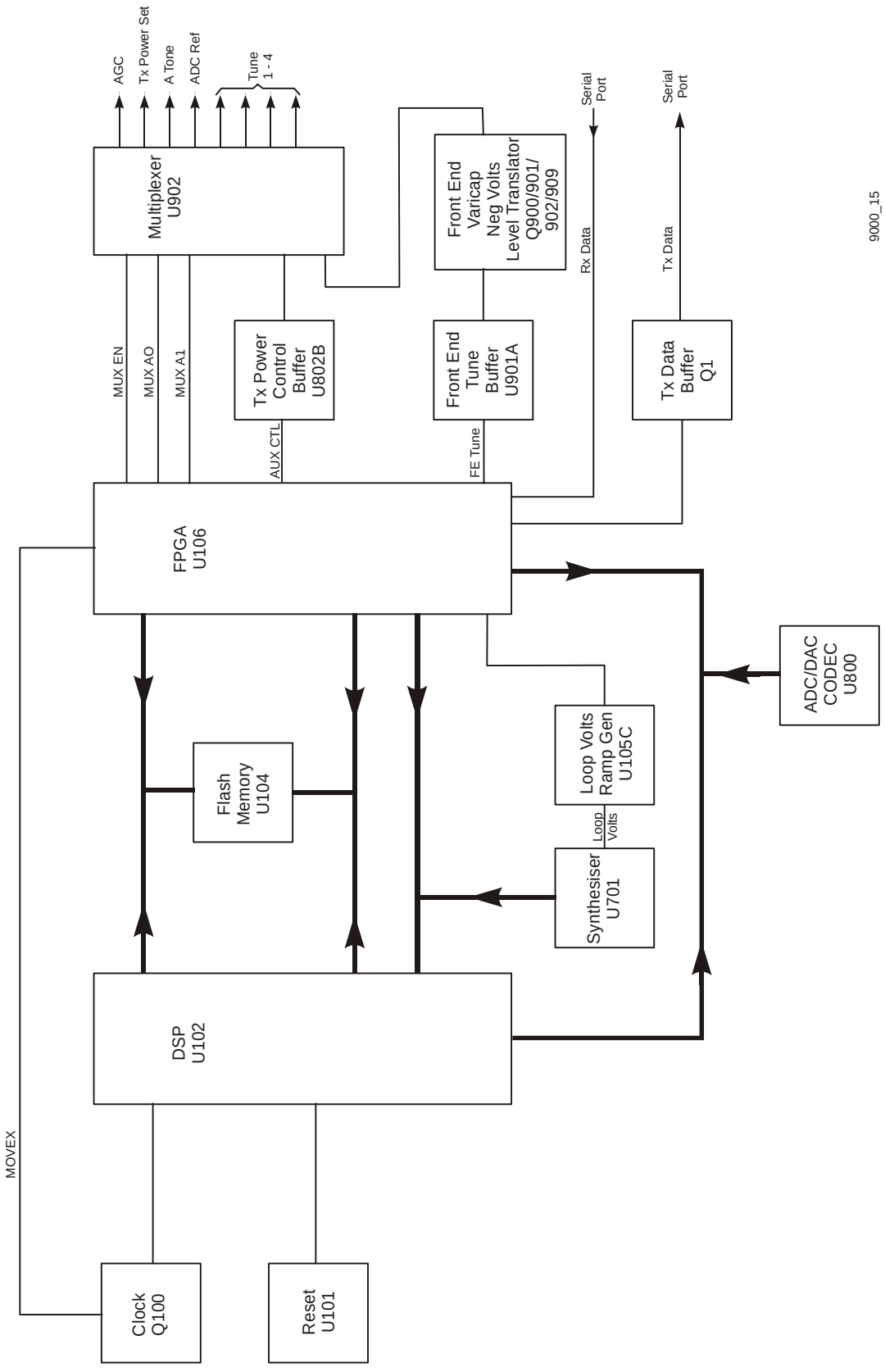

Figure 3-4 VHF/UHF Control Block Diagram

3.4.2 DSP Clock Oscillator

The DSP is clocked by a 15.360MHz oscillator which consists of crystal X100 and an internal DSP oscillator. Q100 forms a crystal switching circuit with C117 which when activated by a command from the FPGA steers the oscillator away from potential interfering frequencies.

3.5 Memory

Memory consists of the internal DSP memory and an external 4MB non-volatile Flash Memory U104. When power is off, program and data is retained in Flash Memory. At power-on, a boot program downloads the DSP's program from Flash Memory to its internal RAM for faster program execution and access to data.

3.5.1 Multiplexer

U902 contains 2 separate 4-channel multiplexers providing a total of 8 independently controlled analog switches. Under software control, the multiplexers produce tuning voltages from supplied data for the receiver front end (TUNE 1 to 4), TX power setting (TX PWR SET), receiver AGC (AGC-1), alert tone (A TONE) and FPGA ramp generator (ADC REF).

Buffer U802B is fed with a composite digital tuning signal (AUX CTL) from the DSP/FPGA containing the data for AGC, A TONE, ADC REF and TX PWR SET settings. The level is dependent on channel frequency and tuning and varies between 0.1 to 3.0V. This signal is applied to one group of 4 analog switches in U902 via a common input connected to pin 13. The second group of 4 switches is fed with the receiver front end tuning signal FE TUNE (to provide outputs for TUNE 1 to 4) via the second common input at pin 3 as described in the receiver front end section.

The 2 groups of analog switches are independently controlled by FPGA binary signals MUX A0 and A1 and enable line MUXEN to output the required tuning voltages as a series of pulses. These pulses are converted to steady state voltages by integration capacitors C904 to 911 and C921 to 925.

3.6 Power Supplies

3.6.1 Power On Function

The unregulated 13.8V DC input is routed directly to high current devices and is also switched via FET Q350. The output from Q350 feeds three, low drop out series regulators and associated switched and auxiliary supplies which along with a negative voltage generator provide all the switched power requirements of the transceiver.

Q315/316/317 and U313 form a power on/off latch circuit which is activated by a pulse from the control unit or microphone/handset via PWR ON or PWR OFF and controls the FET power switch Q350. A PWR OFF operation requires the button to be held down for more than 2 seconds. This is then sensed by the FPGA via the PWR SENSE line which turns the radio off by placing a positive pulse on the PWR OFF line thereby resetting U313B.

3.6.2 Power Supplies

The following is a list of the SRM9000 power supplies and some of the devices and circuits they supply.

3.6.2.1 +8V Regulator U310

Regulated +8.0V supply (8V0 and +8V)

- TX buffer Q612
- VCOs and VCO buffers via active filter Q615
- RX second local oscillator via Q403

Regulated +8.0V switched supply (RX PSU)

- RX front end
- IF Amplifier
- Various switching functions

3.6.2.2 +5V Regulator U311

Regulated +5.0V supply (5V0 and +5V)

- RX front end varactor positive bias
- Synth. buffer Q607
- VCO varactor negative supply Q700 to Q703
- TCXO U700
- RX audio amplifiers U803A/B
- RX mute switch Q810/813
- Multiplexer U902
- FE TUNE level translator and buffer U901A, Q900/901

Regulated +5.0V switched supply (TX PSU and TX PSU+)

- TX power control U3
- TX buffer Q606
- Microphone amplifier Q812
- Various switching functions

3.6.2.3 +3.3V Regulator U312

Regulated +3.3V supply (3N3)

- Digital supply for CODEC U800
- DSP U102
- FPGA U106

Regulated +3.3V supply (3Q3)

- I Q demodulator U401

Regulated +3.3V supply (3C3)

- Analog supply for CODEC U800

Regulated +3.3V supply (3P3)

- PLL U701
- TCXO divider U702

Unregulated 13.8V (13V8 UNSW)

- TX PA module U2
- TX PA power control circuit Q3
- Active filter Q14/17/18/19
- Antenna changeover switch Q4/8/11
- RX mute switch Q811
- RX speaker amplifier U5

3.6.2.4 Negative Power Supply U300B/C

Provides -17.0V output (-17V0)

- Negative rail for VCO Varicap Negative Supply Q700, 701, 702 and Q703

-12.0V Output (-12V0)

- Negative rail for FE TUNE level translator Q900, 901, 902, 903 and multiplexer U902