OPERATIONAL DESCRIPTION OF Philips 868

The equipment under test (EUT) is the transmitter of Philips 868, a tri-band (900/1800/1900) GSM/GPRS mobile phone. The transmitter operates in a half-duplex system according to the GSM standards.

The majority of the phone circuitry consists of a four device chipset; the SI4206 Transceiver IC, the SKY77328 HBT IC Power Amplifier, the AD6537 Mixed Signal Device (A/D,D/A IC) and the AD6525 Baseband Processor. The remainder of the major radio components are the receiver SAW filters and transmit/receive switch. There is also a combination Flash Memory/SRAM IC. The system is powered by a rechargeable lithium-ion battery with a nominal voltage of 3.7 volts.

The transmitter oscillators which comprise the translational loop architecture are internal to the transceiver IC and are phase locked to a 13 MHz reference signal derived from the 13 MHz crystal oscillator. The SI4206 has an offset phase-locked loop (OPLL) used for local oscillator control in both receive and transmit mode. The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO. For receive mode, the LO frequency is between 1737.8 and 1989.9 MHz, and is divided by two for EGSM 900 modes. For transmit mode, the LO frequency is between 1272 and 1483 MHz, and is divided by two for EGSM 900 modes.

The main oscillator signals are amplified by the power amplifier, routed to transmit/receive (T/R) switch then delivered to the antenna. The detected signal is used in the integrating power control loop which resides internal to the transceiver IC for setting and controlling the output power. The power settings are calibrated at the factory and stored in the flash memory IC. These settings are used as the reference level for the power control loop. Power ramping functions are also controlled by the mixed signal device.

The GMSK modulation is provided in-loop by quadrature I/Q signals which are sent to the transceiver IC from the mixed-signal device which converted the digital stream from the baseband processor into an analog signal used by the modulator. The mixed signal device is controlled by the baseband processor. The RF performance conforms to the ETSI specifications for spectrum due to modulation, transient switching modulation spectrum, power ramp, and power output, as well as all the other ETSI requirements.

The receiver is a low-IF receiver architecture that allows for on-chip integration of the channel selection filters, eliminating the external RF image reject filters and the IF SAW filter required in conventional superheterodyne architectures. The RF preamplifiers are internal to the transceiver and provide the signal to two down converting mixers, one for the low bands (900 MHz) and one for the high bands (1800 and 1900 MHz). The output is down converted to baseband with a digital 100 kHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interference signals. The received signals now at baseband frequencies are routed from the transceiver to the mixed-signal device for further processing and ultimately to the baseband processor.

The mixed signal device digitizes the baseband I/Q signals using Sigma-Delta DACs and sends them to the baseband processor through a serial digital interface. This IC also has analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to directly interface to the handset speaker and microphone. The voiceband Codec section provides a 32 ohm interface to the speaker and microphone and also provides Line In/Out signals for the headset. Additional the mixed signal device contains some of required system power supply regulators.

The baseband processor handles all physical layer radio control signals and network interfaces. The 32.768 KHz clock oscillator operates the baseband IC from a backup battery when the main battery is removed. The baseband processor is a dual-core device that splits the processing between a DSP core and an ARM-7 THUMB ™ processor. The DSP handles the physical and layer 1 processing, while the ARM7 executes the layer 2 and layer 3 protocol and the man-machine interface (MMI). The dual cores communicate through a dedicated block of dual port memory. It also communicates with the Subscriber Identity Module (SIM) through an interface to the mixed signal device. The baseband processor also communicates to the calibration system or external devices through a digital serial link that is available on the system connector. The other main signals on the system connector include the digital audio interface (DAI) and allows for an external battery charging voltage.

The MMI completes the phone design and includes the displays, touch panel, keypads, vibration motor, LEDs, speaker/receiver, microphone, headset, and 2.0M CMOS camera