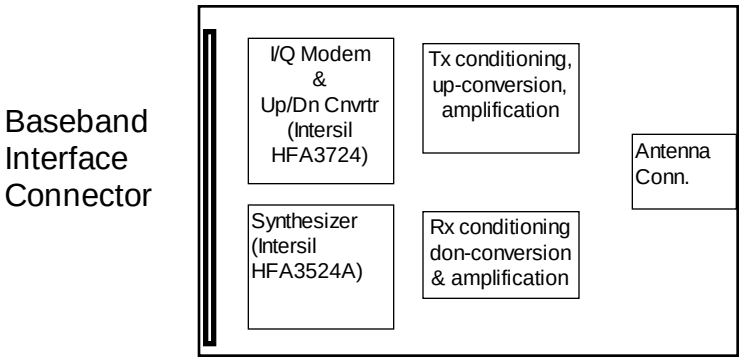
Description of Radio function used in MF24 Products (2.4 GHz)

The radio function for all MF24 products in the MultiSite series combines on-board baseband processing and networking functions with an RF/IF daughter-card (mXII24). This radio function provides a wireless DSSS networking interface that can operate at 384 or 192 kbps. The operation is proprietary but similar to IEEE 802.11 as it uses certain Intersil PRISM IEEE 802.11 chipset components.

The mXII24 daughter-card contains the following blocks:

- Baseband interface
- IF Modem, that takes care of quadrature up/down conversion
- Synthesizer, that generates the RF and IF local oscillators
- Tx Chain, that conditions, up-converts and amplifies the transmit signal
- Rx Chain, that amplifies, down-converts and conditions the receive signal
- Antenna connector, that provides a connection to external antenna

mXII24 Daughter-card Overview



Baseband Processing and control functions are located on the host MF24 main board. The Baseband Processor is the Intersil HFA3824A and the radio controller is a Motorola 68HC908GP32 Microcontroller. See detailed block-diagram of Figure 1 for more detail. The main processor on the MF24 transfers digital serial data to and from the radio (i.e. the wireless network) via an HDLC serial communications controller.

The technical specification for the radio function is outlined on the next page.

TECHNICAL SPECIFICATION
MultiSite MF24 Radio Products (2.4 GHz)

Data Signalling Rate:	192 and 384 kbit/s
Media Access Protocol:	Proprietary TDMA
Bit Error Rate:	Better than 10^{-5} (10^{-3} FER, 100 bit packets)
Baseband Modulation: (before spreading)	384 kbps: Differential Quadrature Phase Shift Keying (DQPSK) 2 bits/symbol 192 kbps: Differential Binary Phase Shift Keying (DBPSK) 1 bit/symbol
Spread Spectrum:	Direct Sequence with 16 chips/symbol interval. Pseudo random extended 16-bit Barker code sequence
Chipping Rate:	3.072 Mchips/s
Carrier Frequency:	Selectable from factory pre-programmed set: 2405, 2412, 2419, 2426, 2433, 2440, 2447, 2454, 2461, 2468 and 2475MHz
Peak Output Power:	< 25 dBm

MultiSite MF24 Block-Diagram

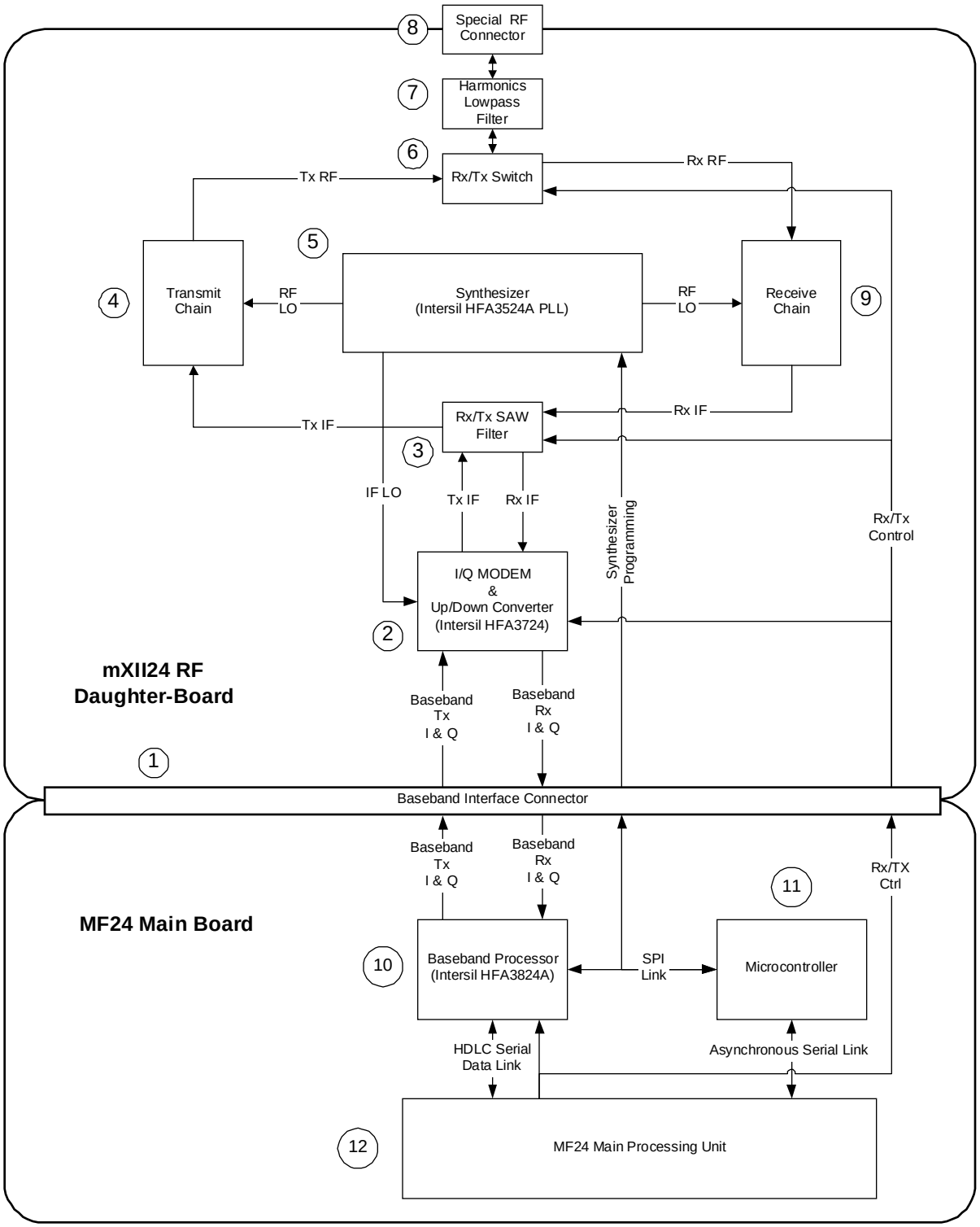


Figure 1: MultiSite MF24 Block-Diagram

DESCRIPTION OF THE MF24 2.4 GHz BLOCK DIAGRAM

The various parts of the Block diagram (Figure 1) are numbered and an explanation of these blocks and radio operation is given below. First, transmitter operation will be described followed by receiver operation.

Transmitter operation:

A) The Baseband Processor (10) chip accepts the digital data from MF24 Main Processing Unit (12) from which it generates spreaded quadrature signals with an extended Barker sequence of 16. The original raw data rate of 192 or 384 kbps is differentially encoded (DQPSK or DBPSK), producing a symbol rate of 192 kBAUD. The resulting data stream is then multiplied by the 16 chip spreading code to produce a chipping rate of 3.072 Mcps. The unfiltered data comes out as Tx I and Q signals and goes to the Baseband Interface Connector (1) where it will be picked off by the I/Q MODEM (2).

B) The I/Q MODEM (2) chip combines a lowpass filter and a quadrature up-converter in its transmit path. It accepts a 570MHz IF Local Oscillator (IF LO) from the Synthesizer (5) which is divided by 2 to 285MHz. The above Tx I&Q signals are taken from the Baseband Interface Connector (1), shaped (filtered) and up-converted (in 2) using the quadrature up-converter to an Intermediate Frequency (IF) of 285 MHz. The up-converted signal comes out as Tx IF and goes to the Rx/Tx SAW Filter (3).

The Rx/Tx SAW (3) filters all unwanted mixing products, such that only the 285 MHz band remains before the signal is fed to the Transmit Chain (4). This filter is shared by both the Tx and Rx paths. The Rx/Tx control signal sets the RF switches in (3) to insert the SAW filter in the proper path.

The filtered Tx IF signal goes into the Transmit chain (4) where it is up-converted to the selected RF channel, amplified and filtered. The Transmit Chain accepts an RF LO from the Synthesizer (5) in the range of 2115 to 2190 MHz. The up-converted RF signal is amplified in (4) to an output level of about 24 dBm. A variable attenuator in the transmit path allows the maximum power output level to be adjusted at production tuning. The signal comes out as Tx RF and goes to the Rx/Tx Switch (6).

The Rx/Tx switch (6) brings the signal to the Harmonics Lowpass filter (7) which removes all unwanted harmonics before feeding the RF signal to the Antenna Connector (8).

Receiver operation:

The receive signal enters the antenna, passes Harmonics Lowpass filter (7) and the RX/TX switch (6) which is now set to RX mode. The received signal comes out as Rx RF and goes to the Receive Chain (9).

The signal goes through the Receive Chain (9) where it is filtered, amplified and down-converted to the 285 MHz IF frequency. A Low Noise Amplifiers (LNA) (in 9) is

used to amplify the weak signal to a level fit for down-conversion. The Receive Chain accepts an RF LO from the Synthesizer (5) in the range range of 2115 to 2190 MHz. The down-converted signal comes out as Rx IF and goes to the Rx/Tx SAW Filter (3).

The Rx/Tx SAW (3) filters all unwanted mixing products, such that only the 285 MHz band remains for the I/Q MODEM (2). This filter is shared by both the Tx and Rx paths. The Rx/Tx control signal sets the RF switches in (3) to insert the SAW filter in the proper path.

The I/Q MODEM (2) combines a limiting amplifier, a quadrature down-converter and a lowpass filter in its receive path. It accepts a 570MHz IF Local Oscillator (IF LO) from the Synthesizer (5) which is divided by 2 to 285MHz. The above Rx IF signal is amplified by the limiting amplifier before being down-converted in the quadrature down-converter to an Intermediate Frequency (IF) of 285 MHz. The down-converted signal is then lowpass filtered, then comes out as Rx I&Q and goes to the Baseband Interface Connector (1) where it will be picked off by the Baseband Processor (10).

The Rx I&Q signals are digitised, de-spread and de-modulated by the Baseband Processor (10) which automatically detects DBPSK or DQPSK modulation. The resulting output of the processor is a received data rate of 192 or 384 kbps, depending on the received signal modulation.

Synthesizer Block (5):

The Synthesizer (5) combines a dual PLL, a 10 MHz VCXO reference oscillator, an IF VCO and an RF VCO to generate 2 single tone signals (local oscillators) for up/down conversion. The IF LO is fixed at 570 MHz. The RF LO can be programmed by the Microcontroller (11) in the range of 2115 to 2190 MHz.

Microcontroller (11):

The Microcontroller contains all radio operating parameters, limits and failsafes. At power-up, it programs the Baseband Processor (10) and Synthesizer (5) for proper operation. In the event of any failure that may cause un-intended RF transmission, the Microcontroller locks out the MF24 Main Processing Unit (12) from activating the Tx mode.

MF24 Main Processing Unit (12):

The MF24 Main Processing Unit (12) is the radio’s host. It transmits and receives digital data to and from the radio (i.e. the wireless network) using an HDLC serial communications controller. The MF24 Processing Unit communicates with the Microcontroller (11) via an asynchronous link to select one of the preset radio channels and the operating data rate. It can also read registers on the Microcontroller to determine parameters such as signal strength and radio status.