# Introduction

Clarity 2 is a "one chip" digital camera solution for many imaging applications. It consists of both a custom ASIC which is based upon the popular ARM 7, 32 bit RISC processor, and a complete software ensemble for rapid OEM development.

Market applications include:

- Digital Still Cameras
- Dual Mode Cameras (Still and PC)
- "Smart" Security Cameras
- Toys
- Television Set-Top-Box Image Viewers
- Remote and Wireless Imaging

## Rapid Development Kits

Clarity 2.0 offers the most advanced feature set available at the highest level of integration for the development of a digital camera or imaging system. Thus, Clarity 2 based designs can achieve minimum cost and complexity. Several Rapid Development Kits and Engineering Evaluation Kits are offered so as to make initial product development rapid and simple. The Engineering Evaluation Kit is designed to provide an engineer with a development environment for testing design changes, sensor performance and software modifications.

The Rapid Development Kits are designed to enable OEM customers to rapidly deploy a Clarity 2 based product. They include:

- Complete schematics in both PDF and DSN format.
- Gerber files for sample circuit boards
- Bill of materials
- Working prototypes
- Firmware and Host Software

We currently have several RDK models including:

- SV1301 RDK – Low Cost CMOS VGA Digital Still Camera
- SV1300 RDK – Low Cost 1.3M Pixel Digital Still Camera
- SV1500 RDK – Low Cost 1.45M Pixel Digital Still Camera
- SV1307 RDK – Low Cost Toy Dual Mode Camera
- SV1308 RDK – Low Cost "Smart" Security Camera
- SV1309 RDK – Docking Station and Set-Top-Box
- SV1303 RDK – MP-3 Player and Digital Camera
- SV1306 RDK – BlueTooth Digital Camera

Additional detailed information on Clarity 2 and the available Rapid Development Kits and Engineering Evaluation Kits can be found on our web site:

http://www.soundvisioninc.com - Home page

https://www.ultranet.com/soundvisioninc/Clarity2/Clarity_2_ASIC_Specification.PDF is a link to a complete PDF document that can be downloaded from our web site.

# Specifications

**ARM720 RISC Processor**
- 8K bytes Cache
- Interrupt Controller
- MMU
- Timer
- 5 DMA Controllers with FIFOs

**Several I/O Alternatives**
- USB
- RS-232

**Several Display Alternatives**
- NTSC/PAL Composite Video
- Digital LCD Panel
- Kopin Cyberdisplay

**Several Sensor Alternatives**
- CCD
- CMOS

**12 Bit A/D Input**

**$I^2C$ Bus**

**Several Removable Storage Alternatives**
- Compact Flash
- SSFDC (Smart Media)

**Synchronous DRAM Support for up to 64 Mbytes**

**NVRAM Support for 1-4Mbytes**

**CODEC Interface for Sound**

**Numerous General Purpose I/O**

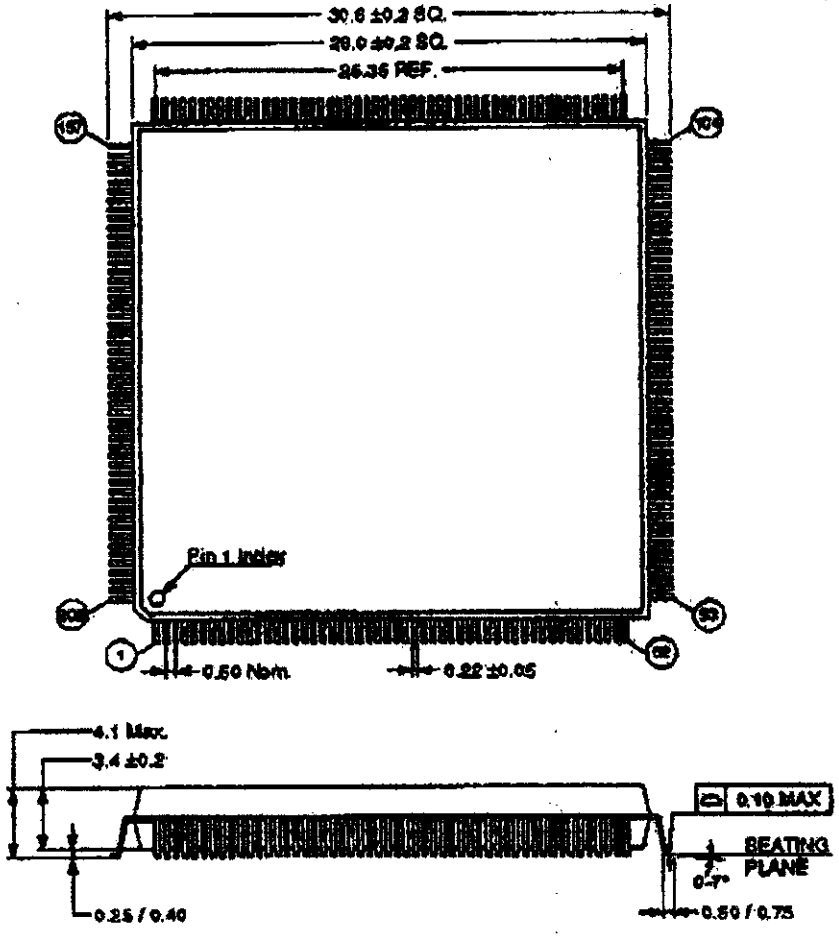
**Support for Several Lens and Shutter Alternatives**
- Focal Plane Shutter
- Fixed Focus Lens
- Auto Focus Lens
- Zoom Support

**Advanced Firmware Library**
- Nucleus Operating System
- Image Processing Library
- GUI Library
- Advanced Host Software Library
- PC Interface
- Macintosh Interface

## Physical ASIC Description

The Clarity 2 ASIC is available in a 208 Pin PQFP (Plastic Quad Flat Pack). It requires a 3.3Volt supply at approximately 200mA. However, current will vary depending uponthe application. It runs at 48MHz with an externally supplied 6 MHz crystal. It can operate from 0-70 degrees Celsius.

*Alternative packaging including the availability of raw dies are available. Please consult the factory for details.*




Dimensions in millimeters.

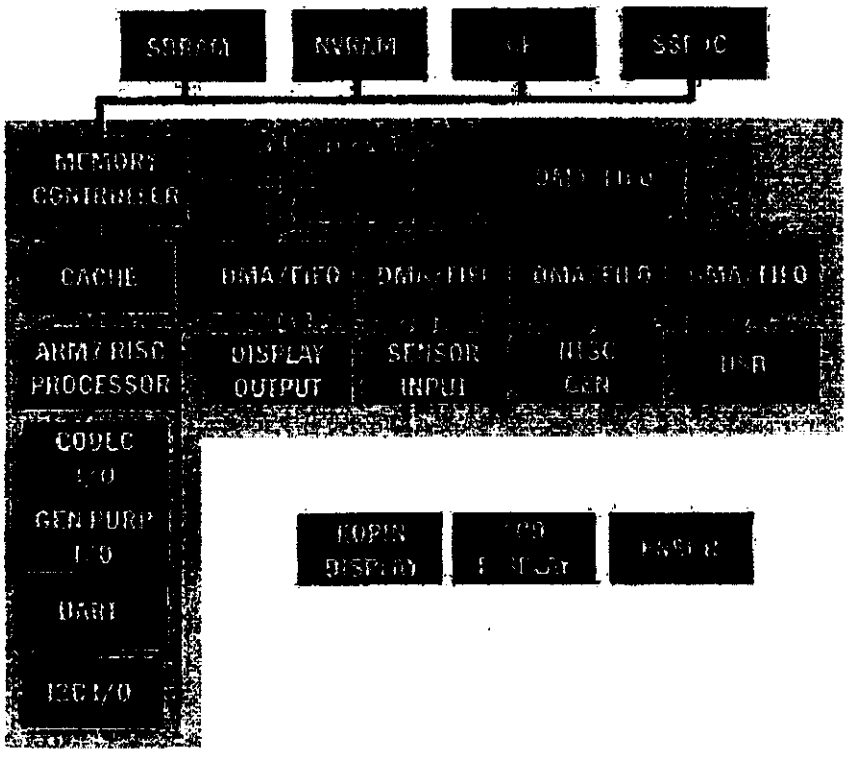
# Hardware Description

This section contains a brief description of the blocks that exist within the Clarity 2 ASIC. For more information refer to the detailed Clarity 2 ASIC specifications that can be downloaded from our web site:

https://www.ultranet.com/soundvisioninc/Clarity2/Clarity_2_ASIC_Specification.PDF

## Simplified Block Diagram

The following block diagram shows the Clarity 2 ASIC (Yellow) surrounded by a typical set of peripheral devices. Internally, the AMBA high speed bus and a lower speed peripheral bus interconnect the processor, memory, fifos and other peripherals.




### *ARM 7 TDMI, Interrupt and Memory Controllers*

The ARM7TDMI is a 32 bit RISC (Reduced Instruction Set) processor that operates at 48MHz. It includes both a 32 bit and a 16 bit (Thumb Extension) instruction set. Advantages of the ARM processor include:

- Multiple Upgrade Paths to the ARM9, 9E, and 10

- Advanced Development Tools
- Fast Single Cycle Multiplier (8 Bit Boothe Implementation)
- Portable Core for many foundries

Attached to the processor is an 8Kbyte, single cycle, Cache for both instructions and data.

The Interrupt Controller provides real time interrupts that indicate various events including DMA and I/O completion.

The Memory Controller arbitrates all memory accesses between the external memory bus which is typically attached to a combination of SDRAM, NVRAM or ROM storage, and a set of internal DMA controllers and the Cache. Key to the Memory Controller is its ability to use burst accesses for all memory operations in order to sustain an average memory bandwidth of 48Mbytes per second.

*Clarity 2 can be operated at oscillator speeds up to 64MHz. However, at these speeds, certain of the peripherals cannot be used. Please consult the factory for details.*

### DMA Controllers and FIFOs

All of the internal high speed peripherals attach to the memory controller through a combination of a DMA controller and a small 8 to 32 word FIFO. These FIFOs provide for the ability to burst data transfers into or out of memory, thus maintaining optimum performance.

### USB and RS-232 (UART)

External interface to a host computer is typically obtained though either the USB or UART interface. The USB interface includes a 16kbyte buffer memory that holds packets that are in the process of transmission between the systems. Data correction and retransmission is completely controlled within the USB interface.

The UART has adjustable baud rate that can be set by the ARM processor up to 115kbaud. It attaches to the peripheral bus and provides an interrupt on various events. An external device is required to achieve the voltage levels associated with the RS-232 specification.

### NTSC/PAL Output

The NTSC/PAL output generator includes a D/A converter and therefore produces an analog (base-band) signal that is compatible with the "video" input of most televisions. The ARM processor can set the interface, through software, to a number of different standards including NTSC, PAL B, M, N and CN.

An independent PLL (Phased Locked Loop) which is locked to the main oscillator (48MHz) creates the oscillator standard for these transmission modes. Therefore, no second crystal is required.

### Kopin and Digital LCD

Two other image display types are supported. These include a Kopin CyberDisplay 320C module (a miniature color LCD) and a 1.8 inch digital Epson/Seiko LCD with 312 pixels x 230 rows, each pixel being 8 bits.

### $I^2C$ Bus

An $I^2C$ Bus controller is included. It is typically attached to a "time of day" clock device, a status LCD driver or an external micro controller that can be used to extend the peripheral controls to additional buttons and display types.

### Button Scanning

The button scan and sense logic supports up to 24 inputs using a set of 3 external 8:1 multiplexers. Button scanning and de-bouncing is done automatically without processor intervention.

### Audio

The CODEC interface provides the timing and control necessary to perform proper handshaking with the Texas Instruments TLV320AC family of VoiceBand Audio Processors. It supports transmission and reception of serial data, generation of the associated frame sync pulses, along with a reference audio clock. The frame sync and master clock rates are selectable to support use with the 320AC36 and 320AC40 devices.

An RDK with an MP-3 Audio decoder is also available. However, for this implementation, the CODEC interface is not used, but rather, a small additional ASIC interfaces to the high quality stereo CODEC from the Memory Bus.

### Motor Controls

Both stepper-motor and solenoid-actuated shutters can be controlled. In a typical digital camera, these interfaces are used for the shutter, auto-focus motor and zoom features.

### Auto-Focus

The auto focus state machine provides the timing and control for interfacing with the Sharp IR3S72 auto-focus IC that uses IR triangulation. Automatic focus can also be implemented completely in software by using rapid frame acquisition with processing to test the focus quality and subsequent lens adjustment.

### Automatic Exposure and Flash Interface

A hardware interface is provided for an independent photo-diode measurement of exposure. This same photo-diode can be used for an IGBT type flash controller where the flash duration is controlled actively by the processor based upon the amount of reflected light.

### General Purpose I/O

There are eight groups of general purpose I/O (GPIO) signals, GPIOA– GPIOH; each group is multiplexed with other functions. An enable bit for each GPIO group selects between GPIO and the pre-defined functions.

### Compact Flash and Smart Memory Interface

Two types of external removable memory can be used with the Clarity 2 design: Smart media (also known as SSFDC) or Compact Flash.

### *Memory Interface*

Clarity 2 can be connected to various external memory types including 100MHz SDRAM varying in size from 2Mbytes to 64Mbytes, and NVRAM or ROM ranging from 1Mbyte to 4Mbytes.

### *Sensor Interface*

The Sensor Interface includes a 12 bit digital port that is attached to an external A/D converter (sometimes included within a CMOS detector). The interface contains several counters that can be either internally or externally synchronized to horizontal and vertical clocks. Therefore, it can easily be attached to a wide variety of CMOS and CCDs with their related interface components.

## Embedded System Development

Developing and debugging code for the Clarity 2 ASIC is similar to most embedded systems. A host PC, with either the Windows 95,98,2000 or NT operating system is attached to the embedded target system through an in circuit JTAG port. The ARM JTAG interface module attaches to the PC through the Parallel Port.

Source code can be written and managed using the Microsoft Visual C Developer's Studio. The ARM Compiler and Linker is used to compile C or Assembly code into machine format.

The debug environment allows C Source level debugging including download, trace, break and inspection.

Final code is typically downloaded into on-board NVRAM or can be programmed into a ROM.