AR-B9641 PC Compatible Information Appliance System-on-Chip

The AR-B9641 integrates a standard generation x86 core, a Synchronous DRAM controller, a graphics subsystem, a video pipeline, and support logic including PCI, ISA, and IDE controllers to provide a single consumer orientated PC compatible subsystem on a single device.

The device is based on a tightly coupled Unified Memory Architecture (UMA), sharing memory between the CPU, the graphics and the video.

At the heart of the STPC Consumer-II is an advanced 64-bit x86 processor block. It includes a 64-bit SDRAM controller, advanced 64-bit accelerated graphics and video controller, a high-speed PCI local-bus controller and Industry standard PC chip set functions (Interrupt controller, DMA Controller, Interval timer and ISA bus).

The STPC Consumer-II has in addition, an EIDE Controller, I 2 C Interface, a Local Bus interface and a JTAG interface.

The STPC Consumer-II makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and graphics frame-buffer. This means a reduction in total system memory for system performances that are equal to that of a comparable frame buffer and system memory based system, and generally much better, due to the higher memory bandwidth allowed by attaching the graphics engine directly to the 64-bit processor host interface running at the speed of the processor Bus rather than the traditional PCI bus.

The 64-bit wide memory array provides the system with 528MB/s peak bandwidth. This allows for higher resolution screens and greater color depth.

The ‘standard’ PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated together with the x86 processor core, additional functions such as communications ports are accessed by the STPC Consumer-II via internal ISA bus.

The PCI bus is the main data communication link to the STPC Consumer-II chip. The STPC Consumer-II translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports generation of Configuration cycles on the PCI bus, as a PCI bus agent (host bridge class), fully complies with PCI specification.

Description of the operation of the RF module:

1. Fundamental frequency spec.–10 to + 70 ℃ ±25 ppm which was generated by 44 MHz crystal oscillator(U6).It supply the reference clock to CPU and PLL.

2.Synthesizer

The frequency-synthesized circuits consists of crystal oscillator (U6), RF PLL IC (U11), IF PLL IC (U9) and IF VCO (U14). The frequency is controlled through CPU (U4) and generate different frequency band Which made by RF PLL and IF PLL. Receive and transmitter are same frequency; IF PLL (U13) generate 748MHz which is divided by 2(U9) to 374 MHz, which is IF LO. RF LO comes from VCO U14 and U11 PLL, the LO frequency is 2038– 2110 MHz, 5 MHz per step, total 14 channels. Transmitter/receiver freq. is 2412 and 2484 MHz.

3.Transmitter

Transmitter path is through (ANT1), switch (U8), band pass filter (FL3), IC (U11) transmitter, band pass filter (FL5), SAW filter (FL1), Quad IF Converter (U9) to Base band processor.

Transmitter frequency, channel 1 is 2412 MHz and channel 14 is 2484MHz,each channel has 5 MHz step. Transmitter power is 12 to 13 dBm.

4.Modulation

Modulation from CPU (U4), transmitter data into base band processor generate the I, Q signal then mixed with the IFLO which is 374MHz differential signal (phase difference 90 degree) then the I, Q sum up together. The modulation is DBPSK for 1M data rate, DQPSK for 2M data rate, CCK for 5 and 11 M data rate.

Demodulation: IF signal through U9 mixed with IFLO which is 374MHz differential signal (phase difference 90 degree). Generate the I, Q signal then through U4 base band processor demodulate into data. And send to CPU (U4) for data processing.

5.Receiver

RF signal 2412 to 2484 MHz, received from antenna, band pass TX/RX switch (U8), filter (FL6), through RF/IF converter (U11), mixed with RFLO down to 374MHz IF. Then IF through SAW filter into U9 mixed with IFLO, which is 374MHz differential signal (phase difference 90 degree). Generate the I, Q signal then

through U4 base band processor demodulate into data. nd send to CPU (U4) for data processing. Both U9 and U11 have AGC circuit to auto control the receiver signal for the best receiver sensitivity.

6.Signal Control

Signal control consists of CPU (U4), SRAM (U1), and Flash ROM (U5), Voltage regulator (U15/U7)

6-1.PLL control: Two PLL IC controlled by U4, one is IFLO, 748MHz, the other is RFLO from 2038 to 2110 MHz, with channel step 5 MHz.

6-2.TX/RX control: control the TX/RX switch (U8), U9, U11, U5 to perform TX/RX function.

6-3.VCO control: control the power supply of the RF VCO (U14) and IF VCO (U13)

6-4.Interface control: control Mini PCI interface through this interface communicate with system, which have TCP/IP and NDIS protocol.

6-5.Memory: In the flash memory contain the MAC address, firmware, product information, series number and other relative information.

7.Power supply:

Main power supply is from 3.3 V Mini PCI interface then into 2 regulator (U15, U7), which generate 2.85 V for RFIC and VCO.