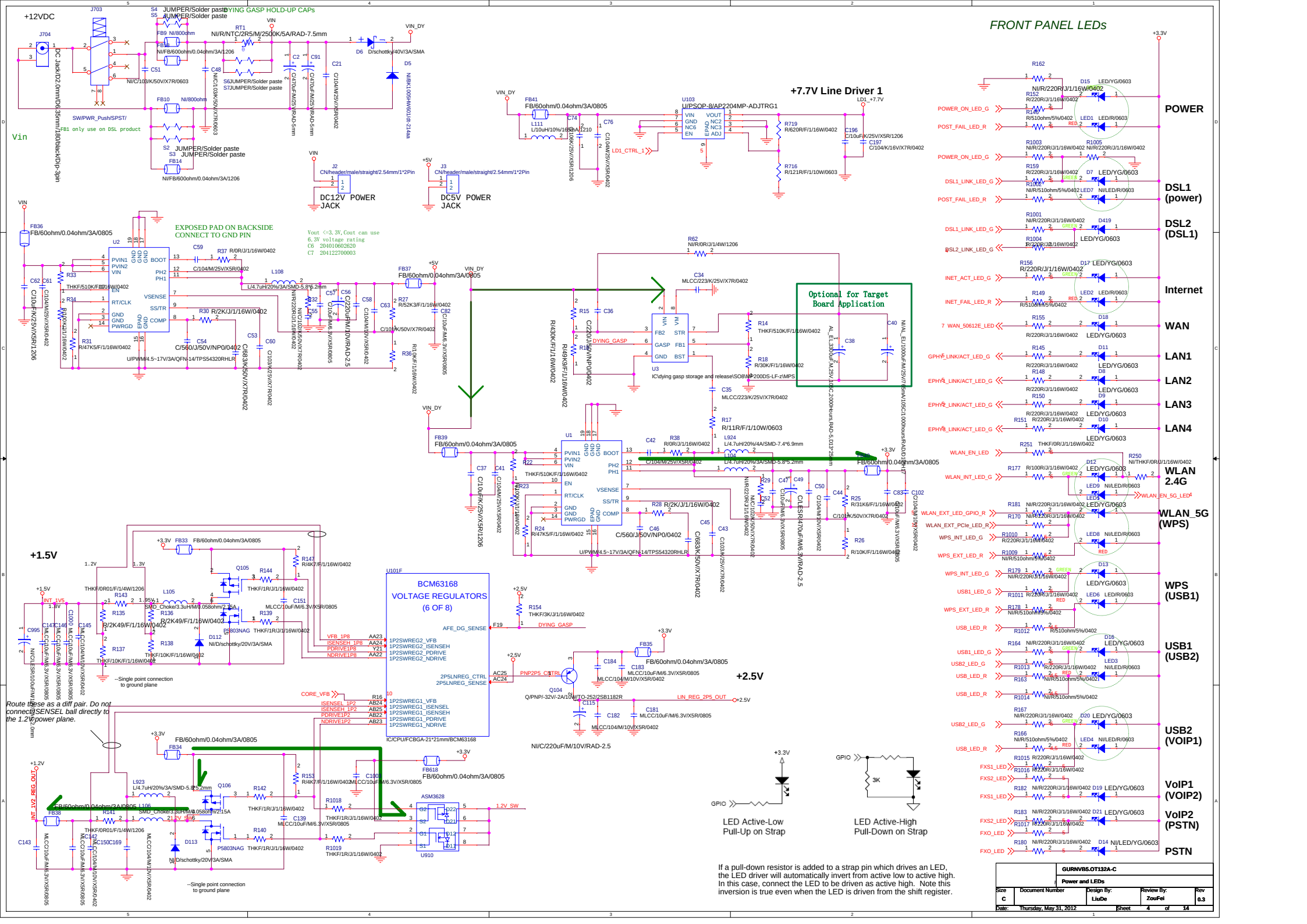

+12VDC
DYING GASP HOLD-UP CAPs
JUMPER/Solder paste
NI/R/NTC/2R5/M/2500K/5A/RAD-7.5mm
DC Jack/D2.0mm/D6.35mm/180/black/dip-3pin
SW/PWR_Push/SPST/
FB1 only use on DSL product
Vin
JUMPER/Solder paste
DC12V POWER JACK
DC5V POWER JACK
+7.7V Line Driver 1
FRONT PANEL LEDs
POWER
DSL1 (power)
DSL2 (DSL1)
Internet
WAN
LAN1
LAN2
LAN3
LAN4
WLAN 2.4G
WLAN_5G (WPS)
WPS (USB1)
USB1 (USB2)
USB2 (VOIP1)
VoIP1 (VOIP2)
VoIP2 (PSTN)
PSTN
EXPOSED PAD ON BACKSIDE CONNECT TO GND PIN
Optional for Target Board Application
+1.5V
+2.5V
BCM63168 VOLTAGE REGULATORS (6 OF 8)
Route these as a diff pair. Do not connect SENSEL ball directly to the 1.2V power plane.
LED Active-Low Pull-Up on Strap
LED Active-High Pull-Down on Strap
If a pull-down resistor is added to a strap pin which drives an LED, the LED driver will automatically invert from active low to active high. In this case, connect the LED to be driven as active high. Note this inversion is true even when the LED is driven from the shift register.
GURNVB5.0T132A-C
Power and LEDs
Size C
Document Number
Design By: LiuDe
Review By: ZouFei
Rev 0.3
Date: Thursday, May 31, 2012
Sheet 4 of 14

DDR SDRAM layout rules:

All timing is relative the CLK/CLKb that arrive at the destination DDR SDRAM chip.

1) X = CLK/CLKb should be a matched differential pair with a length < 4"
2) Address and control should be X +/- 20mm
3) DQS and DQM should be X +/- 20mm
4) All DQs should match corresponding byte lane DQS/DQMs within +/- 10mm
5) Trace impedances should be 50 ohms +/- 10% (45-55 ohms)
6) Route VREF with 30-mil trace and at least 1 high quality ceramic bypass capacitor for each connection to a device.
7) All traces should have a >= 3 to 1 spacing ratio from the reference GND/PWR layer. (e.g. 15 mil line-to-line spacing for a 5 mil dielectric thickness)

Place C201-C218, close to U201

Place C201-C218, close to U201

Swap high/low byte lanes to allow for layout of DDR3.
Also swap bits within byte lanes.

Place C229 near R210, R225.

Place one at each IC pin.

Place R202-203 and C233 as close as possible to U201

1Gbit DDR3 SDRAM 64Mx16

MAIN MEMORY DDR3 SDRAM 128-256 MBYTES

U/DDR3-SDRAM/1Gbit/BGA-96/NT5CB64M16DP-CF

MAIN MEMORY DDR2 SDRAM 32-256 MBYTES

JTAG

BCM63168 MEMORY AND GPIO (1 OF 8)

U101A

IC/CPU/FCBGA-21*21mm/BCM63168

R207-208 are for test only. Remove for production.

OPTIONAL SPI Serial FLASH MEMORY: 2-32 MBYTES

NI/Flash/32Mbit/2.7~3.6V/SO8-208mils/W25X32VSSIG

U8 Flash/128Mbit/2.7~3.6V/SO16-300mils/S25FL128P0XMFI001

LED USAGE:

a) LED connections only supported on LED[23:0]
b) USB_DEVICE_LED always use ball B3
c) INET_LED always use LED[8]
d) EPHY[3:1]_ACT_LED always use LED[11:9]
e) GPHY_ACT_LED always use LED[12]
f) EPHY[3:1]_SPD_LED always use LED[15:13]
g) GPHY_SPD_LED[1:0] always use LED[1:0]
h) WLAN LED only supported through GPIO[38:36]
i) Applications using NAND flash cannot access LED[7:2] through GPIO[7:2], and may shift out LED[7:0] through SERIAL_LED_CLK and SERIAL_LED_DATA.

Bootstrap inputs are muxed onto GPIO[31:11]. Be aware that placing a pull-down resistor on any of these gpio will change the default bootstrap configuration.

GPIO[51:40] are not accessible on a 4-layer PCB.
GPIO[51:36] do not have internal pull ups.

Shift registers for serial LED driver are shown as an example. Use only if there are not enough gpio available for LEDs

NAND FLASH

U209 TSOP48

THKF/3K/J/1/16W/0402 NAND Flash/1Gbit/2.7~3.6V/TSOP48/NAND01GW3A2CN1E/ST

U210 NI/U/63-ball VFBGA/MT29F1G01ZACHC:C

Register/SOIC-14/SN74HC164D

Reset to default

Wlan Push-button

WPS Button

ESD/smd/2pin/2.1x1.1

NI/Supervisor/SOT-23/MAX809STRG

BCM63168 Strap Options

Strap settings change for B0 and C0 or later silicon

NAND_SPARE_16B		
Silicon Revision	B0	C0
16 Bytes	0	1
27 Bytes	1	0

NAND_ENABLE_ECC		
Silicon Revision	B0	C0
Enable	0	1
Disable	1	0

NAND ECC SEL[2:0]		
Silicon Revision	B0	C0
1-bit Hamming	001	111
4-bit BCH	010	100
8-bit BCH	011	101
12-bit BCH	100	010

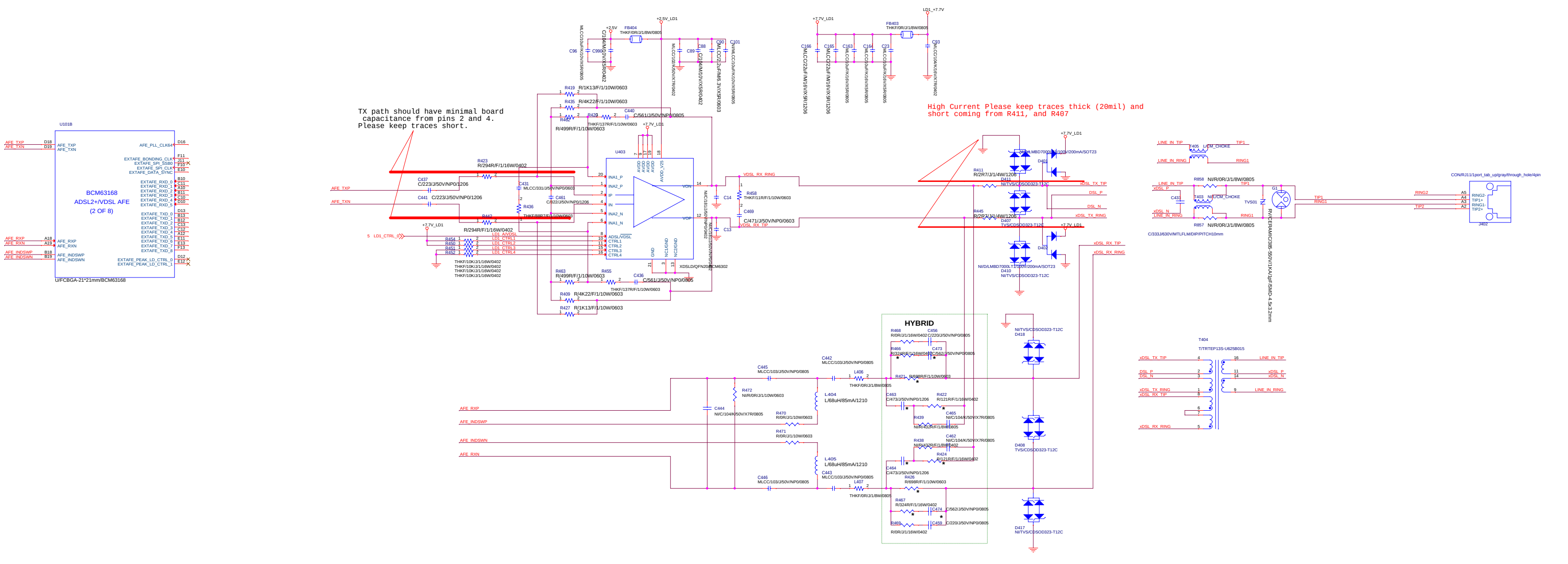
* All other values = No ECC

If a pull-down resistor is added to a strap pin which drives an LED, the LED driver will automatically invert from active low to active high. In this case, connect the LED to be driven as active high. Note this inversion is true even when the LED is driven from the shift register.

LED Active-Low Pull-Up on Strap

LED Active-High Pull-Down on Strap

	GURNVB5.0T132A-C	
	SDRAM and FLASH	
Size: Custom	Document Number: LiuDe	Design By: ZouFei
Review By:	Rev: 0.3	
Date: Thursday, May 31, 2012	Sheet 5 of 14	



AFE Version A.7.2.30
AFE ID:0X10608700

	GURNVB5.OT132A-C			
	EXT AFE-Bonding or 30A Profile			
Size: E	Document Number	Design By: LiuDe	Review By: ZouFei	Rev 0.3
Date: Thursday, May 31, 2012		Sheet 6 of 14		

MII/TMII/RGMII - Layout Guidelines & Notes

1. Route traces with 50ohm characteristic impedance.
2. Match trace lengths to a tolerance of 385 mil within TX and RX separately.
3. Keep the receive and transmit signals kept away from each other and other analog and clock signals.
4. Place capacitors and ferrite beads close to VDD traces and routes short.

CONNECT MIIx_VDDO1 & 2 TO 3.3V WHEN USED IN MII, RvMII, TMII MODE, OR WHEN NOT USED
CONNECT MIIx_VDDO1 & 2 TO 2.5V WHEN USED IN RGMII MODE, OR WHEN NOT USED

No decoupling cap necessary when MII port not used.

BCM63168
MII INTERFACES
(4 OF 8)

IC/CPUIFCBGA-21*21mm/BCM63168

MII/GMII/RGMII - Layout Guidelines & Notes

1. Route traces with 50ohm characteristic impedance.
2. Match trace lengths to a tolerance of 0.5mm.
3. Keep the receive and transmit signals kept away from each other and other analog and clock signals.
4. Voltage on PHY and CPU's VDD pins must be the same and must match the rgmii mode selected.

Place R546/R548/R550/R554/R556/R557 close to 6368 MII outputs have 50 driver impedance. Use value to match trace impedance.
Rtrace = Rterm + Rdriver. Increase value to reduce EMC.

Place R529/R532/R533/R534/R535/R536 close to 6368 MII outputs have 50 driver impedance. Use value to match trace impedance.
Rtrace = Rterm + Rdriver. Increase value to reduce EMC.

BCM50612E

Route TRD+/- pairs with 100-ohms differential trace impedance

PHY ADDR: 0x18

TEST[3:2] = 11 for PHYA mode in which addr = 0x18 + PHYA0

To support EEE sleep/wark power surges,set C28 to 10uF, C18,C73 to 22uF and C69 to 33uF,Also install R61

B50612E PHY Address

PHY Addr	TEST[3:2]	PHYA0
0x00	00	0
0x01	00	1
0x18	11	0
0x19	11	1

Strap the B50612E to RGMII 3.3V mode to preserve LED configuration and allow LED4 to be compatible with IRQ (open-drain with pull-up). Software configures the B50612E to the correct RGMII mode (2.5V RGMII).

B50612E RGMII MODE SELECTION TABLE

RGMII Mode	MODE_SEL[1:0]	Pin Configuration
RGMII 3.3V	00	TEST[3:2] = 00 or 11, LED[3]=0 LED[2]=0 LED[4]=0
RGMII 2.5V	01	TEST[3:2] = 00 or 11, LED[3]=0 LED[2]=1 LED[4]=0
RGMII HSTL	10	TEST[3:2] = 00 or 11, LED[3]=1 LED[2]=0 LED[4]=0
Reserved	11	TEST[3:2] = 00 or 11, LED[3]=1 LED[2]=1 LED[4]=0
-> RGMII 3.3V	00	TEST[3:2] = 00 or 11, LED[3]=0 LED[2]=X LED[4]=1
RGMII HSTL	10	TEST[3:2] = 00 or 11, LED[3]=1 LED[2]=X LED[4]=1

X = Don't Care

	GURNVBSLOT132A-C		
	GPHY-BCM50610		
Size: D	Document Number	Design By: LiuDa	Review By: ZeeFei
			Rev: 0.3
Date: Thursday, May 31, 2012		Sheet 7 of 16	

Ephy 10/100 and GPHY - Layout Guidelines & Notes

1. Route RDN, RDP and TDN, TDP pairs differentially, with 100ohm differential impedance, adjacent to the ground plane.
2. Keep differential pairs within a port separated by 3H distance and pairs between ports separted by 5H where H is the hieght of traces above the ground plane, i.e. H = the dielectric thickness.
3. Match differential pair trace length within the pair (P and N) to 10mils. No need to match trace length between differential pairs (RD and TD).

BCM63168
PHY INTERFACES
(3 OF 8)

U101C

IC/CPU/FCBGA-21*21mm/BCM63168

T701
T/ENET/DIP-2.0mm/20pin/MT1642CJ

T702
T/ENET/DIP-2.0mm/20pin/MT1642CJ

J705
CN/RJ45_Nonshielded/4port_tab_down/Yellow/DIP-32pin/55.5*15.1*16.2MM

Route PCIe traces with 100ohm differential characteristic impedance.

U907
U/USB Switch/MSOP-8/TPS2065DGNG4

U906
U/USB Switch/MSOP-8/TPS2065DGNG4

U908
NI/TVS/Array/5V/25A/500W/10pF/SOT-143/SR05

U909
NI/TVS/Array/5V/25A/500W/10pF/SOT-143/SR05

J8
CN/USB-A/F/1port/DIP-4+2PIN/shihui

J7
CN/USB-A/F/180/1*4PIN/1port/USB-13.7/180DIP

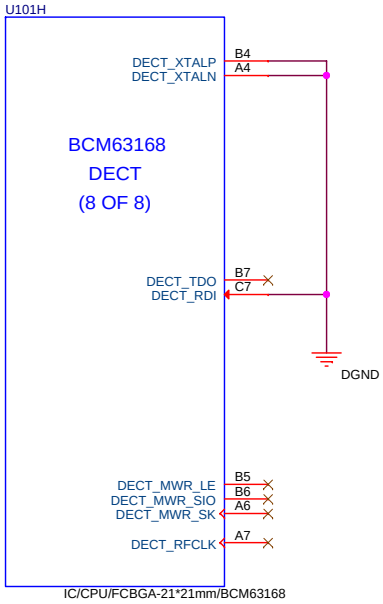
J708
SERIAL CONSOLE PORT
Header/male/180/1*4/6-2.54-3MM/black/DIP-2.54mm/PIN 0.64*0.64MM

R529	460ohm	230ohm
	USB_500mA	USB_1A

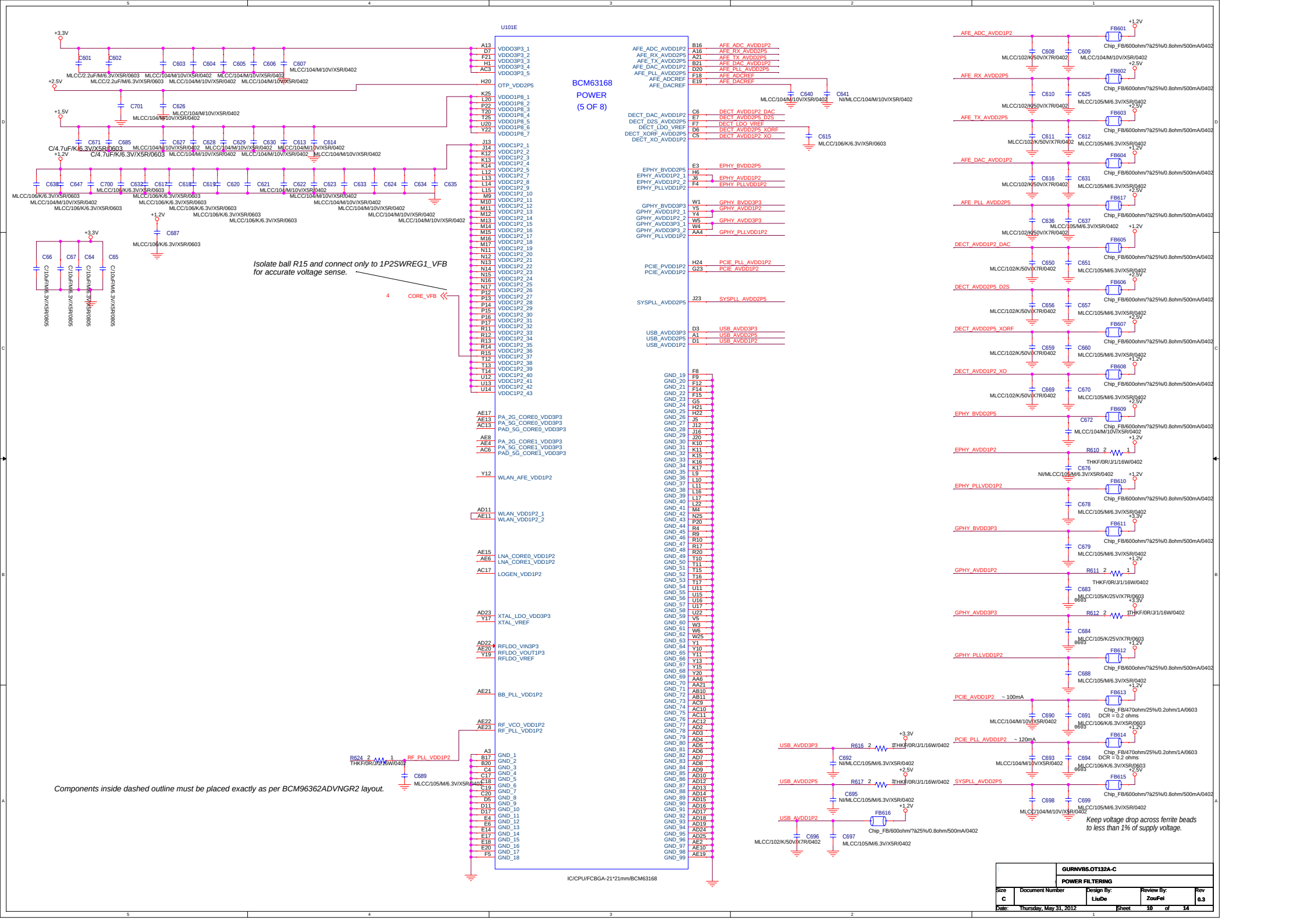
USB2.0 - Layout Guidelines & Notes

1. The Dp and Dn traces are length matched, with max differential skew, within 20mils
2. Differential trace length must be less than 5 inches
3. No more than 2 vias per trace, prefer zero.
4. Never split the ground plane under differential pair routing
5. Route differential pairs above the GND plane.
6. Differential impedance is 90 ohms for USB.
7. Adjacent differential pairs should be separated by at least 3 times the trace width. (e.g. 7.5 mil trace, leave >22.5mils between adjacent diff pairs)
8. Stitch gnd vias around each differential pair, but NOT between a given pair.

	GURNVB5.OT132A-C		
	Quad EPHY-UART-USB		
Size: C	Document Number:	Design By: LiuDe	Review By: ZouFei	Rev: 0.3
Date: Thursday, May 31, 2012		Sheet 8 of 14	



	GURNVB5.OT132A-C			
	DECT			
Size: B	Document Number:	Design By: LiuDe	Review By: ZouFei	Rev: 0.3
Date: Thursday, May 31, 2012		Sheet 9 of 14		

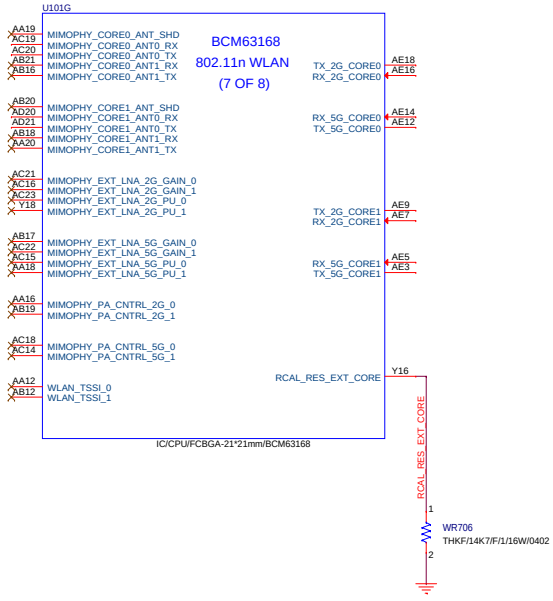

U101E
BCM63168
POWER
(5 OF 8)
IC/CPU/FCBGA-21*21mm/BCM63168
Isolate ball R15 and connect only to 1P2SWREG1_VFB for accurate voltage sense.
Components inside dashed outline must be placed exactly as per BCM96362ADVNGR2 layout.
Keep voltage drop across ferrite beads to less than 1% of supply voltage.
GURNVB5.OT132A-C
POWER FILTERING
Size C
Document Number
Design By: LiuDe
Review By: ZouFei
Rev 0.3
Date: Thursday, May 31, 2012
Sheet 10 of 14

The following traces must have 50 ohm RF impedance

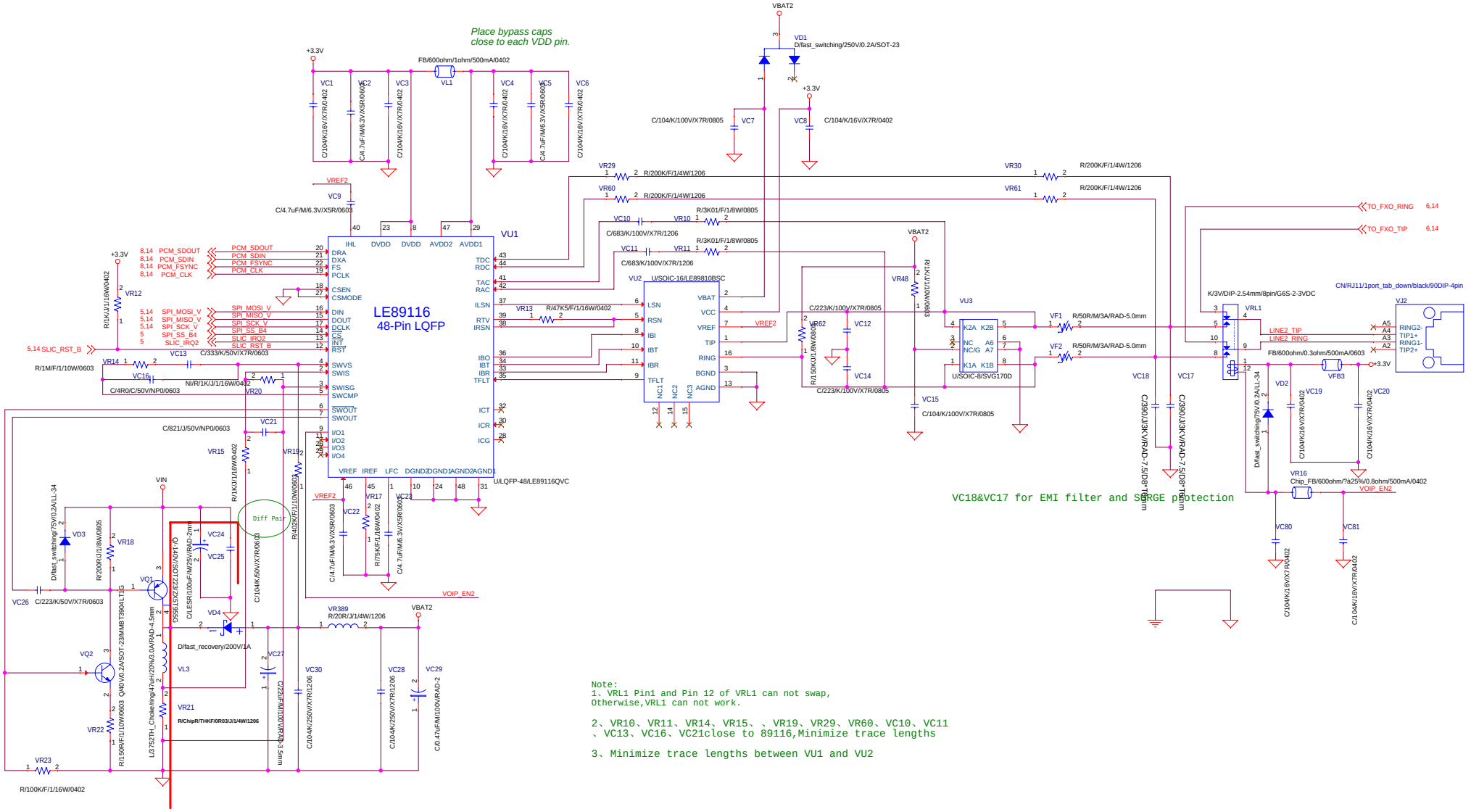
TXG_0, TXG0_IN, TXG0_OUT, TXG0_OUT_0
RXG_0, RXG0_OUT, RXG0_IN, RXG0_IN_0
RXA_0, RXA0_OUT, RXA0_IN, RXA0_IN_0
TXA_0, TXA0_IN, TXA0_OUT, TXA0_OUT_0

TXG_1, TXG1_IN, TXG1_OUT, TXG1_OUT_0
RXG_1, RXG1_OUT, RXG1_IN, RXG1_IN_0
RXA_1, RXA1_OUT, RXA1_IN, RXA1_IN_0
TXA_1, TXA1_IN, TXA1_OUT, TXA1_OUT_0

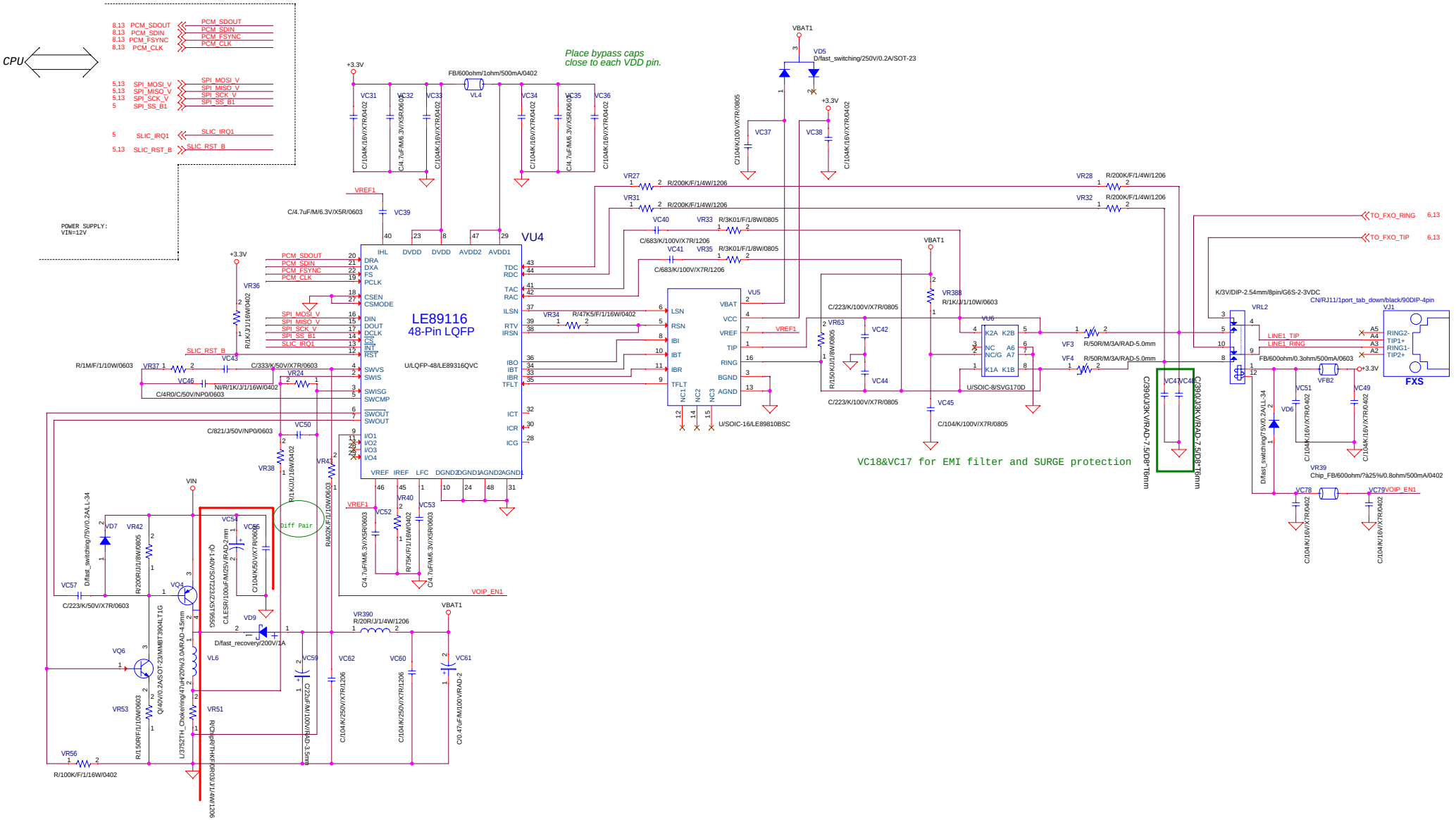
A0, WLAN_A0, A1, WLAN_A1



	GURNVB5.OT132A-C			
	WLAN			
Size: C	Document Number:	Design By: LiuDe	Review By: ZouFei	Rev: 0.3
Date: Thursday, May 31, 2012		Sheet 11 of 14		



	GURNVB5.OT132A-C			
	FXS			
Size: C	Document Number:	Design By: LiuDe	Review By: ZouFei	Rev: 0.3
Date: Thursday, May 31, 2012		Sheet 13 of 14		



Note:
1.Pin1 and Pin 12 of VRL2 can not swap,
Otherwise,VRL1 can not work.

2.PCB Capacitor VC63、VC69、VC71:

PCB thickness		PCB Cap Diameters	
0.8mm	0.031"	3.71mm	0.146"
1.27mm	0.050"	4.57mm	0.180"
1.55mm	0.062"	4.95mm	0.195"
2.40mm	0.094"	5.87mm	0.231"

3. Populate VC64 &VC68 If Necessary For Immunity Standard Compliance.

4. Populate VC67 & VL7 If Increased Out-Of-Band Immunity Is needed
---Please Refed To The VE8911 ERRATA For More Details.

5. Poulate VC73 AND VR74 Are Only Needed For The NEW ZEALAND Complex Impedance.
Note That AUSTRALIA Impedance Is Also Acceptable In NEW ZEALAND.

6. Place VR44 & VR52 close to VU7 pin.

7. Minimize trace lengths between VU4 and VU5 .

8. VR27、VR31、VR33、VR35、、VR37、VR38、VR43、VC40、VC41
、VC43、VC46、VC50close to 89316,Minimize trace lengths .

	GURNVB5.OT132A-C
	FXO
Size: C	Document Number:
Design By: LiuDe	Review By: ZouFei
Rev: 0.3	
Date: Thursday, May 31, 2012	Sheet 14 of 14