Module Number	GURN5.OT142A-C
Product Type	4FE LAN+1GE WAN+2.4G WIFI 2T2R +2USB HOST+A/VDSL(30a) +PCIe

Revision History

Version	Description	Designer	Date
0.1	Initial release Base on GURNV5.OT148A-9_30A ,change 5GE to 4FE+1GE	Lin Xian	2012/07/12
Gerber	B50612E's LED	Lin Xian	2012/10/22

GURN5.OT142A-C				
Cover Page				
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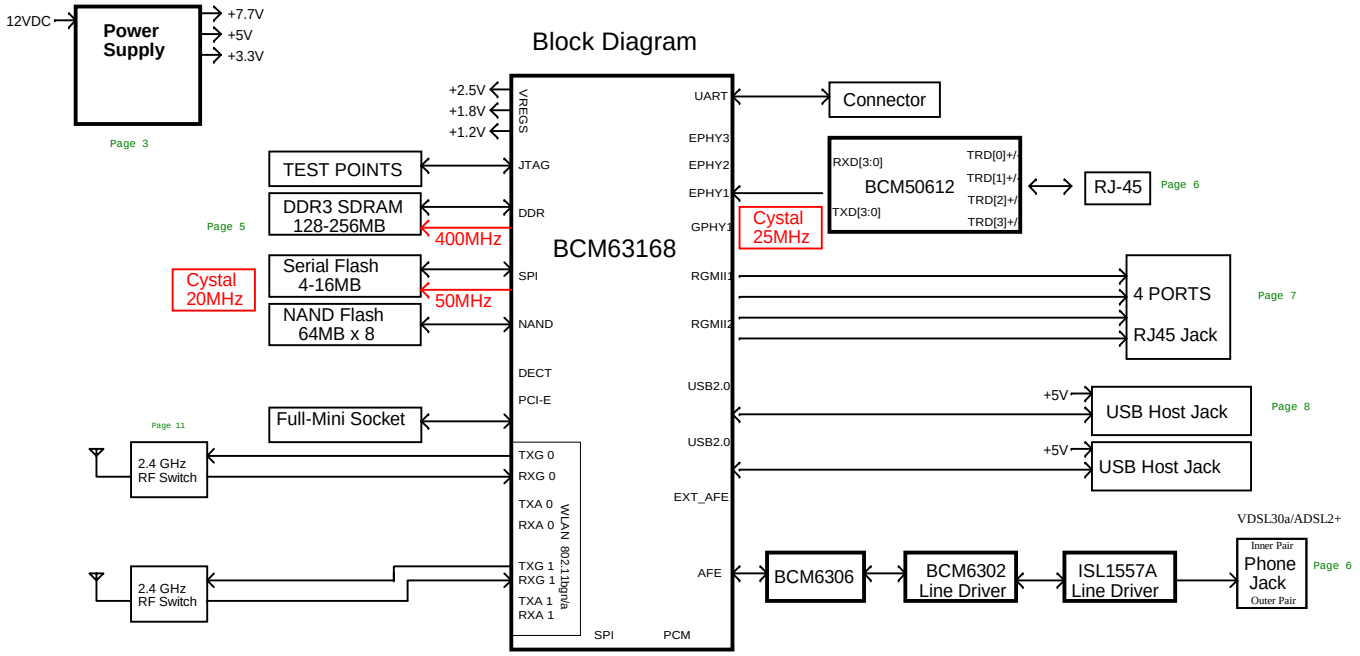
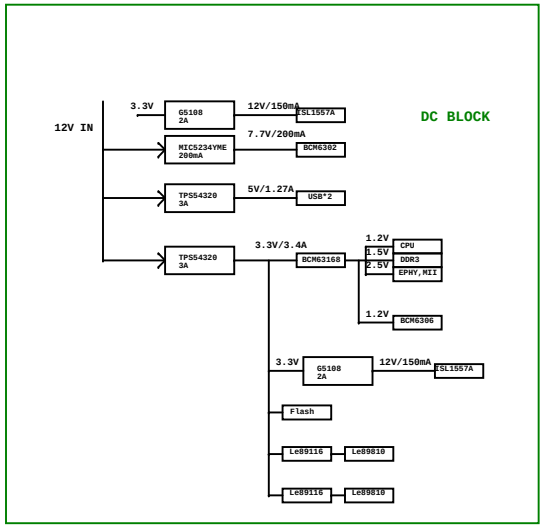
GURN5.OT142A-C- 4FE LAN+1GE WAN+2.4G WIFI 2T2R+2USB HOST+A/VDSL(30a) +PCIe

Block Diagram





T&W ELECTRONICS	GURN5.OT142A-C		
	Block Diagram		
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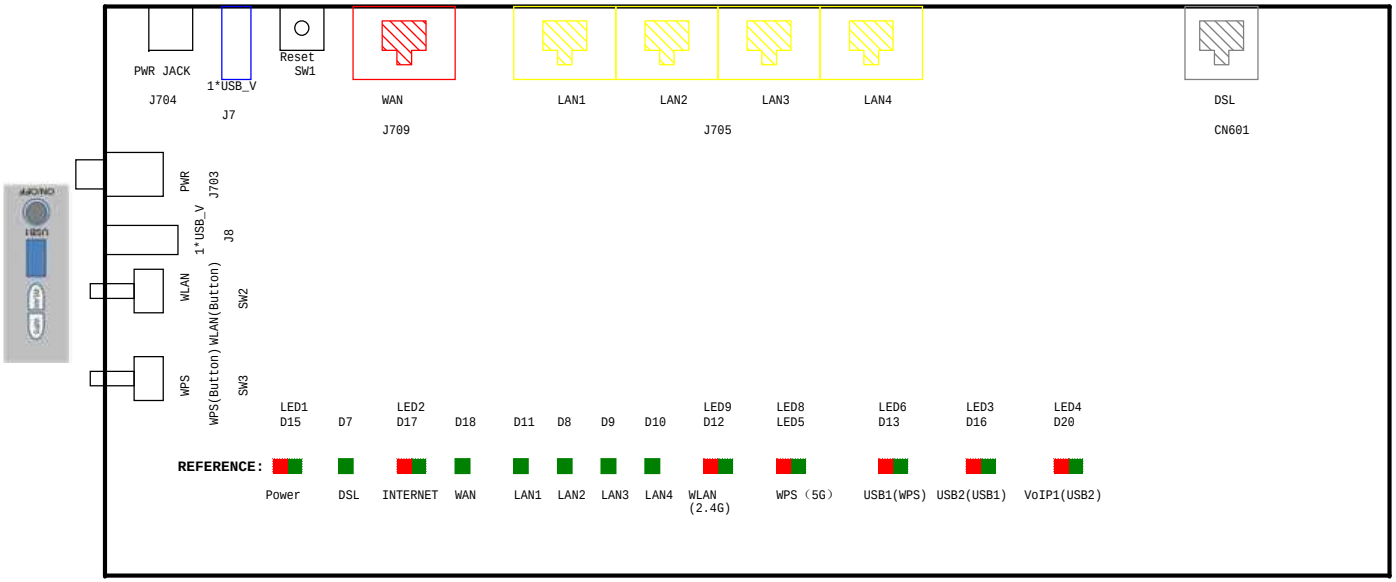

FIDUCIAL-MARK	SCREW HOLE:	FIXED HOLE:
TOP: M1 M2 M3 BOTTOM: M4 M5 M6		

T&W ELECTRONICS	GURN5.OT142A-C			
	Machine Diagram			
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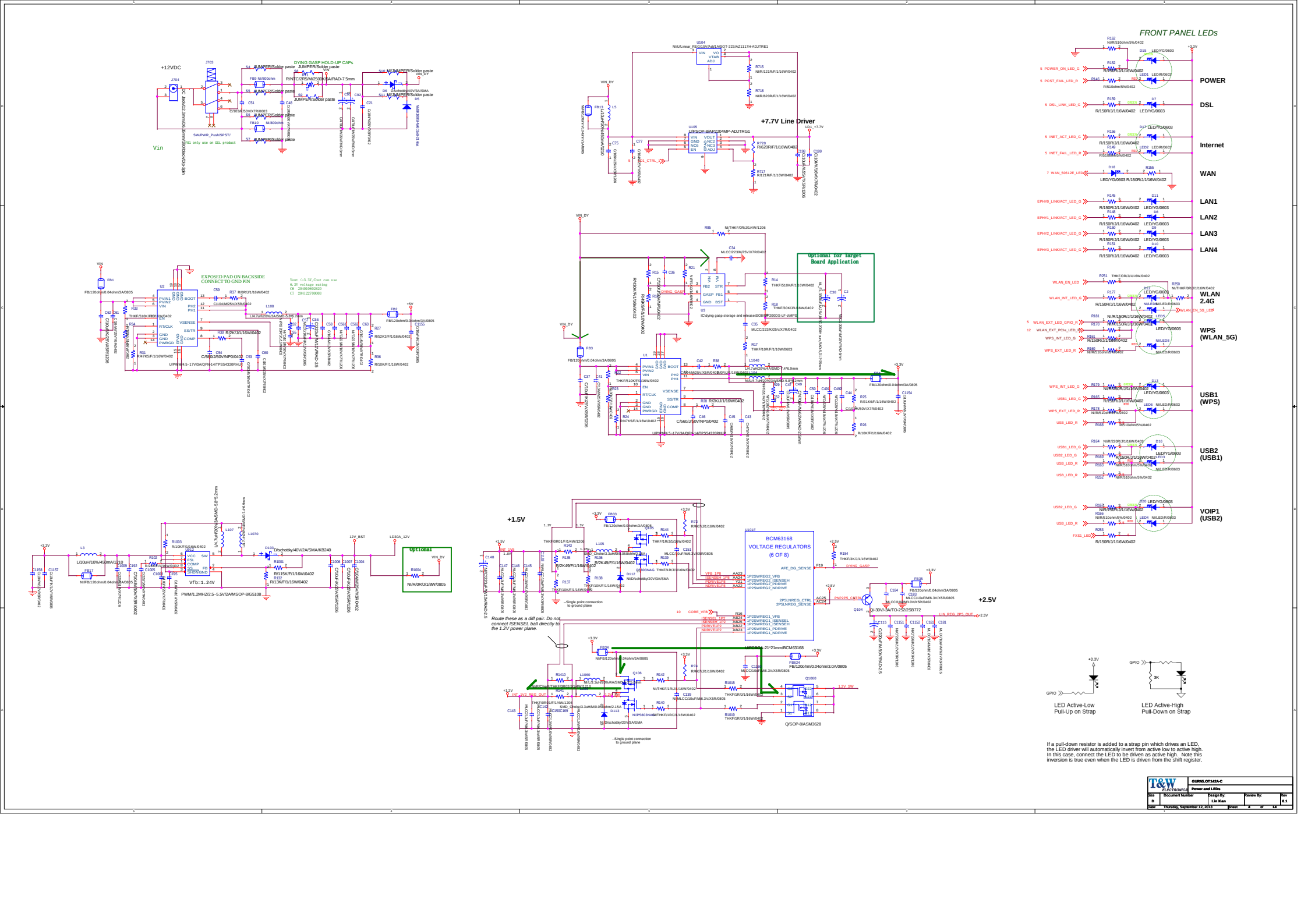
FRONT PANEL LEDs
POWER
DSL
Internet
WAN
LAN1
LAN2
LAN3
LAN4
WLAN 2.4G
WPS (WLAN_5G)
USB1 (WPS)
USB2 (USB1)
VOIP1 (USB2)
+12VDC
Vin
DYING GASP HOLD-UP CAPs
+7.7V Line Driver
Optional for Target Board Application
+1.5V
+2.5V
Optional
LED Active-Low Pull-Up on Strap
LED Active-High Pull-Down on Strap
If a pull-down resistor is added to a strap pin which drives an LED, the LED driver will automatically invert from active low to active high. In this case, connect the LED to be driven as active high. Note this inversion is true even when the LED is driven from the shift register.
T&W ELECTRONICS
GUR65.OT142A-C
Power and LEDs
Lin Xian
Thursday, September 12, 2013

DDR SDRAM layout rules:

All timing is relative the CLK/CLKb that arrive at the destination DDR SDRAM chip.

1) X = CLK/CLKb should be a matched differential pair with a length < 4"
2) Address and control should be X +/- 20mm
3) DQS and DQM should be X +/- 20mm
4) All DQs should match corresponding byte lane DQS/DQMs within +/- 10mm
5) Trace impedances should be 50 ohms +/- 10% (45-55 ohms)
6) Route VREF with 30-mil trace and at least 1 high quality ceramic bypass capacitor for each connection to a device.
7) All traces should have a >= 3 to 1 spacing ratio from the reference GND/PWR layer. (e.g. 15 mil line-to-line spacing for a 5 mil dielectric thickness)

Place C201-C218, close to U201

Place C201-C218, close to U201

Swap high/low byte lanes to allow for layout of DDR3. Also swap bits within byte lanes.

BCM63168 MEMORY AND GPIO (1 OF 8)

1Gbit DDR3 SDRAM 64Mx16

MAIN MEMORY DDR3 SDRAM 128-256 MBYTES

Place C229 near R210, R225.

Place one at each IC pin.

Place R202-203 and C233 as close as possible to U201

R207-208 are for test only. Remove for production.

OPTIONAL SPI Serial FLASH MEMORY: 2-32 MBYTES

U8 U/Flash/128Mbit/SO16-300mils/S25FL128SAGMFI001

LED USAGE:

a) LED connections only supported on LED[23:0]
b) USB_DEVICE_LED always use ball B3
c) INET_LED always use LED[8]
d) EPHY[3:1]_ACT_LED always use LED[11:9]
e) GPHY_ACT_LED always use LED[12]
f) EPHY[3:1]_SPD_LED always use LED[15:13]
g) GPHY_SPD_LED[1:0] always use LED[1:0]
h) WLAN LED only supported through GPIO[38:36]
i) Applications using NAND flash cannot access LED[7:2] through GPIO[7:2], and may shift out LED[7:0] through SERIAL_LED_CLK and SERIAL_LED_DATA.

Reset to default

Wlan Push-button

WPS Button

MAIN MEMORY DDR2 SDRAM 32-256 MBYTES

JTAG

U/DDR3-SDRAM/1Gbit/BGA-96/NT5CB64M16DP-CF

Bootstrap inputs are muxed onto GPIO[31:11]. Be aware that placing a pull-down resistor on any of these gpio will change the default bootstrap configuration.

GPIO[51:40] are not accessible on a 4-layer PCB. GPIO[51:36] do not have internal pull ups.

IC/CPU/FCBGA-21*21mm/BCM63168

Shift registers for serial LED driver are shown as an example. Use only if there are not enough gpio available for LEDs

Register/SOIC-14/SN74HC164D

BCM63168 Strap Options

Strap settings change for B0 and C0 or later silicon

NAND_SPARE_16B		
Silicon Revision	B0	C0
16 Bytes	0	1
27 Bytes	1	0

NAND_ENABLE_ECC		
Silicon Revision	B0	C0
Enable	0	1
Disable	1	0

NAND ECC SEL[2:0]		
Silicon Revision	B0	C0
1-bit Hamming	001	111
4-bit BCH	010	100
8-bit BCH	011	101
12-bit BCH	100	010

* All other values = No ECC

If a pull-down resistor is added to a strap pin which drives an LED, the LED driver will automatically invert from active low to active high. In this case, connect the LED to be driven as active high. Note this inversion is true even when the LED is driven from the shift register.

LED Active-Low Pull-Up on Strap

LED Active-High Pull-Down on Strap

T&W ELECTRONICS	GURNS.OT142A-C
	SDRAM and FLASH
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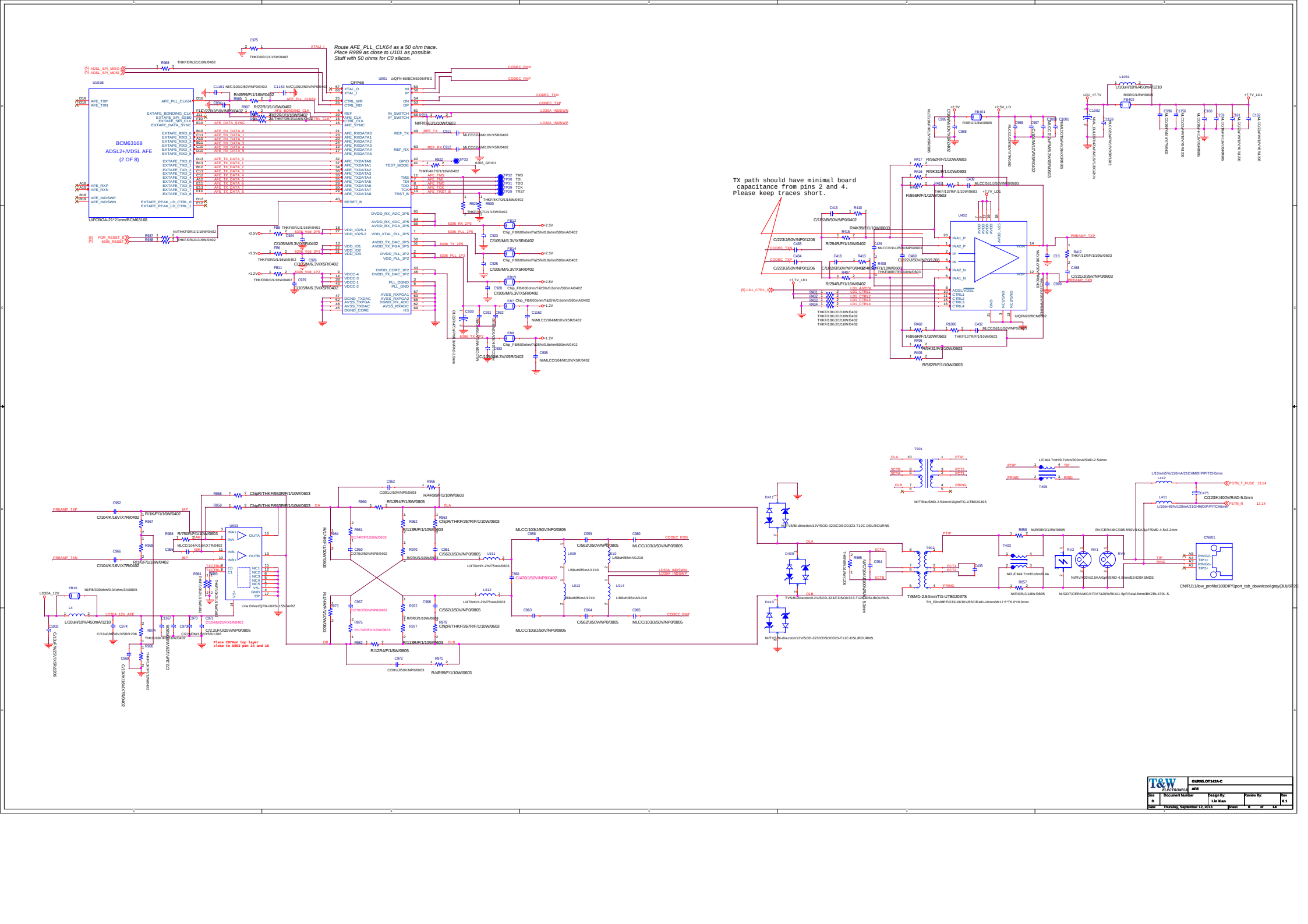
Route AFE_PLL_CLK64 as a 50 ohm trace.
Place R989 as close to U101 as possible.
Stuff with 50 ohms for C0 silicon.
BCM63168
ADSL2+/VDSL AFE
(2 OF 8)
U1FCBGA-21*21mmBCM63168
TX path should have minimal board capacitance from pins 2 and 4.
Please keep traces short.
Place C970on top layer close to U903 pin 14 and 15
Line Driver/IQFN-16/SLI35 AIRZ
U1QFN20/BCM6302
T/SMD-2.54mm/TG-UTB02037S
CN/RJ11/low_profile/180DIP/1port_tab_down/cool gray/3U/6P2C
T&W ELECTRONICS
GURN5.0T142A-C
AFE
Lin Xian
Thursday, September 12, 2013
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Ephy 10/100 and GPHY - Layout Guidelines & Notes

1. Route RDN, RDP and TDN, TDP pairs differentially, with 100ohm differential impedance, adjacent to the ground plane.
2. Keep differential pairs within a port separated by 3H distance and pairs between ports separted by 5H where H is the hieght of traces above the ground plane, i.e. H = the dielectric thickness.
3. Match differential pair trace length within the pair (P and N) to 10mils. No need to match trace length between differential pairs (RD and TD).

T1.3 can not tie to 2.5V

T1 T/ENET/DIP-2.0mm/20pin/MT1642CJ

T2 T/ENET/DIP-2.0mm/20pin/MT1642CJ

BCM63168
PHY INTERFACES
(3 OF 8)

IC/CPU/FCBGA-21*21mm/BCM63168

CN/RJ45_Nonshielded/4port_tab_down/Yellow/DIP-32pin/55.5*15.1*16.2MM

Route PCIe traces with 100ohm differential characteristic impedance.

USB2.0 - Layout Guidelines & Notes

1. The Dp and Dn traces are length matched, with max differential skew, within 20mils
2. Differential trace length must be less than 5 inches
3. No more than 2 vias per trace, prefer zero.
4. Never split the ground plane under differential pair routing
5. Route differential pairs above the GND plane.
6. Differential impedance is 90 ohms for USB.
7. Adjacent differential pairs should be separated by at least 3 times the trace width. (e.g. 7.5 mil trace, leave >22.5mils between adjacent diff pairs)
8. Stitch gnd vias around each differential pair, but NOT between a given pair.

SERIAL CONSOLE PORT

Header/male/180/1*4/6-2.54-3MM/black/DIP-2.54mm/PIN 0.64*0.64MM

R529	460ohm	230ohm
	USB_500mA	USB_1A

T&W ELECTRONICS	GURN5.OT142A-C
	Quad EPHY-UART-USB

Size	Document Number	Design By:	Review By:	Rev
C		Lin Xian		0.1

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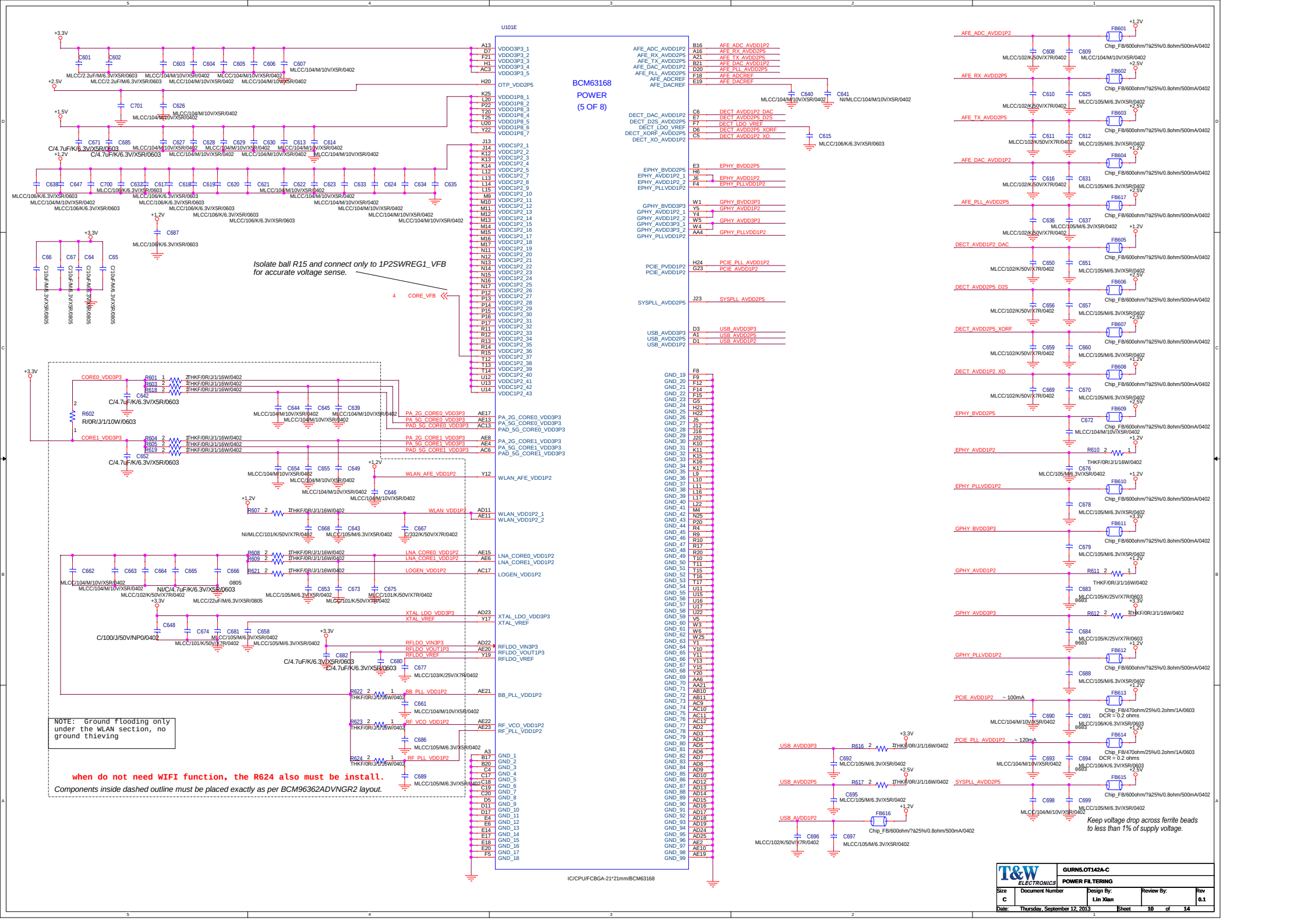
U101E
BCM63168
POWER
(5 OF 8)
IC/CPU/FCBGA-21*21mm/BCM63168
Isolate ball R15 and connect only to 1P2SWREG1_VFB for accurate voltage sense.
NOTE: Ground flooding only under the WLAN section, no ground thieving
when do not need WIFI function, the R624 also must be install.
Components inside dashed outline must be placed exactly as per BCM96362ADVNGR2 layout.
Keep voltage drop across ferrite beads to less than 1% of supply voltage.
T&W ELECTRONICS
GUR5.0T142A-C
POWER FILTERING
Size C
Document Number
Design By: Lin Xian
Review By:
Rev 0.1
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The following traces must have 50 ohm RF impedance

TXG_0, TXG0_IN, TXG0_OUT, TXG0_OUT_0
RXG_0, RXG0_OUT, RXG0_IN, RXG0_IN_0
RXA_0, RXA0_OUT, RXA0_IN, RXA0_IN_0
TXA_0, TXA0_IN, TXA0_OUT, TXA0_OUT_0

TXG_1, TXG1_IN, TXG1_OUT, TXG1_OUT_0
RXG_1, RXG1_OUT, RXG1_IN, RXG1_IN_0
RXA_1, RXA1_OUT, RXA1_IN, RXA1_IN_0
TXA_1, TXA1_IN, TXA1_OUT, TXA1_OUT_0

A0, WLAN_A0, A1, WLAN_A1

Band pass filters, FL701-708 are necessary for coexistance with DECT Phone or 3G UMTS.

U101G
BCM63168
802.11n WLAN
(7 OF 8)
IC/CPU/FCBGA-21*21mm/BCM63168

ANTENNA A0_2.4G
ANTENNA A1_2.4G

T&W ELECTRONICS	GURN5.0T142A-C		
	WLAN		
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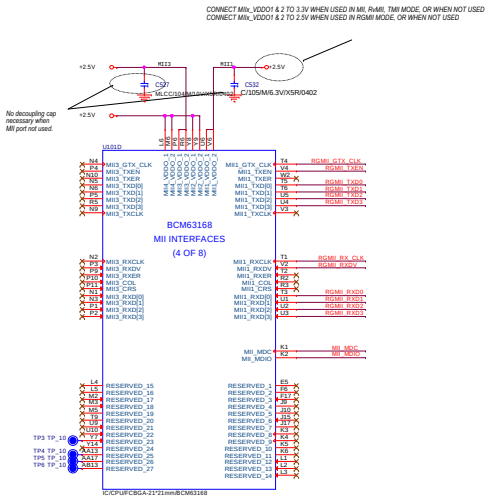
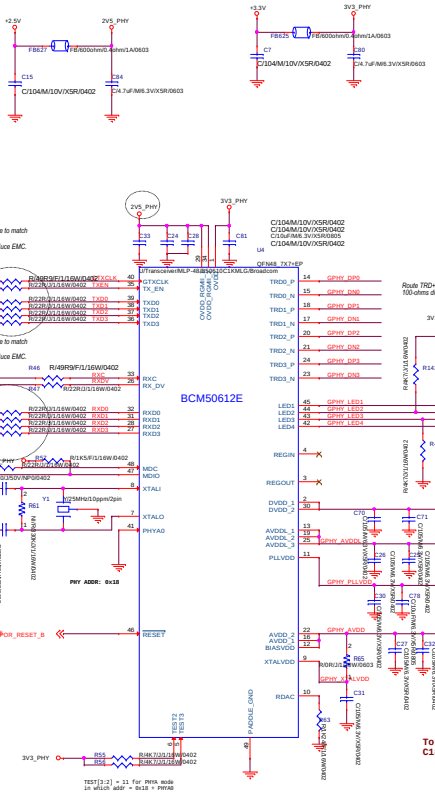
MII/TMII/RGMII - Layout Guidelines & Notes

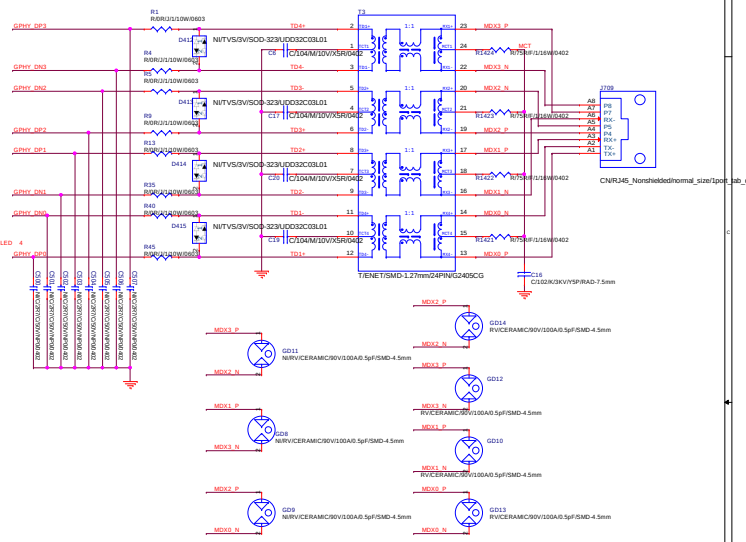
1. Route traces with 50ohm characteristic impedance.
2. Match trace lengths to a tolerance of 385 mil within TX and RX separately.
3. Keep the receive and transmit signals kept away from each other and other analog and clock signals.
4. Place capacitors and ferrite beads close to VDD traces and routes short.



MII/GMII/RGMII - Layout Guidelines & Notes

1. Route traces with 50ohm characteristic impedance.
2. Match trace lengths to a tolerance of 9.0mm.
3. Keep the receive and transmit signals kept away from each other and other analog and clock signals.
4. Voltage at VHT and CKTL to pin 46 should be the same and must match the rgmii mode selected.





RGMII LED Mode

RGMII modes can be selected by setting LED[3:2] during power on reset. Table 16 shows the various MAC interface (RGMII) modes available in the device.

Note: LED[4] = 0.

Table 16: 48-Pin MLP RGMII Mode

LED[3:2]	*MAC RGMII Mode*
0 0	RGMII 3.3V
0 1	RGMII 2.5V
1 0	RGMII HSTL 1.8V
1 1	Reserved

LOM LED Mode

LOM LED mode is a simplified LED reporting mode that uses LED[2:1] to show the operating link signal rate. Table 17 shows the definition of LED link signal rate reporting. The LOM LED can be enabled by pull-high LED[4] during power on reset.

Table 17: 48-Pin MLP LOM LED Link Signal Rate Reporting

LED[2:1]	*MAC RGMII Mode*
0 0	–
1 0	1G Link
0 1	100M Link
1 1	Others

This mode has two RGMII modes (voltage-level communicating with MAC) shown in Table 18.

Table 18: 48-Pin MLP RGMII Modes for LOM LED Operation

LED[3]	*MAC RGMII Mode*
0	RGMII 3.3V
1	RGMII HSTL 1.8V

PHY Addr	TEST[3:2]	PHYA0
0x00	00	0
0x01	00	1
0x18	11	0
0x19	11	1

B50612E PHY Address

Strap the B50612E to RGMII 3.3V mode to preserve LED configuration and allow LED4 to be compatible with IRQ (open-drain with pull-up). Software configures the B50612E to the correct RGMII mode (2.5V RGMII).

B50612E RGMII MODE SELECTION TABLE

RGMII Mode	MODE_SEL[1:0]	Pin Configuration
RGMII 3.3V	00	TEST[3:2] = 00 or 11, LED[3]=0 LED[2]=0 LED[4]=0
RGMII 2.5V	01	TEST[3:2] = 00 or 11, LED[3]=0 LED[2]=1 LED[4]=0
RGMII HSTL	10	TEST[3:2] = 00 or 11, LED[3]=1 LED[2]=0 LED[4]=0
Reserved	11	TEST[3:2] = 00 or 11, LED[3]=1 LED[2]=1 LED[4]=0
-> RGMII 3.3V	00	TEST[3:2] = 00 or 11, LED[3]=0 LED[2]=X LED[4]=1
RGMII HSTL	10	TEST[3:2] = 00 or 11, LED[3]=1 LED[2]=X LED[4]=1

X = Don't Care

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	GPHY-B50612E		
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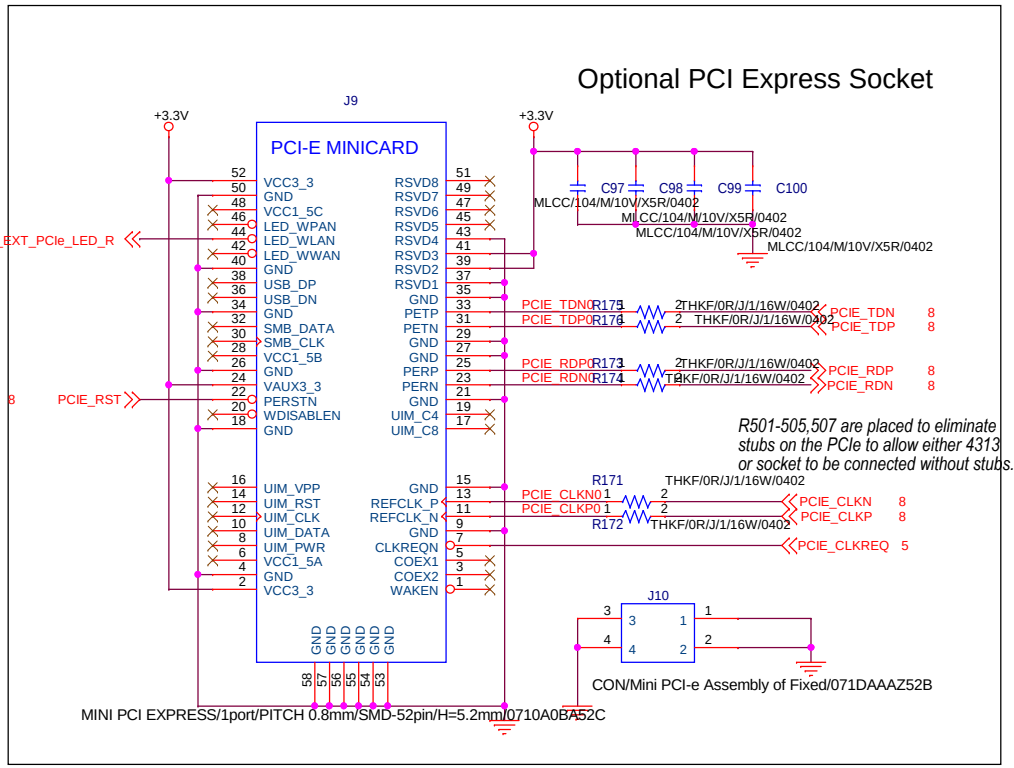

T&W ELECTRONICS	GURN5.OT142A-C			
	PCIE interface			
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