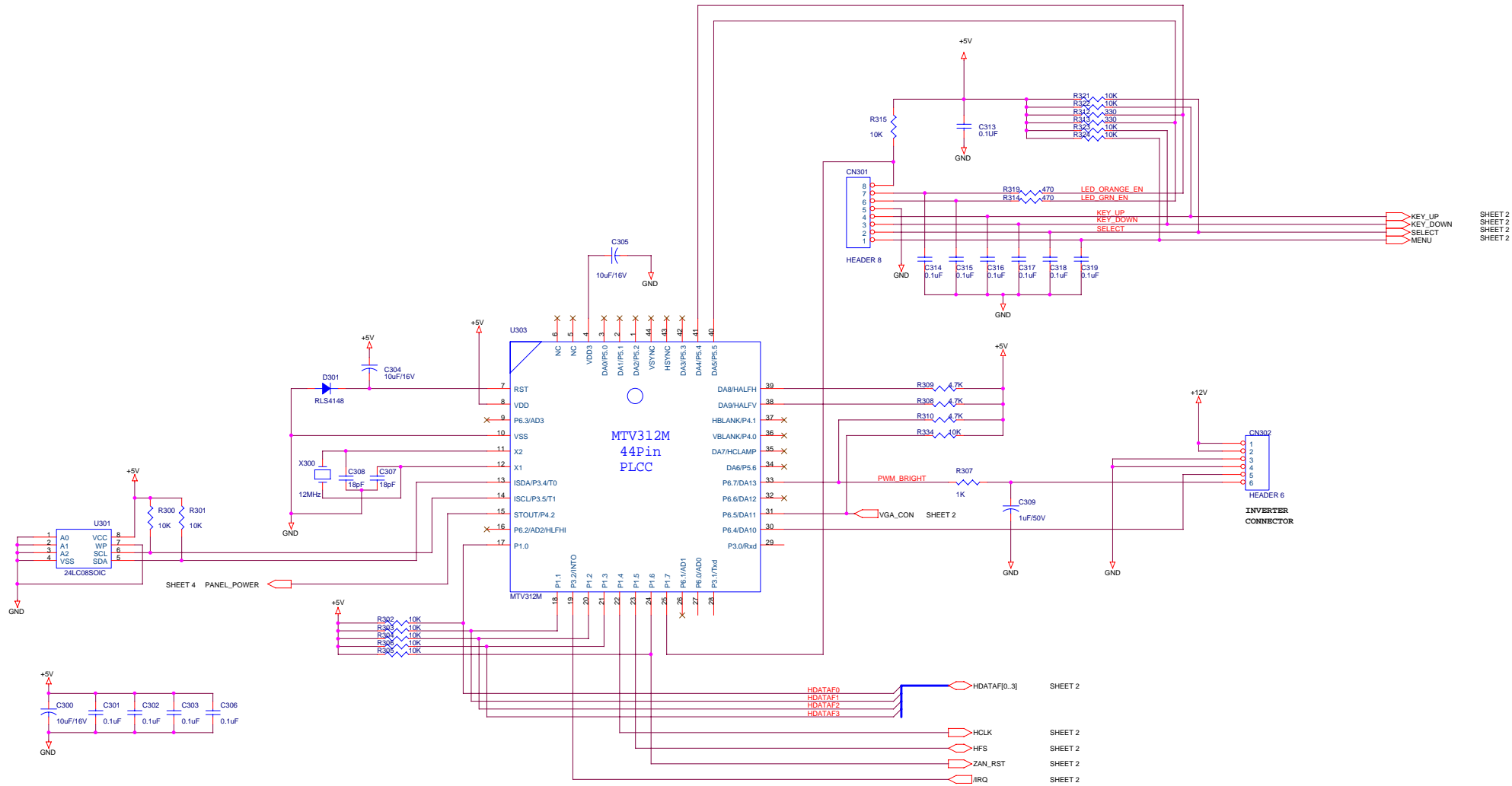


SHEET 3	HFS	HFS
SHEET 3	HCLK	HCLK
SHEET 3	HDATA0	HDATA0
SHEET 3	ZAN_RST	RESSETn
SHEET 3	IRQ	IRQ
SHEET 3	MFB0	MFB0
SHEET 3	MFB1	MFB1
SHEET 3	MFB2	MFB2
SHEET 3	MFB3	MFB3
SHEET 3	MFB4	MFB4
SHEET 3	MFB5	MFB5
SHEET 3	MFB6	MFB6
SHEET 3	MFB7	MFB7
SHEET 3	MFB8	MFB8
SHEET 3	MFB9	MFB9
SHEET 3	MFB10	MFB10
SHEET 3	MFB11	MFB11

PD0	71	ER0	ER[0..5]	SHEET 5
PD1	70	ER1		
PD2	69	ER2		
PD3	68	ER3		
PD4	67	ER4		
PD5	66	ER5	EG[0..5]	SHEET 5
PD6	65	EG0		
PD7	64	EG1		
PD8	63	EG2		
PD9	62	EG3		
PD10	61	EG4		
PD11	60	EG5	EB[0..5]	SHEET 5
PD12	59	EB0		
PD13	58	EB1		
PD14	57	EB2		
PD15	56	EB3		
PD16	55	EB4		
PD17	54	EB5		
PD18	53	OR0	OR[0..5]	SHEET 5
PD19	52	OR1		
PD20	51	OR2		
PD21	50	OR3		
PD22	49	OR4		
PD23	48	OR5	OG[0..5]	SHEET 5
PD24	47	OG0		
PD25	46	OG1		
PD26	45	OG2		
PD27	44	OG3		
PD28	43	OG4		
PD29	42	OG5	OB[0..5]	SHEET 5
PD30	41	OB0		
PD31	40	OB1		
PD32	39	OB2		
PD33	38	OB3		
PD34	37	OB4		
PD35	36	OB5		
PD36	35			
PD37	34			
PD38	33			
PD39	32			
PD40	31			
PD41	30			
PD42	29			
PD43	28			
PD44	27			
PD45	26			
PD46	25			
PD47	24			
PD48	23			
PD49	22			
PD50	21			
PD51	20			
PD52	19			
PD53	18			
PD54	17			
PD55	16			
PD56	15			
PD57	14			
PD58	13			
PD59	12			
PD60	11			
PD61	10			
PD62	9			
PD63	8			
PD64	7			
PD65	6			
PD66	5			
PD67	4			
PD68	3			
PD69	2			
PD70	1			
PD71	0			
PCLKA	44	PCLKA	SHEET 5	
PDISPE	45	PDISPE	SHEET 5	
PVS	73	PVS	SHEET 5	
PHS	74	PHS	SHEET 5	
PPWR	76			
PBUS	75			

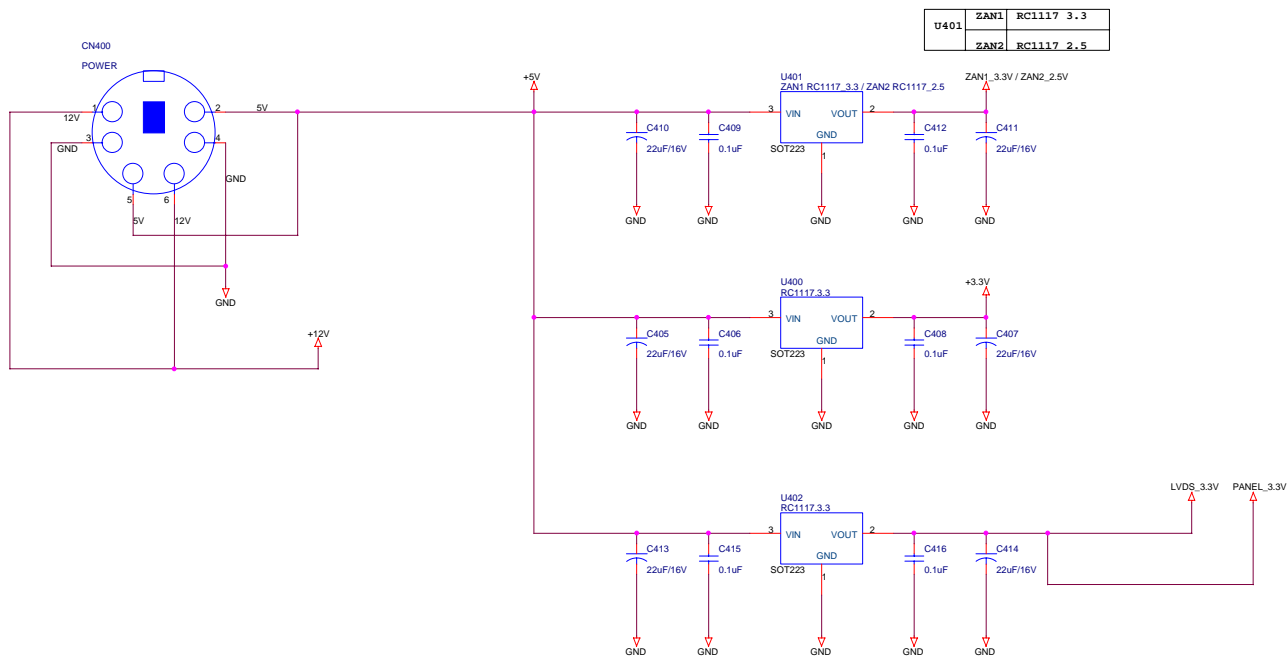
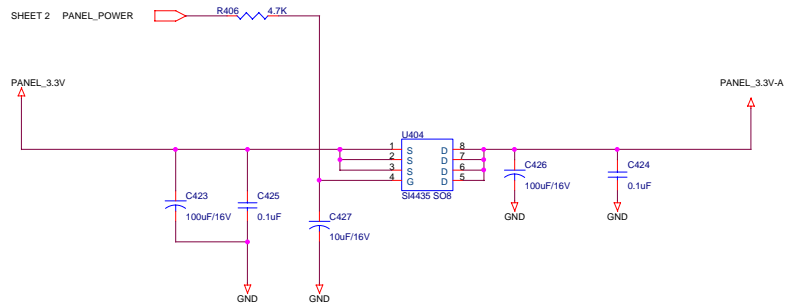
NOTE: ANALOG AND DIGITAL GROUNDS MUST BE INTERCONNECTED AT A SINGLE POINT



SHEET 2
SHEET 2
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SHEET 2

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SHEET 2

Title		3. MCU(MTV312M)	
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U401	ZAN1	RC1117 3.3
	ZAN2	RC1117 2.5

Panel Output
Damping
Network

