# RAY218　Description of Circuit

## 1. Power supply section

1-1 The equipment provided with a rated operation voltage of 13.6 dcV is allowed to operate at voltages within a range of 10.8 dcV through 15.6 dcV.
In case the input supply voltage exceeds 17.0V, the over-voltage detection circuit (D303, Q308) is actuated to cut off the POWER MOS (Q305) for the main power supply.
Erroneous reverse connection of the power supply is prevented thanks to a diode D304.

Turn on the power switch when the POWER MOS (Q305) is turned "ON" a bringing the equipment to start its operation.

## 2. Receiver section

2-1 ANT switch

After passing through the low-pass filter, the RF-signal is supplied to the High pass filter via the ANT switch.
At transmitting a signal the switch diodes (D3, D4) become conductive, while at receiving they become non-conductive.

2-2 Channels receiving section

1) RF amplifier

The RF amplifier consists of the amplifier (Q14) and a BPF (SAW filter)
Then the RF signal, having been mixed with the 1st local signal * by the 1st mixer (D17) after passed the BPF, is converted to the 1st IF signal (21.6 MHz).

*** Note :** The 1st local signal generated by a synthesizer has a frequency lower than the desired frequency by 21.6MHz.　The 1st local signal is fed to the 1st mixer (D17) after being amplified by the buffer amplifier (Q5).

2) 1st IF

The 1st IF signal of 21.6 MHz supplied via the crystal filter (F2A,F2B) is amplified by the 1st IF amplifier (Q19)

3) 2nd IF

The 1st IF signal, having been mixed with the 2nd local signal (21.145 MHz) in the

IC (IC8.... Mix, Osc, Amp, Limit, Det) for the 2nd IF, is converted into the 2nd IF signal with a frequency of 455 kHz.
Further, after subjected to amplification and successive amplitude limitation via the ceramic filter (F3), the signal is demodulated by the Quad detector (quadrature detection) into an audio signal.

4) De-emphasis

An audio signal is subjected to a correction in the frequency characteristic to a -6 dB/oct by the de-emphasis circuit (IC9).

5) Squelch

The high-frequency noises outside the voice band among the DISC outputs are converted into a De-voltage by the detection circuit after amplified with the noise amplifier (IC8).
Then, the converted voltage is further amplified by the DC amplifier (IC9) to be a BUSY1 signal, which is fed to the squelch control port (A/D).
The operation level of the squelch is determined according to the electronically controlled volume (IC302) and the set value for the A/D action of the CPU, respectively.

## 3. Transmitter section

3-1 IDC (Instantaneous Deviation Control)Circuit

The microphone and DSC signals from the control system are supplied to an amplitude limiting circuit after subjected to pre-emphasis of a 6 dB/oct in the IDC circuit (IC301).
Further, the signals, having been modulated through passing the fifth low-pass filter for splatter prevention, is supplied to the VCO.
Maximum Frequency Deviation is set with the electronic volume (IC 302).

3-2 Buffer driver amplifier

The carrier frequency from the VCO is supplied via the diode switch (D7) to the buffer (Q4). The carrier is then amplified up to about 50 mW, finally boosted to 25 W by the RF -amplifier (IC1) at the final stage.
The transmitting power is supplied to the antenna by operating the ANT switch (D3) via the LPF.

3-3 APC circuit

After subjected to DC-detection in the detection circuit (D2), the transmitting power is compared with the standard set value of the output at the comparator circuit (IC2). This output controls both the PA comparator circuit (IC2) so that a stable transmitting power may be supplied to the ANT. The switch-over of the power between 25 W and 1 W is effected with the output change-over switch (IC2) The transmitting power is set by CPU (IC 407).

## 4. PLL circuit

The standard frequency 12.8MHz for the PLL is oscillated and de-multiplied into 25 kHz (= 1/850) by the PLL IC (IC5).

The oscillation frequency of the VCO, which has been de-multiplied into 25 kHz being same as the standard, is subjected to phase comparison by a phase comparator within an IC5, then a pulse output corresponding to the deviation is produced. The output pulse is converted into a DC value through the charge pump circuit (Q11 and Q12) externally installed and a loop filter, thereafter as a frequency control voltage it is supplied to the control terminal of the VCO.

A part of the output from the VCO is fed back to the PLL IC (Fin) via the buffer amplifier (Q13).

The loop filter is provided with a time-constant changeover-switch using the IC4 to meet the requirement for high-speed response by accelerating the rise characteristic at the time of transmission/ reception change-over and frequency change-over. Thanks to the detection circuit (IC6), the PLL unlocking signal can be output free from fluttering.

## 5. AF control section

5-1 AF selection

AF signals (RxAF, FOG, Hail) are selected by the AF selector (IC305).

5-2 Line selection

The microphone and the DSC signal or the IDC input (modulation input) are selected by the line selector (IC305).

## 6. RAYMIC I/O

To connect with the RAYMIC circuit such an interface unit is provided that is suitable for both audio and digital applications.

### 6-1 Audio I/O

Between the equipment main and the Raymic transmission of an AF signal is made in a low impedance circuit via a buffer circuit effected by the operational amplifier (IC305 ,IC301).

### 6-2 Digital I/O

With the anti-noise characteristics taken into consideration, the telecommunication of a control data is effected using the buffer(IC405).

## 7. NMEA I/O

The section composes a basic interface for signal reception using the photo -couples (PC401).

# RAYMIC

## Operation Overview of The Circuit's Function

### 1. Outline

The RAYMIC is connected to Base Unit via 10m cable. The Raymic performs all operations except Turning ON/ OFF of the power supply. LCD is used for the Display of the Raymic with a back-light furnished. The Distress switch in normally illumined state is provided with a dedicated protective covers.

### 2. Circuit constitution

The circuit consists of the following components：

* Power supply system circuit
  - Digital system +3.3V Voltage Regulator (IC 601)
  - Analog system +10V Voltage Regulator (Q601)
* Single Chip CPU (IC 608)
* LED Driver Circuit (Q605,606,607)

### 3. Power supply system

The input voltage of the main supply power is +13.6 V.
The internal operation voltages for the respective applications are as following：+3.3V by the voltage regulator (IC601) for CPU.

### 4. CPU

A single-chip micro computer- $\mu$ PD78F0515 (IC608).

### 5. Controller・driver for LCD display

The LCD display is controlled by an integrated circuit S6A0094, which is assembled on the LCD substrate.

### 6. LED driver circuit

Lighting (luminosity) of LCD can be changed-over in 10 levels by switching with Q605, Q606 and Q607, respectively.

### 7. Electronically-controlled volume

The receiver's sound volume on the hand-set is controlled by the IC608 and IC 605.