Digital IF PCB Circuit description

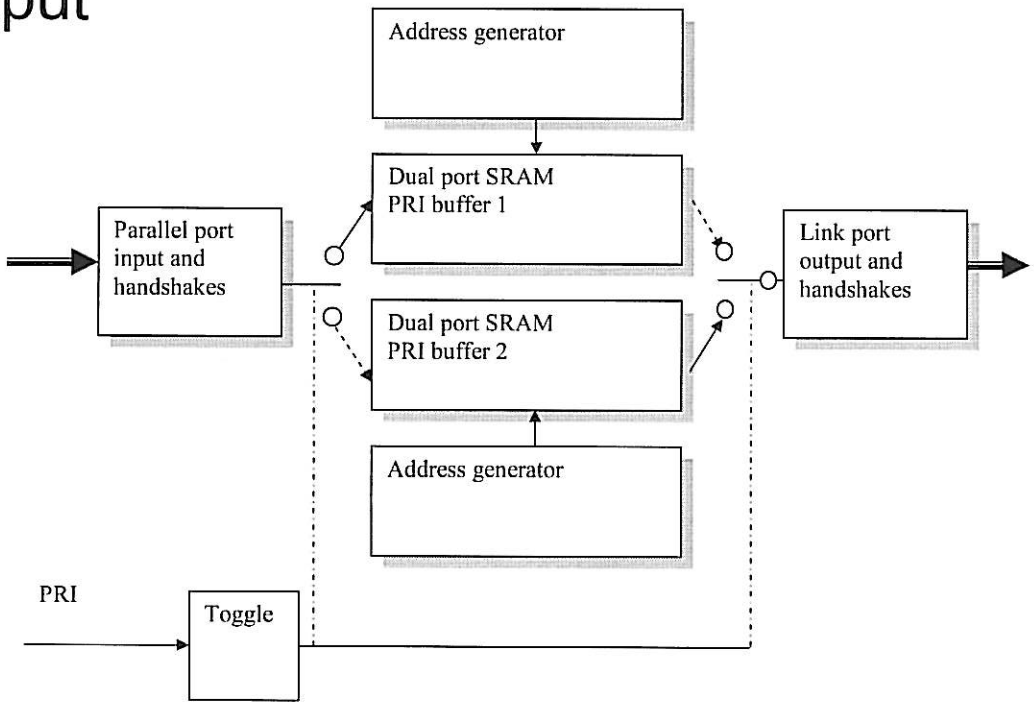
- Digital Filter
  - ADC converters analogue signal to digital
  - Parallel channels of mixing and filtering
  - Mixer mixes with quadrature Numerically Controlled Oscillator (NCO) to produce complex (I,Q) samples at baseband
  - Multiple filter stages to provide matched bandwidth
  - Parallel busses to FPGA for filter samples (I, Q)

Function of the FPGA

- Receives timing and control signals from Modulator (EARLY_PRI, LongRange)
- Produces PRI (synchronised to ADC sampling clock)
- Parallel input busses for baseband Sample data from digital filter
- Buffers sample data and converts from IQ to Magnitude/ Phase
- LVDS link port for magnitude data to DSP
- SPI bus interface to tuning DAC Two I2C busses for EEPROM and sequencer
- UART interface to modulator
- GPIO for reception and interlock of SHP AZI etc
  - Interrupt generator
- Parallel bus for STC/TVG DAC control. Double data rate

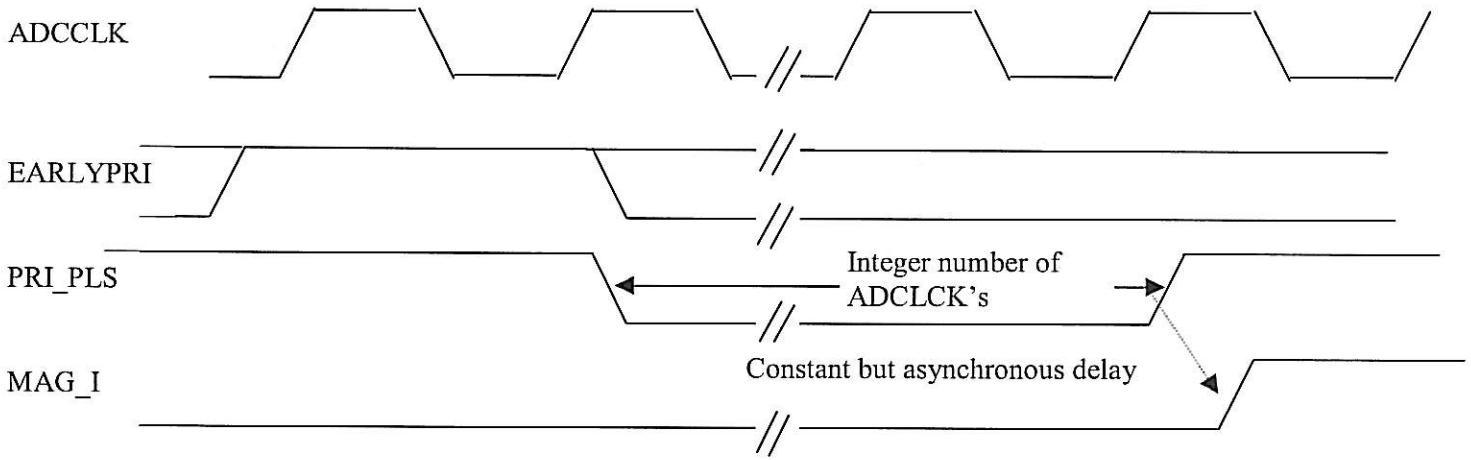
Function of the FPGA

- Buffers sample data and converts rate from peak to on parallel port input average rate on Link Port output



Function of the FPGA

- Produces timing control signals



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DSP

- Digital Signal Processor
- Analog Devices Tiger Sharc
- 100MHz external 32 bit data bus
- 500 MHz, 2.0 ns instruction cycle rate
- Floating and Fixed point - Single-precision IEEE 32-bit and extended-precision 40-bit floating-point data formats and 8-, 16-, 32-, and 64-bit fixed-point data formats 12M bits of internal—on-chip—DRAM memory
- Dual-computation blocks—each containing an ALU, a multiplier, a shifter, and a register file
- Dual-integer ALUs, providing data addressing and pointer manipulation
- Integrated I/O includes 14-channel DMA controller, external port, four link ports, SDRAM controller, programmable flag pins, two timers, and timer expired pin for system integration

Digital IF PCB Circuit description

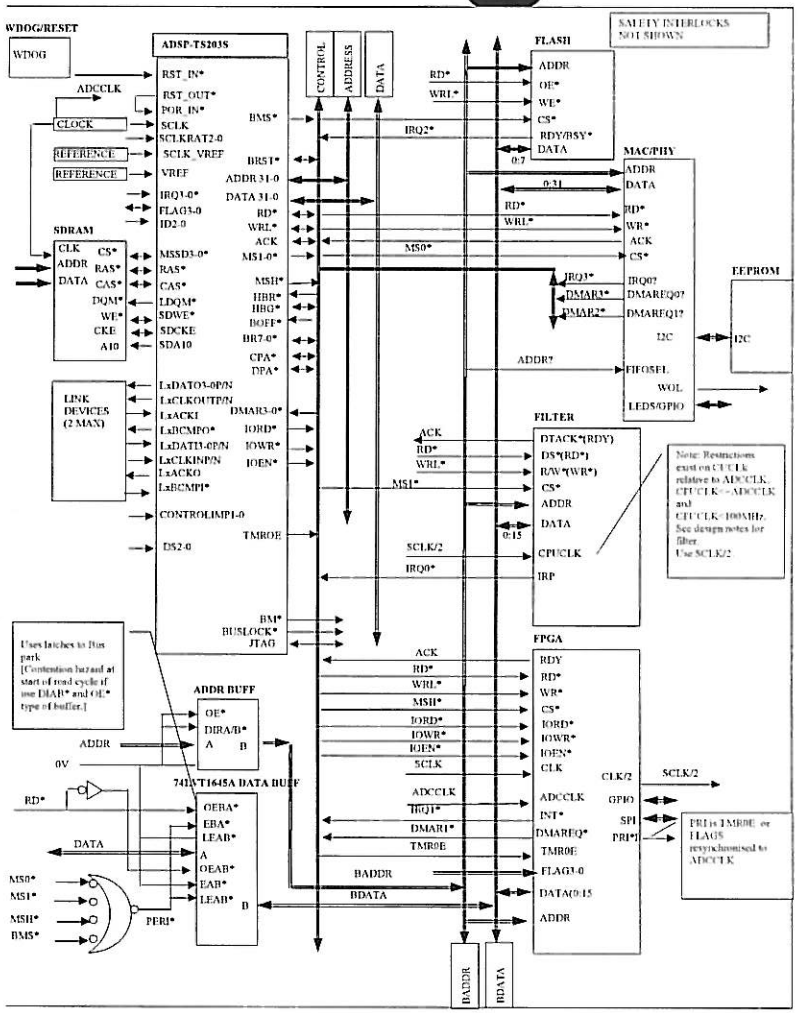
- Ethernet LAN IC
  - 100MBit Ethernet MAC and PHY
  - Always powered when supply connected
  - Low power state when waiting for Wake-up packet
  - Wake-up on LAN controls main modulator PSU via PSU sequencer
- Ethernet connector contains Ethernet magnetics

Digital IF PCB Circuit description

- Memory
  - SDRAM two 16Mbyte device fitted
  - FLASH for non-volatile program storage
    - Contains Boot code, Application and FPGA configuration
    - Boot sector locked in hardware
  - Serial I2C EEPROM for configuration data and PCB serial number

Digital signals

See Block-detail_E.doc



Ribbon cable signals

Pin	Type	Level	Name	From/to	Function	
1	SUPPLY IN		+26VIN		Supply	
2	GND	CHASSIS	GND			
3	IN LOGIC	0/3V3 Totem pole. Tri-stateable	EARLY_PRI	IO [inp] of FPGA and FLA	Active low, trailing (rising) edge triggers pulse	Strong pull up on IF, strong pull up to 3V3 on mod
4	SUPPLY IN		3V3IN		Supply	
5	SUPPLY IN		3V3IN		Supply	
6	SUPPLY IN		3V3IN		Supply	
7	SUPPLY IN		3V3IN sense		Supply	Connect to 3V3 via 100R on mod
8	SUPPLY IN		3V3STNDBY		Supply	
9	GND	CHASSIS	GND			
10	SUPPLY IN		-5VIN		Supply	
11	SUPPLY IN		+5VIN		Supply	
12	SUPPLY IN		+12VRAW		Supply	
13	SUPPLY IN		+12VRAW		Supply	
14	GND	CHASSIS	GND			
15	BI LOGIC	0/3V3 Totem pole. Tri-stateable	PRI_PLS	nPRI [out] of FPGA	Active low, trailing (rising) edge triggers pulse	Weak pull down on IF, strong pull up to 3V3 on mod
16	GND	CHASSIS	GND			
17	BI LOGIC	0/3V3 O/C	PWRFAIL*	IO [inp] of FPGA	Active low	Weak pull down on IF, strong pull up to 3V3 on mod
18	OUT LOGIC	0/3V3 O/C	MOTOR_EN	IO [inp + o/c out] of FPGA	Active high motor enable	Weak pull down on mod, strong pull up to 3V3 on IF
19	IN LOGIC	0/3V3 totem	LONGRANGE	LONG [inp] of FPGA and F	Active high long range. Synchronises pulse length to correct FPGA buffer. Long range is set by Mod board just after rising edge of PRI, and read by the FPGA on the IF board on the rising edge of EarlyPRI	Weak pull down on IF, strong pull up to 3V3 on mod
20	BI LOGIC	0/3V3 O/C	SHP_IN	IO [inp] of FPGA	SHP only mark. Heading mark - '0'	Weak pull down on mod. Strong pull up on IF to 3V3
21	IN LOGIC	0/3V3 O/C	AZI	IO [inp] of FPGA and FLA	Active low AZI/SHP Heading mark - '0'	Weak pull down on mod. Strong pull up on IF to 3V3
22	OUT LOGIC	0/3V3 O/C	RADAR_TX_EN	IO [inp + o/c out] of FPGA	Active high transmit enable	Weak pull down on mod, strong pull up to 3V3 on IF
23	OUT LOGIC	0/3V3 totem	REMOTE_SW+	Monitor chip	Active high main PSU enable	Weak pull down on mod, strong pull up to 3V3STNDBY on IF
24	OUT LOGIC	0/3V3 totem	IFTXD	TX DATA of FPGA	Async serial IF TX data CMOS level	Idle = Mark = logic 1 = 3V3. Start bit = space = '0',
25	GND	CHASSIS	GND			
26	IN LOGIC	0/3V3 O/C	IFRXD	RX DATA of FPGA	Async serial IF RX data CMOS level	Idle = Mark = logic 1 = 3V3. Start bit = space = '0',

Note: In and out defined from the perspective of the IF PCB

Glossary of signal names -example

For full list see Signal_names.xls

PB14	Parallel data bus from digital filter to FPGA	Only used in dual range
PB15	Parallel data bus from digital filter to FPGA	Only used in dual range
PBACK	Parallel data bus Acknowledge - FPGA to digital filter	Only used in dual range
PBCH0	Parallel data bus Channel indicator - digital filter to FPGA	Only used in dual range
PBCH1	Parallel data bus Channel indicator - digital filter to FPGA	Only used in dual range
PBCH2	Parallel data bus Channel indicator - digital filter to FPGA	Only used in dual range
PBGAIN	Parallel data bus Gain indicator - digital filter to FPGA	Only used in dual range
PBIQ	Parallel data bus Inphase (not quadrature) indicator - digital filter to FPGA	Only used in dual range
PBREQ	Parallel data bus request - digital filter to FPGA	Only used in dual range
PCLK	Parallel bus clock - digital filter to FPGA	
PME	Watchdog and Wake-up on LAN indicator (normally 1Hz square wave)	
PREAMP OUT	Pre-amplifier output - analogue signal 70MHz	
PRI_PLS	Magnetron firing pulse demand - rising edge trigger to modulator PCB	
PWRFAIL*	Power fail. Open collector active low. Either PCB can de-assert	
RADAR_TX_EN	Transmit enable. Open collector active true. Either PCB can de-assert	
RAS*	Row address strobe to DRAM	
RD	Read strobe active high	
RD*	Read strobe active low	
RDAC_PIN OUTB	Gain control DAC output - analogue signal - inverse of that used by PIN attenuator	
RDAC_VGA OUTB	Gain control DAC output - analogue signal - inverse of that used by VGA	
RDAC1CLK	Gain DAC clock	
RDAC1DAT0	Gain DAC data bus	
RDAC1DAT1	Gain DAC data bus	

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Clocks

- SCLK – 100MHz produced by crystal oscillator module used for DSP bus and by DSP to generate 500MHz core clock
- ADCLK - 57MHz produced by crystal oscillator module used by digital filter for sampling
- PCLK – 99.75MHz Digital Filter uses PLL to produce = 57MHz *7/4. Parallel bus speed
- LVDS bus clock. 50MHz Produced by FPGA by dividing down SCLK. LVDS clock does not run all of the time

Parallel bus PA(0:15) and PB(0:15)

- I and Q sample data connection digital filter to FPGA

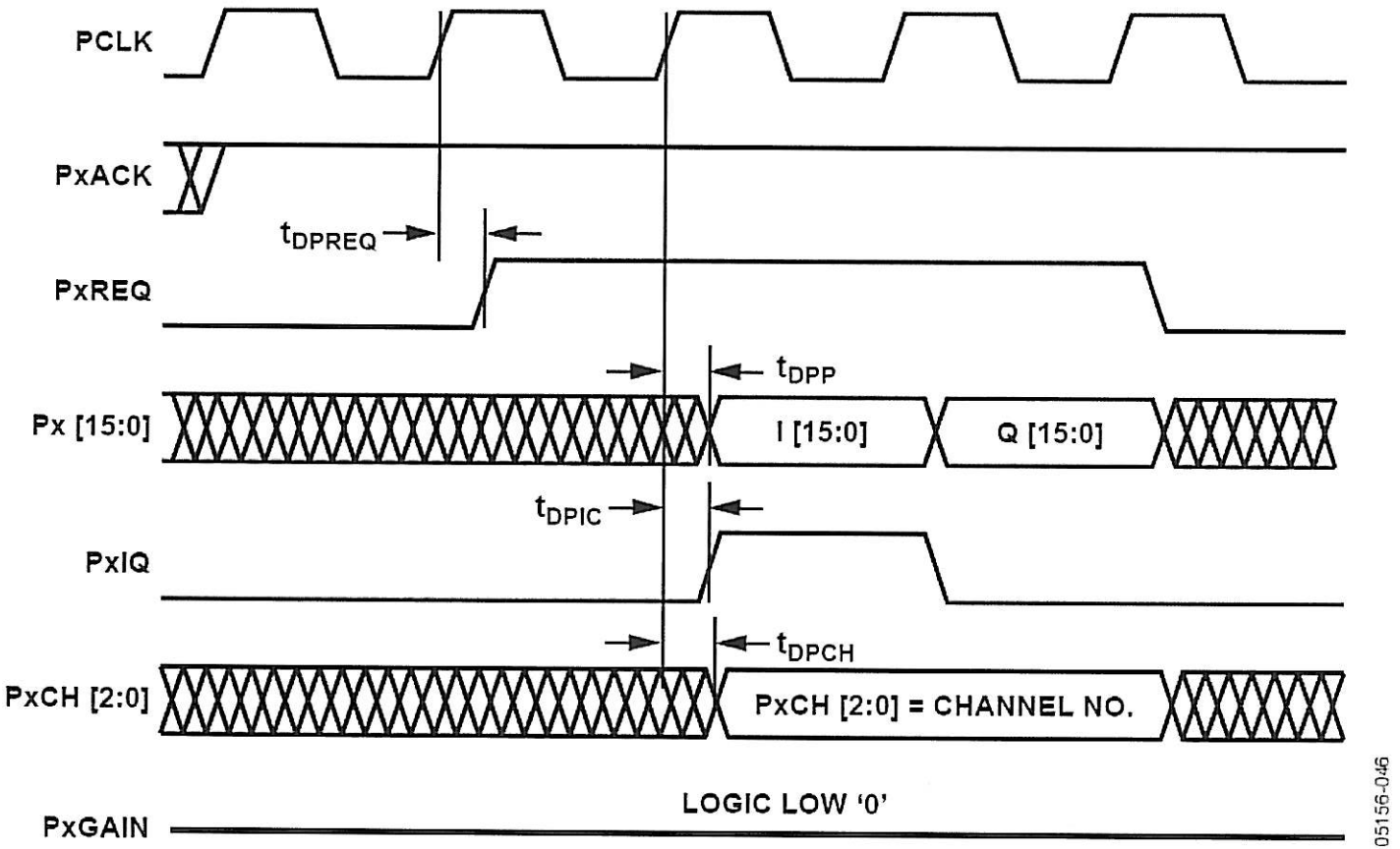

Figure 57. Interleaved I/Q Mode Without an AGC Gain Word

Link Ports LXDATI(0:3)_P (or N) – Differential pairs of LVDS signal buffered sample data from FPGA to DSP

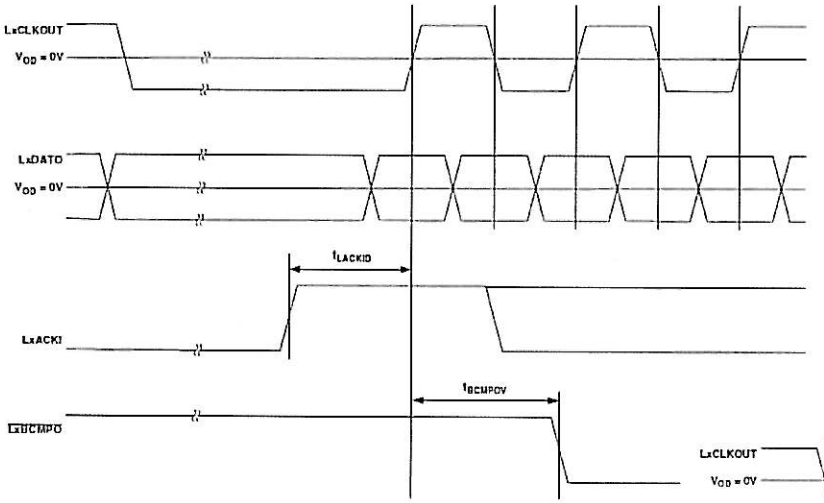

Figure 20. Link Ports—Transmission Start

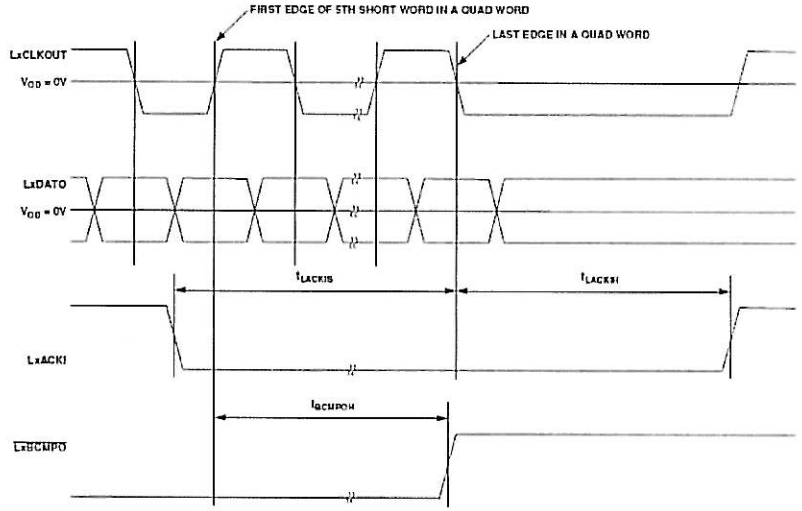

Figure 21. Link Ports—Transmission End and Stops

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DSP Bus

- 32 bit Data
- 24 bits of address. Unusually the address is a long word address, i.e. A(0) increments on 32 bit boundaries. Note the unusual connection of addresses to peripherals
- Low speed peripherals connected to buffered Address and Data busses
- Data bus buffers latch data to "Park" the buffered side in a known state when not in use. Prevents high dissipation in input buffers of CMOS parts
- Address and Data busses also used for SDRAM, when the address is multiplexed as Row and Column address and strobed into the SDRAM using RAS and CAS

Booting, Sleeping and waking

- First application of power only – PSU Sequencer and LAN chips reset themselves when +3V3_STBY supply comes up
- Then
  - When power is applied PSU sequencer starts all supplies and resets DSP and Digital Filter
  - DSP runs boot loader from FLASH
  - FPGA loaded
  - Loads application program
  - Start Ethernet communication with display if there is one
  - If no display, application prepares LAN chip for Wake-up on LAN
  - LAN chip signals to PSU sequencer (via PME) to shutdown all but sequencer and LAN chip
  - Sequencer shuts down modulator PSU
  - LAN chip receives Wake-up packet
  - Above sequence starts again
- If external power removed, then whole sequence restarts

Power supply sequencer - Function and operation

- Sequences the internal power supplies in accordance with the manufacturers specification. Both on the way up and on the way down
- Verifies supplies are within +/-5% tolerance (Beware - +3V3 Standby supply not measured for over-voltage)
- Performs system reset function – double reset needed by digital filter IC
- Performs watchdog function – if toggled once, then PME must change every 500ms +/-100ms or the board will shutdown
- Controls main PSU via Remote_Switch+
- Sequences Wakeup-on-LAN function

Tuning

- "Tune offset" measured in core site FATE, stored in EEPROM
- Tune DAC controls tune voltage to LNC
- Main bang amplitude measured
- Coarse tune finds rough tuning
- Fine tune seeks accurate tune
- On short ranges tuning "dithers" around this voltage to constantly check fine tuning
- If range change or main bang amplitude falls too much then sequence restarts
- On Long ranges "tune offset" applied
- Periodically removes "tune offset" and seeks fine tune
- If range changes or main bang amplitude falls too much then sequence restarts