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Digital IF

Assembly: 4610-016-xx

Description

2007

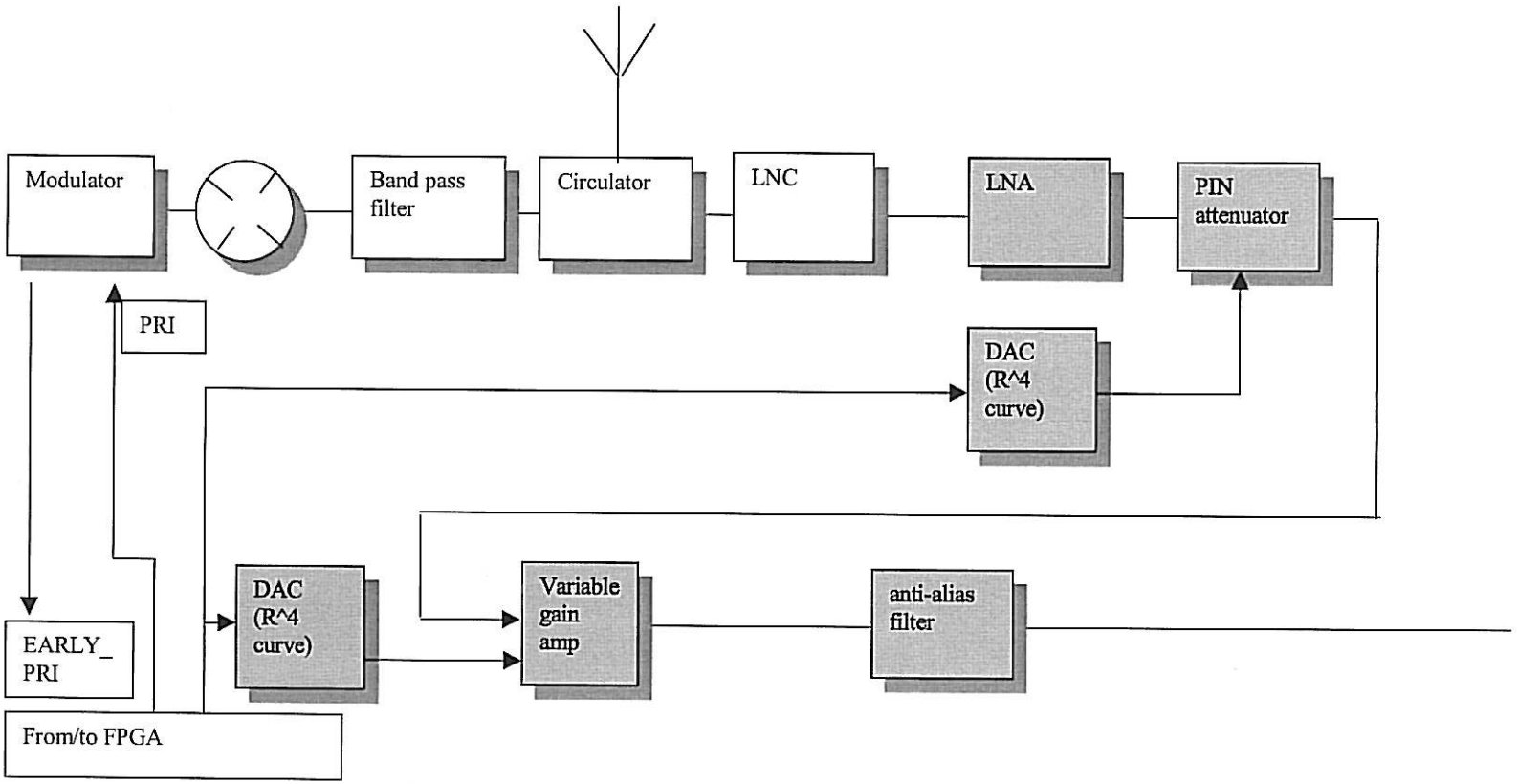
Part Numbers and Current and Recent Revisions

Title	Digital IF
No.	4610-016
Product	New Generation Scanners

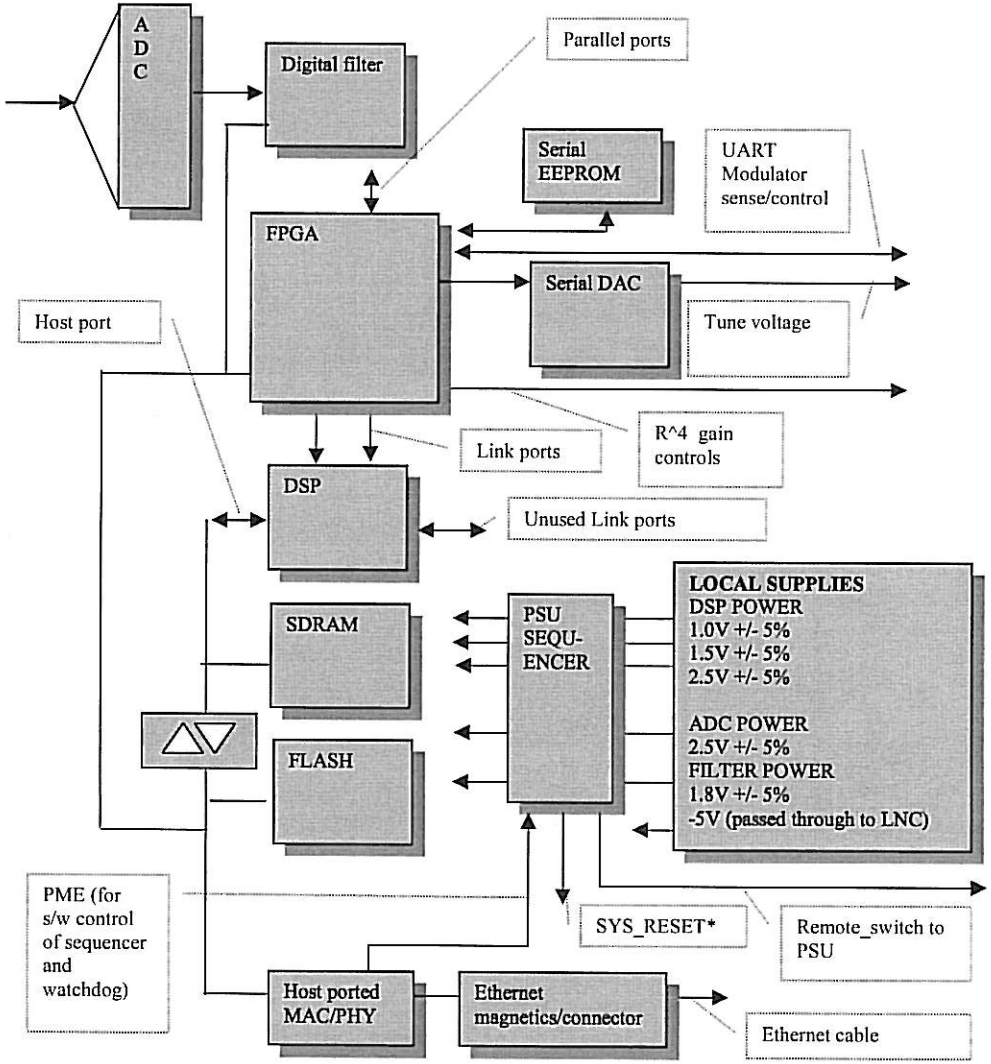
		Drg/Part/File No.	History Revision Status	History Revision Status	History Revision Status
Owner	PCB Assembly Control Revision	4610-016	G		
	Last Updated		07/02/2007	13/02/2007	14/05/2007
PCB Design	PCB Assembly Drawing	4610-016	F	G	H
Mech. Design	IDF	3015-380	384d_ideas_v11	384d_ideas_v11	384d_ideas_v11
PCB Design	PCB Artwork/Gerber data	3015-384	E	E	E
PCB Design	Circuit Diagram	4610-007	F	G	H
Manf. Eng Mgr	Manman Surface Mount BOM	4610-016SM	n/a	n/a	n/a
Manf. Eng Mgr	Manman Manual Place BOM	4610-016	n/a	n/a	n/a
PED SM Engr	Surface Mount P&P File - Top	4610016_top	n/a	n/a	n/a
PED SM Engr	Surface Mount P&P File - Bot	4610016_bot	n/a	n/a	n/a
Test Engr	ATE Program File	4123123	n/a	n/a	n/a
Test Engr	Functional ATE (FATE) File	4123123	n/a	n/a	n/a
Software Engr	Software Version				
Software Engr	Software Checksum				
Software Engr	Software Label				
	Change ECO/Eng. Dev. Status		Repanelisation only	4610-016_006	4610-016_007

Block Diagram (1)

Analogue stages – IF parts in green



Block Diagram (2)



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Matched Bandwidth, Sampling and Nyquist

- The optimum bandwidth for a rectangular pulse is BW= 1/T e.g. 1usec pulse BW=1MHz
- Nyquist did NOT say that the sampling rate must be twice the input frequency for information not to be lost. He DID say it must be more than twice the Bandwidth
- When sampling at less than twice the frequency, then the information is aliased to a new frequency centred at the difference.
- Think of it as mixing (multiplying) the input signal with an impulse at the sample frequency. Gives sum and differences
- This is called under-sampling
- Lowers cost of ADC and reduces the hardware cost

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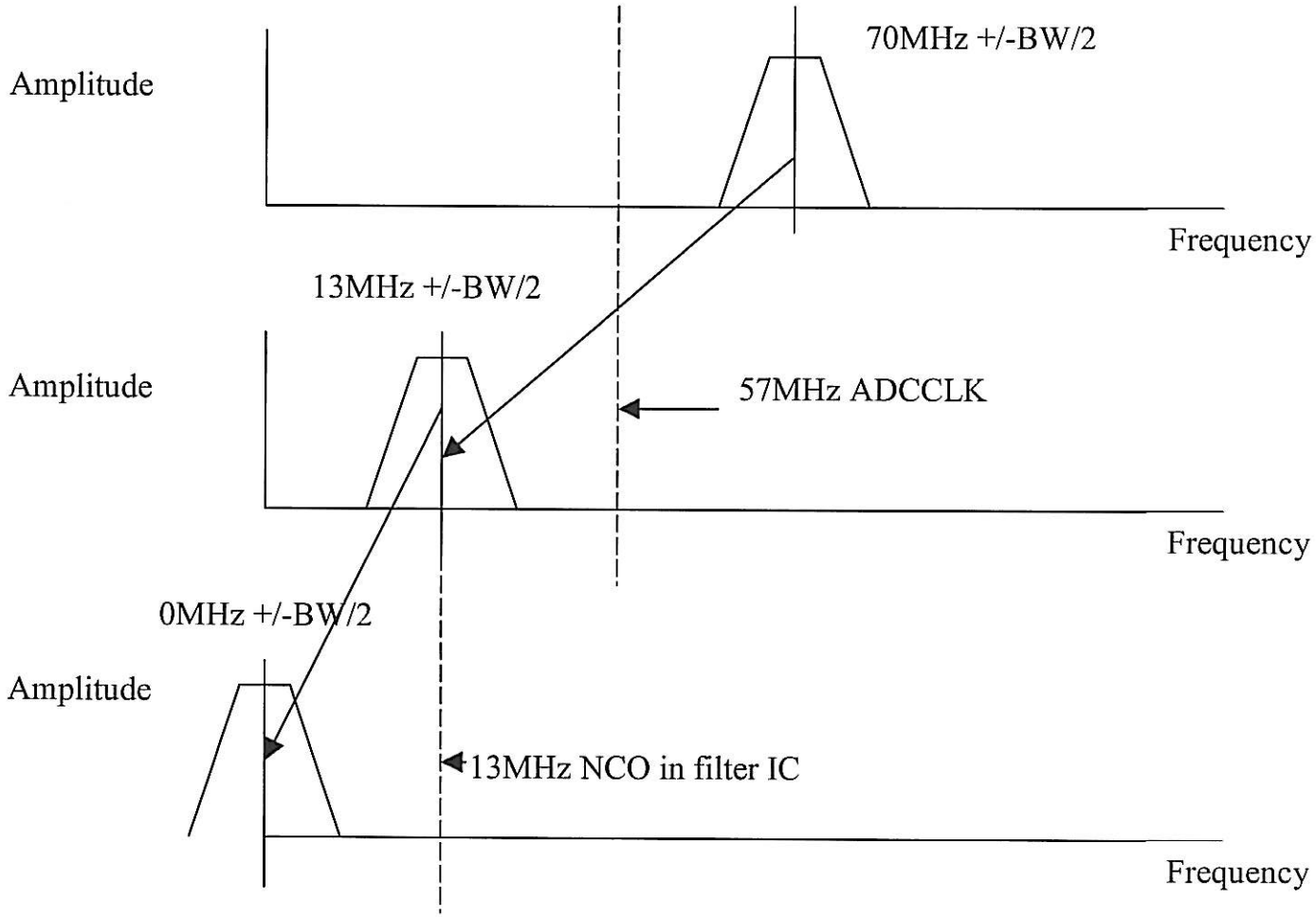
Sampling and down conversion

- Input signal to ADC is amplified 70MHz
- We need to extract the baseband amplitude signal
- Incoming signal is centred at 70MHz and has a bandwidth (BW) = 1/(pulse width)
- Down conversion – 2 stage process
- (1) undersampling with 57MHz aliases to 13MHz
- (2) Mixing with 13MHZ NCO in digital filter IC converts to complex baseband

Down conversion – 2 stage process



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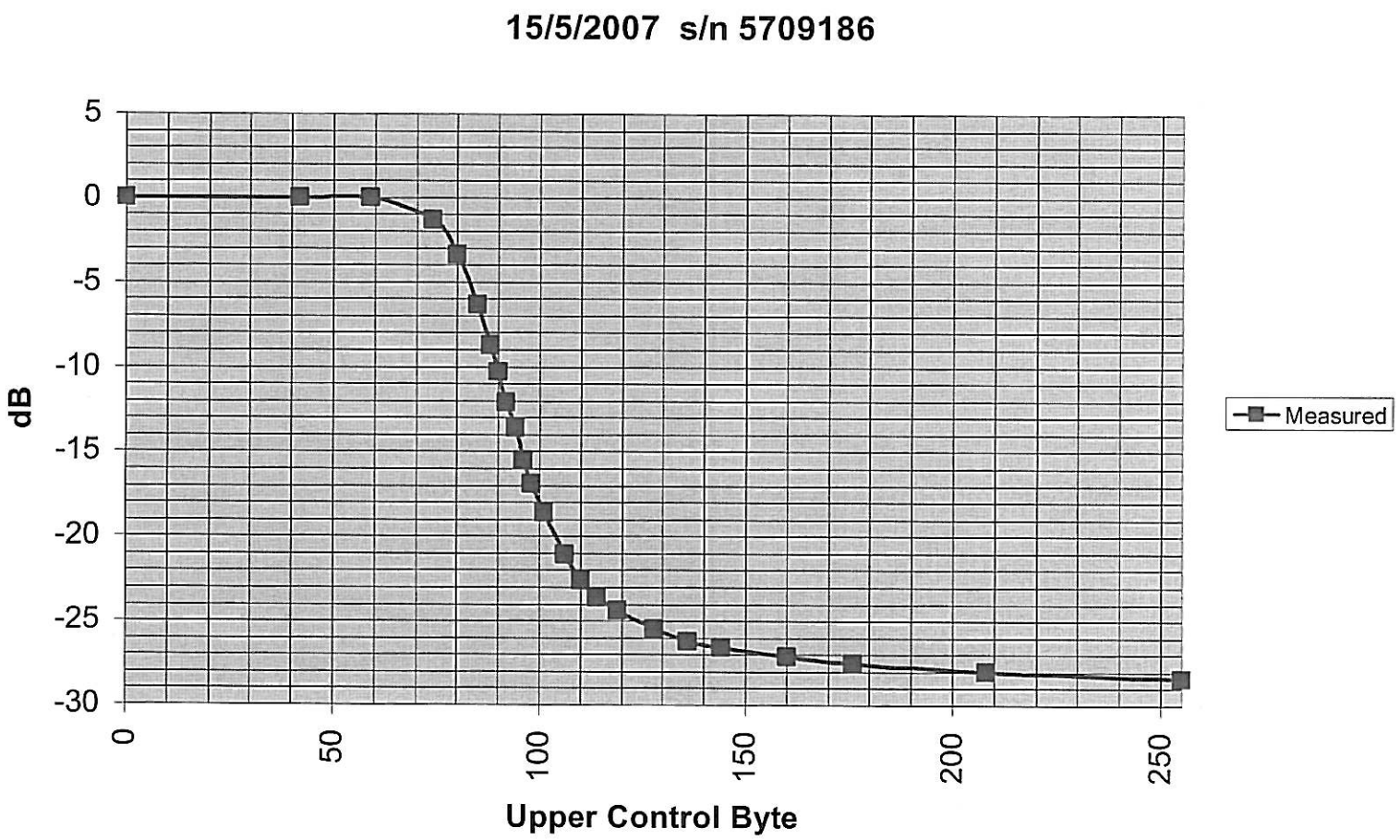
Gain

- Provide for correction of R^4 variation of amplitude targets with Range
- Provides calibration of required gain
- Two analogue gain control stages
- Pin diode attenuator
  - Highly non linear voltage to dB
  - Calibrated at IF FATE
- Variable gain amplifier
  - Linear voltage to dB

Pin Diode Attenuator calibration – every PCB has its own curve measured in IF FATE



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Schematics

Circuit description by reference to the schematics

Digital IF PCB Circuit function

- IF PCB assembly converts incoming low level IF to "Spoke data"
- Spoke Data sent as Ethernet packets
- Spoke data is the received signal amplitude as a function of Range and scanner azimuth angle (AZI)
- Display converts spoke data into Plan view (PPI)
- AZI measured relative to Ships heading marker (SHP)
- Status packets
- Command packets received from display(s) control rotation, transmission and range (PRF and PW)
- Extensive built in self-test (BIST) and interlocks for safe operation

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Digital IF PCB Circuit description

- Power
- Clocks
- LNA, PIN attenuator, VGA and tuning
- Anti-alias filter
- Digital Filter
- FPGA
- DSP
- Ethernet MAC
- Memory

Digital IF PCB Circuit description

- Power supplies
  - Sequencer IC controls the sequencing and monitoring of all supplies except –5V
  - +3.3V standby is on all the time the scanner is powered and powers the supply monitor/sequencer and LAN chip for power-on over LAN
  - +3.3V, +5V, -5V received directly from modulator PSU
  - Other supplies generated on board by linear or switching regulators for internal core voltages and I/O

Digital IF PCB Circuit description

- LNA, VGA and tuning
  - Input signals are received from the separate Low Noise Converter (LNC)
  - Amplified by Low Noise Amplifier (LNA)
  - Attenuated by PIN diode to provide range dependant attenuation at short ranges. Controlled by a DAC
  - Further amplified by Variable Gain Amplifier (VGA). Controlled by a DAC. Range dependant gain at longer ranges. Serial bus tuning DAC generates control voltage to a vari-cap tuner in the LNC.
  - Tuning voltage amplified and shifted for correct range for vari-cap ~(+4 to +24V)