

Model: T7004  
FCC ID: PIYT7004T1

## **Technical Description**

### **General**

During the normal operation, the dog tag will collect the motion and sound data and then send to dongle every 2 minutes. The middleware (a PC program) will convert a set of received data into a message and post on the Twitter website.

The ball and Mic sensor is used to detect dog's movement and bark sound respectively. The MCU of dog tag will collect both sensors' status for 2 minutes and then send it to the dongle. Upon receiving the data from the dog tag, the dongle will flash the LED one time and then reply an ACK (acknowledgement) signal to the dog tag to confirm the reception. If the ACK signal is received, the dog tag will start to collect both sensors' status again for 2 minutes again.

### **RF**

The RF part consists of one single chip, model: MRF49XA. The MRF49XA is a low-power, Zero-IF, multi-channel FSK transceiver. All the RF and baseband functions and processes are integrated in the MRF49XA. The device for its operation requires only a single, 10 MHz crystal as a reference source and an external, low-cost host microcontroller. The MRF49XA supports the following functions:

- Reset
- Power Amplifier and Low Noise Amplifier
- Synthesizer (PLL, VCO and Oscillator)
- I/Q Mixers and Demodulators
- Baseband Filters and Amplifiers
- Received Signal Strength Indicator
- Low Battery Detector
- Wake-up Timer/Low Duty Cycle Mode
- Data Quality Indicator

**Channel number and frequency table:**

<b>Ch</b>	<b>Center Freq (Mhz)</b>	<b>Ch</b>	<b>Center Freq (Mhz)</b>
<b>6</b>	908.65	<b>14</b>	915.85
<b>7</b>	909.55	<b>15</b>	916.75
<b>8</b>	910.45	<b>16</b>	917.65
<b>9</b>	911.35	<b>17</b>	918.55
<b>10</b>	912.25	<b>18</b>	919.46
<b>11</b>	913.15	<b>19</b>	920.35
<b>12</b>	914.05	<b>20</b>	921.25
<b>13</b>	914.95	<b>21</b>	922.15

Channel spacing = 0.9 MHz.



# MRF49XA

## ISM Band Sub-GHz RF Transceiver

### Features

- Fully Integrated Sub-GHz Transceiver
- Supports Proprietary Sub-GHz Wireless Protocols
- 4-Wire Serial Peripheral Interface (SPI) Compatible Interface
- CMOS/TTL Compatible I/Os
- Clock and Reset Signals for Microcontroller
- Integrated 10 MHz Oscillator Circuitry
- Integrated Low Battery Voltage Detector
- Supports Power-Saving Modes
- Operating Voltage: 2.2V-3.8V
- Low-Current Consumption, Typically:
  - 11 mA in RX mode
  - 15 mA in TX mode
  - 0.3  $\mu$ A in Sleep mode
- Industrial Temperature Range
- 16-Pin TSSOP Package

### RF/Analog Features

- Supports ISM Band Sub-GHz Frequency Ranges (433, 868 and 915 MHz)
- Modulation Technique: FSK with FHSS Capability
- Supports High Data Rates:
  - Digital mode 115.2 kbps, max.
  - Analog mode 256 kbps, max.
- Differential RF Input/Output:
  - -110 dBm Typical Sensitivity with 0 dBm Maximum Input Level
  - +7 dBm Typical Transmit Output Power
- High-Resolution Programmable PLL Synthesizer
- Integrated Power Amplifier
- Integrated Low Phase Noise VCO Frequency
- Synthesizer and PLL Loop Filter
- Automatic Frequency Control

### Baseband Features

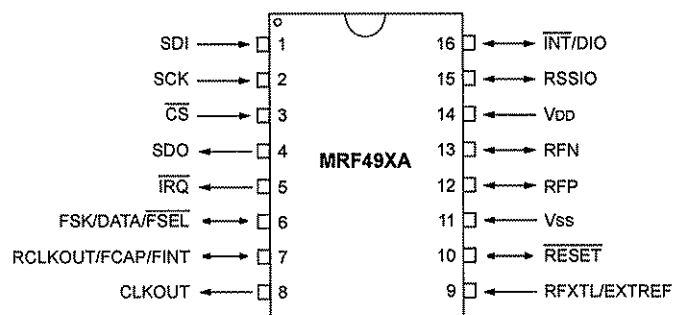
- Supports Programmable TX Frequency Deviation and RX Baseband Bandwidth
- Analog and Digital RSSI Outputs with Dynamic Range
- RX Synchronous Pattern Recognition
- 16-Bit RX Data FIFO
- Two 8-Bit TX Data Registers
- Low-Power Duty Cycle Mode
- Advanced Adjacent Channel Rejection/Blocking Capability
- Internal Data and Clock Recovery
- Supports Data Filtering
- Data Quality Indicator

### Typical Applications

- Home/Industrial Automation
- Remote Control
- Wireless PC Peripherals
- Remote Keyless Entry
- Vehicle Sensor Monitoring
- Telemetry
- Data Logging Systems
- Remote Automatic Meter Reading
- Security Systems for Home/Industrial Environment
- Automobile Immobilizers
- Sports and Performance Monitoring
- Wireless Toy Controls
- Medical Applications

# MRF49XA

Pin Diagram: 16-Pin TSSOP



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## 1.0 INTRODUCTION

Microchip Technology's MRF49XA is a fully integrated Sub-GHz RF transceiver. This low-power single chip FSK baseband transceiver supports:

- Zero-IF architecture
- Multi-channel and multi-band
- Synthesizer with Phase Locked Loop (PLL)
- Power Amplifier (PA)
- Low Noise Amplifier (LNA)
- I/Q down converter mixers
- I/Q demodulator
- Baseband filters and amplifiers

The simplified functional block diagram of MRF49XA is shown in Figure 1-1. The MRF49XA is an ideal choice for low-cost, high-volume, low data rate (< 256 kbps), two-way, short range wireless applications. This transceiver can be used in the unlicensed 433, 868 and 915 MHz frequency bands, and for applications looking for FCC, IC or ETSI certification in the ISM band.

The MRF49XA has a low phase noise and provides an excellent adjacent channel interference, Bit Error Rate (BER) and larger communication coverage along with higher output power. The MRF49XA device's Automatic Frequency Control (AFC) feature allows for the use of a low-accuracy, low-cost crystal. In order to minimize the total system cost, a communication link in most of the applications can be created using a low-cost, generic 10 MHz crystal, a bypass filter and an affordable microcontroller. The MRF49XA provides a clock signal for the microcontroller and avoids the need for a second crystal on the circuit board. The transceiver can be interfaced with many popular Microchip PIC® microcontrollers via a 4-wire SPI, interrupt (IRO) and Reset. The interface between the microcontroller and MRF49XA is shown in Figure 1-2.

The MRF49XA supports the following digital data processing features:

- PLL and I/Q VCO with Calibration
- Receiver Signal Strength Indicator
- Data Quality Indicator
- Automatic Frequency Control
- Baseband Power Amplifier
- TX and RX Buffers

The receiver's Baseband Bandwidth (BBBW) can be programmed to accommodate various deviations, data rates and crystal tolerance requirements.

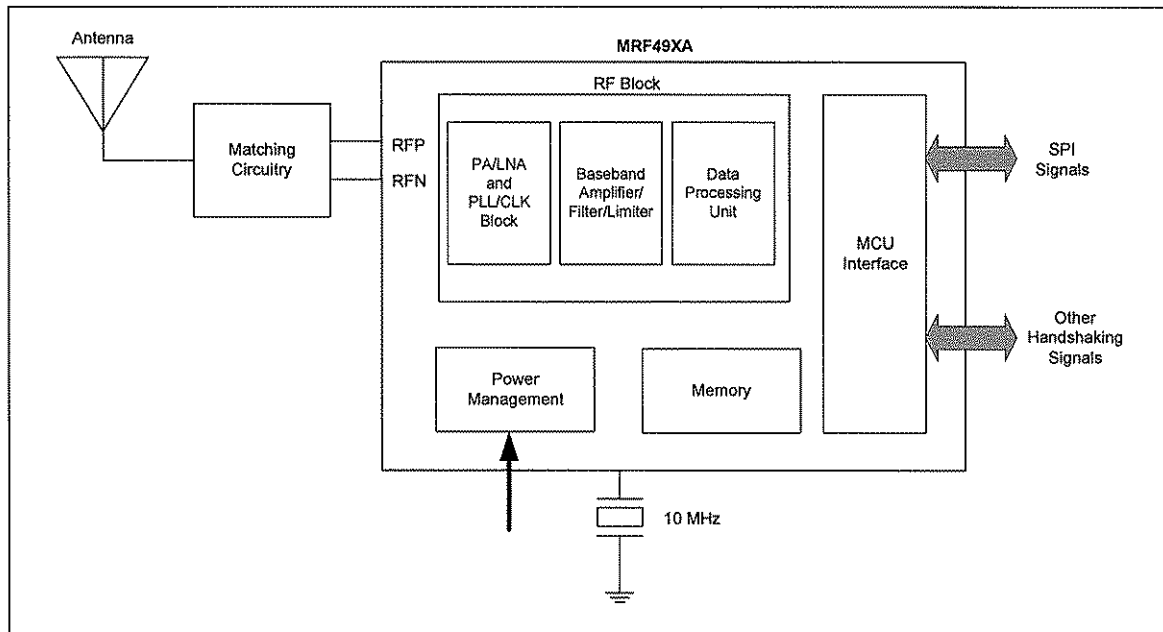
The high-resolution PLL allows:

- The usage of multiple channels in any of the bands
- The rapid settling time allows for faster frequency hopping, bypassing multipath fading and interference to achieve robust wireless links

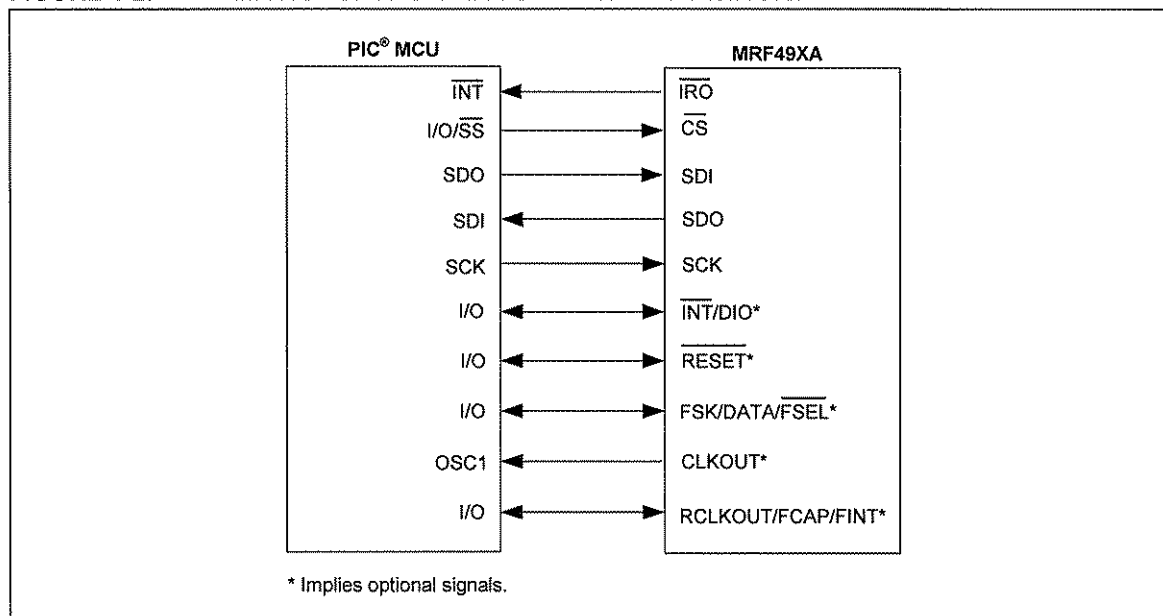
The transceiver is integrated with different Sleep modes and an internal wake-up timer to reduce the overall current consumption, and to extend the battery life. The device's small size with low-power consumption makes it ideal for various short range radio applications.

# MRF49XA

**FIGURE 1-1: FUNCTIONAL NODE BLOCK DIAGRAM**



**FIGURE 1-2: MICROCONTROLLER TO MRF49XA INTERFACE**



## 2.0 HARDWARE DESCRIPTION

The MRF49XA is an integrated, single chip ISM Band Sub-GHz Transceiver. A simplified architectural block diagram of the MRF49XA is shown in Figure 2-1.

The frequency synthesizer is clocked by an external 10 MHz crystal and generates the 433, 868 and 915 MHz radio frequency. The receiver with a Zero-IF architecture consists of the following components:

- Low Noise Amplifier
- Down Conversion Mixers
- Channel Filters
- Baseband Limiting Amplifiers
- Receiver Signal Strength Indicator

The transmitter with a direct conversion architecture has a typical output power of +7 dBm. An internal transmit/receive switch combines the transmitter and receiver circuits into differential RFP and RFN pins. These pins are connected to the impedance matching circuitry (Balun) and to the external antenna connected to the device.

The device operates in the low-voltage range of 2.2V to 3.8V, and in Sleep mode, it operates at a very low-current state, typically 0.3  $\mu$ A.

The quality of the data is checked or validated using the RSSI and DQI blocks built into the transceiver. Data is buffered in transmitter registers and receiver FIFOs. The Automatic Frequency Control feature allows the use of a low-accuracy and low-cost crystal. The CLKOUT is used to clock the external controller. The transceiver is controlled via a 4-wire SPI, interrupt ( $\overline{\text{INT/DIO}}$  and  $\overline{\text{IRO}}$ ), FSK/DATA/FSEL, RCLKOUT/FCAP/FINT and  $\overline{\text{RESET}}$  pins. See Table 2-1 for pin details.

The MRF49XA supports the following feature blocks:

- Clock Generation
- Data Filtering and Amplification
- Data Pattern Recognition and Timing
- Data Processing and Storage
- Independent Transmit and Receiver FIFO Buffers
- Registers

These features reduce the processing load, and hence, allows the use of low-cost 8-bit microcontrollers for data processing.