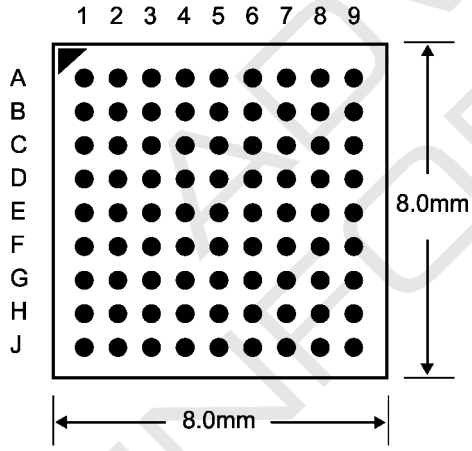
BlueCore™01
Single Chip Bluetooth System

General Description

BlueCore™01 is a true single chip radio and baseband IC for Bluetooth, 2.4GHz radios, implemented in CMOS technology. Together with an external Flash ROM containing the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system for data and voice communications. The design is optimised to require very few external RF components to facilitate a rapid design of the motherboard, and therefore the fastest possible time-to-market and lowest overall cost. For example, a low receiver IF is utilised to allow on-chip channel filtering.
A novel synthesiser technique removes the requirement for external varactor diodes and resonator capacitors. The use of digital techniques allows a higher performance to be achieved in the demodulator and modulator as well as providing improved immunity to interference and easier Interoperability with other Bluetooth systems. The on-chip 16 bit microcontroller is powerful enough to support full rate Bluetooth data communications (723.2/57.6Kbps).
The device works from a regulated supply in the range 2.7V to 3.3V. It is available in a BGA 81 ball package.

Package

81 ball BGA (8mm X 8mm)
Top view



Ball pad sizes = 0.4mm
Ball pad pitch = 0.8mm

Auxiliary Features

- Internal, low dropout, linear, voltage regulator. (Uses external pass transistors)
- Crystal oscillator with built-in digital trimming
- Power management including digital shut-down and wake-up commands and a low power relaxation oscillator for ultra-low park/sniff/hold mode power consumption

Radio Features

- No external trimming required in production
- Extensive built-in-self-test to minimise end product final test time
- Full RF reference design available

Transmitter

- Up to +4dBm RF transmit power with level control over greater than 30dB dynamic range controlled from 6-bit DAC
- Supports class 2 and class 3 radios
- Support for external PA for higher output powers with power control pin controlled by internal 6-bit current DAC and external RF TX/RX switch

Receiver

- Out of band blocking immunity sufficient for embedding in mobile phones
- Integrated channel filters
- Digital demodulator for better co-channel rejection
- Digitised RSSI
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser - No external VCO varactor diode or resonator

Baseband and Software Features

Baseband and Audio DSP

- Dedicated logic for forward error correction, header error control, cyclic redundancy check, encryption bitstream generation, whitening, transmit pulse shaping, demodulation and access code correlation
- Transcoders for A-law, μ-law and linear voice from host and A law, μ-law and CVSD voice over air

Physical Interfaces

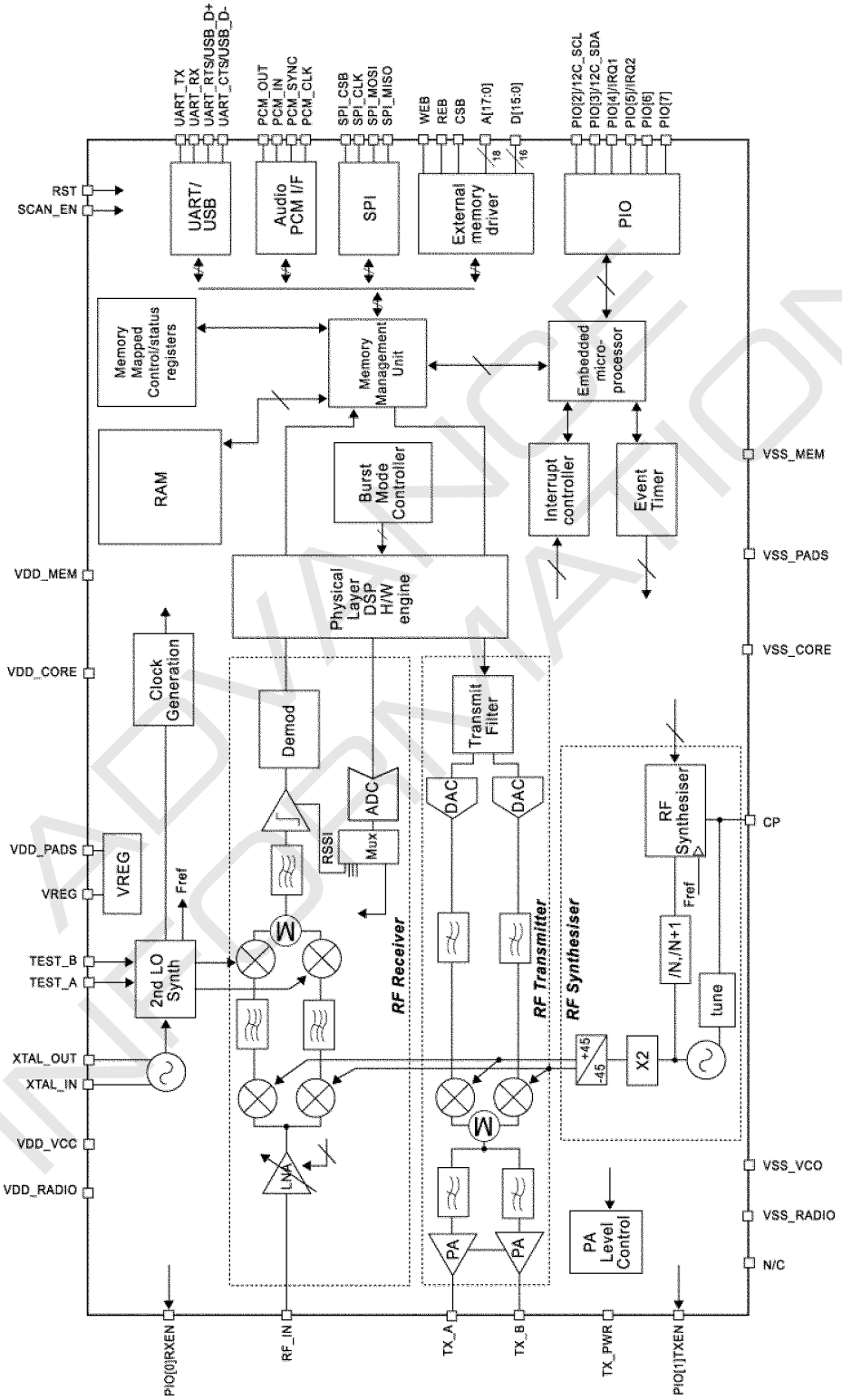
- Synchronous serial interface up to 4Mbaud
- UART interface with programmable baud rate up to 1.5MBaud
- Full Speed USB Interface. Supports OHCI and UHCI
- 13bit PCM, 8kss^{-1} synchronous bi-directional serial audio interface
- Serial interface to optional, I^{2}C compatible EEPROM
- Interface to external programme memory(16 bit data, 18 bit address)
- 8 bit, programmable input/output port

Bluetooth stack running on internal microcontroller

- 16 bit RISC microcontroller
- Link Controller, Link Manager and HCI
- All packet types (including 3 and 5 slot packets)
- Multiple voice channels
- Multiple data channels at all Bluetooth data rates
- On-chip implementation of L2CAP and RFCOMM and SDP, optimised for GSM dial-up networking
- Evaluation system available separately

Contact: sales@CambridgeSiliconRadio.com Telephone: +44 (0)1223 424167

Ref No: BCLF190100/1



Terminal Functions The ball assignments below are preliminary only.

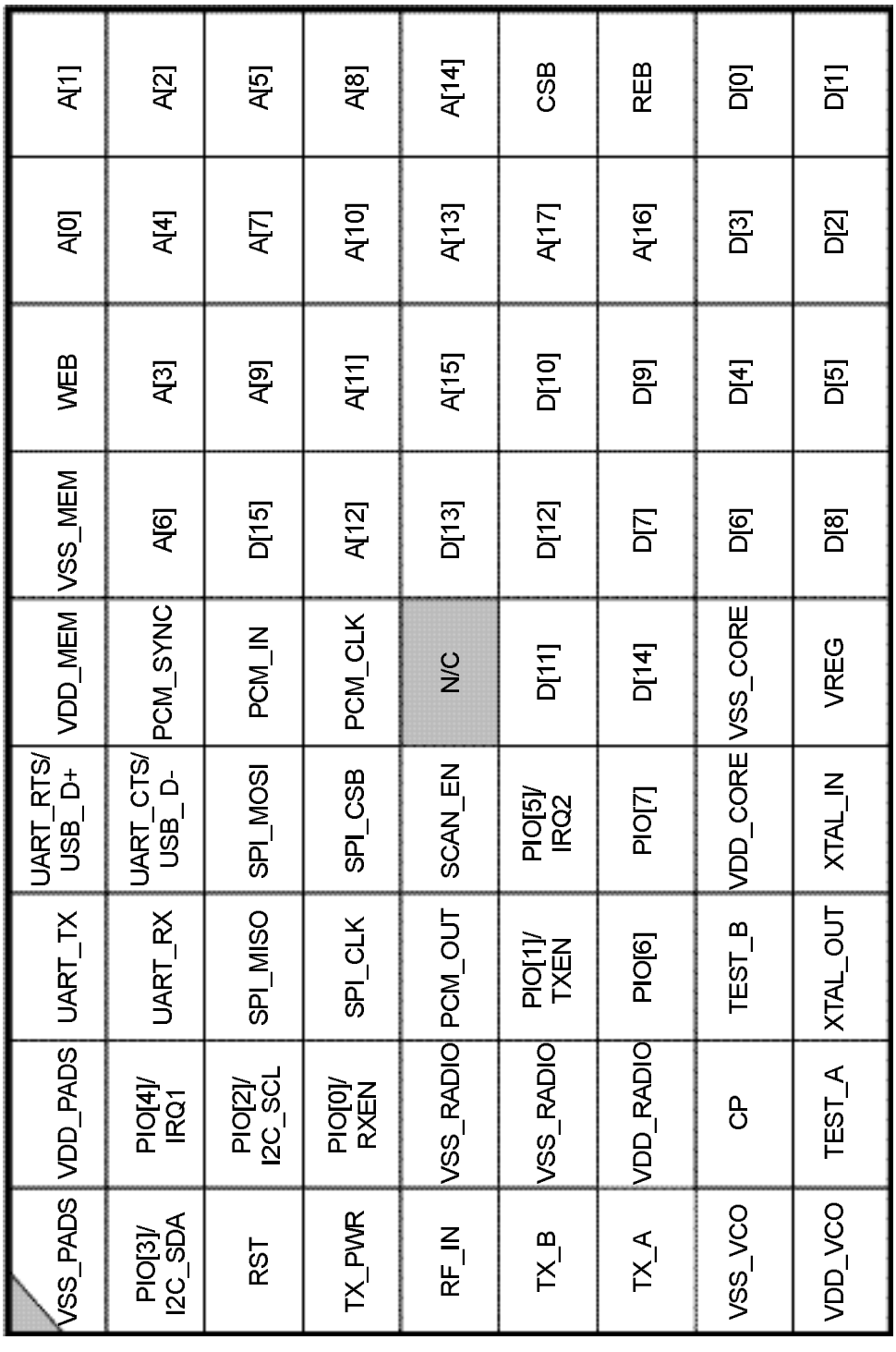
Terminal Name	Type	Ball	Description
Radio			
RF_IN	Analog	E1	Input to LNA
PIO[1] / TXEN	Bi-Dir	F3	Control output for external PA (Class 1 only) (=PIO[1])
PIO[0] / RXEN	Bi-Dir	D2	Control output for external LNA if fitted (=PIO[0])
TX_PWR	Analog	D1	Current output sets external PA level
TX_A	Analog	G1	Transmitter output
TX_B	Analog	F1	Compliment of TX_A
Synthesiser and oscillator			
CP	Analog	H2	Charge pump output
XTAL_IN	Analog	J4	For crystal or external clock input
XTAL_OUT	Analog	J3	For crystal or external clock input
External memories			
A[17:0]	CMOS op	See Below ♣	Address bus for external memory
D[15:0]	Tristate	See Below ♠	Data bus for external memory
WEB	CMOS op	A7	Write enable bar for external memory
REB	CMOS op	G9	Read enable bar for external memory
CSB	CMOS op	F9	Chip select bar for external memory
PIO[3] / I2C_SDA	Bi-Dir	B1	Data line for EEPROM interface (=PIO[3])
PIO[2] / I2C_SCL	Bi-Dir	C2	Clock for EEPROM interface (=PIO[2])
Digital communications			
PCM_OUT	CMOS op	E3	Synchronous $8kss^{-1}$ data out
PCM_IN	CMOS ip	C5	Synchronous $8kss^{-1}$ data input
PCM_SYNC	Bi-Dir	B5	Synchronous data strobe
PCM_CLK	Bi-Dir	D5	Synchronous data clock
UART_TX	CMOS op	A3	Asynchronous serial data out
UART_RX	CMOS ip	B3	Asynchronous serial data input
UART_RTS / USB_D+	CMOS op	A4	Asynchronous serial data RTS / USB Data +
UART_CTS / USB_D-	CMOS ip	B4	Asynchronous serial data CTS / USB Data -
SPI_CSB	CMOS ip	D4	Chip select for Synchronous Serial Interface
SPI_CLK	CMOS ip	D3	Synchronous Serial Interface Clock (and scan clock)
SPI_MOSI	CMOS ip	C4	Synchronous Serial Interface data input (and scan out)
SPI_MISO	CMOS op	C3	Synchronous Serial Interface data output (and scan out)
Configuration and testing			
TEST_A	Analog	J2	Analog test port A
TEST_B	Analog	H3	Analog test port B
RST	Schmitt pd	C1	Reset if high
SCAN_EN	CMOS ip	E4	Selects mode of Synchronous Serial Interface port during scan test
Auxiliary functions			
VREG	Analog	J5	LDO linear voltage regulator o/p to external pass transistors
PIO[6:7]	Bi-Dir	See Below ♦	Programmable I/O lines
PIO[4] / IRQ1	Bi-Dir	B2	Programmable I/O line/ Interrupt request 1
PIO[5] / IRQ2	Bi-Dir	F4	Programmable I/O line/ Interrupt request 2
Power supplies			
VDD_CORE	VDD	H4	For internal digital circuitry
VDD_RADIO	VDD	G2	For RF circuitry
VDD_VCO	VDD	J1	For VCO and synthesiser
VDD_PADS	VDD	A2	For I/O
VDD_MEM	VDD	A5	For external memory port
VSS_CORE	VSS	H5	For internal digital circuitry
VSS_RADIO	VSS	F2, E2	For RF circuitry
VSS_VCO	VSS	H1	For VCO and synthesiser
VSS_PADS	VSS	A1	For I/O
VSS_MEM	VSS	A6	For external memory port
N/C		E5	Not connected

♣ A(0):A8; A(1):A9; A(2):B9; A(3):B7; A(4):B8; A(5):C9; A(6):B6; A(7):C8; A(8):D9; A(9):C7; A(10):D8; A(11):D7; A(12):D6; A(13):E8; A(14):E9; A(15):E7; A(16):G8; A(17):F8

♠ D(0):H9; D(1):J9; D(2):J8; D(3):H8; D(4):H7; D(5):J7; D(6):H6; D(7):G6; D(8):J6; D(9):G7; D(10):F7; D(11):F5; D(12):F6; D(13):E6; D(14):G5; D(15):C6

♦ PIO[6]:G3; PIO[7]:G4

Pinout - Top View



	1	2	3	4	5	6	7	8	9
A	VSS_PADS	VDD_PADS	UART_TX	UART_RTS/ USB_D+	VDD_MEM	VSS_MEM	WEB	A[0]	A[1]
B	PIO[3]/ I2C_SDA	PIO[4]/ IRQ1	UART_RX	UART_CTS/ USB_D-	PCM_SYNC	A[6]	A[3]	A[4]	A[2]
C	RST	PIO[2]/ I2C_SCL	SPI_MISO	SPI_MOSI	PCM_IN	D[15]	A[9]	A[7]	A[5]
D	TX_PWR	PIO[0]/ RXEN	SPI_CLK	SPI_CSB	PCM_CLK	A[12]	A[11]	A[10]	A[8]
E	RF_IN	VSS_RADIO	PCM_OUT	SCAN_EN	N/C	D[13]	A[15]	A[13]	A[14]
F	TX_B	VSS_RADIO	PIO[1]/ TXEN	PIO[5]/ IRQ2	D[11]	D[12]	D[10]	A[17]	CSB
G	TX_A	VDD_RADIO	PIO[6]	PIO[7]	D[14]	D[7]	D[9]	A[16]	REB
H	VSS_VCO	CP	TEST_B	VDD_CORE	VSS_CORE	D[6]	D[4]	D[3]	D[0]
J	VDD_VCO	TEST_A	XTAL_OUT	XTAL_IN	VREG	D[8]	D[5]	D[2]	D[1]

Absolute Maximum Ratings

Storage Temperature Range ..... -30°C to +85°C
Supply Voltage, VDD..... 3.6 V
Other Terminal Voltages .....VSS-0.3V to VDD+0.3V

Damage may occur to the device if these ratings are exceeded.

Recommended Operating Conditions

Operating Temperature Range ..... -20°C to +75°C
Supply Voltage, VDD (all supplies) ..... 2.7V to 3.3V

The device will be functional inside the recommended operating conditions. However, the DC and AC characteristics below are only valid over the test conditions and applications circuit described separately.

Power Consumption

VDD = 2.8V. Temperature = 20˚C

Mode	Min	Typ	Max	Unit
During receive slots		41		mA
During transmit slots (+4dBm output)		41		mA
Data connection 723.2Kbps / 57.6 Kbps (DH5)		40		mA
Voice only connection - HV3 packets		15		mA
Voice only connection - HV1 packets		30		mA
R1 Page scan mode		420		uA
Inquiry scan mode, plus R1 page scan		560		uA
Park mode with a 1 second interval		120		uA
Leakage current when off			10	uA

Radio Characteristics

T=25°C,
F=2.400 - 2.497GHz
Unless otherwise stated

VDD=2.8V,
Parametric limits guaranteed only when tested with the CSR reference design

Parameter (1)	Min	Typ	Max	Unit
Radio Receiver				
Sensitivity		-80		dBm
Maximum received signal		-20		dBm
Co-channel interference rejection (Bluetooth interferer) $C/I_{co\text{-}channel}$		+10		dB
Adjacent channel selectivity. C/I_{1MHz}		0		dB
2nd adjacent channel selectivity. C/I_{2MHZ}		-32		dB
3rd and greater adjacent channel selectivity. $C/I_{\geq 3MHZ}$ (2)		-40		dB
Image rejection. C/I_{mirror}		-14		dB
1dB compression point in presence of out-of-band blocker (3)		-12		dBm
Maximum level of intermodulation interferers (4)		-39		dBm
Fast AGC range		40		dB
Radio Transmitter				
Maximum RF transmit power	+1		+4	dBm
RF power stability over operating temperature range	-2		+2	dm
RF power control range	30			dB
RF power range control step size		2		dB
Modulation accuracy			1	%
Frequency stability over 5 slots			10	KHz
Spurious transit power in DCS1800 receive band, 1805-1880MHz, measured in 100KHz bandwidth			-81	dBm

Notes

(1) All radio parameters are measured according to the Bluetooth specification. All parameters are referenced to the antenna connector on CSR reference design PCB. (ie. before the antenna itself).

(2) Up to five spurious responses within Bluetooth limits are allowed.

(3) Maximum level of out-of-band interferer that results in 1dB reduction in the actual sensitivity (at 0.1% BER) of the IC. 1.95GHz <F> 2.95GHz.

(4) Measured at $|f_1-f_2|$ = 5MHz.

Description of Functional Blocks

Radio Transceiver and Synthesiser

The receiver features a near-zero IF architecture that allows the channel filters to be integrated. The 1dB out-of-band blocking specification at the LNA input allows the radio to be used in close proximity to a 900MHz, 1.8GHz or 1.9GHz cellular 'phone transmitter without being de-sensitised, even without the need for a high Q, ceramic filter at the RF input. The use of a digital FSK discriminator means that no (pre-) trimmed discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore™01 to exceed the Bluetooth requirements for co-channel and adjacent channel rejection. Fast AGC is implemented by measuring the RSSI on a slot-by-slot basis and adjusting the front-end LNA gain to keep the first mixer input signal within a limited range. This improves the dynamic range of the receiver in interference limited environments.

The transmitter features a direct IQ modulator at 2.4GHz to minimise the frequency drift during a transmit timeslot and also results in a well controlled modulation index. A digital baseband transmit filter provides the required spectral shaping.
The maximum transmit power of +4dBm allows BlueCore™01 to be used in class 2 and class 3 radios and its support for transmit gain control allows a simple implementation for class 1 with an external, one or two stage RF power amplifier.

The radio synthesiser is fully integrated with no requirement for external VCO cans, varactor tuning diodes or LC resonators, and it works at half of the Radio Frequency to minimise coupling to the RF amplifiers.

The radio has several built-in automatic calibration loops. These use resident calibration routines running on the microcontroller to maintain dynamically the radio performance within specification across temperature and aging thus ensuring that high tolerance external RF components are not needed.

Auxiliary Features

The device contains two clock sources: one reference oscillator for the RF carrier frequency, and one low frequency clock oscillator that is used as an interval timer during 'Sleep' modes, ie Sniff, Hold or Park.

An on-chip reference oscillator is provided with a current consumption of 100uA when enabled, and requires an external crystal. Alternatively, the crystal pins can be driven from an external reference clock. The provision of the on-chip second LO synthesiser means that the reference frequency chosen can be in the range of 10-20MHz (on a multiple of 0.25MHz).

The low frequency clock oscillator is entirely on-chip. It is calibrated automatically under software control every time just before the reference crystal oscillator is disabled, and maintains an accuracy of better than 250ppm over the 41 second maximum Park/Hold/Sniff mode interval. This oscillator consumes less than 2uA, and is left permanently enabled.

Description of Functional Blocks - continued

Physical Layer DSP Hardware Engine

A dedicated logic implementation for most of the required DSP functions is used to provide a low power solution whilst providing the required data throughput. The functions implemented in hardware include: forward error correction, header error control, cyclic redundancy check, encryption, data whitening and access code correlation. Also included is a dedicated hardware implementation of an audio transcoder to translate between A-law, μ-law and linear voice data from the host and A-law, μ-law and CVSD voice data over the air. Voice interpolation for lost packets is included in firmware.

Burst Mode Controller

During radio transmission this block constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from a selected ring buffer in RAM corresponding to the appropriate connection. For radio reception, the burst mode controller stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the interventions required by the processor during packet transmission and reception.

Microcontroller, Interrupt Controller and Event Timer

These run the Bluetooth software stack and control the radio and host interfaces. The 16 bit RISC microcontroller has a very low power consumption and a low gate count.

Memory Management Unit

This provides a number of dynamically allocated ring buffers that hold user data/voice that is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware memory management unit to minimise the overheads on the processor during data/voice transfers.

RAM

On chip RAM is provided and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

External Interfaces

Transmitter Outputs

Pins TX_A and TX_B form a push-pull balanced current output. They require a DC connection to Vdd, and should be connected through a balun to the antenna. The recommended load impedance to present to these outputs is 100 Ohms. The output impedance is capacitive, and remains constant irrespective of whether the transmitter is enabled or disabled.

Receiver Input

The RF_IN pin is single ended and presents a capacitive input of approximately 0.4pF. A swing of up to 0.5V rms can be tolerated at this pin, allowing class 2 and 3 systems to couple the pin directly to the transmitter output (ie an RF TX/RX switch is not required for class 2 and 3 systems). The recommended source impedance at the pin is 100 Ohms.

Asynchronous Serial Data Port (UART)/USB Port

UART_TX, UART_RX, UART_RTS, and UART_CTS form a conventional asynchronous data serial port. The interface is designed to operate correctly when connected to other UART devices such as the NS16550A.The signalling levels are 0V and Vdd (+3.0V nominal). The interface is programmable over a variety of bit rates; no,even or odd parity; one or two stop bits and hardware flow control on or off. The default condition on power-up is pre-assigned in the (external) Flash memory.

The maximum UART data rate is 1.5Mb/s. Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and is active low. UART_CTS is an input and is active low. These signals operate according to normal industry convention.

The port carries a number of logical channels: HCI data (both SCO and ACL), HCI commands and events, L2CAP API, RFCOMM API, SDD-B API and device management. For the UART, these are combined into a robust tunnelling protocol BlueCore™
Serial Protocol (BCSP) where each channel has its own software flow control and cannot block other data channels.

Alternatively a firmware version is available to support full speed (12MBPS) USB. The UART_RTS pin is reconfigured as USB_D+ and the UART_CTS pin is reconfigured as USB_D-. Both OHCI and UHCI are supported.

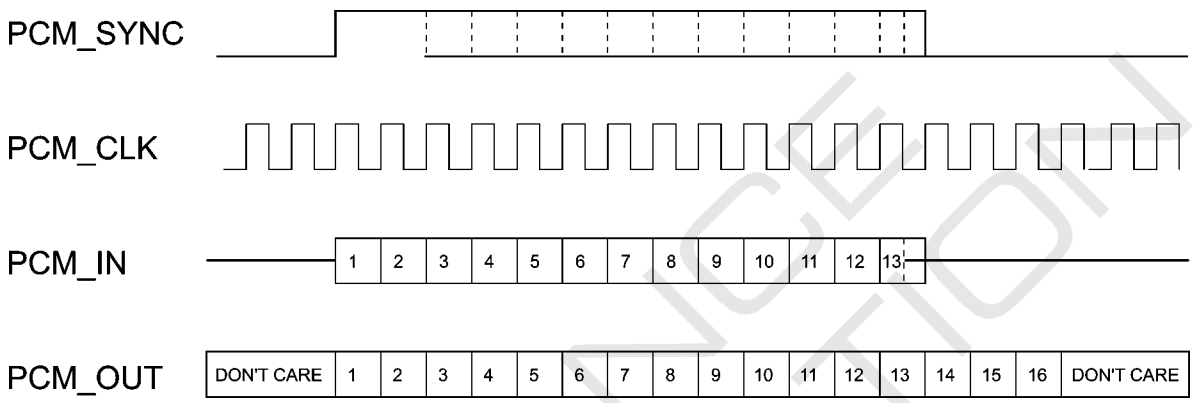
The firmware in Flash can be downloaded through this port if the CSR supplied boot loader is first programmed.
The firmware shipped with BlueCore™01 will include security features to prevent mis-use of this upgrade facility.

PCM Codec Interface

PCM_OUT, PCM_IN, PCM_CLK, PCM_SYNC carry one bi-directional channel of voice data using 13bit PCM at 8ks/s.
The PCM_CLK and PCM_SYNC pins can be configured as inputs or outputs depending on whether BlueCore™01 is the generator of the 8kHz reference. When programmed as outputs, BlueCore™01 interfaces directly to PCM audio devices such as the Motorola MC145483.

External Interfaces-continued

The interface operates according to the following timing diagram:



PCM_SYNC operates at a fixed clock frequency of 8kHz. When PCM_SYNC is operated as an output (master mode) a clock frequency of 8kHz is generated from this pin. When operated as an input (slave mode) 8kHz must be input on this pin.

PCM_CLK operates at a fixed clock frequency of 256kHz. When PCM_CLK is operated as an output (master mode) a clock frequency of 256kHz is generated from this pin. When operated as an input (slave mode) 256kHz must be input on this pin.

Bits 1 to 13 of the PCM_OUT data carry the current output sample value. Bits 14 to 16 carry a three bit signal level value. When used with the Motorola MC145483 codec or compatible devices these 'level bits' allow Bluecore™01 to vary the level of the audio signal output from the codec device.

Synchronous Serial Port

BlueCore™01 is a slave device using pins SPI_MOSI, SPI_MISO, SPI_CLK and SPI_CSB. This port allows access to the logical channels of the UART, as well as being used for program emulation/debug and IC test. It is also the means by which a Flash ROM may be programmed in situ before any 'boot' program is loaded. The designer should be aware that no security protection is built-in to the hardware or firmware associated with this port.

External Interfaces-continued

Parallel PIO Port

Eight lines of programmable, bi-directional IO are provided, PIO[0:7]. Six of these are normally dedicated to TXEN, RXEN, I2C_CLK, I2C_SDA, IRQ1 and IRQ2 but two are available for general use and can be allocated, for example, to the interface of an external button or for software UARTs.

I²C Interface to External EEPROM

PIO[3]/I2C_SDA and PIO[2]/I2C_SCL can be used to form a single master I²C interface to a slave device, usually an EEPROM. The interface is formed using software to drive these lines, and is thus suited only to relatively slow functions.

Off-Chip Program Memory Interface

The external memory port comprises a 16 bit data bus (D[15:0]) and an 18 bit address bus (A[17:0]), thus addressing up to 4Mbits of off-chip code or constants. Control signals WEB, REB and CSB are also provided, which make it possible to use a variety of different memories, including SRAM and Flash.

It is possible to store program or constants in the Flash, even if simultaneous Read/Write memories are not used, by exercising code from the on-chip RAM. This is especially useful for the storage of Bluetooth persistent data.

CSR Bluetooth Software Stack

BlueCore™01 is supplied with a Bluetooth software stack firmware that runs on its microcontroller and is resident in the (external) Flash memory.

Additional Software Supplied for PCs

A UART software driver is supplied that presents the HCI to the PC resident Bluetooth stack layers (ie L2CAP, Bluetooth advisor etc). Also provided is the code for the BlueCore™01 initialisation and management functions. The code is provided as C source or object code.

Additional Software Supplied for Other Embedded Applications

A UART software driver is supplied that presents the HCI, L2CAP, RFCOMM and SDD-B APIs to higher Bluetooth stack layers running on the host. The code is provided as C source or object code.

Other software drivers can be developed on request. Contact CSR sales for more information.

Licence to Source Code for Adapted Layers and the Application Framework for Bluetooth

This software is portable across a range of hardware and software platforms. For details of availability and price contact CSR sales.

BlueCore™ Evaluation System

This is available to allow the evaluation of BlueCore™ hardware and software and as the base of a toolkit for developing host software. For more details also contact CSR sales.

Profiles Supported via HCI

The supplied software stack is a full implementation of Bluetooth up to and including RFC0MM, SDP and L2CAP, so all profiles and associated data rates can be supported, except those involving scatternets and requiring support of Quality of Service. These will be supported in a future software release, once all profiles are fully defined.

CSR Bluetooth Software Stack - continued

Profiles Fully Implemented with On-Chip Software Only

Because the following profiles are fully supported with software supplied with and running on the chip, it will be possible to gain Bluetooth type-approval at the component level for BlueCore™01 for the following profiles.

Headset Profile

BlueCore™01 can, together with a PCM Codec and Filter, implement a cordless headset with no requirement for a host (Headset side).

It is also capable, either via the UART or the voice PCM link, of providing the Bluetooth function inside a mobile telephone or PDA. The on-chip implementation of RFCOMM and SDD-B allow a very simple software interface to the mobile telephone, and the PCM voice port allows direct interaction with GSM hardware (Audio Gateway side).

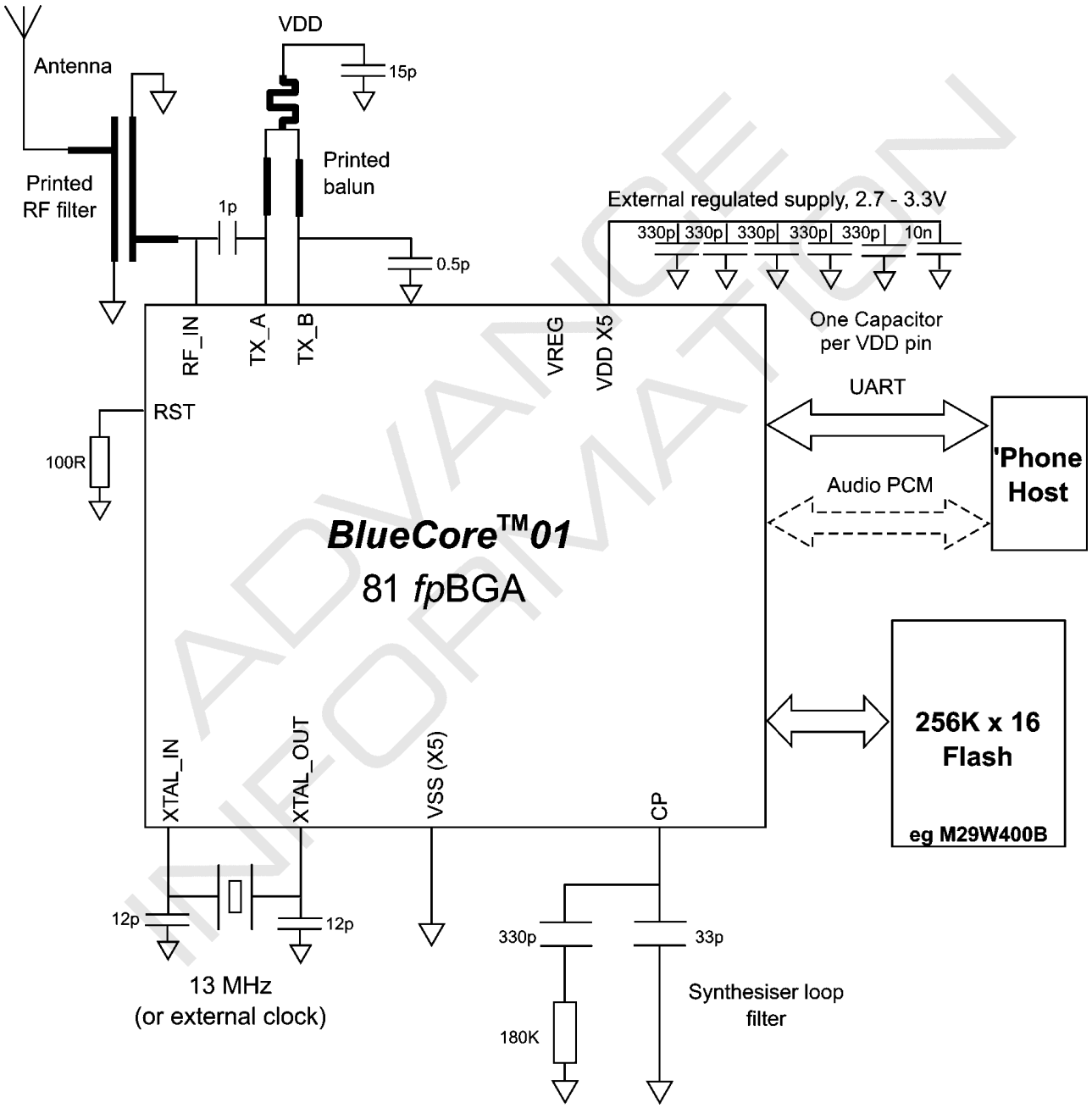
Serial Port Profile

This profile is fully supported, except for the optional Quality of Service feature. The maximum data rate is TBD. This profile can be used concurrently with voice (SCO) traffic. Note also that this profile provides the majority of the functionality of many other profiles, for instance the Fax Profile, which can be supported with additional software running on the host.

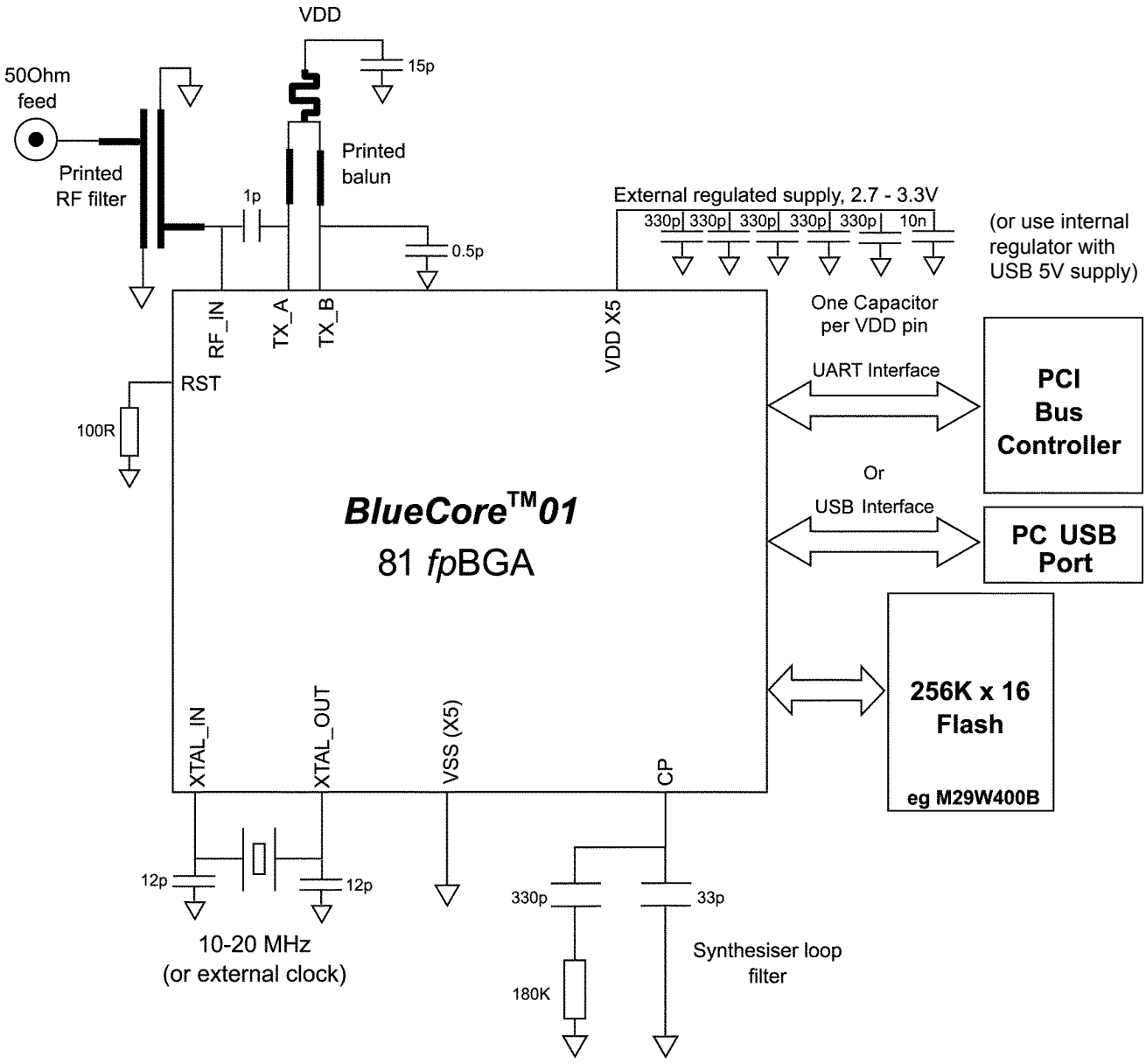
Dial-Up Networking

BlueCore™01 can be used in both the Gateway and Data Terminal sides. In addition to the mandatory requirements, multiple slot packets are supported to make more efficient use of 'air' bandwidth. The maximum average data rate that can be supported is TBD (but is significantly greater than the requirements of GSM cellular telephones using TS 07.10).
This profile can be used concurrently with voice (SCO) traffic but audio feedback is not currently supported.

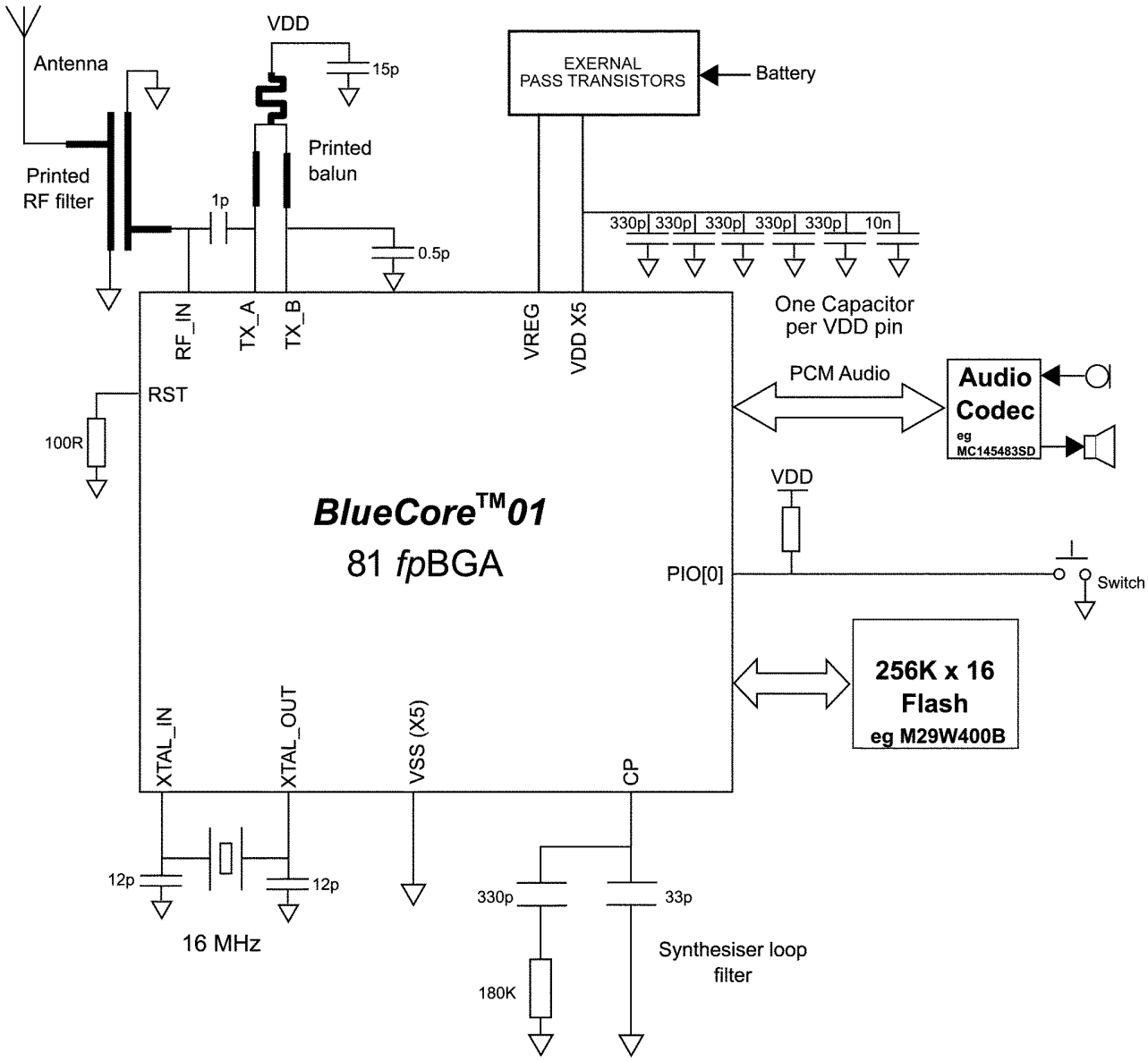
Application 1: Bluecore™01 Inside a Mobile 'Phone



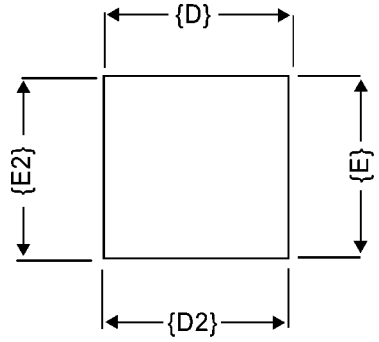
Application 2: Bluecore™01 Inside a PC, or PC add-on



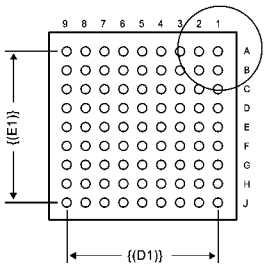
Application 3: Bluecore™01 Inside a Cordless Headset



Package Dimensions

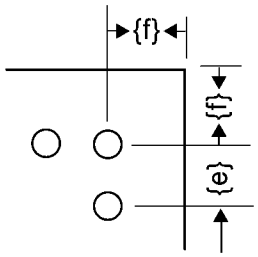


DETAIL B

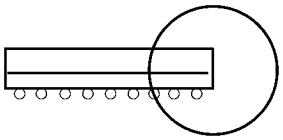


DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.25(1.35)	1.35(1.45)	1.45(1.55)
A1	0.25(0.35)	0.35(0.40)	0.40(0.45)
A2	0.65	0.70	0.75
D	7.80	8.00	8.20
D1		6.40 BSC.	
D2	7.80	8.00	8.20
E	7.80	8.00	8.20
E1		6.40 BSC.	
E2	7.80	8.00	8.20
b	0.35(0.45)	0.40(0.50)	0.45(0.55)
c		0.35	
aaa			0.15
bbb			0.20
ccc			0.25
e	0.725	0.80	0.875
f	0.70	0.80	0.90
m		9	
n		81	

DETAIL B

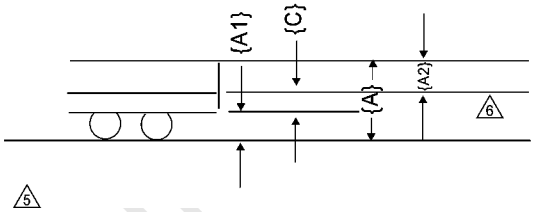


DETAIL A



NX

4



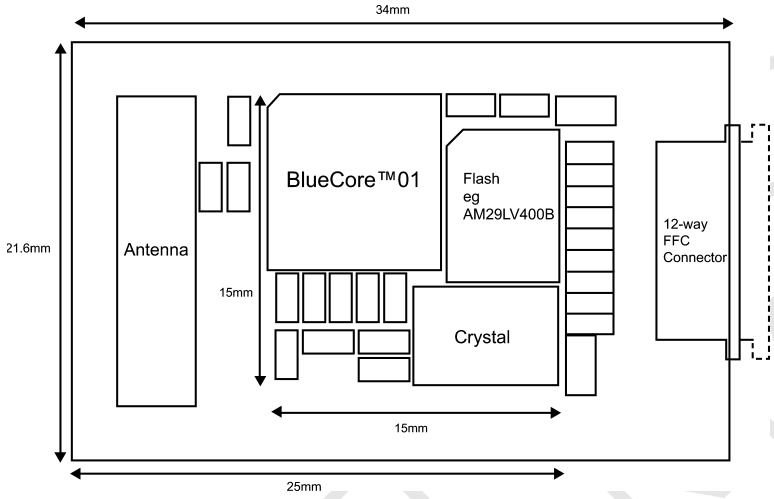
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETRES
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE AND SYMBOL 'N' IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING
4. 'b'IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM-C
5. DIMENSIONS 'aaa' IS MEASURED PARALLEL TO PRIMARY DATUM-C
6. PRIMARY DATUM-C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
7. PACKAGE SURFACE SHALL BE MATTE FINISH CHARMILLES 24 TO 27
8. PACKAGE CENTERING TO SUBSTRATE SHALL BE 0.0760MM MAXIMUM
9. PACKAGE WARP SHALL BE 0.050MM MAXIMUM
10. SUBSTRATE MATERIAL BASE IA BT RESIN
11. THE OVERALL PACKAGE THICKNESS 'A' ALREADY CONSIDERS COLLAPSE BALLS

Reference Design

A full printed circuit reference design including the RF circuit is available for BlueCore™01 (contact CSR directly). The following drawings are shown here as an indication of the size of a stand-alone Bluetooth module built using BlueCore™01, and also of the PCB area used when BlueCore™01 is embedded within a target motherboard.

Component Placement



	X/cm	Y/cm	Area/cm^2
Core	1.5	1.5	2.25
Core + antenna	2.5	2.16	5.40
Core + antenna + connector	3.4	2.16	7.34

Status of Information Provided

This is the long form version of the BlueCore™01 data sheet and was last updated on 19TH January 2000.

Information supplied is on an ADVANCE INFORMATION basis. This means that all data contained herein is subject to change by Cambridge Silicon Radio (CSR) without notice. CSR assumes no responsibility whatsoever for the consequences of the use of the information contained in this document. This document succeeds and replaces all information previously supplied.

Life Support Policy and use in safety-critical applications

CSR's products are not authorised for use in life support or safety-critical applications.

Trademarks and Patents

BlueCore™ is a trademark applied for by Cambridge Silicon Radio.
All other trademarks are acknowledged.
The publishing of this information does not imply that any license is granted under any patent or other patent rights owned by CSR.

Cambridge Silicon Radio
Unit 300, Science Park
Milton Road
Cambridge, CB4 0XL
United Kingdom
Tel: +44 1223 424167
Fax: +44 1223 424178
sales@CambridgeSiliconRadio.com
www.CambridgeSiliconRadio.com