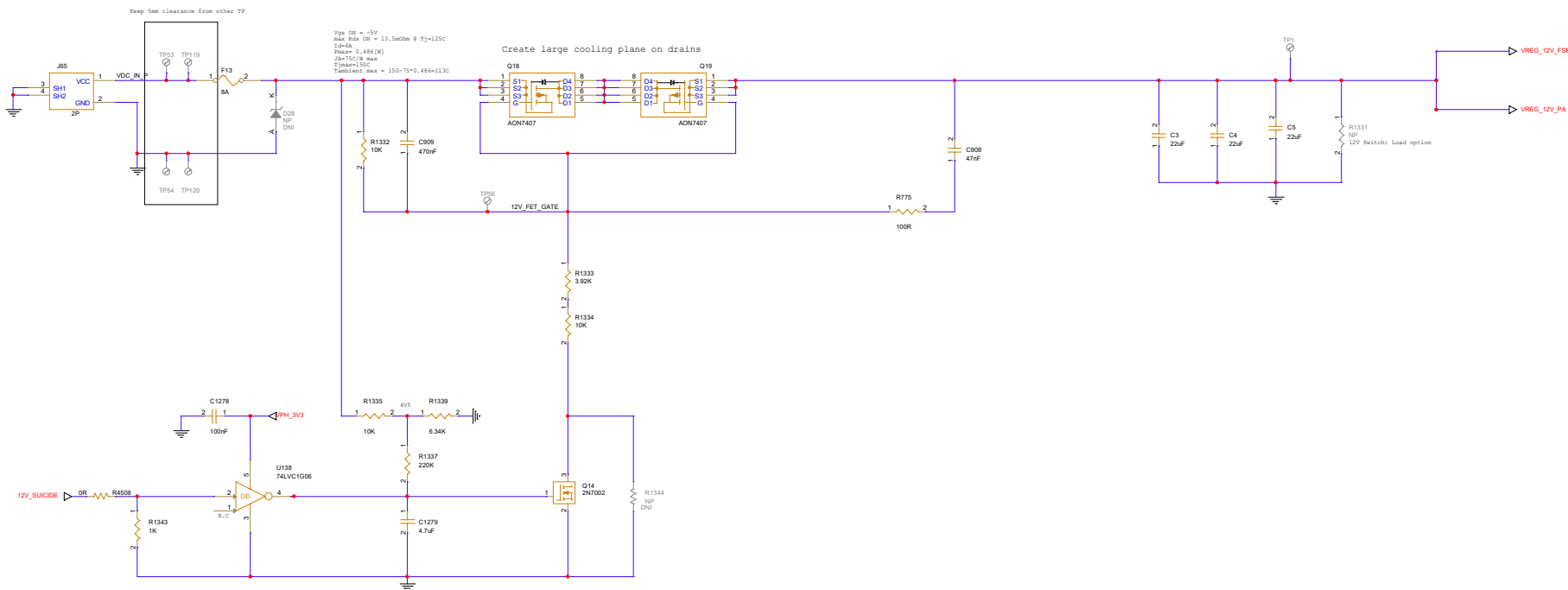
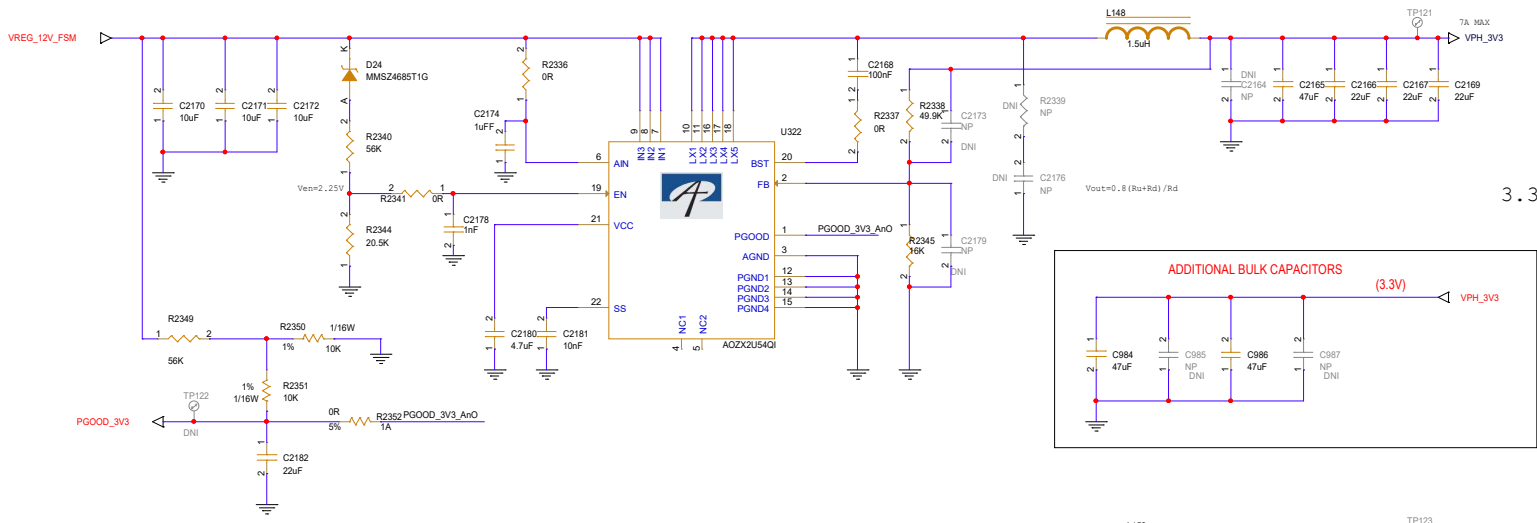


# 12V Input power



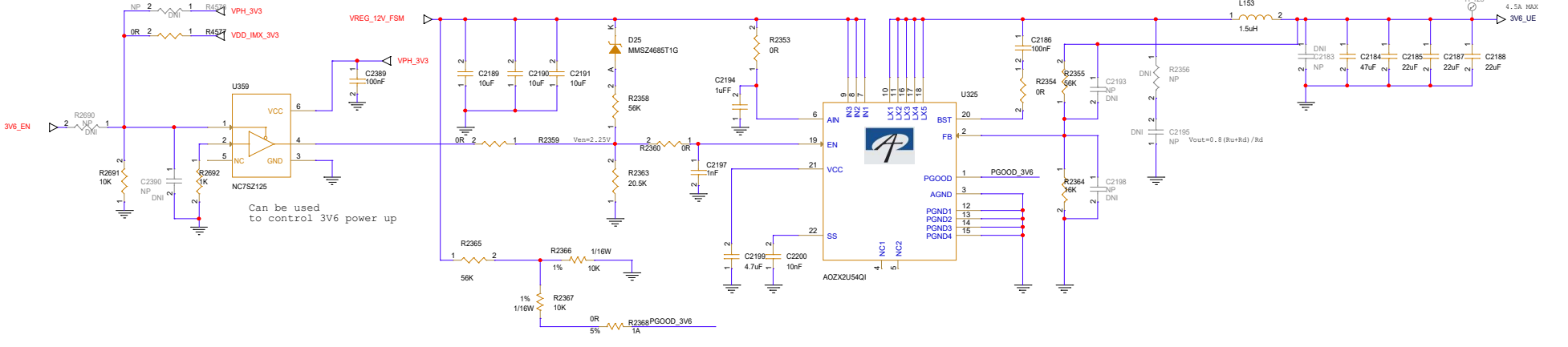
Input PWR

Airspar Networks			
File	AU588 900 13 420 B48 RevA8		
Size	Page Name	Schematic Name	
Custom	PEI-Input_Power	Baseband	
Date	Monday, October 31, 2022	Sheet 1	of 62



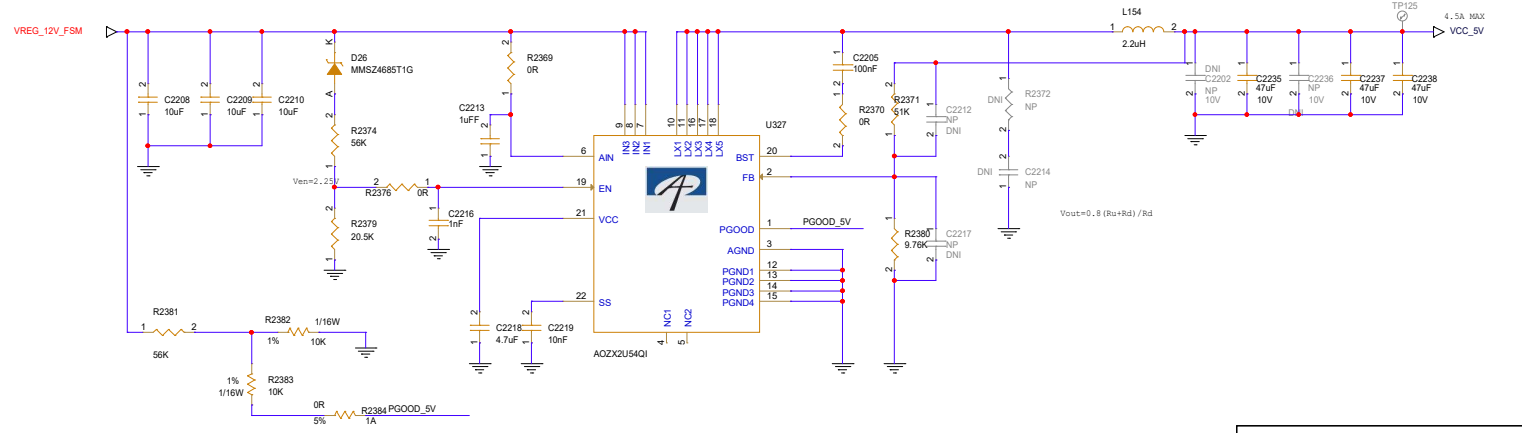
3.3V

Supported options:  
 1. 3V6 is on by default when VPH\_3V3 is present  
 2. 3V6 is on by default when VDD\_IMX\_3V3 is present  
 3. 3V6 is OFF by default. PMR enabled by 1Mx

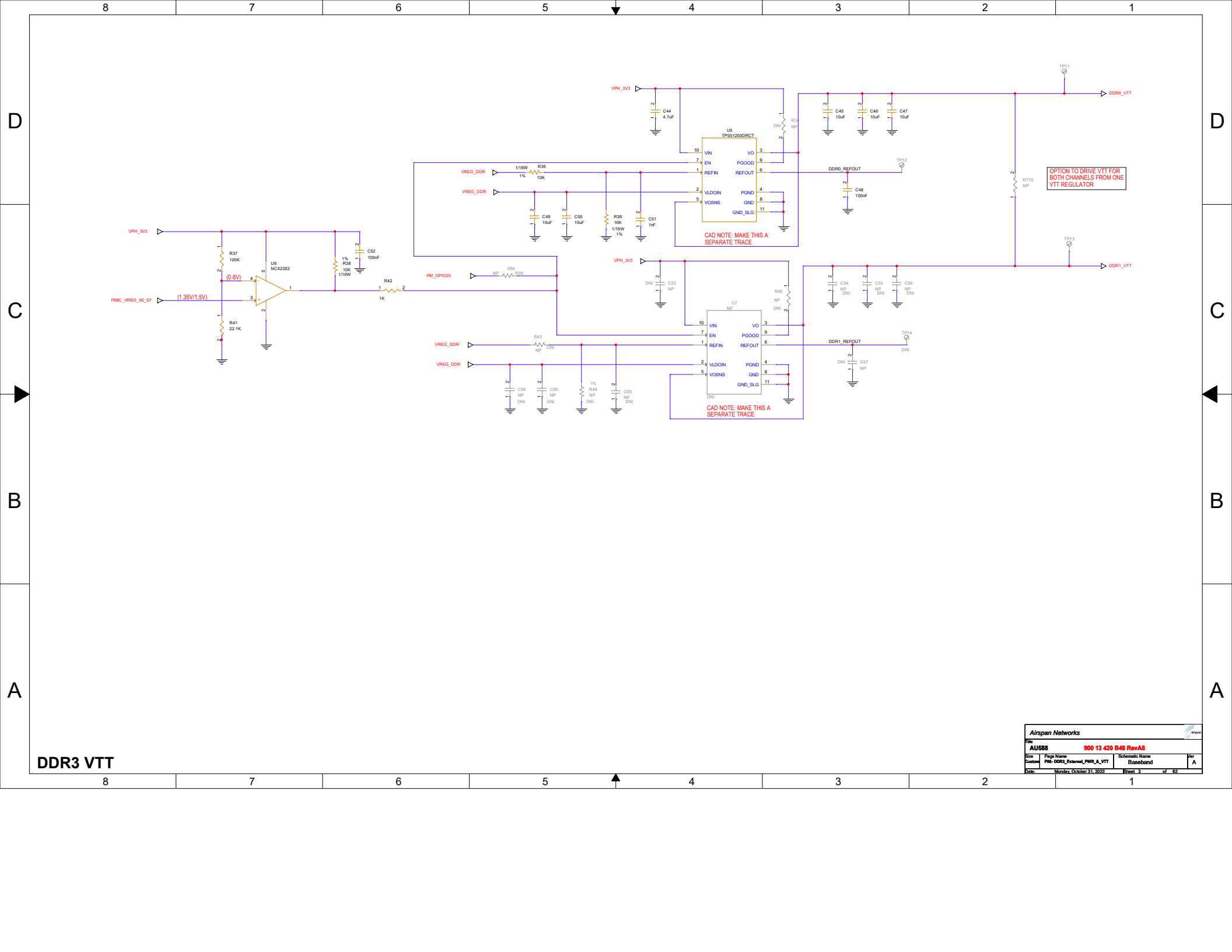


3.6V

Can be used to control 3V6 power up



5V

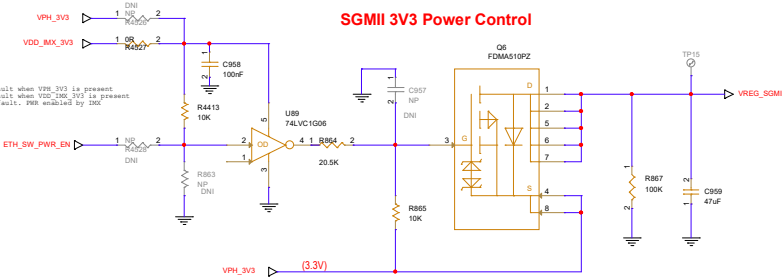


DDR3 VTT

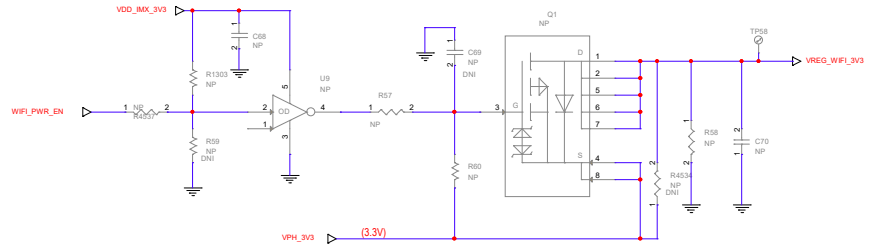
Airsip Networks			
File:	AU588	900 13 420 B48 RevA8	
Sheet:	1	Page Name:	Baseband
Customer:	PEL-DDR3_External_PWR_A_VTT	Schematic Name:	Baseband
Date:	Monday, October 31, 2022	Sheet:	3 of 62

Supported options:  
 1. SW is on by default when VPH\_3V3 is present.  
 2. SW is on by default when VDD\_1M3V3 is present.  
 3. SW is OFF by default. PWR enabled by SW.

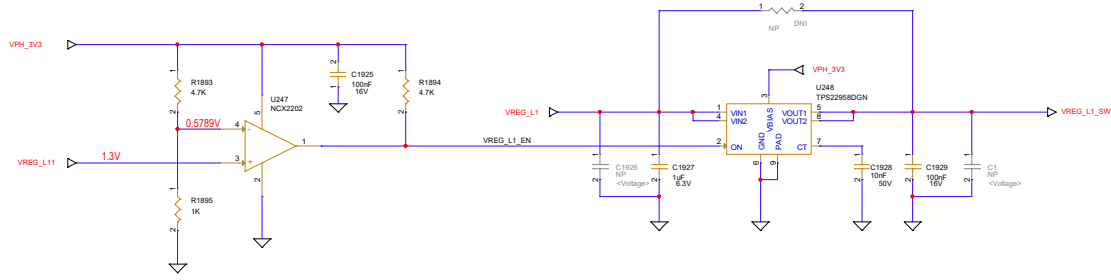
### SGMII 3V3 Power Control



### WIFI 3V3 Power Control

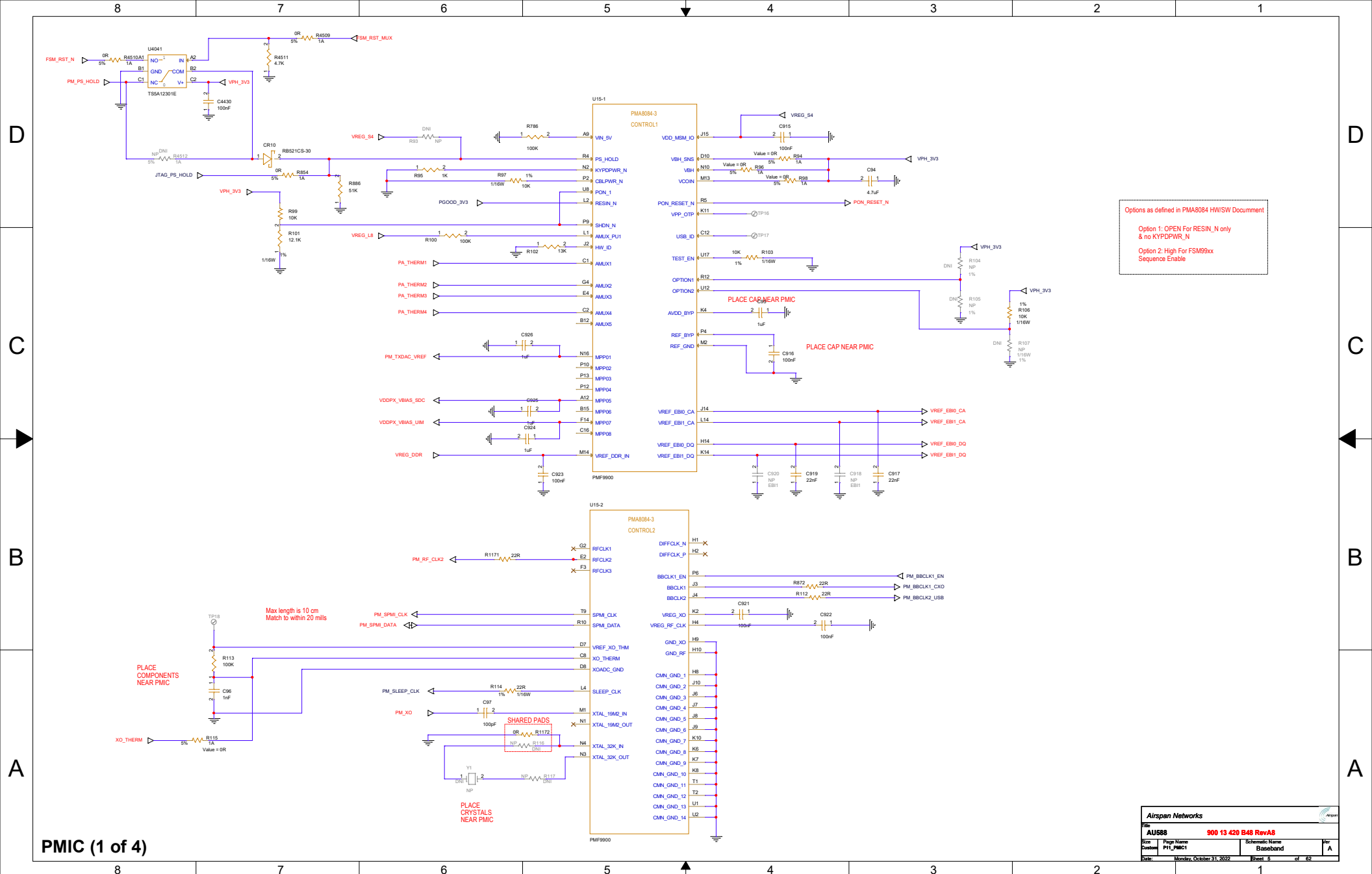


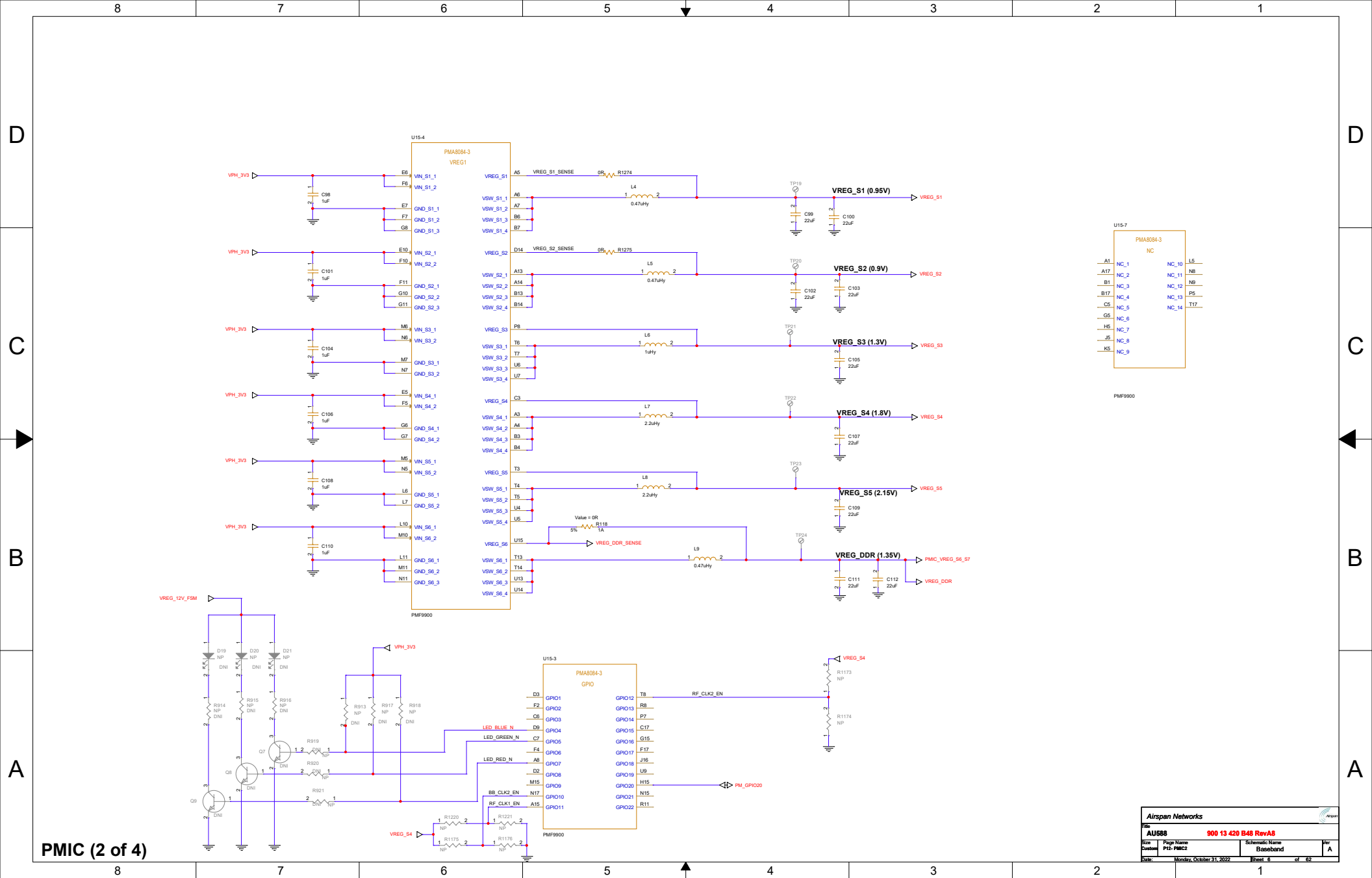
### VREG\_L1 Power Control



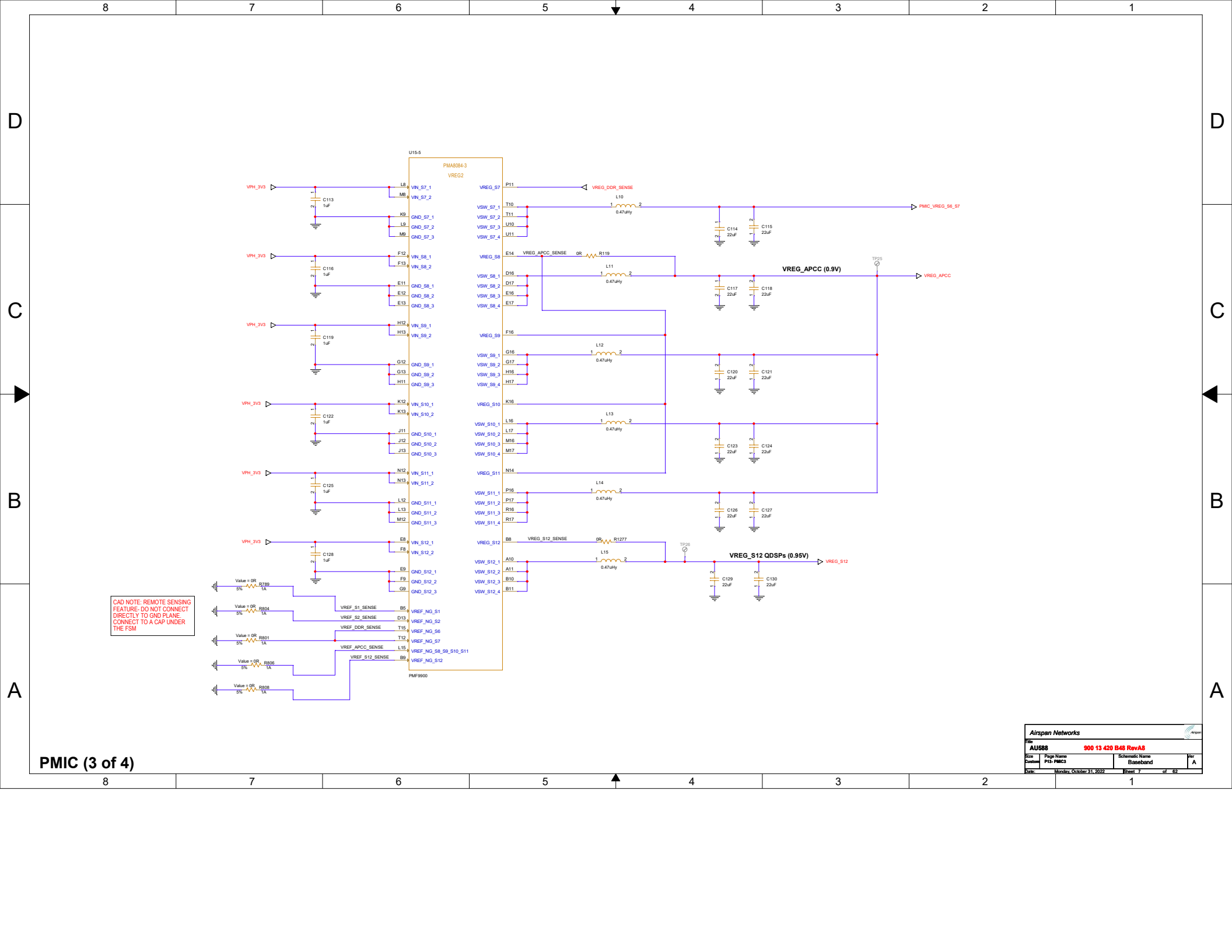
## PCIe & SGMII Power Control

Airspar Networks			
File:	AU588	900 13 420 B48 RevA8	
Rev:	1	900 13 420 B48 RevA8	
Customer:	PCIe-PCs & SGMII Power	Schematic Name	Baseband
Date:	Monday, October 31, 2022	Sheet:	4 of 62





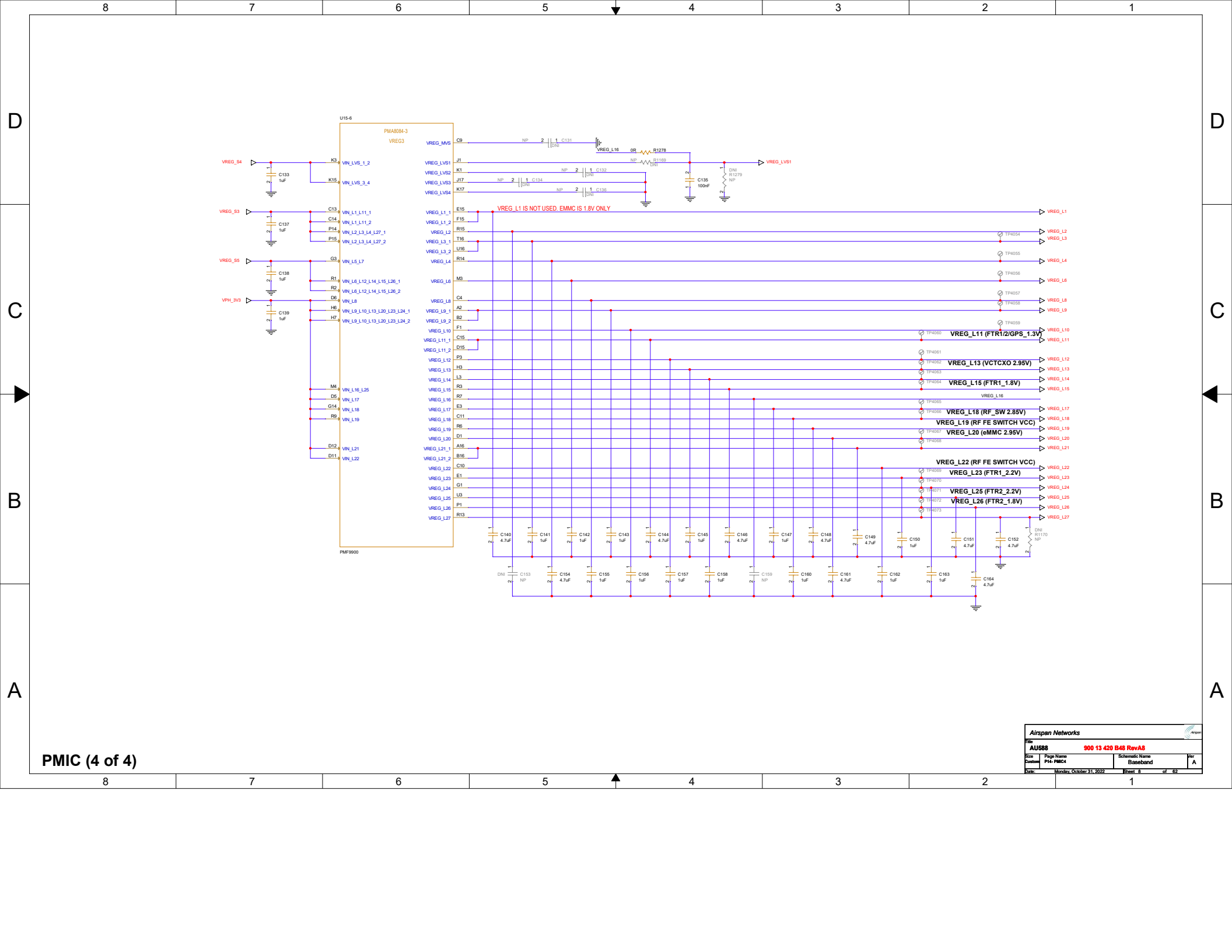
Airsip Networks			
File:	<b>AU588</b>	<b>900 13 420 B48 RevA5</b>	
Rev:	1	Alpha Name	Schematic Name
Custom:	P12-PMIC2	Baseband	Net A
Date:	Monday, October 31, 2022	Sheet 8	of 62



CAD NOTE: REMOTE SENSING FEATURE- DO NOT CONNECT DIRECTLY TO GND PLANE. CONNECT TO A CAP UNDER THE FSM

PMIC (3 of 4)

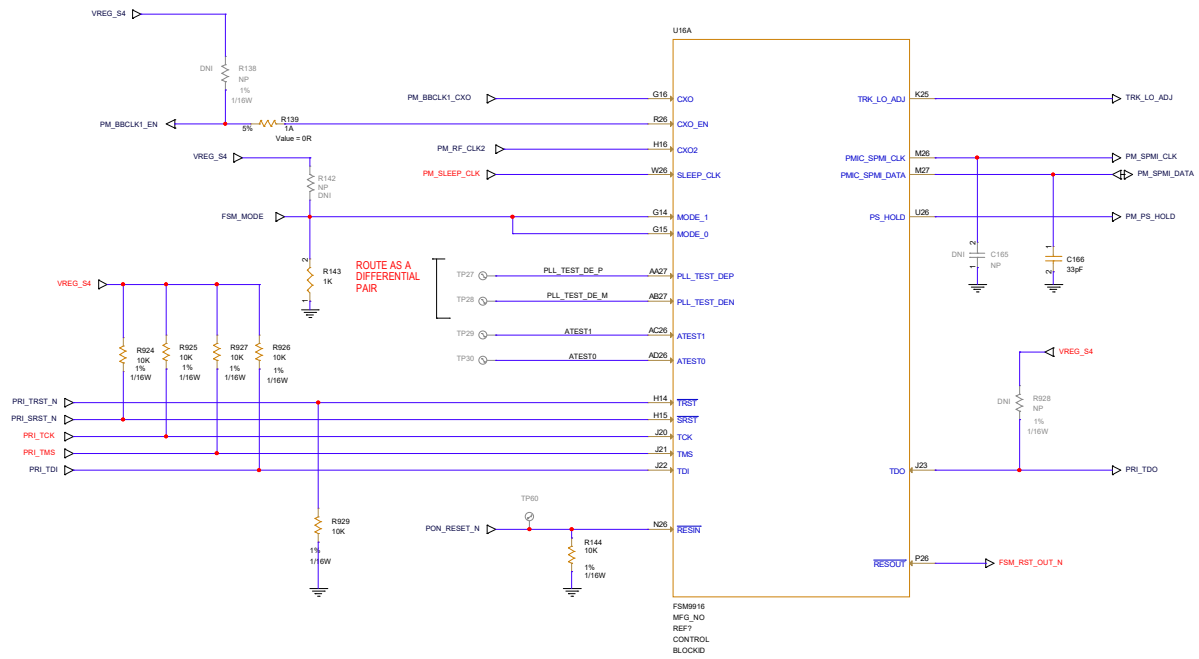
Airspar Networks			
File:	AU588	900 13 420 B48 RevA8	
Rev:	1	Proj Name	Schematic Name
Custom:	P13-PMIC3	Baseband	Net A
Date:	Monday, October 31, 2022	Sheet: 7	of 62



PMIC (4 of 4)

Airspar Networks			
File:	AU588	900 13 420 B48 RevA5	
Rev:	1	Proj Name	Schematic Name
Custom:	P14-PMIC4	Baseband	Rev: A
Date:	Monday, October 31, 2022	Sheet: 8	of 62

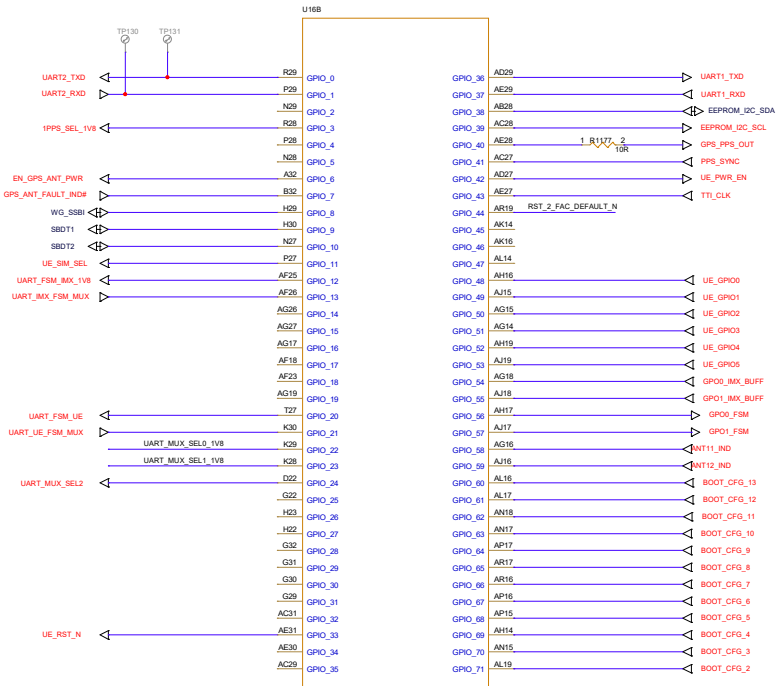
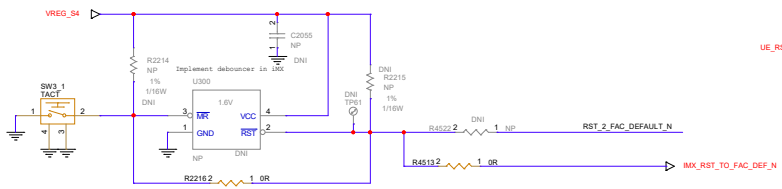
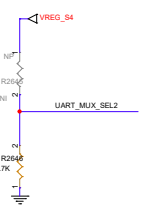
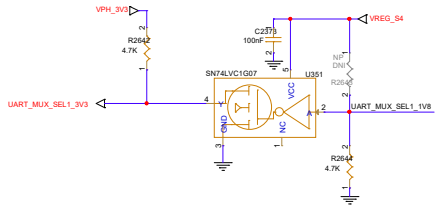
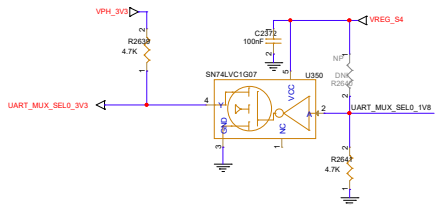




FSM Control

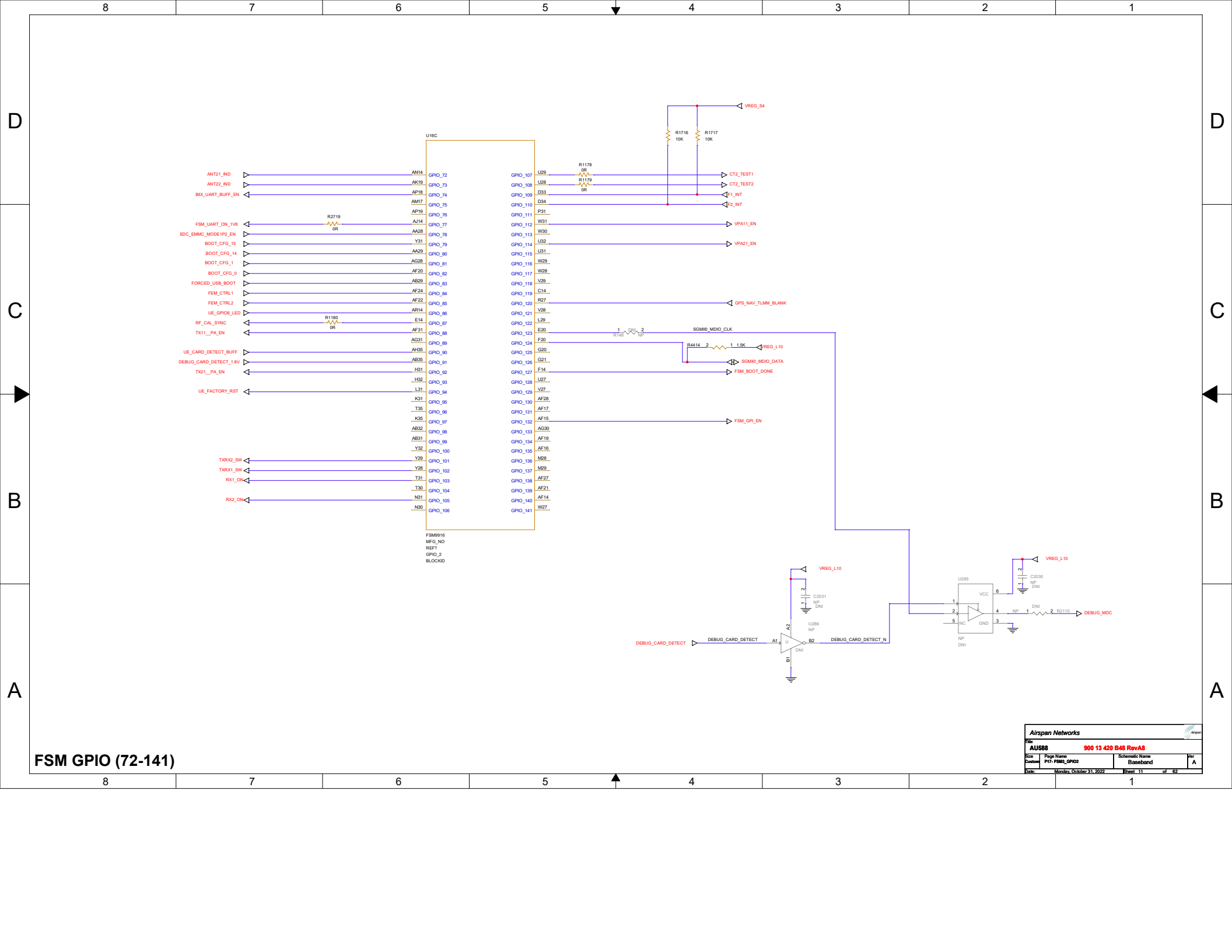
Airspar Networks			
File:	AU588	900 13 420 B48 RevA8	
Size:	1	Uppr Name	Schematic Name
Custom:	P16-FSM1_Control	Baseband	Net A
Date:	Monday, October 31, 2022	Sheet 9	of 62

SSB1 = FTR1  
 SSB2 = FTR2  
 SSB3 = WTR1605 RX  
 SSB4 = WTR1605 TX  
 SSB5 = WTR2605 RX  
 SSB6 = WTR2605 TX  
 SSB7 = WGR7640



FSM GPIO (0-71)

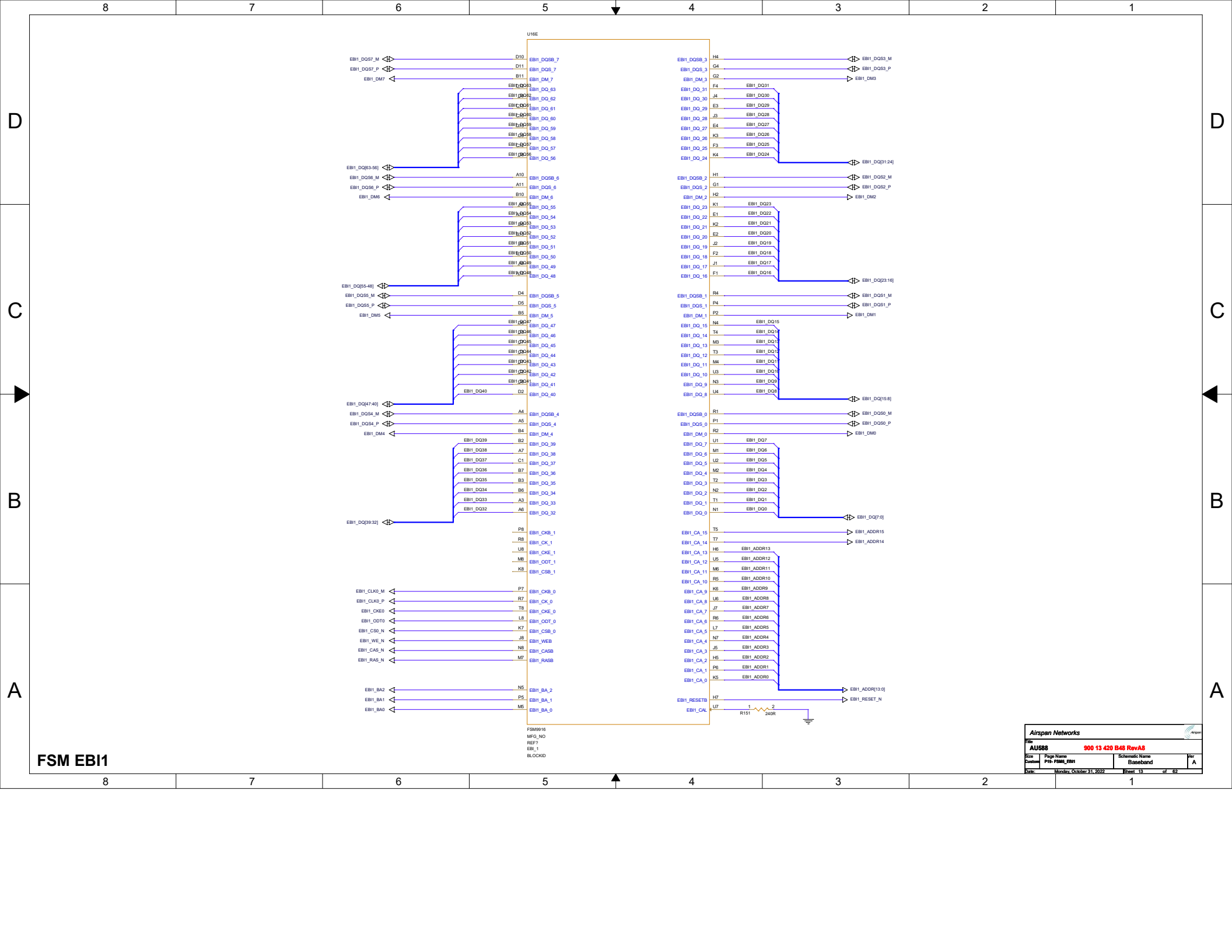
Airspar Networks			
File:	AU588	900 13 420 B48 RevA5	
Rev:	1	Page Name	Schematic Name
Custom:	F16-FSM2_GPIO1	Baseband	Net A
Date:	Monday, October 31, 2022	Sheet 10	of 62



# FSM GPIO (72-141)

Airspar Networks			
File:	AU588	900 13 420 B48 RevA5	
Rev:	1	Signa Name	Schematic Name
Custom:	P17-FSM2_GPIO2	Baseband	Net A
Date:	Monday, October 31, 2022	Sheet 11	of 62

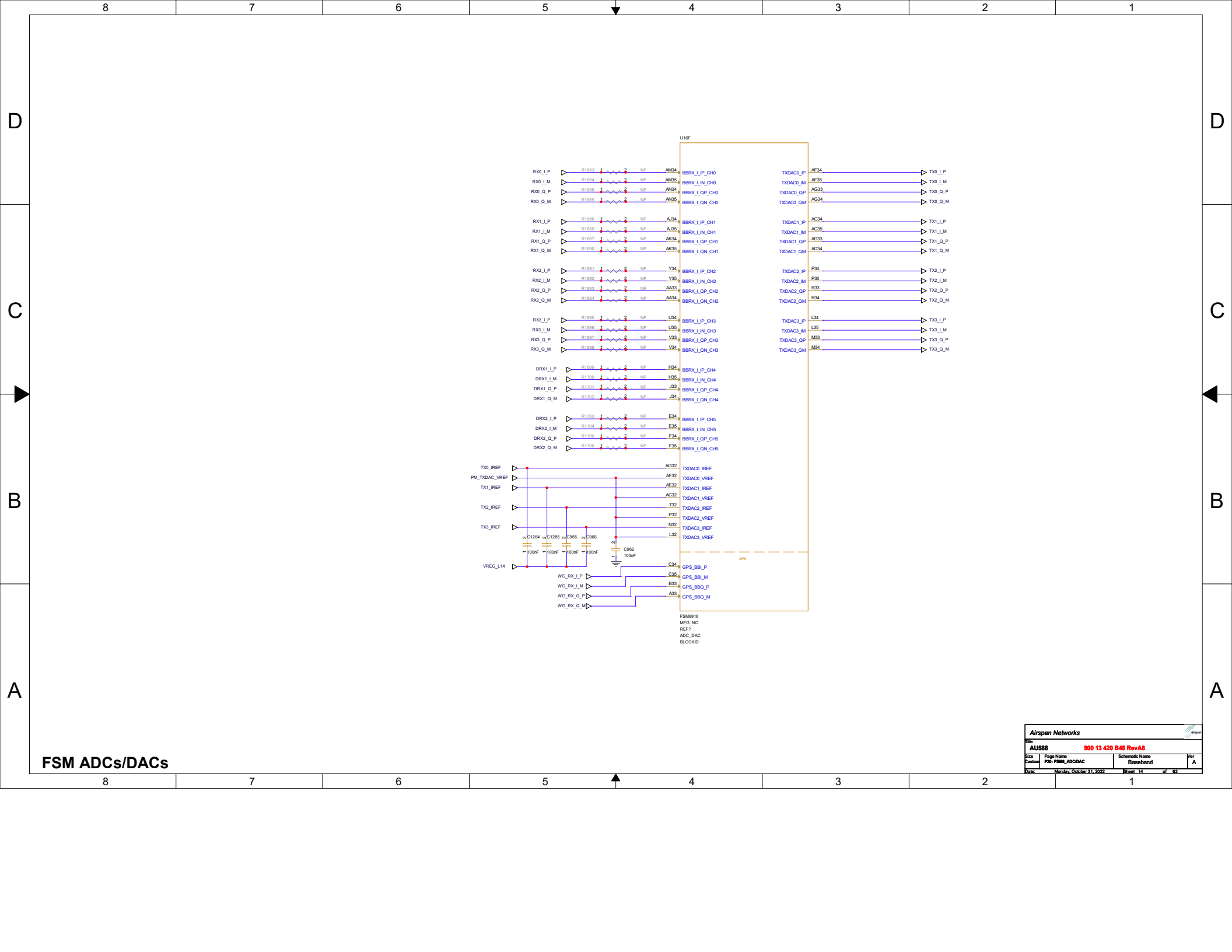




**FSM EB11**

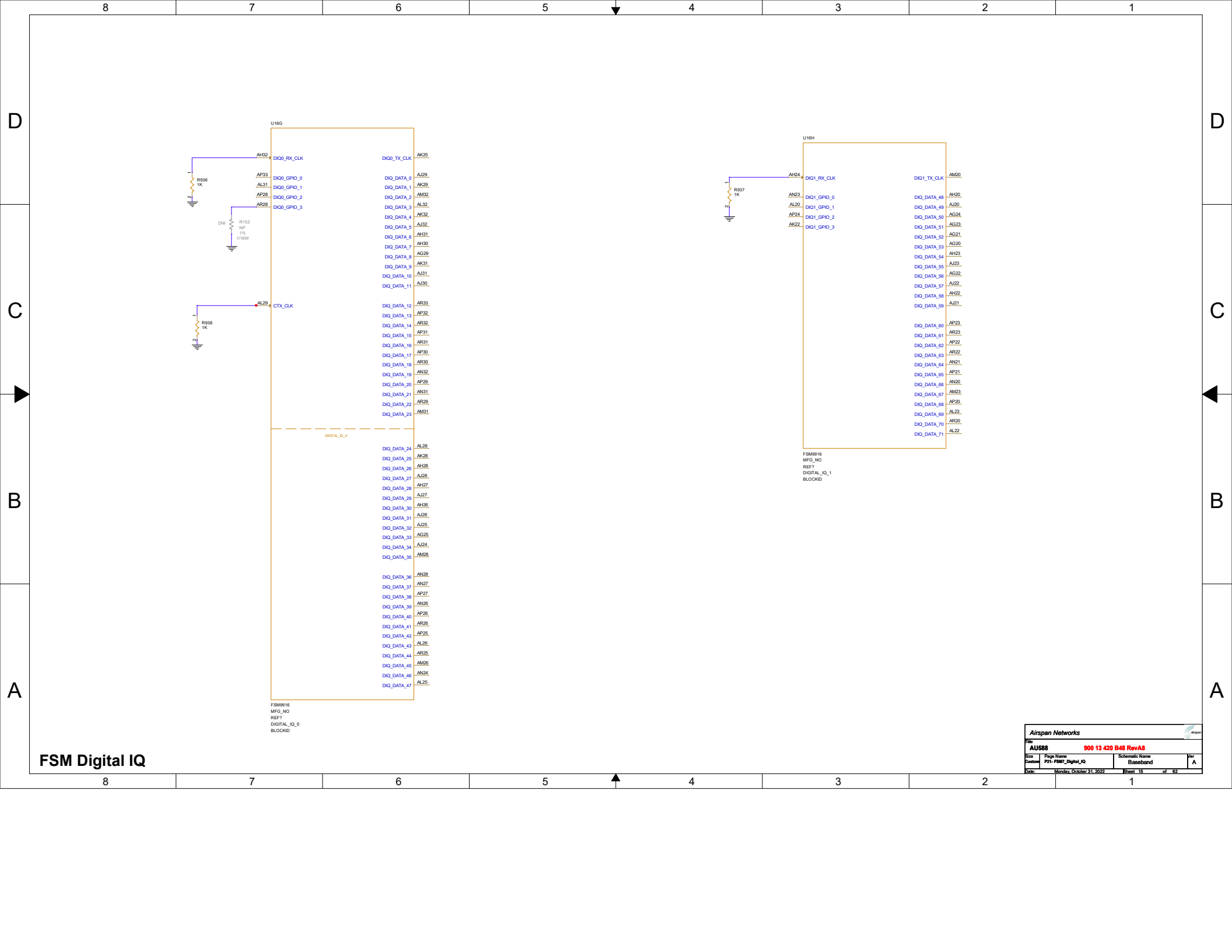
FSM0916  
MFG\_NO  
REF7  
EB1\_1  
BLOCKID

<b>Airspan Networks</b>			
File:	<b>AU588</b>	<b>900 13 420 B48 RevA5</b>	
Rev:	1	Proj Name	Schematic Name
Customer:	PH-FSM0_EB11	Baseband	Net A
Date:	Monday, October 31, 2022	Sheet 13	of 62



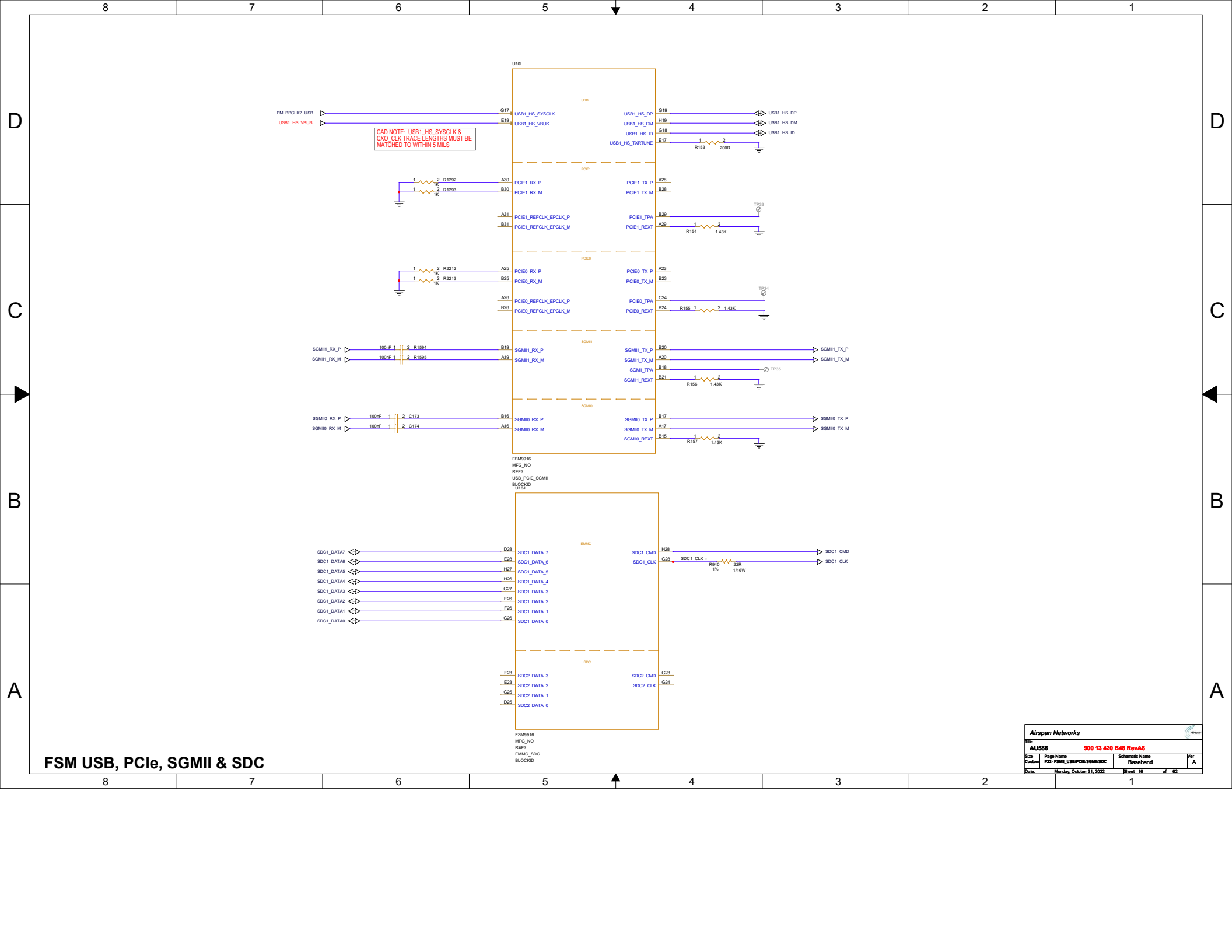
**FSM ADCs/DACs**

Airspan Networks			
File:	AU588	900 13 420 B48 RevA8	
Sheet:	FSM_ADCDAC	Schematic Name:	Baseband
Date:	Monday, October 31, 2022	Sheet:	14 of 62



FSM Digital IQ

Airspar Networks			
File:	900 13 420 B48 RevA8		
Part:	FSM9916	Schema Name:	Baseband
Customer:	FSM-Digital_IQ	Sheet:	15 of 62
Date:	Monday, October 31, 2022		

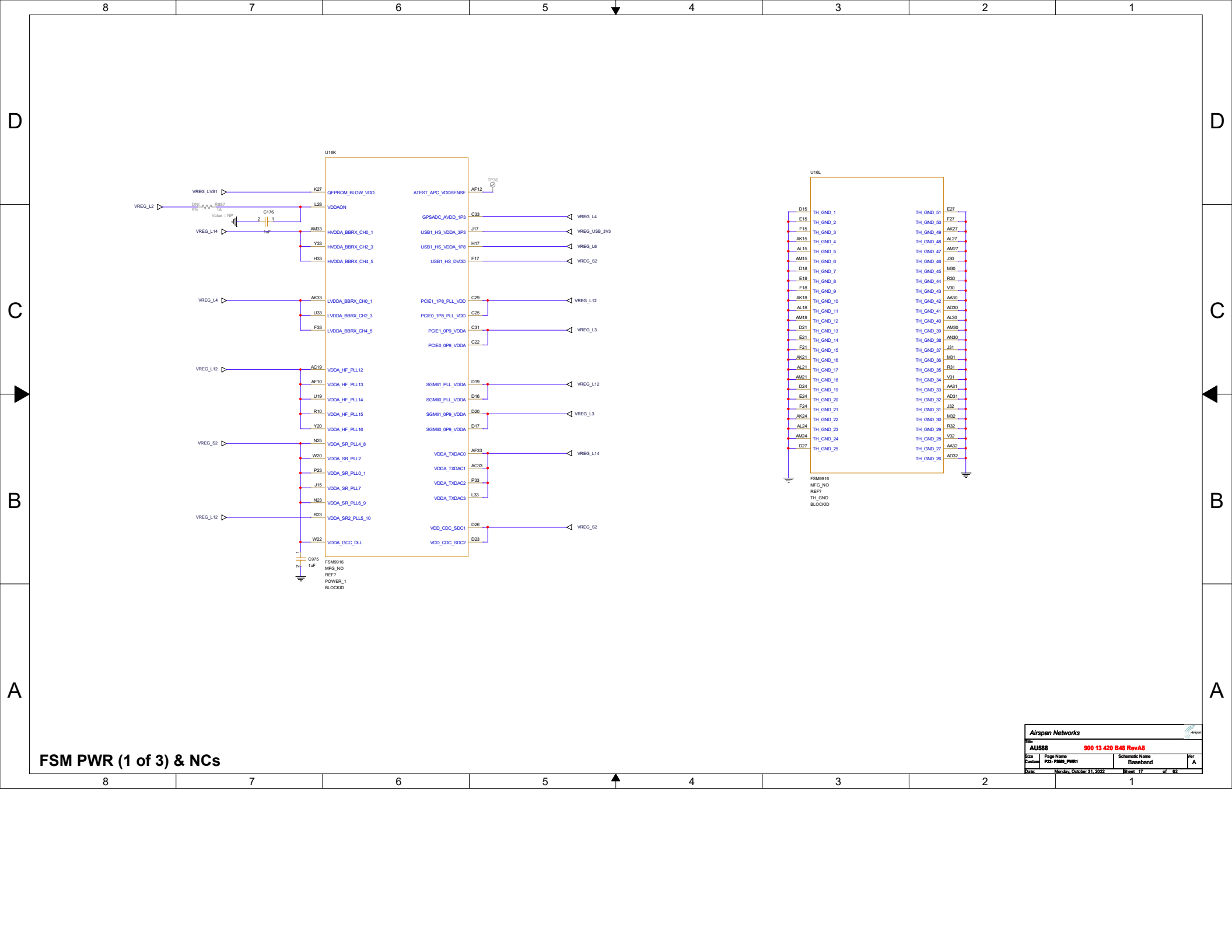


CAD NOTE: USB1\_HS\_SYSDCLK & CLK0\_CLK TRACE LENGTHS MUST BE MATCHED TO WITHIN 5 MILLS

**FSM USB, PCIe, SGMII & SDC**

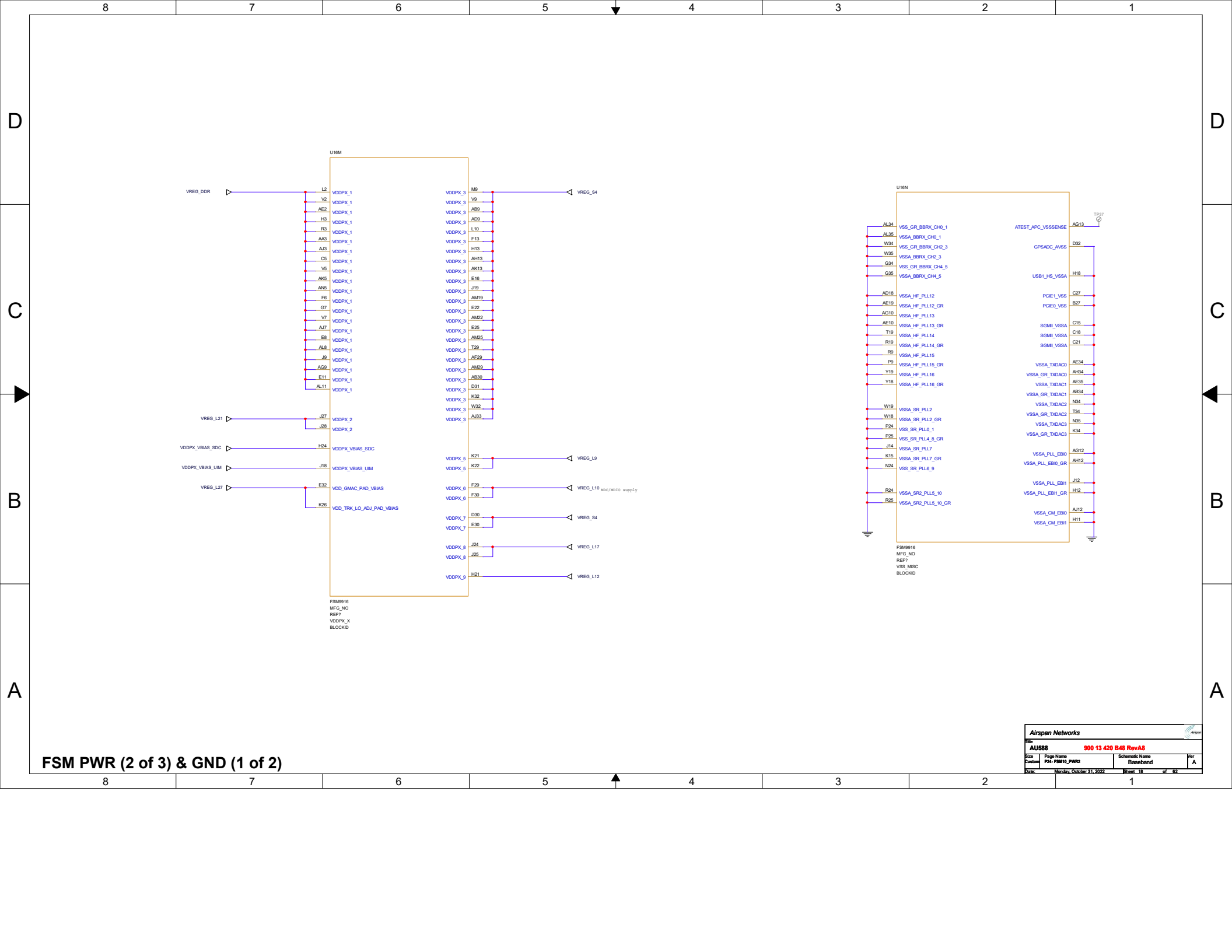
<b>Airspan Networks</b>			
File:	<b>AU588</b>	<b>900 13 420 B48 RevA8</b>	
Rev:	1	Proj Name	FSM_USB_PCIE_SGMII_SDC
Customer:		Schematic Name	Baseband
Date:	Monday, October 31, 2022	Sheet	16 of 62





FSM PWR (1 of 3) & NCs

Airspar Networks			
File:	AU588	900 13 420 B48 RevA8	
Sheet:	1	Page Name:	Baseband
Customer:	F25-FSM9_PWR1	Schematic Name:	Baseband
Date:	Monday, October 31, 2022	Sheet:	17 of 62

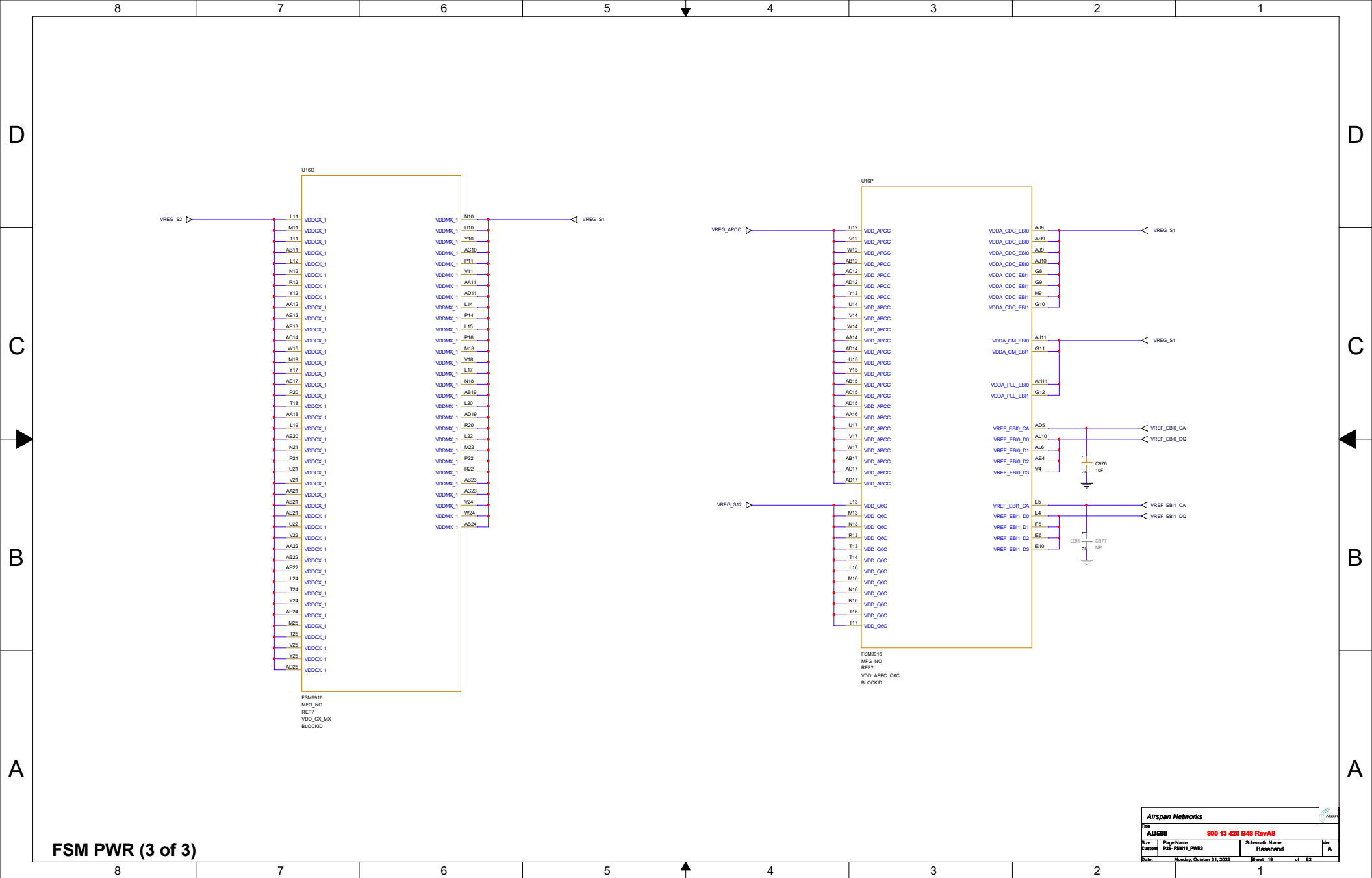


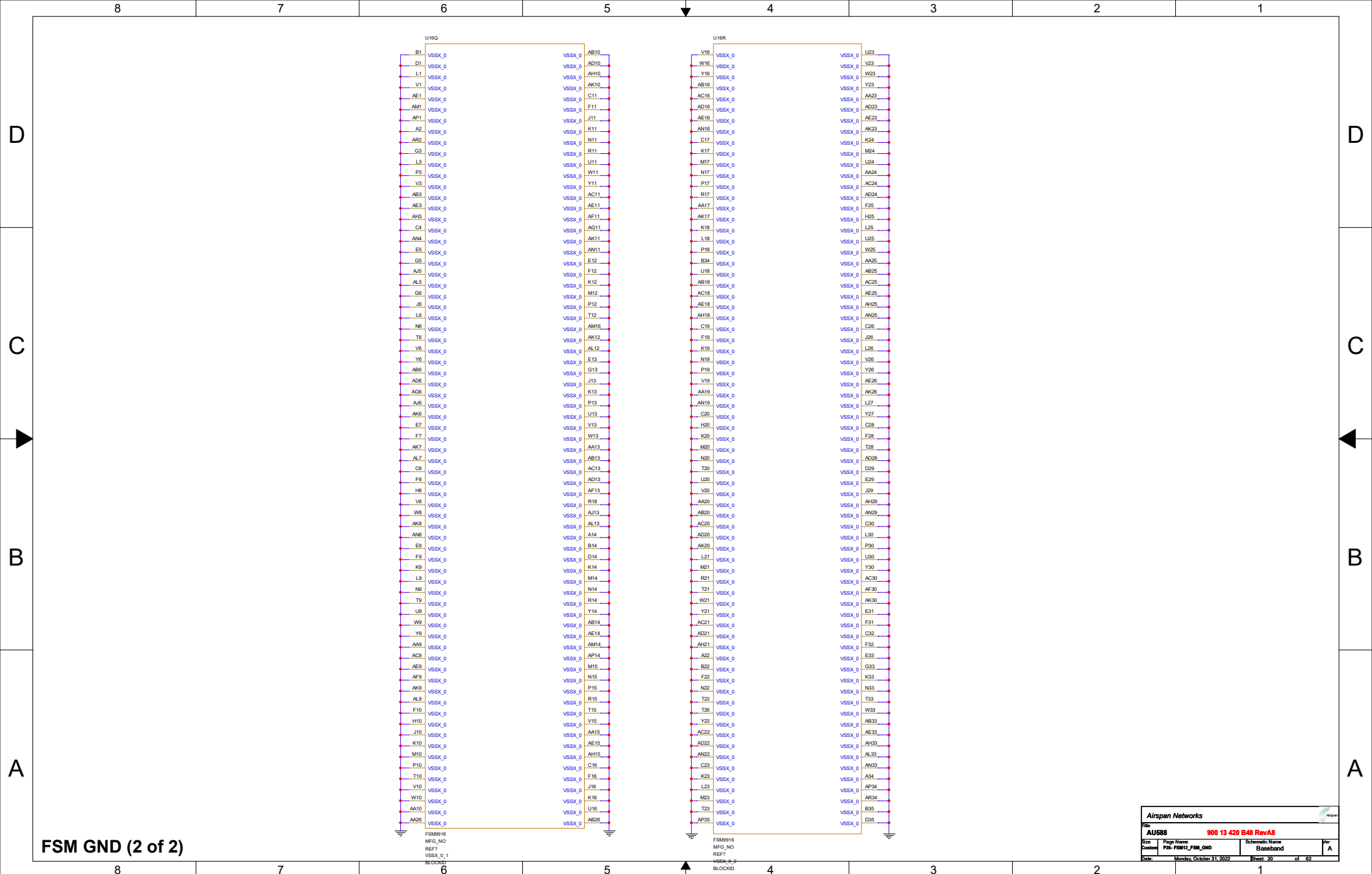
FSM9916  
MFG\_NO  
REF1  
VDDPX\_X  
BLOCKID

FSM9916  
MFG\_NO  
REF1  
VSS\_MISC  
BLOCKID

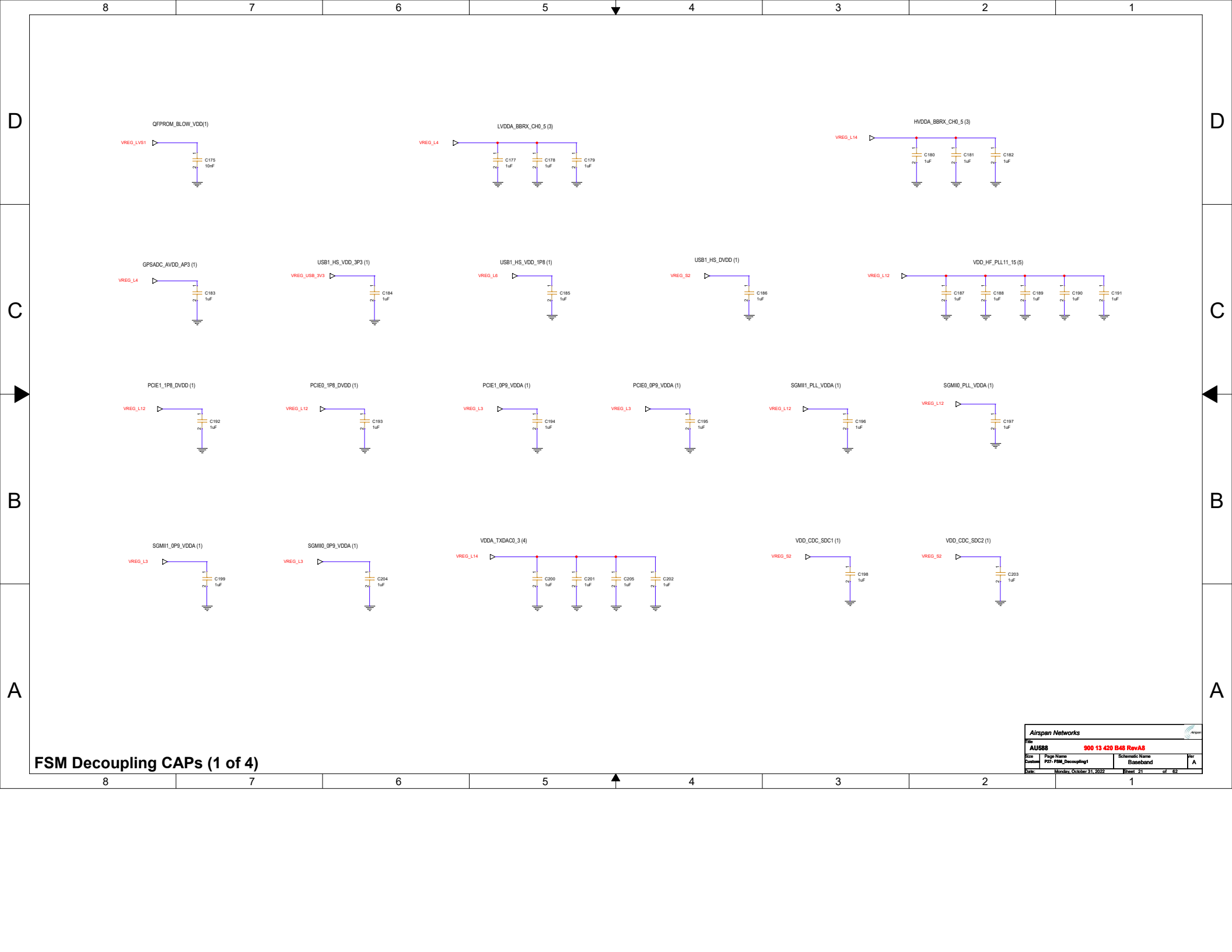
FSM PWR (2 of 3) & GND (1 of 2)

Airspar Networks			
File:	AU588	900 13 420 B48 RevA8	
Item:	1	Sign Name	Schematic Name
Customer:	F24-F2810_PWR2	Baseband	Net A
Date:	Monday, October 31, 2022	Sheet 18	of 62





<b>Airspan Networks</b>			
File:	<b>AU588</b>	<b>900 13 420 B48 RevA5</b>	
Rev:	1	File Name	Schematic Name
Customer:	F2S-F2812_FSM_GND	Baseband	Net A
Date:	Monday, October 31, 2022	Sheet 20	of 62



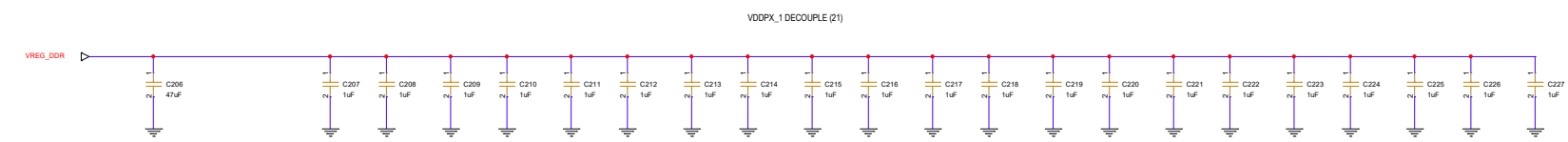
**FSM Decoupling CAPs (1 of 4)**

Airspar Networks			
File:	900 13 420 B48 RevA8		
Size:	1	Page Name:	FSM_Decoupling1
Customer:	P27-FSM_Decoupling1	Schematic Name:	Baseband
Date:	Monday, October 31, 2022	Sheet:	21 of 62

8 7 6 5 4 3 2 1

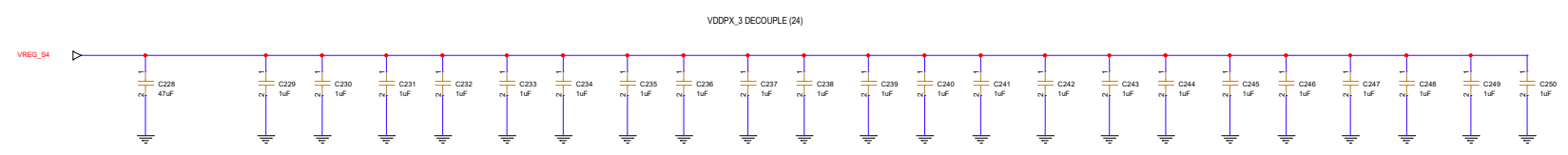
D

D



C

C



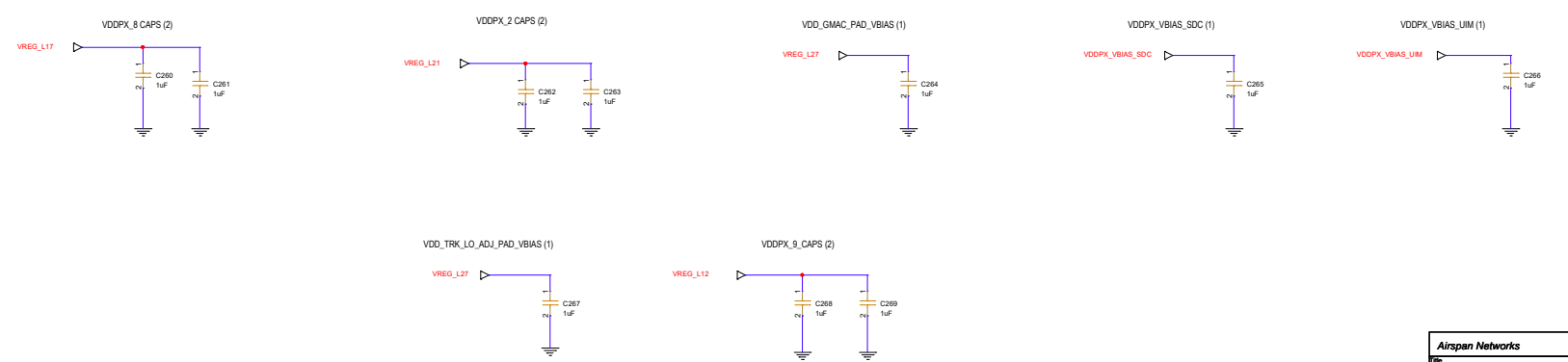
B

B



A

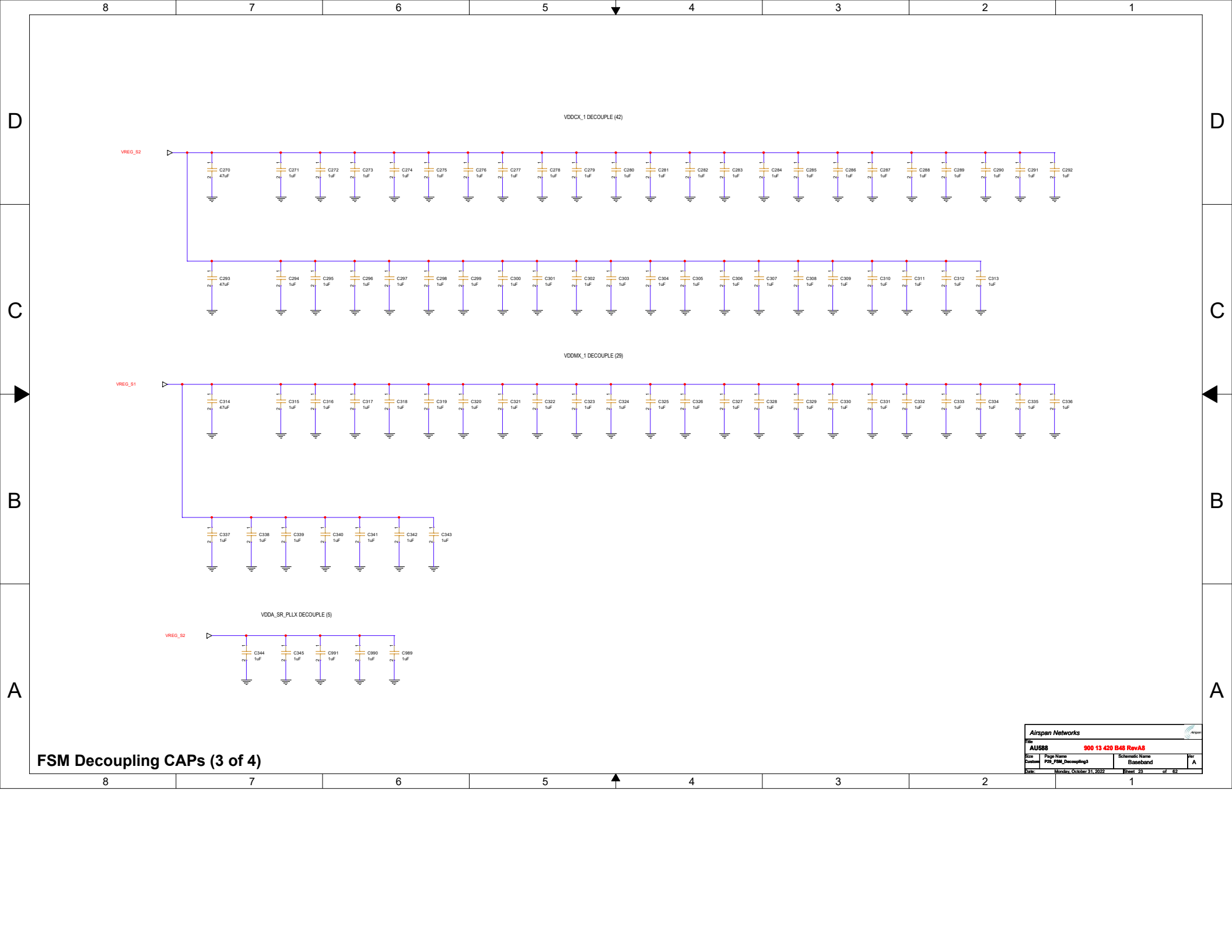
A



### FSM Decoupling CAPs (2 of 4)

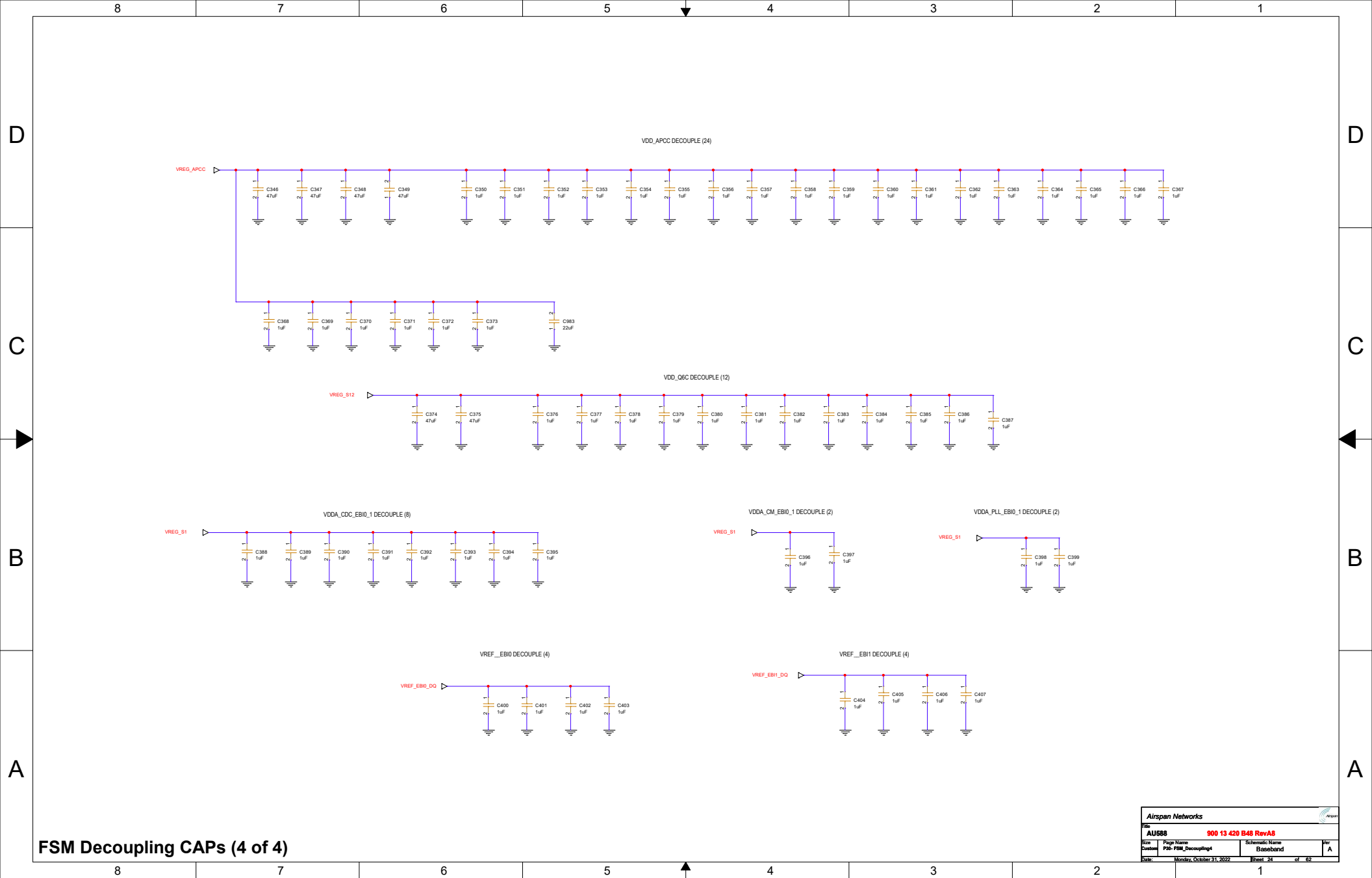
8 7 6 5 4 3 2 1

Airspar Networks			
File	AU588	900 13 420 B48 RevA8	
Rev	1	Alpha Name	Schema Name
Custom	FSM_Decoupling2	Baseband	Net A
Date	Monday, October 31, 2022	Sheet 22	of 62



FSM Decoupling CAPs (3 of 4)

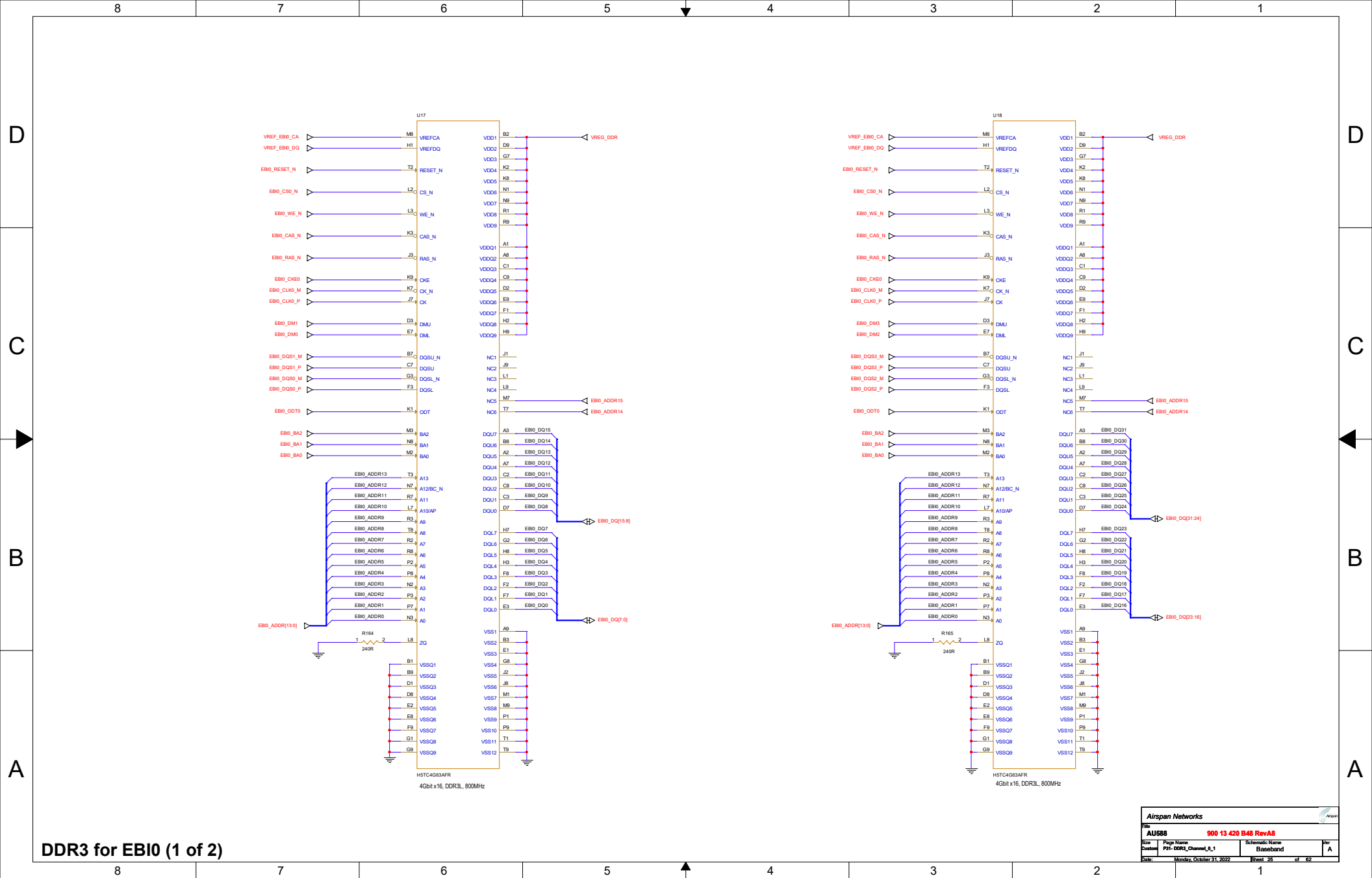
Airspar Networks			
File:	900 13 420 B48 RevA8		
Part:	900 13 420 B48 RevA8	Schematic Name:	
Customer:	FSM_Decoupling3	Schematic Name:	Baseband
Date:	Monday, October 31, 2022	Sheet:	23 of 62



**FSM Decoupling CAPs (4 of 4)**

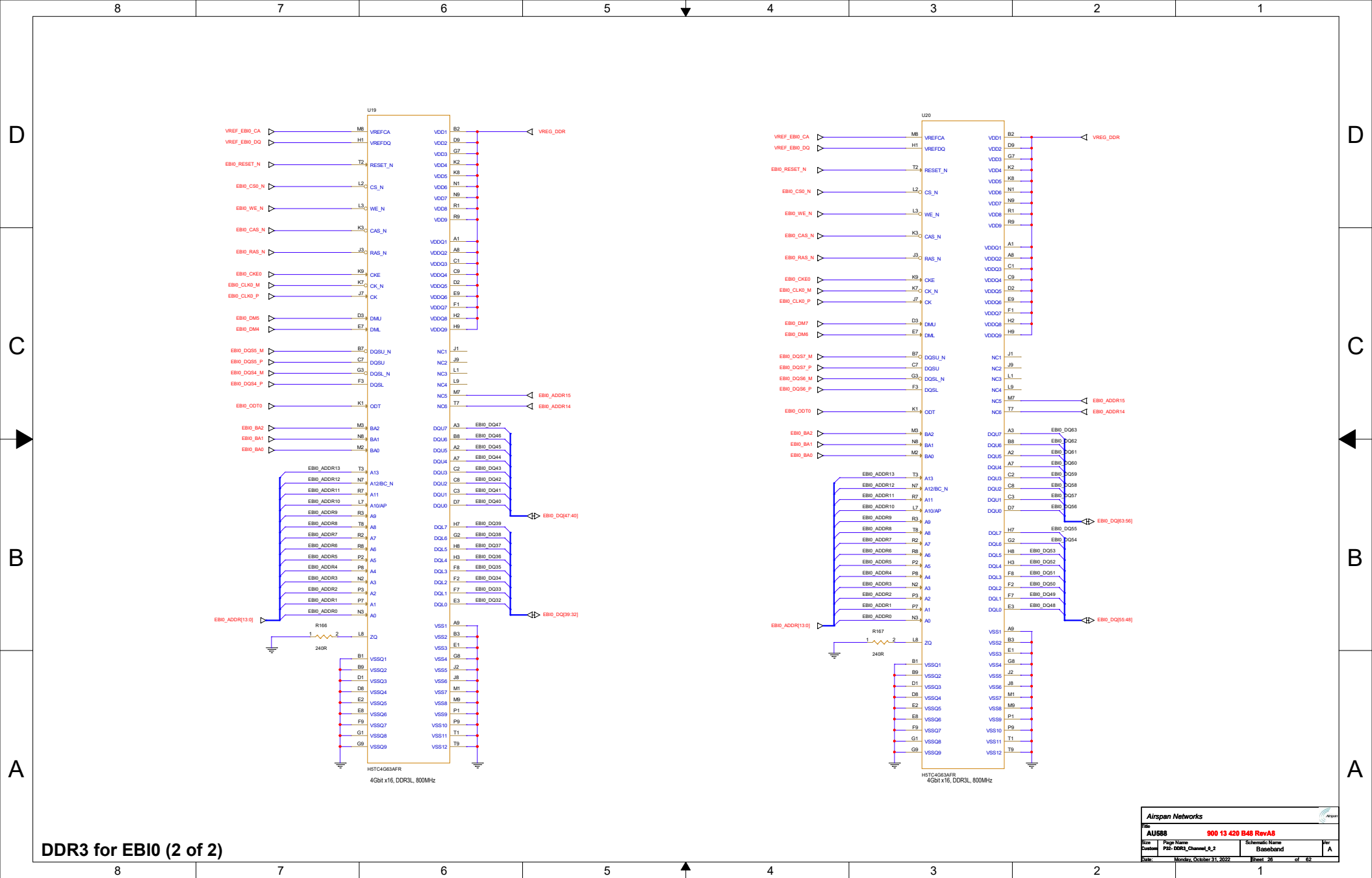
Airspar Networks			
File:	AU588	900 13 420 B48 RevA8	
Sheet:	1	Page Name:	FSM_Decoupling4
Customer:	FSM-FSM_Decoupling4	Schematic Name:	Baseband
Date:	Monday, October 31, 2022	Sheet:	24 of 62





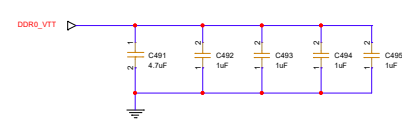
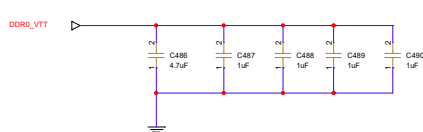
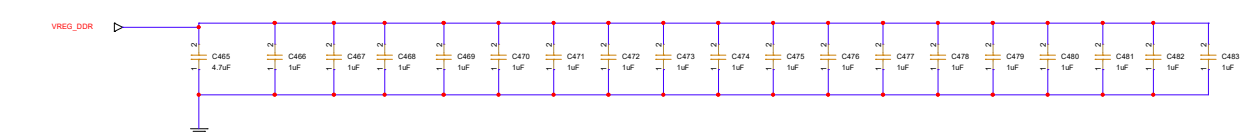
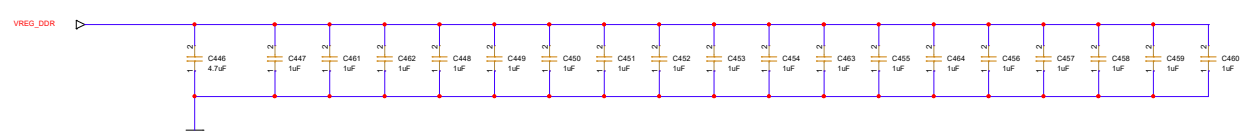
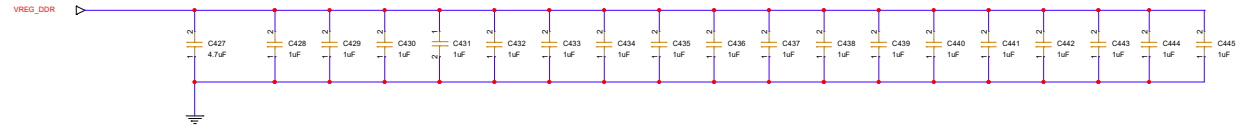
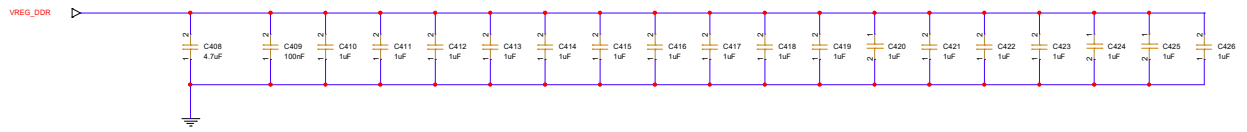
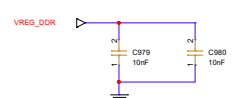
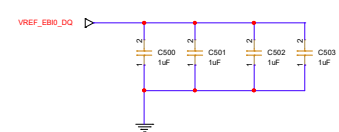
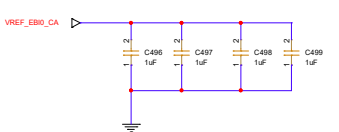
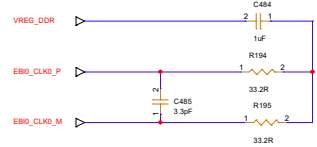
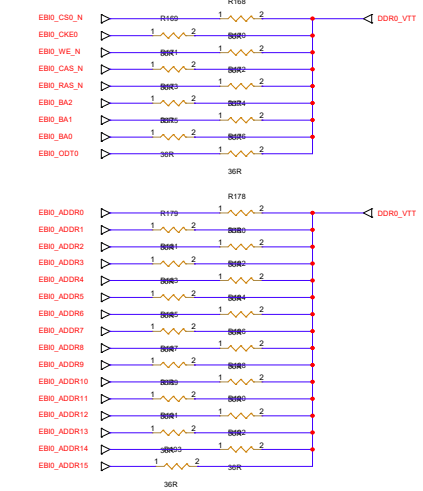
DDR3 for EBIO (1 of 2)

Airspar Networks		File: AU588		900 13 420 B48 RevA8	
Rev: 1	Page Name: P01-DDR3_Channel_8_1	Schematic Name: Baseband		Net: A	
Date: Monday, October 31, 2022	Sheet: 28		of 62		



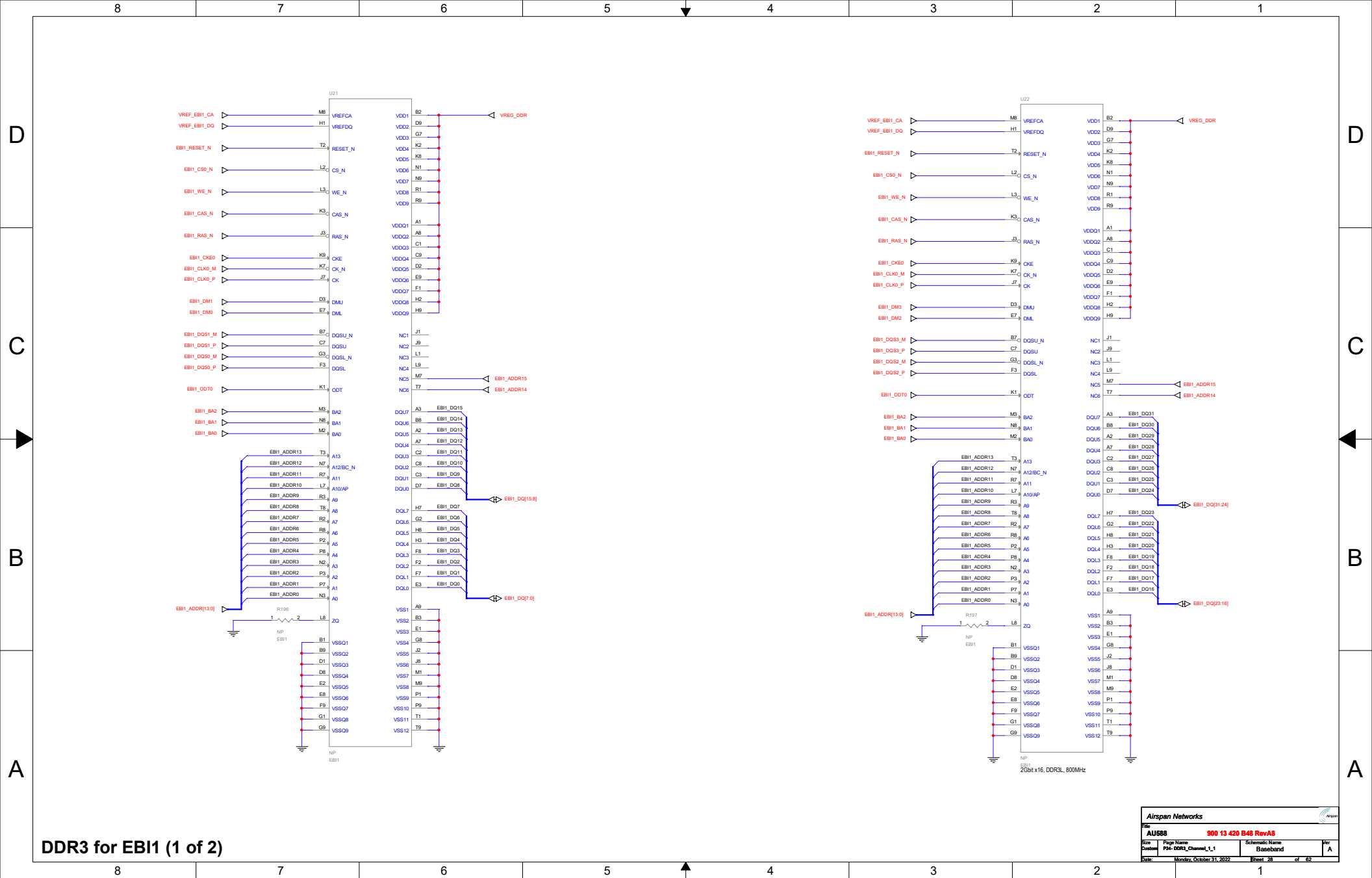
DDR3 for EBIO (2 of 2)

Airspar Networks			
File:	AU588	900 13 420 B48 RevA5	
Sheet:	1	Page Name: P02-DDR3_Channel_0_2	Schematic Name: Baseband
Customer:			
Date:	Monday, October 31, 2022	Sheet: 28	of 62



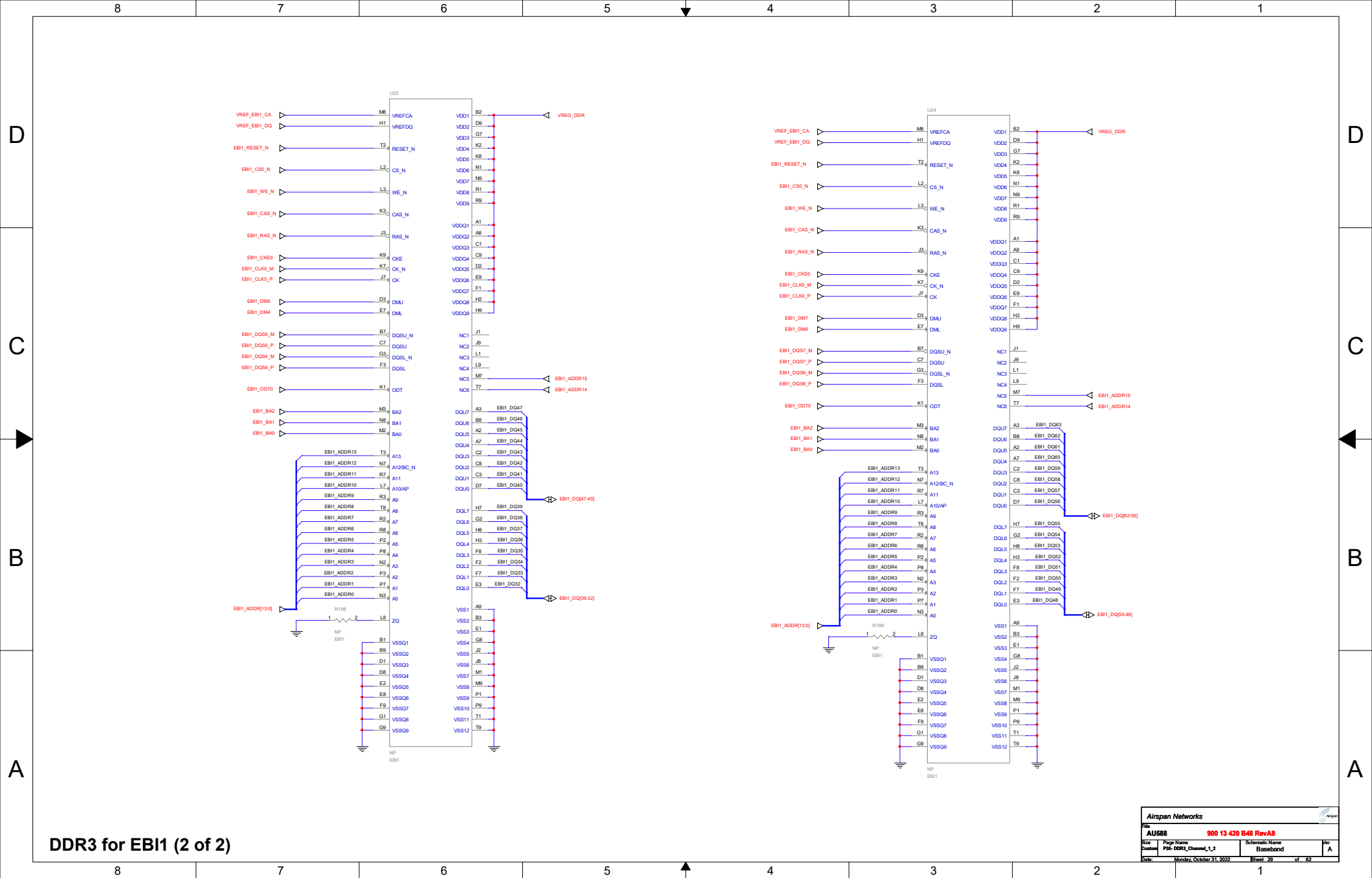
# EBI0 Termination and Decoupling

Airspar Networks			
File:	AU588	900 13 420 B48 RevA8	
Rev:	1	File Name	Schematic Name
Customer:	F33-DDR0_Term_A-Decouple	Baseband	Net: A
Date:	Monday, October 31, 2022	Sheet: 27	of 62

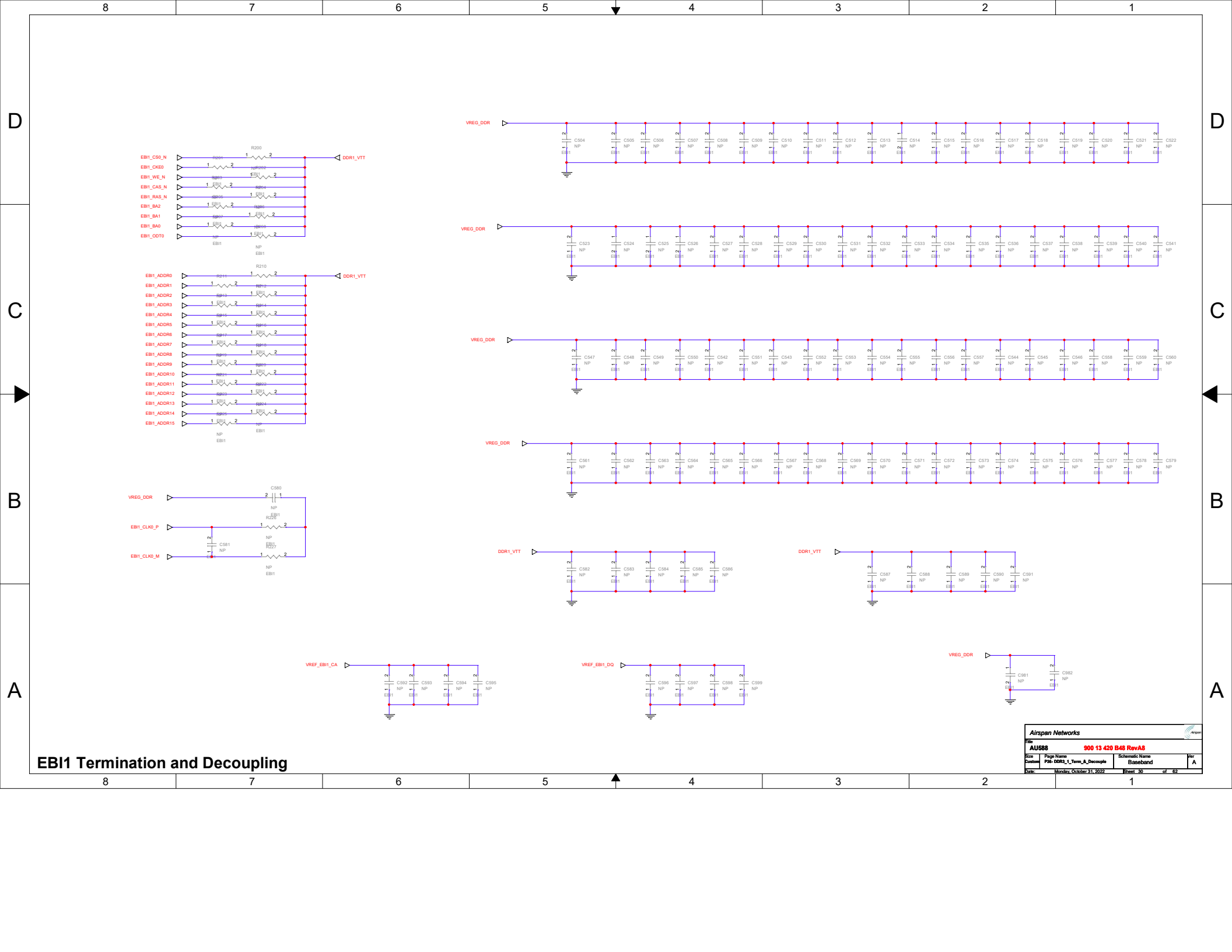


DDR3 for EB11 (1 of 2)

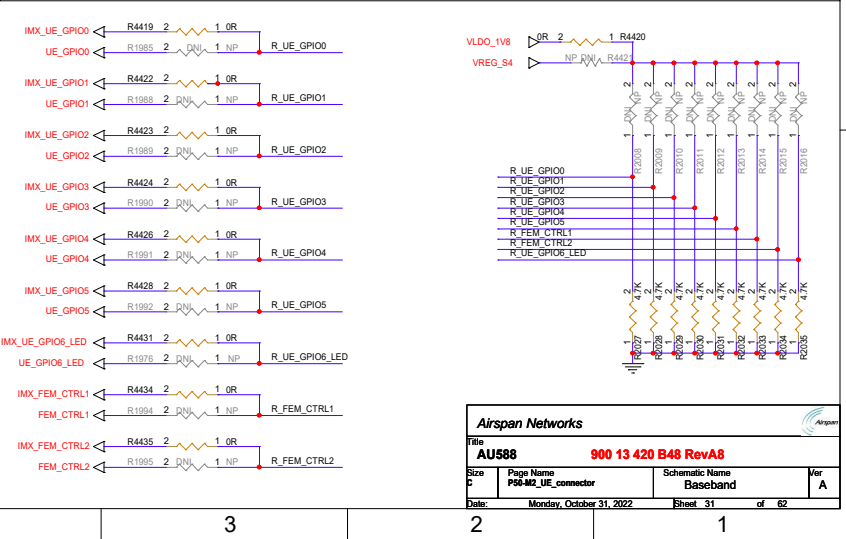
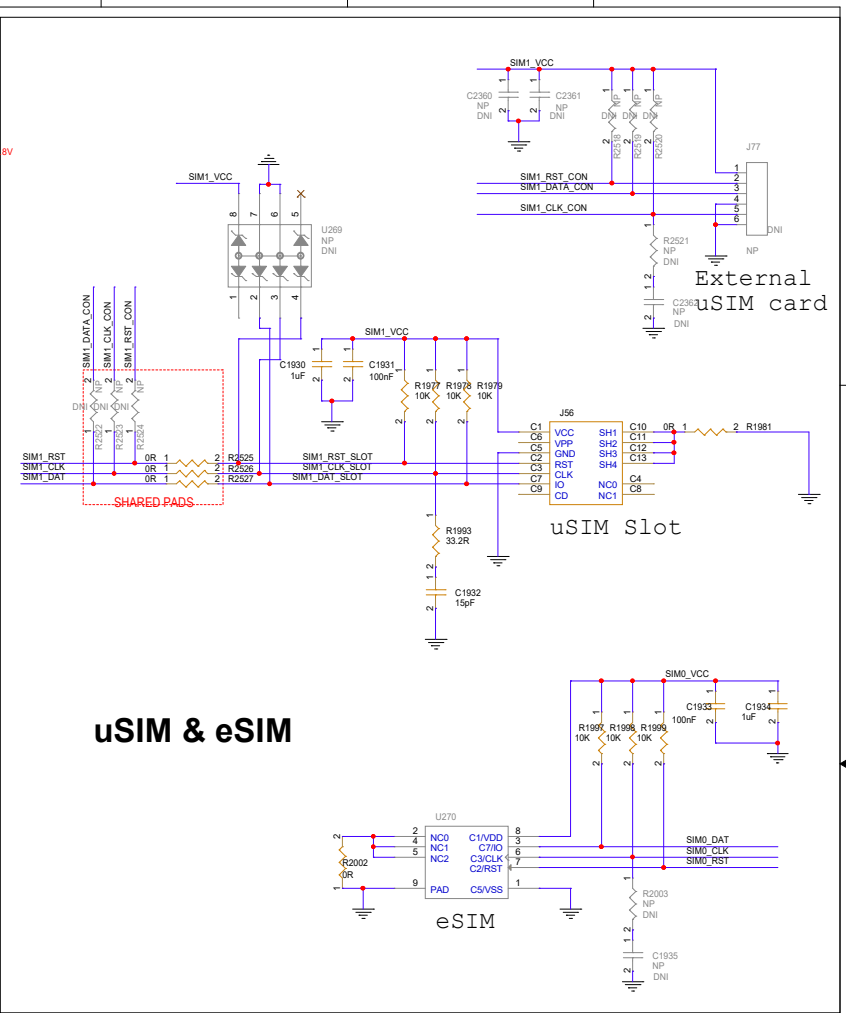
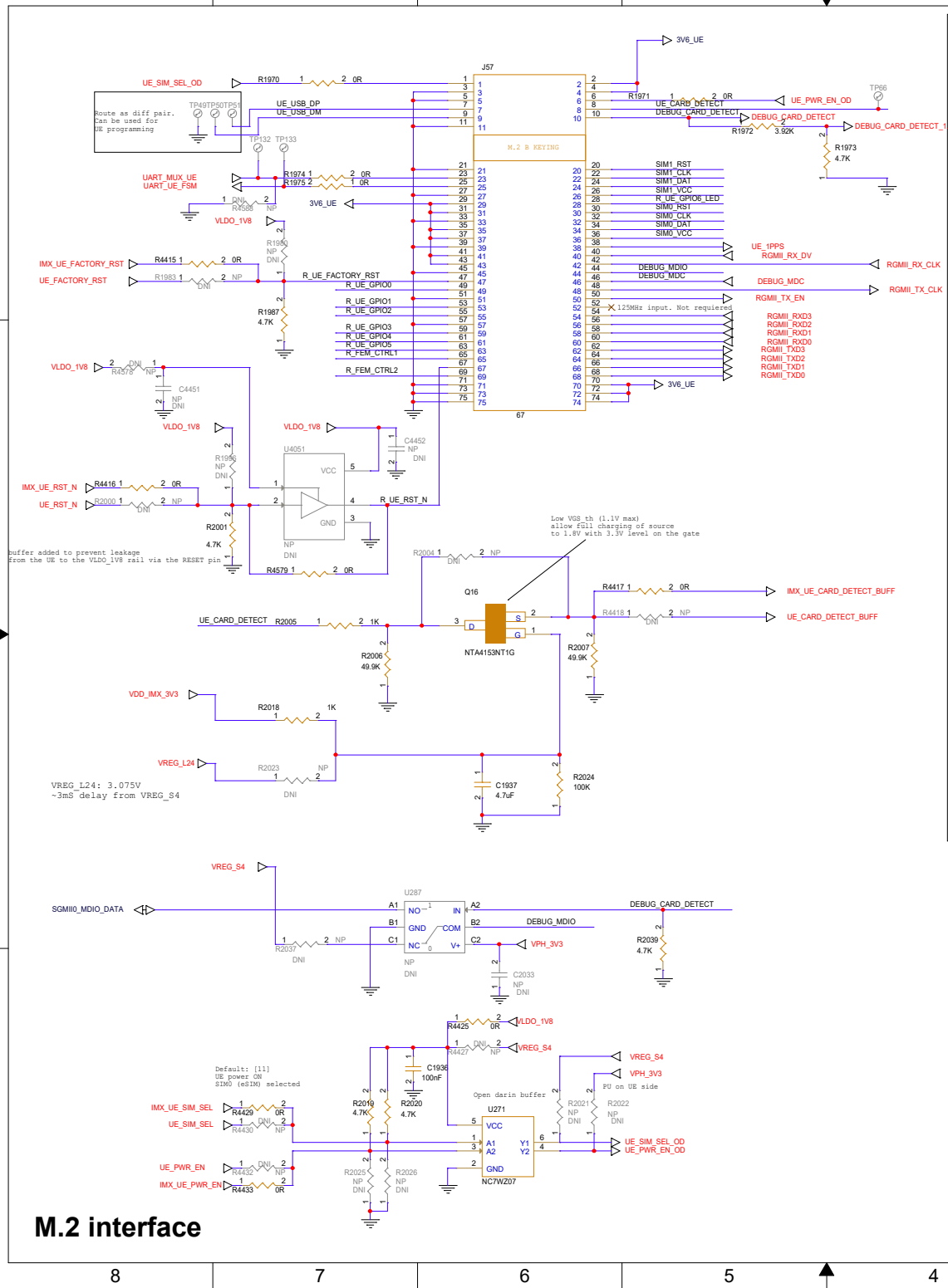
Airspar Networks			
File:	AU588	900 13 420 B48 RevA5	
Sheet:	1	Page Name:	F04-DDR3_Channel_1_1
Customer:		Schematic Name:	Baseband
Date:	Monday, October 31, 2022	Sheet:	28 of 62



DDR3 for EB11 (2 of 2)



# EBI1 Termination and Decoupling



<b>Airspan Networks</b>			
File	AU588 900 13 420 B48 RevA8		
Size	Page Name	Schematic Name	Ver
P	P00-M2_UE_connector	Baseband	A
Date:	Monday, October 31, 2022	Sheet 31	of 62

8 7 6 5 4 3 2 1

D

D

C

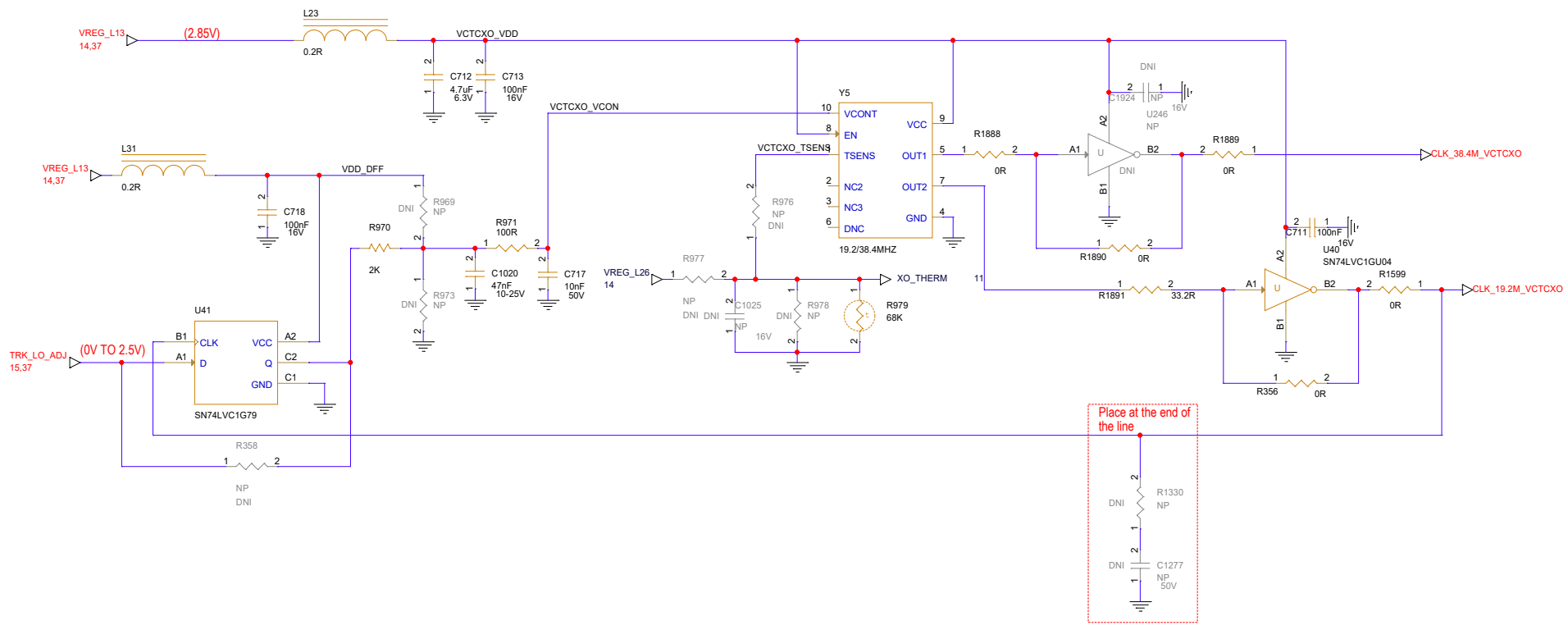
C

B

B

A

A



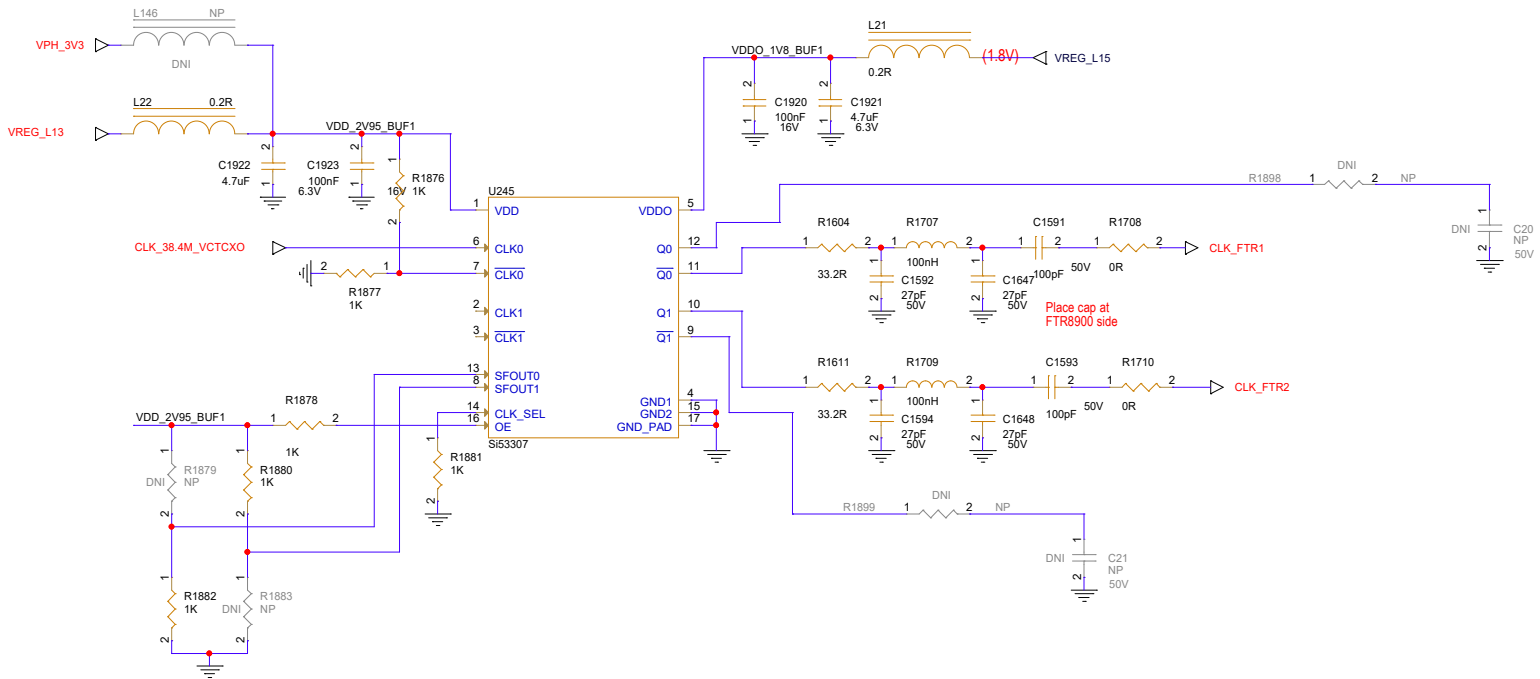
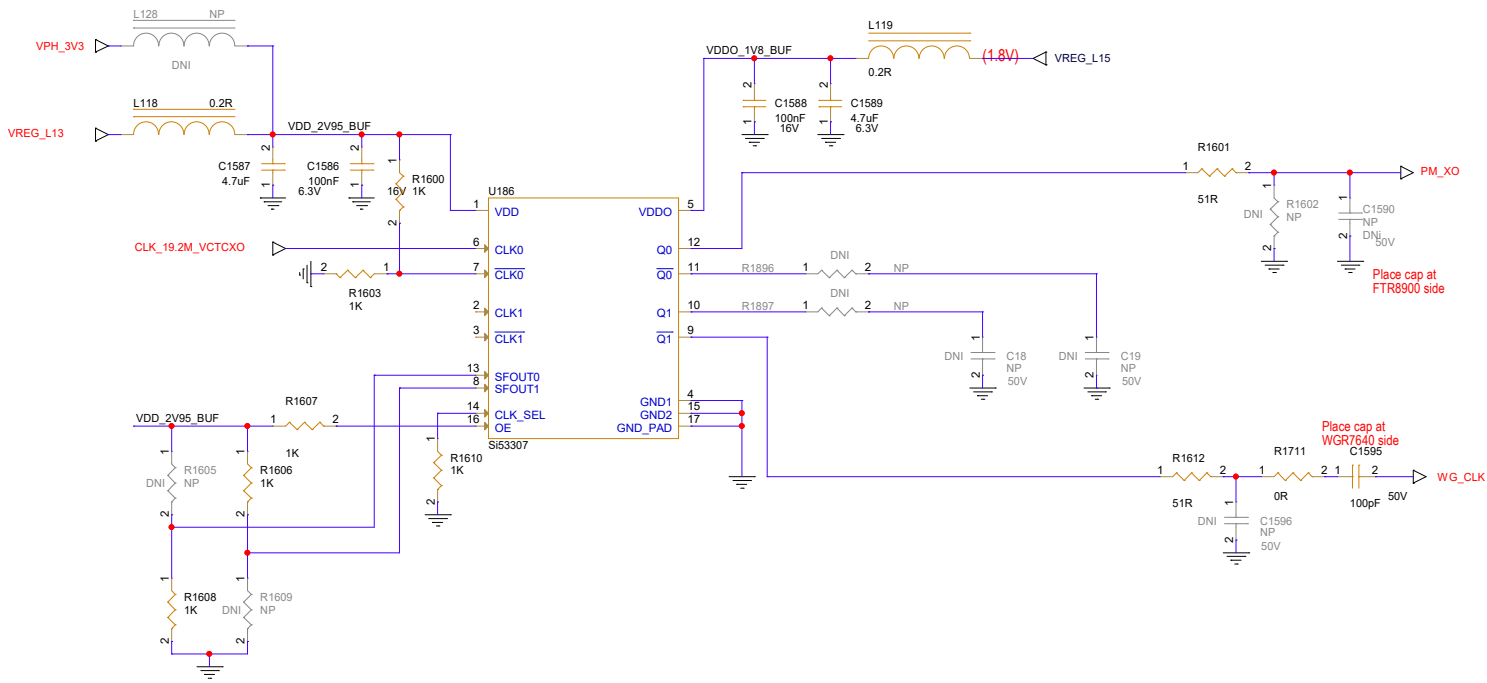
Place at the end of the line

# 19.2 MHz Clock

Airspan Networks			
Title <b>AU588</b> <b>900 13 420 B48 RevA8</b>			
Size <b>A3</b>	Page Name <b>P62- VCTCXO</b>	Schematic Name <b>Baseband</b>	Ver <b>A</b>
Date: <b>Monday, October 31, 2022</b>	Sheet <b>32</b> of <b>62</b>		

8 7 6 5 4 3 2 1

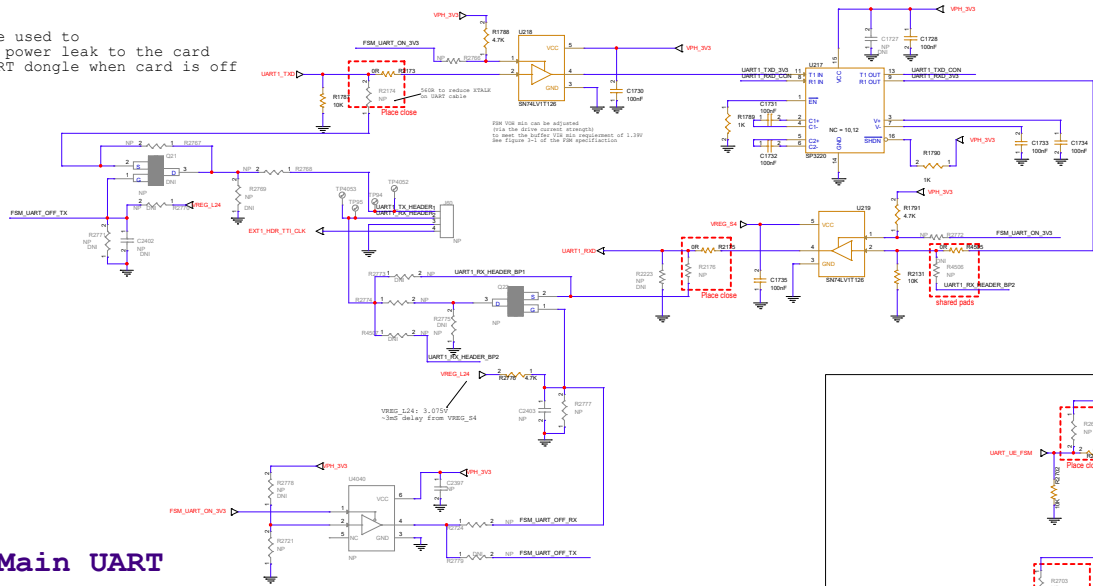




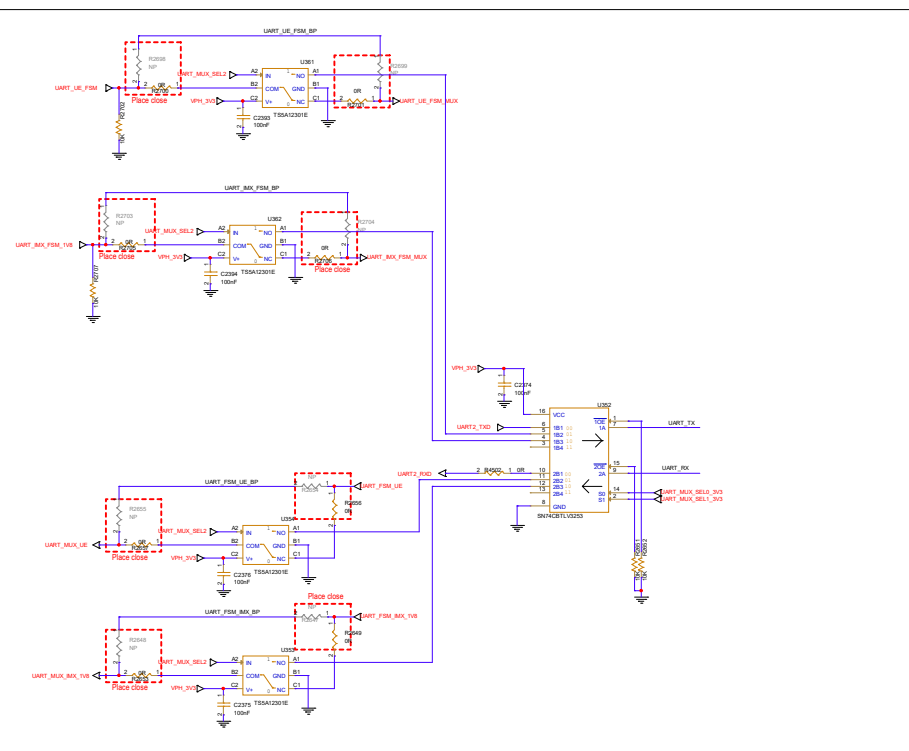
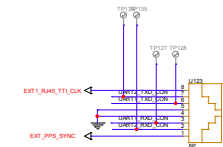
<b>Airspan Networks</b>			
Title			
<b>AU588</b>		<b>900 13 420 B48 RevA8</b>	
Size	Page Name	Schematic Name	Ver
A3	PCS - 19.2M_CLK_BUF	Baseband	A
Date:	Monday, October 31, 2022	Sheet 33	of 62



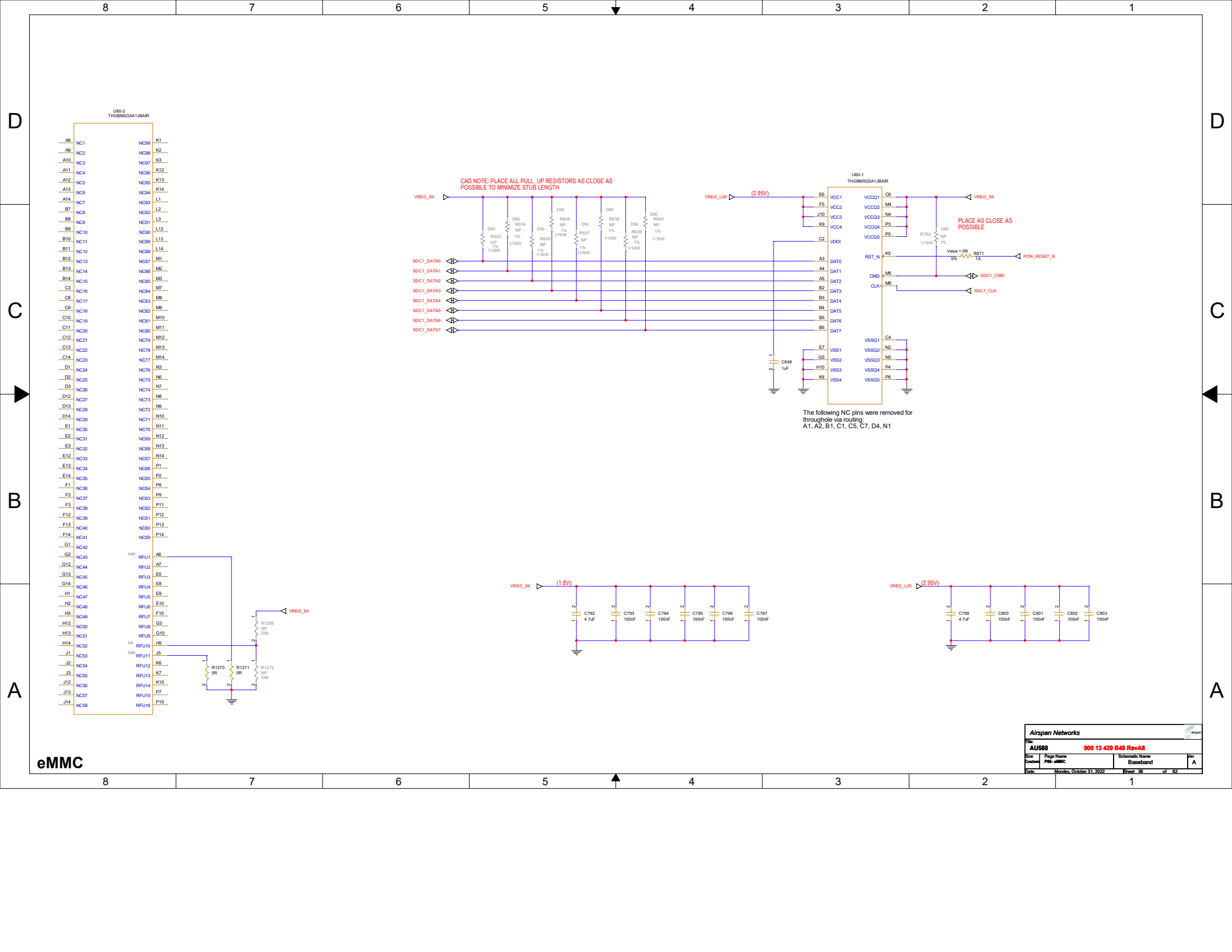
FETs are used to prevent power leak to the card from UART dongle when card is off



UART RJ45 connector

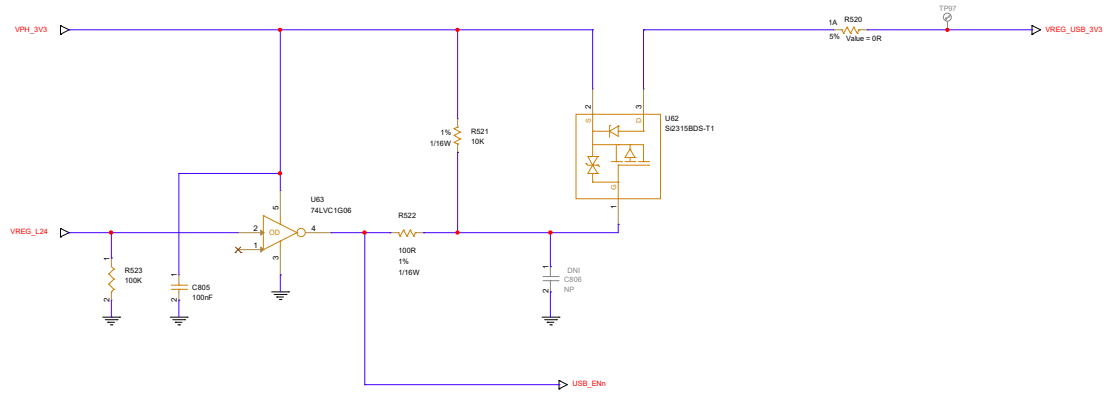


MUX_SEL2	MUX_SEL1	MUX_SEL0	PHY	UE	IMX
0	0	0	RJ45	FSM	FSM
0	0	1	X	FSM	FSM
0	1	0	X	FSM	FSM
0	1	1	X	FSM	FSM
1	0	0	RJ45	X	FSM
1	0	1	X	RJ45	X
1	1	0	X	X	RJ45
1	1	1	X	X	X



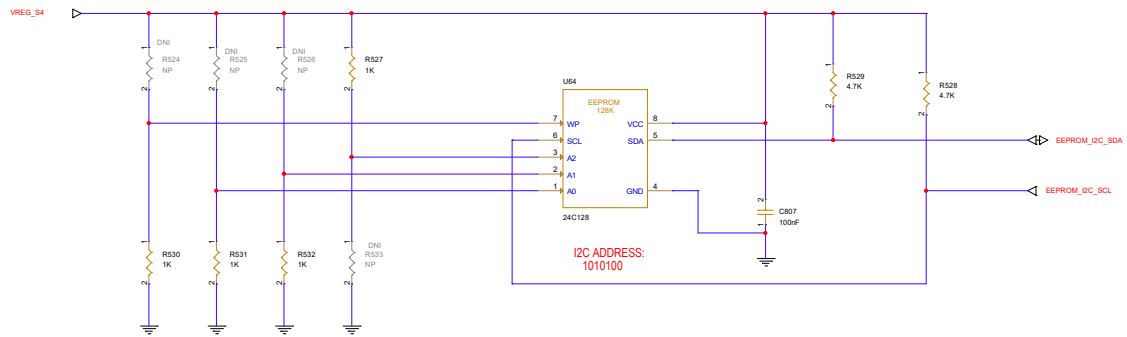
eMMC

Airspar Networks			
File:	AU588	900 13 420 B48 RevA5	
Rev:	1	Proj Name:	900 13 420 B48 RevA5
Customer:	PEB-eMMC	Schematic Name:	Baseband
Date:	Monday, October 31, 2022	Sheet:	38 of 62



USB

Airspar Networks			
File	AU588 900 13 420 B48 RevA8		
Item	Part Name	Customer	Schema Name
	Pre-FSM_USB_SUPPLY	Baseband	
Date	Monday, October 31, 2022	Sheet 37	of 62



SEEPROM

Airspar Networks			
File	AU588 900 13 420 B48 RevA8		
Size	Page Name	Schematic Name	
Custom	PE1-SEEPROM	Baseband	
Date	Monday, October 31, 2022	Sheet 38	of 62

8 7 6 5 4 3 2 1

D

D

C

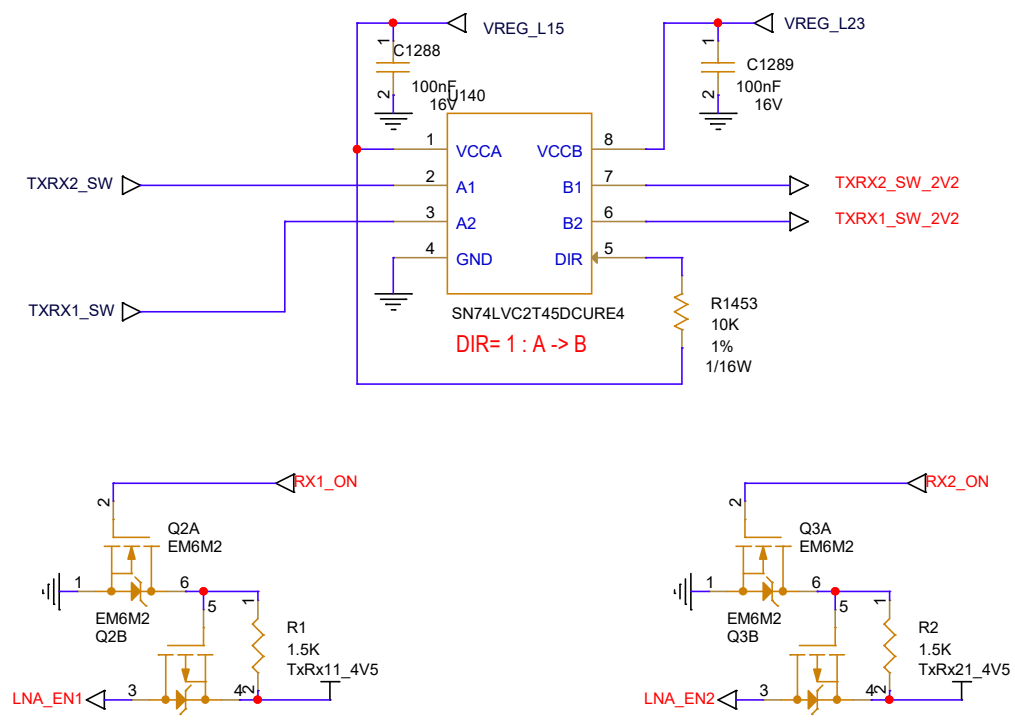
C

B


B

A

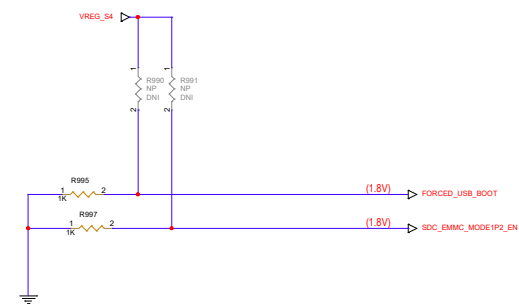
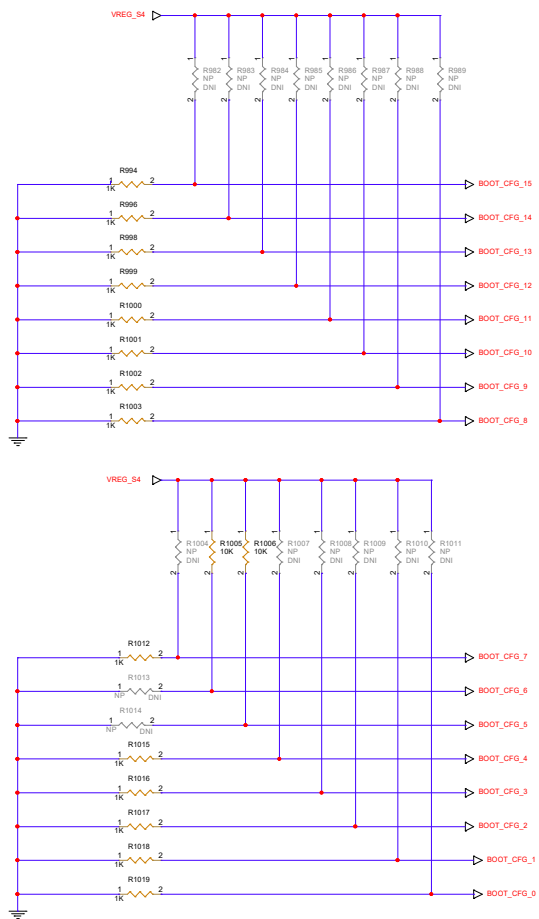
A



# Level Translation

Airspar Networks 			
Title		AU588 <b>900 13 420 B48 RevA8</b>	
Size	Page Name	Schematic Name	Ver
A4	P63_Level_Translation	Baseband	A
Date:	Monday, October 31, 2022	Sheet 39	of 62

8 7 6 5 4 3 2 1



**Boot Config**

Airspar Networks			
File:	AU588	900 13 420 B48 RevA8	
Star:	1	Part Name	900 13 420 B48 RevA8
Custom:	Pre-OP Switches	Schematic Name	Baseband
Date:	Monday, October 31, 2022	Sheet:	40 of 62

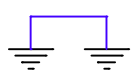
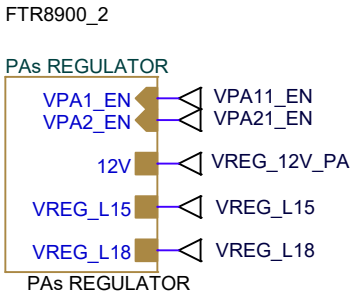
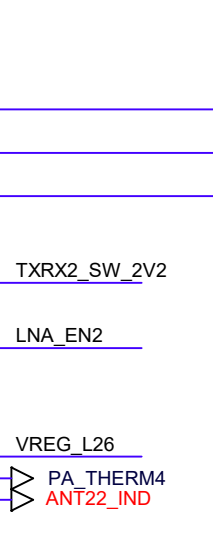
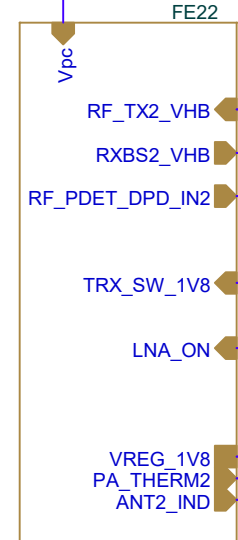
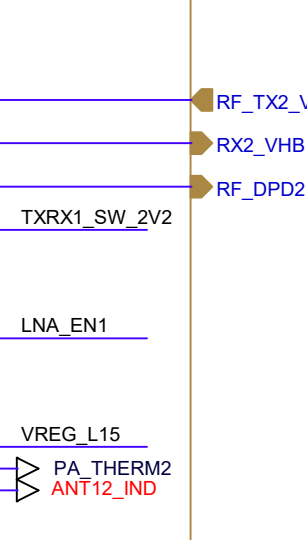
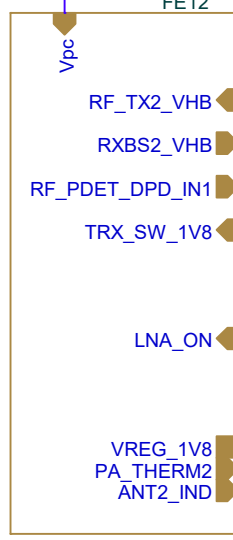
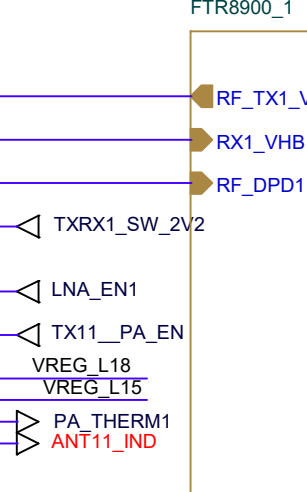
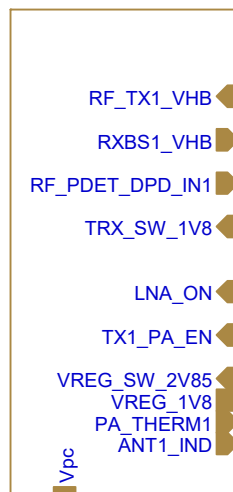
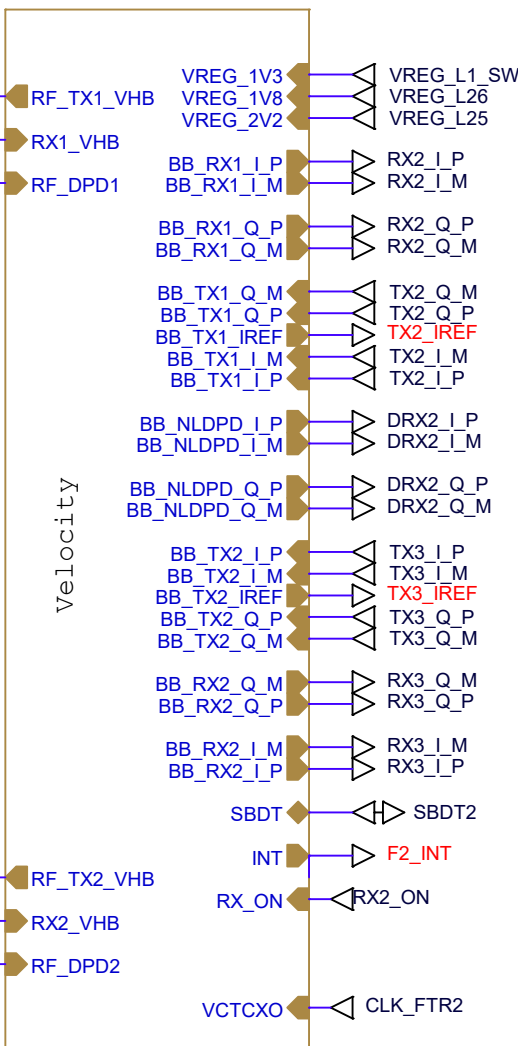
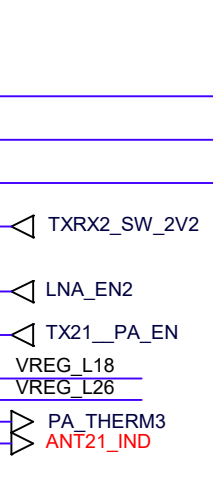
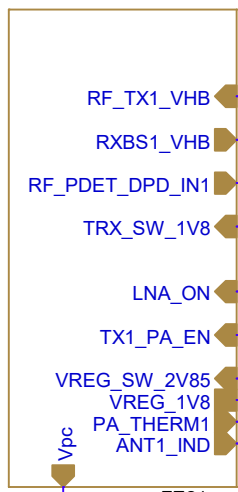


FE21

FTR8900\_2

FE11

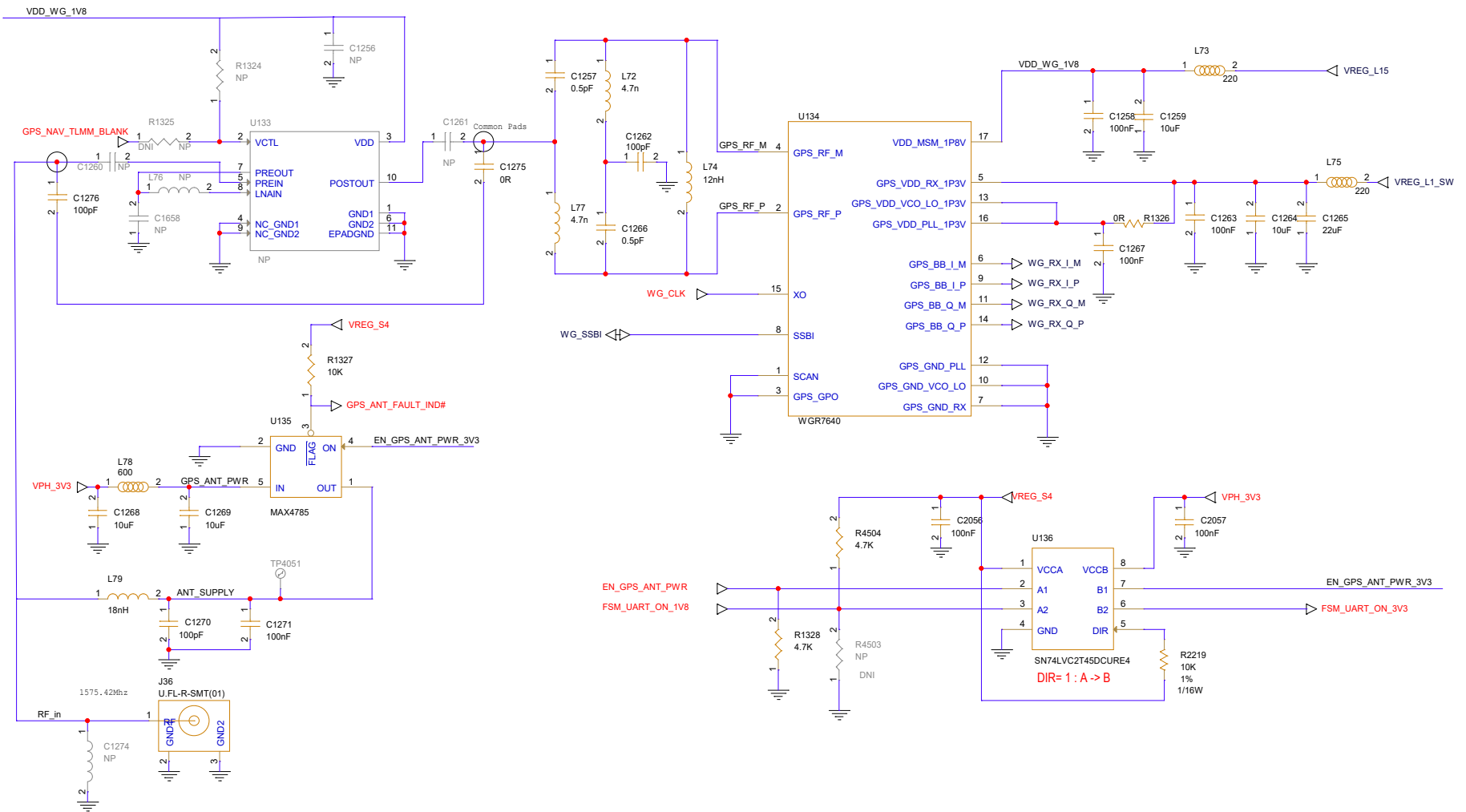
FTR8900\_1



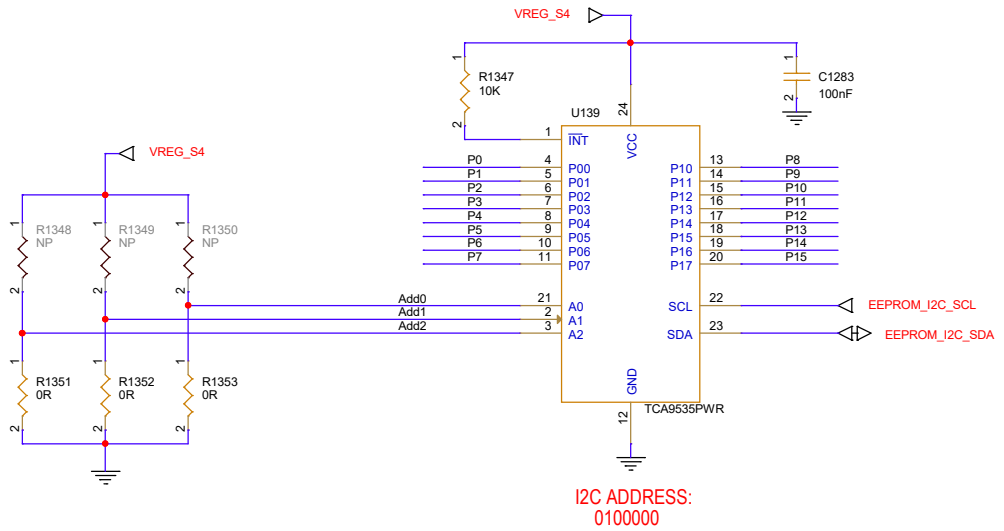
<b>Airspan Networks</b>			
<b>AU588</b>			
<b>900 13 420 B48 RevA8</b>			
Size	Page Name	Schematic Name	Ver
A	P70 - RF_TOP	Baseband	A
Date:		Monday, October 31, 2022	Sheet 41 of 62

Coils on F5SM?

# GPS



<b>Airspan Networks</b>			
Title			
<b>AU588</b>		<b>900 13 420 B48 RevA8</b>	
Size	Page Name	Schematic Name	Ver
A3	P71 - GPS	Baseband	A
Date:	Monday, October 31, 2022		Sheet 42 of 62

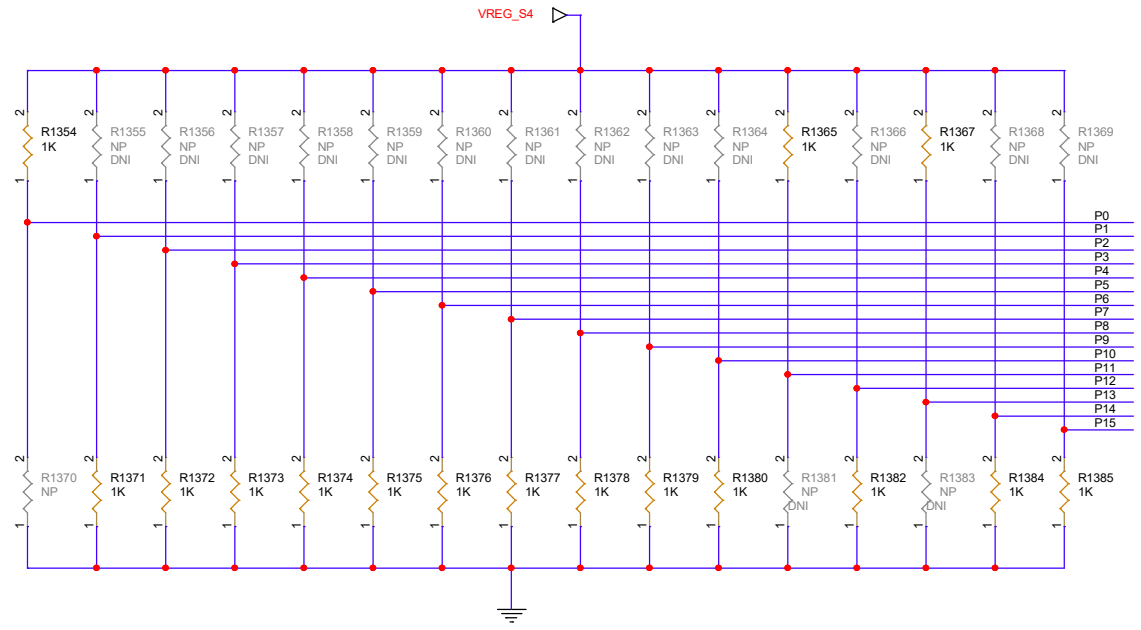


15	14	13	12	,11	10	9	8	,7	6	5	4	,3	2	1	0
Module					Config			TBD			DDR				
Type					Variant						Type				

Card ID: Definition can be found at:  
 R:\RnD\Digital\Velocity\Docs\Card ID\Card ID.docx

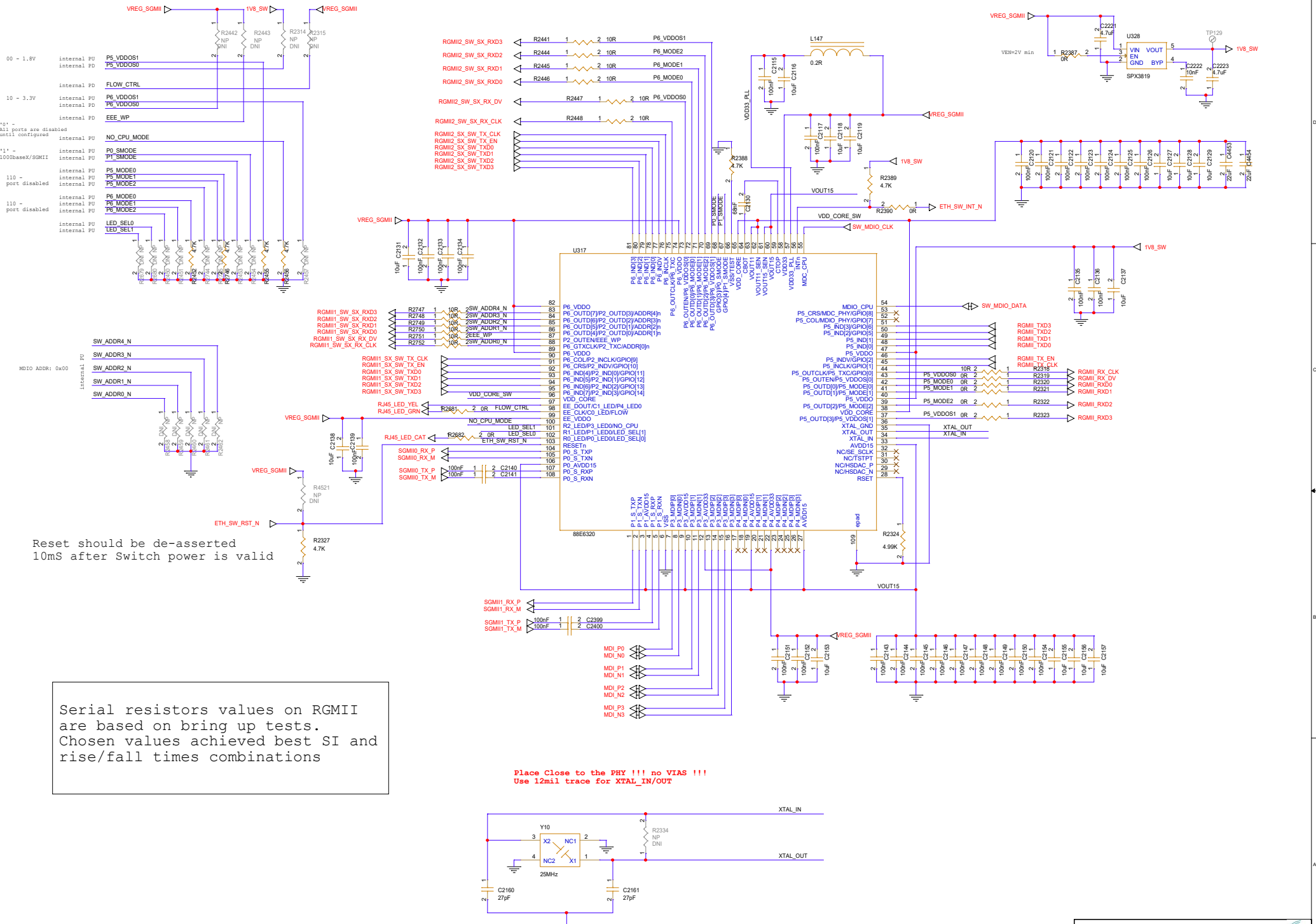
I2C ADDRESS:  
0100000

Card ID: 0x2801



Card ID

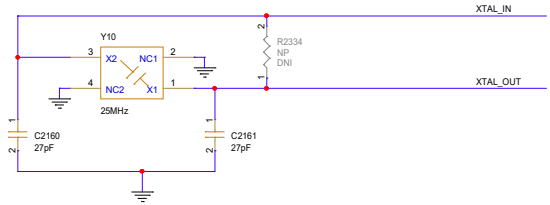
<b>Airspan Networks</b>			
Title			
<b>AU588</b>		<b>900 13 420 B48 RevA8</b>	
Size	Page Name	Schematic Name	Ver
B	P72 - I/O Expander	Baseband	A
Date:	Sunday, December 11, 2022	Sheet 43	of 62

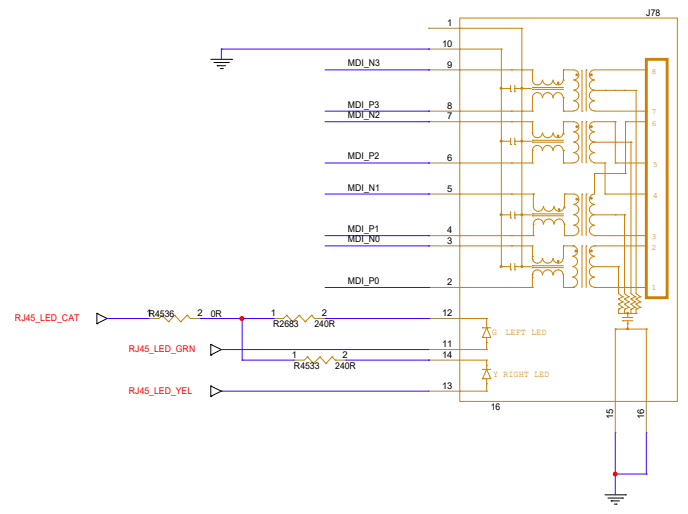
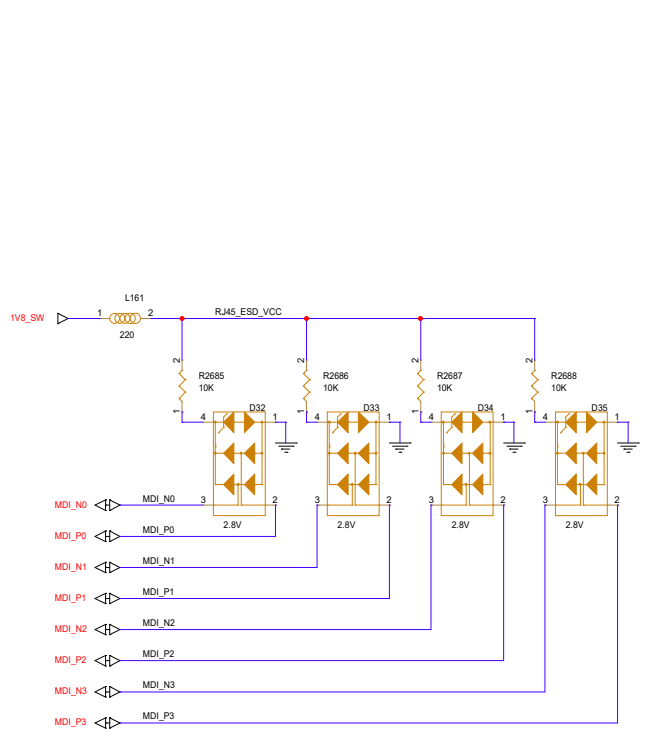


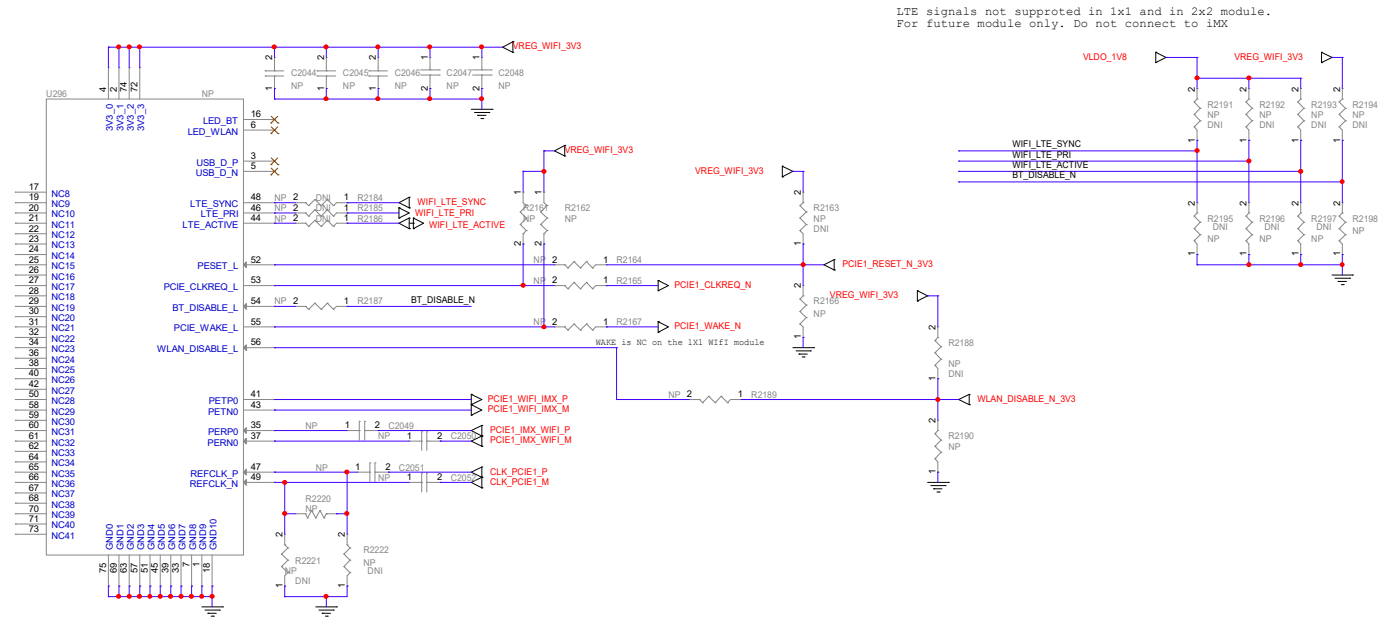
Reset should be de-asserted 10ms after Switch power is valid

Serial resistors values on RGMII are based on bring up tests. Chosen values achieved best SI and rise/fall times combinations

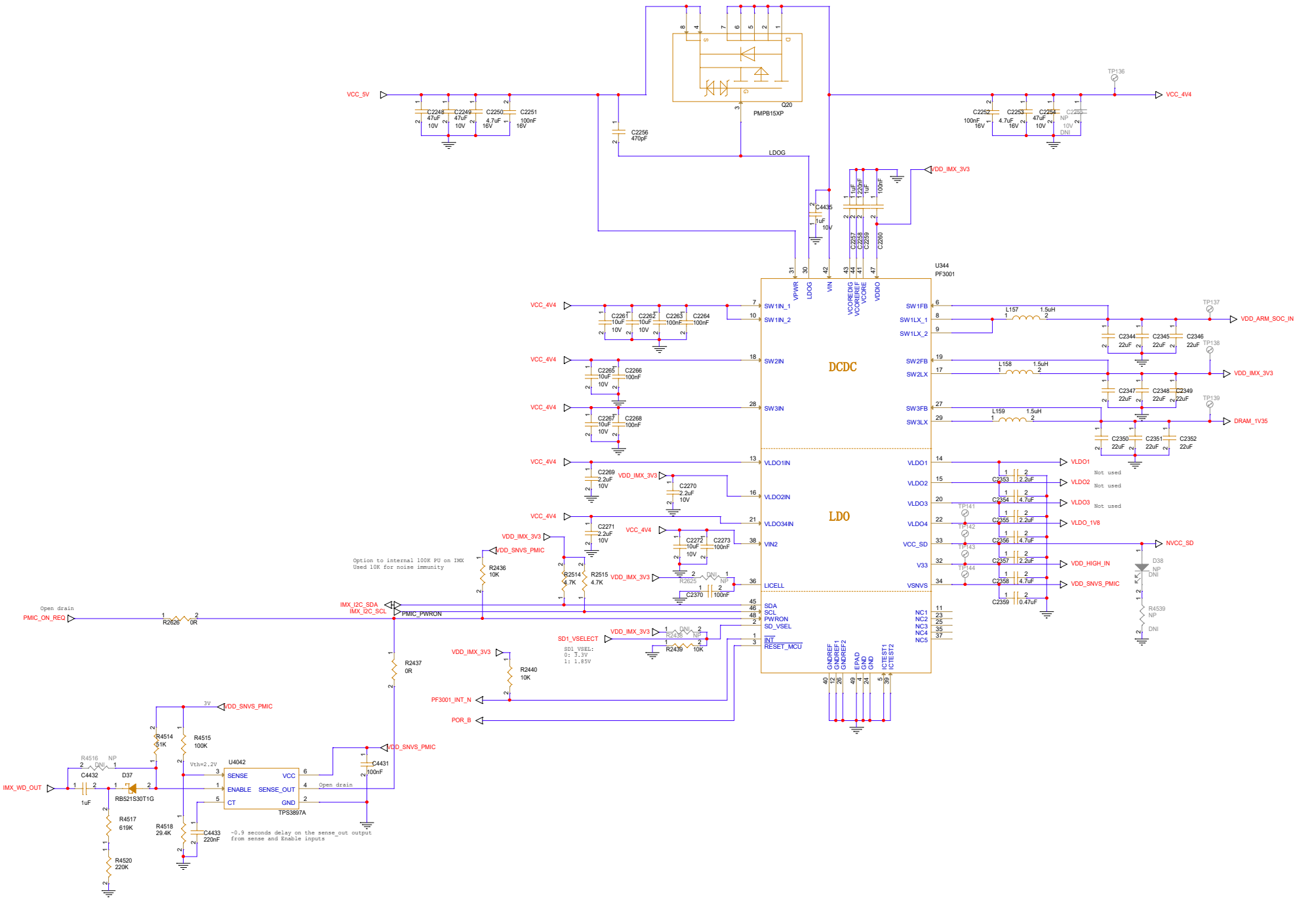
Place Close to the PHY !!! no VIAS !!!  
Use 12mil trace for XTAL\_IN/OUT





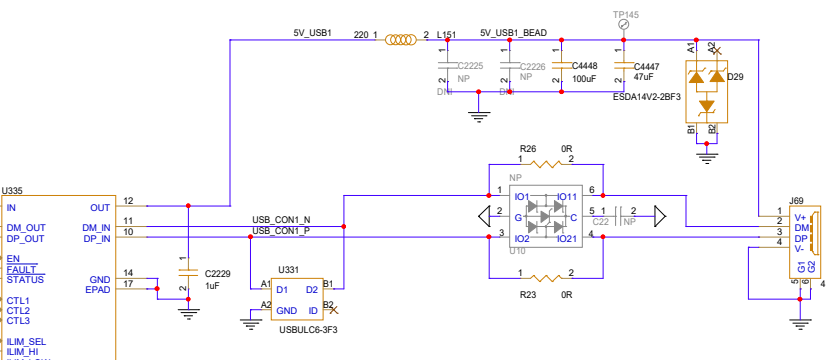
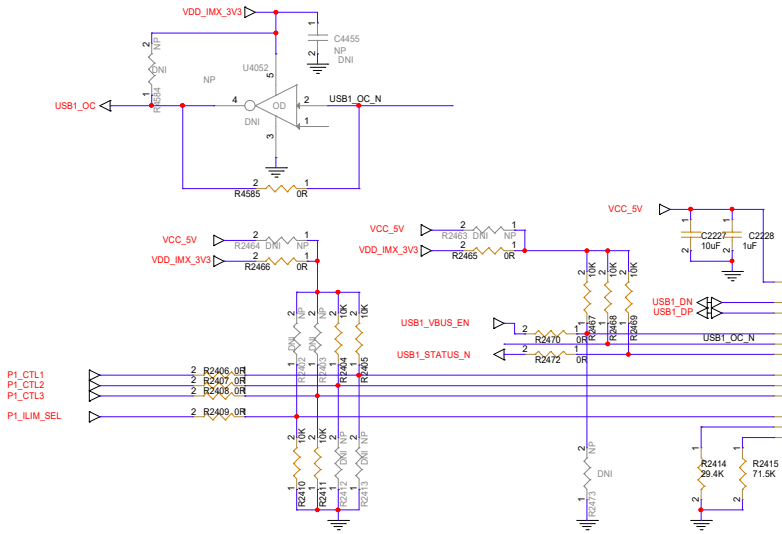


LTE signals not supported in 1x1 and in 2x2 module.  
For future module only. Do not connect to IMX

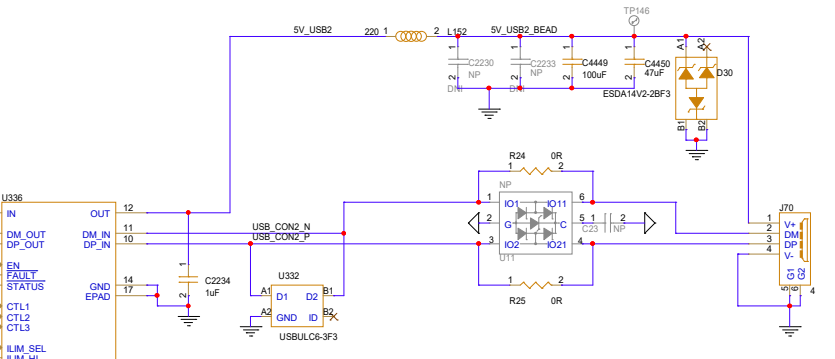
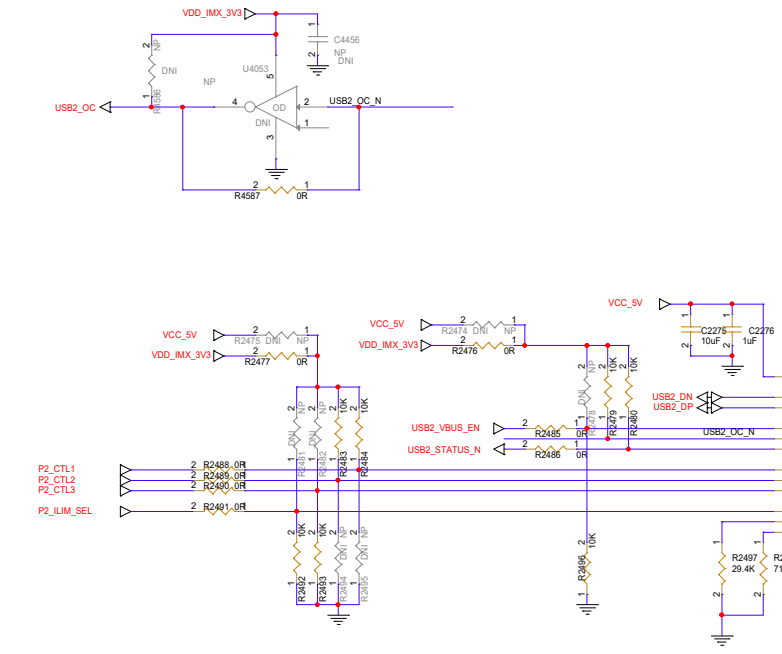


Option to internal 100K PU on IMX  
Used 10K for noise immunity

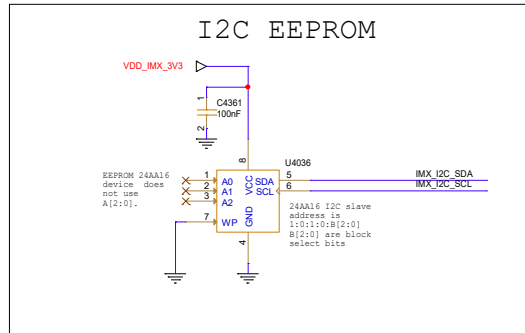
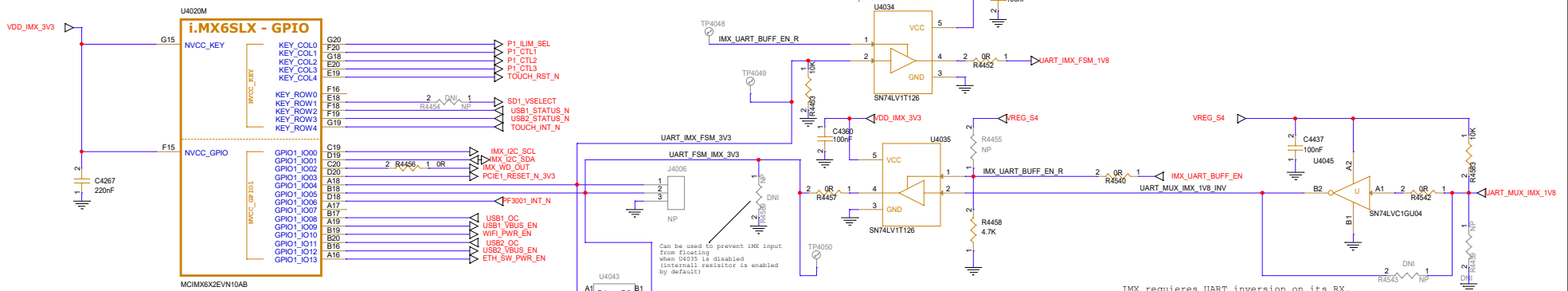
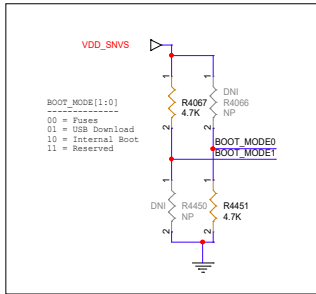
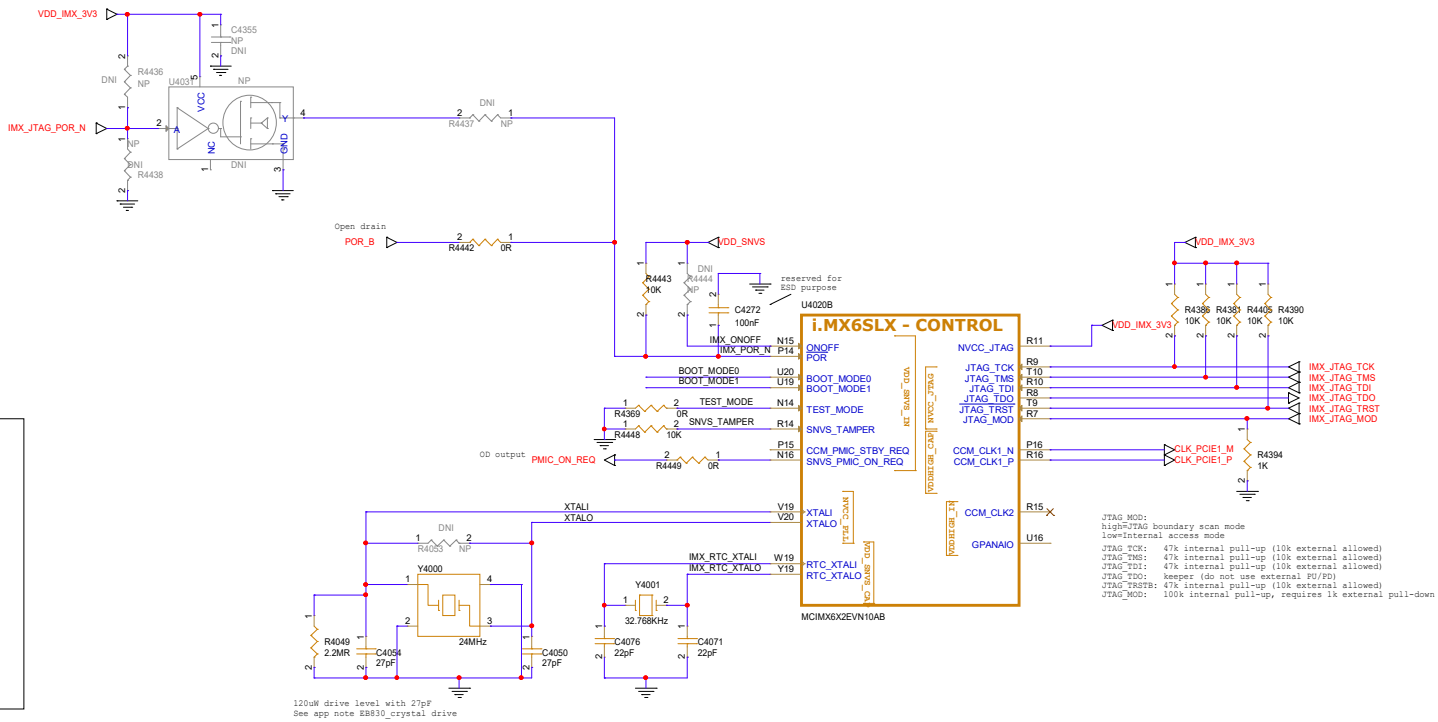
-0.9 seconds delay on the sense\_out output  
from sense and Enable inputs

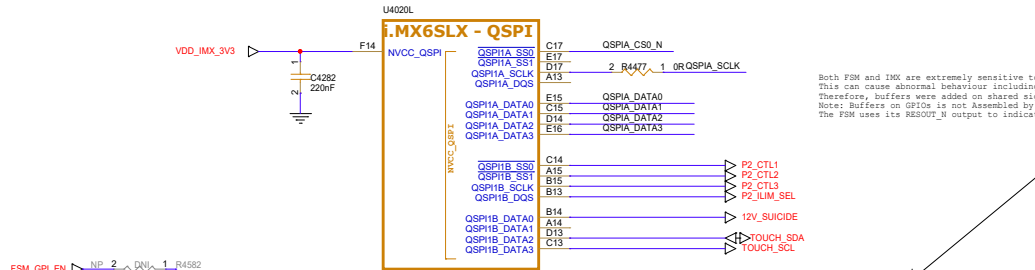
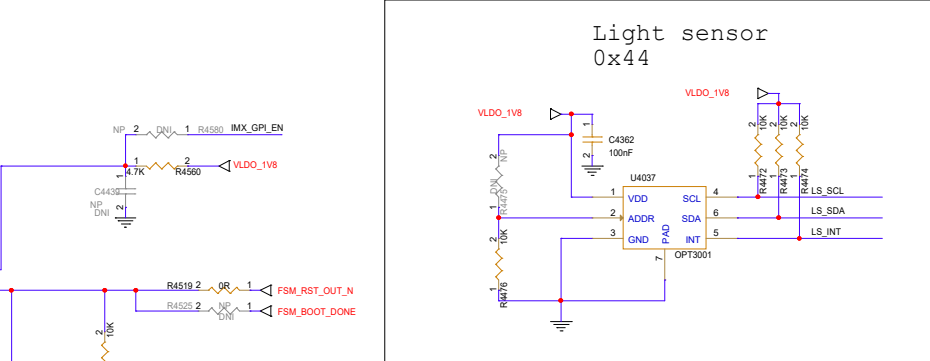
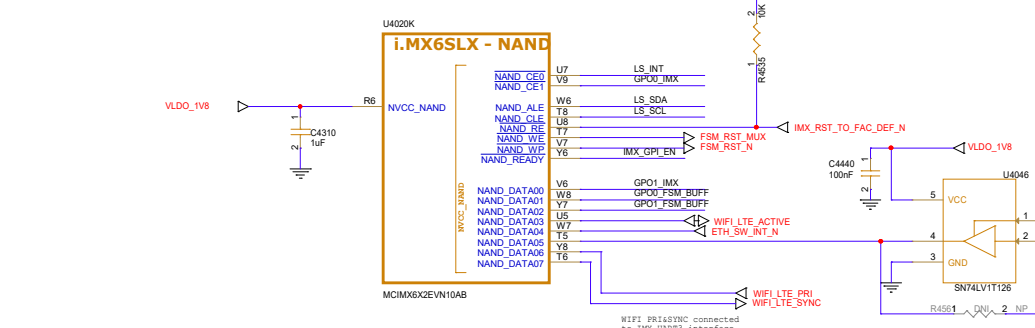
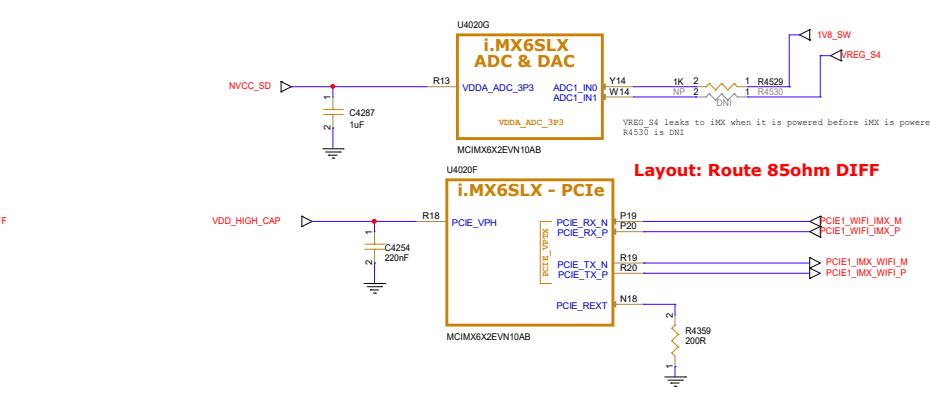
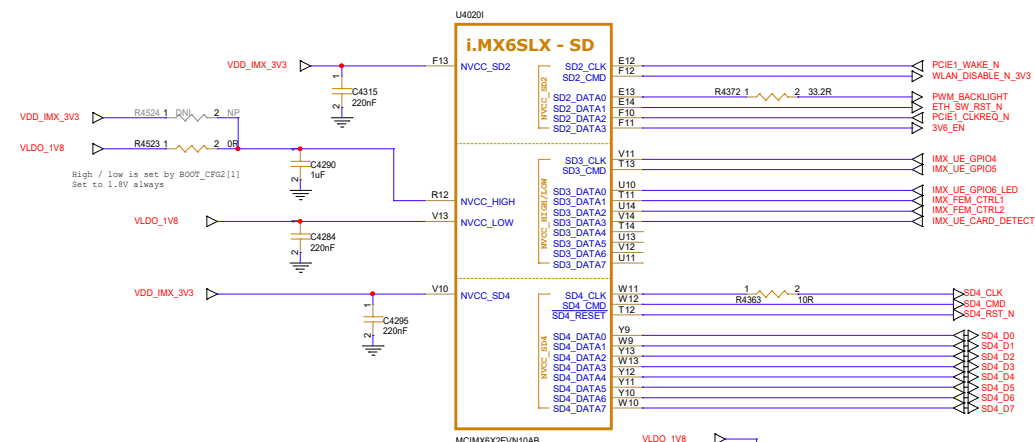


ILIM HIGH = 1.5A  
 ILIM LOW = 0.5A  
 Default mode: SDP

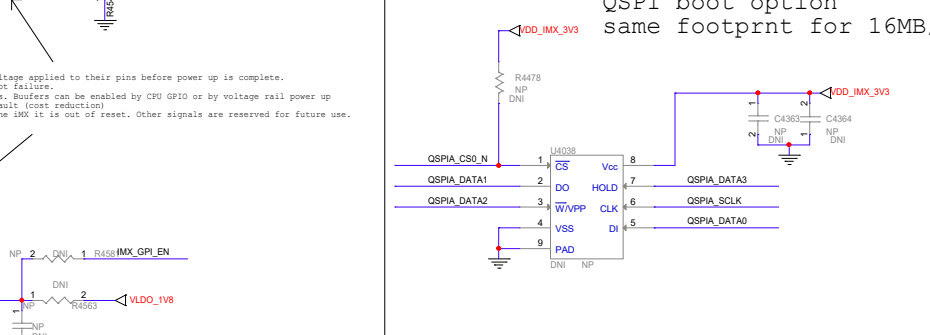
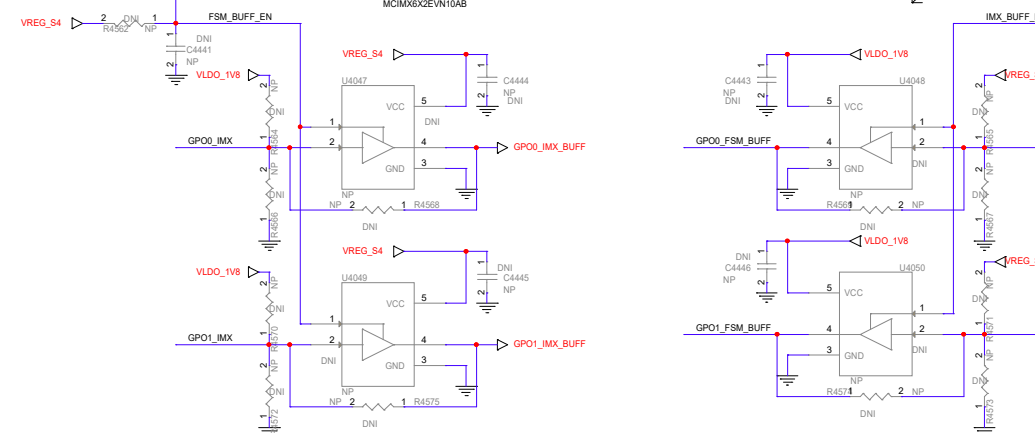


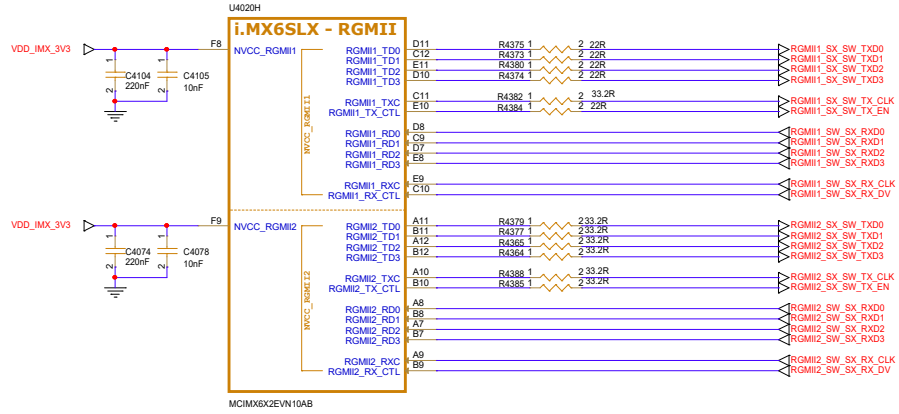




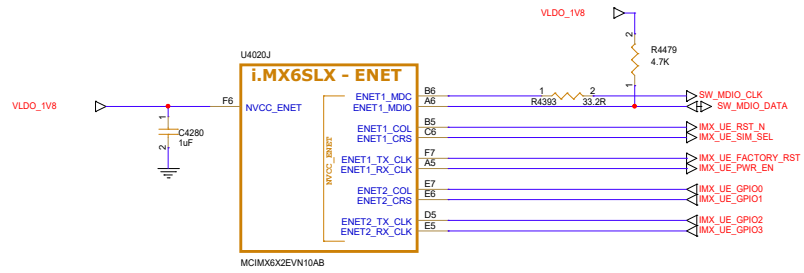


Both FSM and IMX are extremely sensitive to voltage applied to their pins before power up is complete. This can cause abnormal behaviour including boot failure. Therefore, buffers were added on shared signals. Buffers can be enabled by CPU GPIO or by voltage rail power up. Note: Buffers on GPIOs is not Assembled by default (cost reduction). The FSM uses its RESOUT\_N output to indicate the IMX is out of reset. Other signals are reserved for future use.

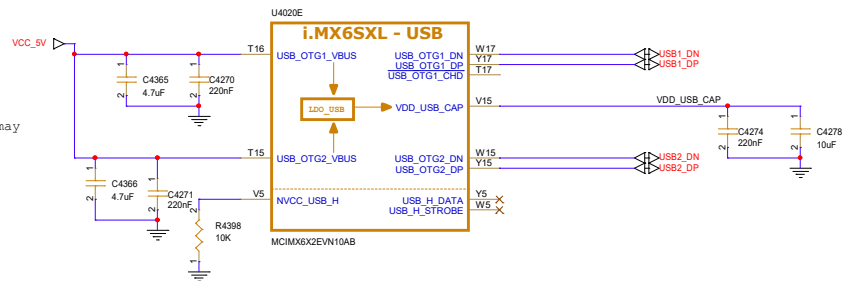




Serial resistors values on RGMII are based on bring up tests. Chosen values achieved best SI and rise/fall times combinations



USB\_OTG1\_VBUS and USB\_OT2\_VBUS are not part of the power supply sequence and may be powered at any time.



DRAM\_DATA[0:31]

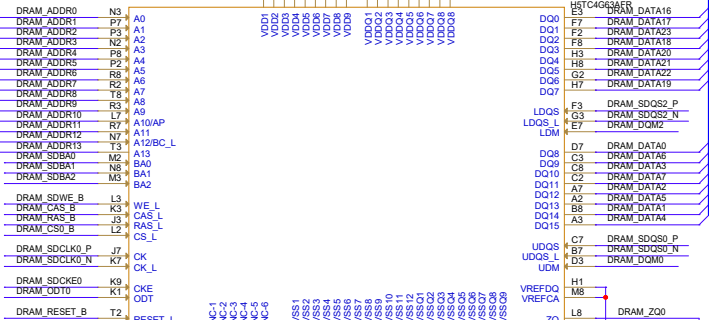
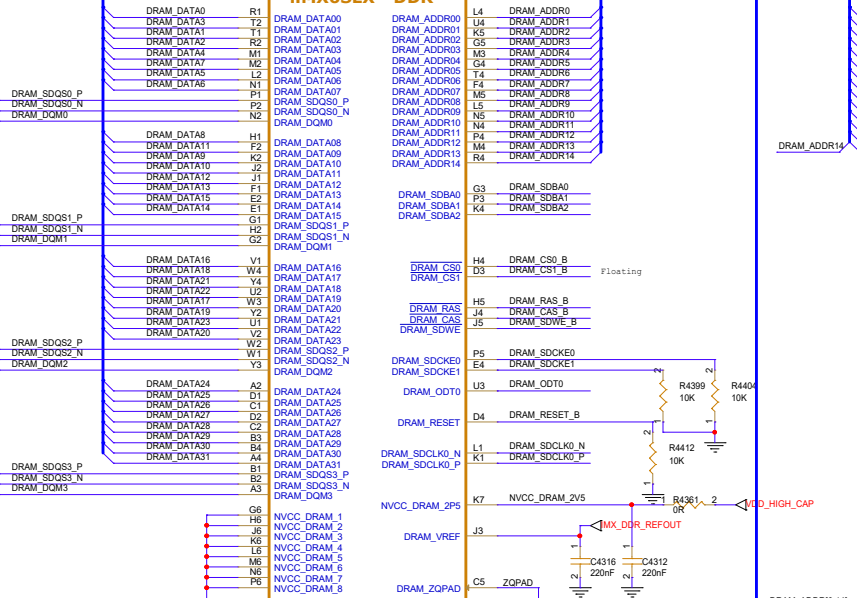
DRAM\_IV35

DRAM\_ADDR[0:14]

DRAM\_DATA[0:31]

U4020C

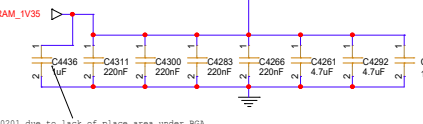
i.MX6SLX - DDR



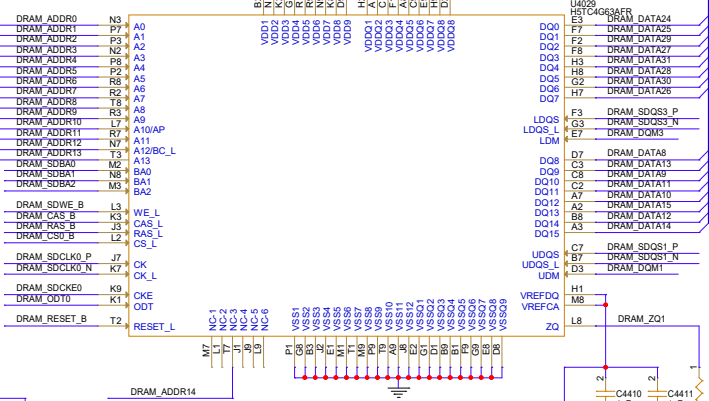
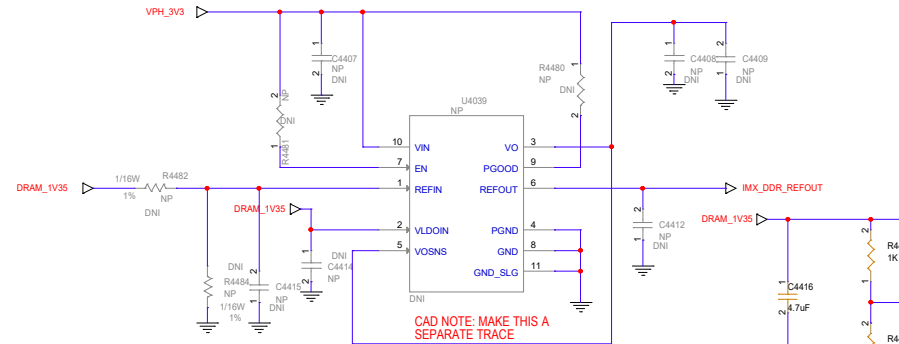
2 x 4Gbit DDR3L memory devices

DRAM\_IV35

DRAM\_DATA[0:31]

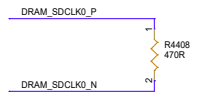


0201 due to lack of place area under BGA

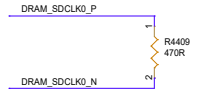


IMX\_DDR\_REFOUT

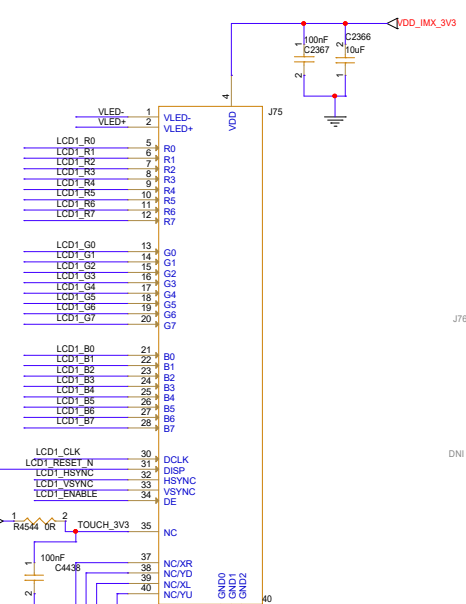
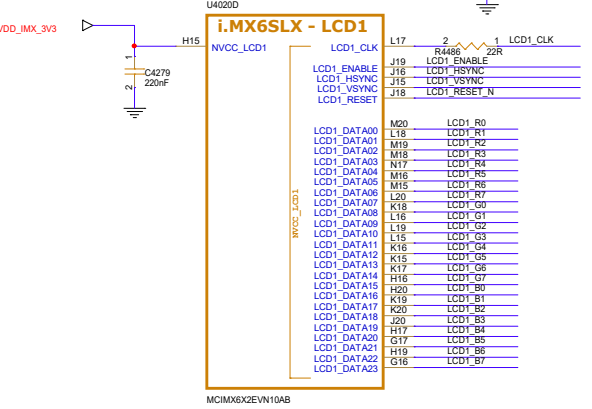
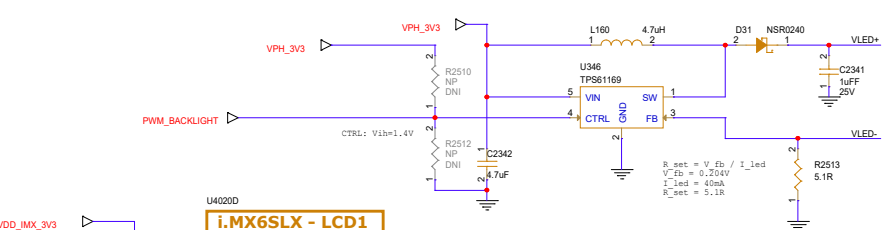
Note: CLK termination: Place close to DDR



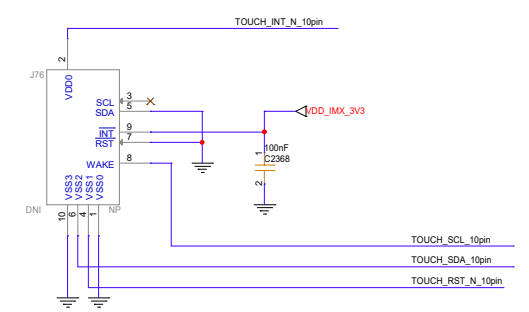
Note: CLK termination: Place close to DDR



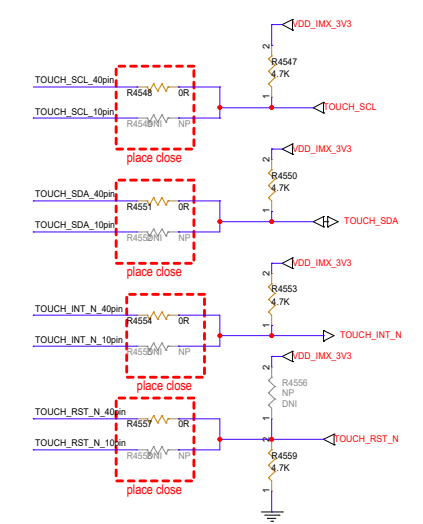
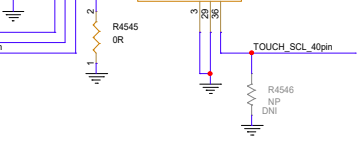
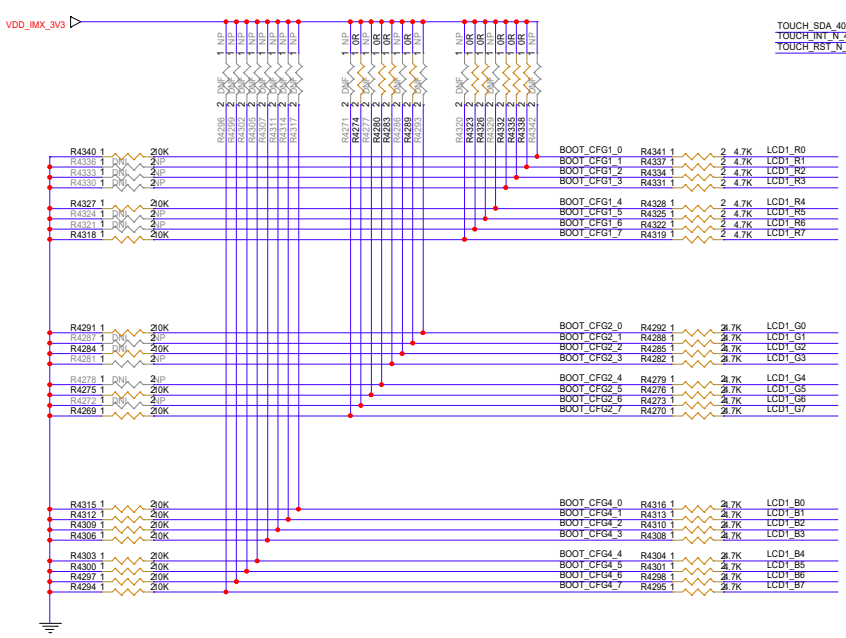
Backlight boost is powered from VPH\_3V3  
 Digital section powered from VDD\_IMX\_3v3  
 Done to reduce consumption from IMX PMIC 3V3 rail



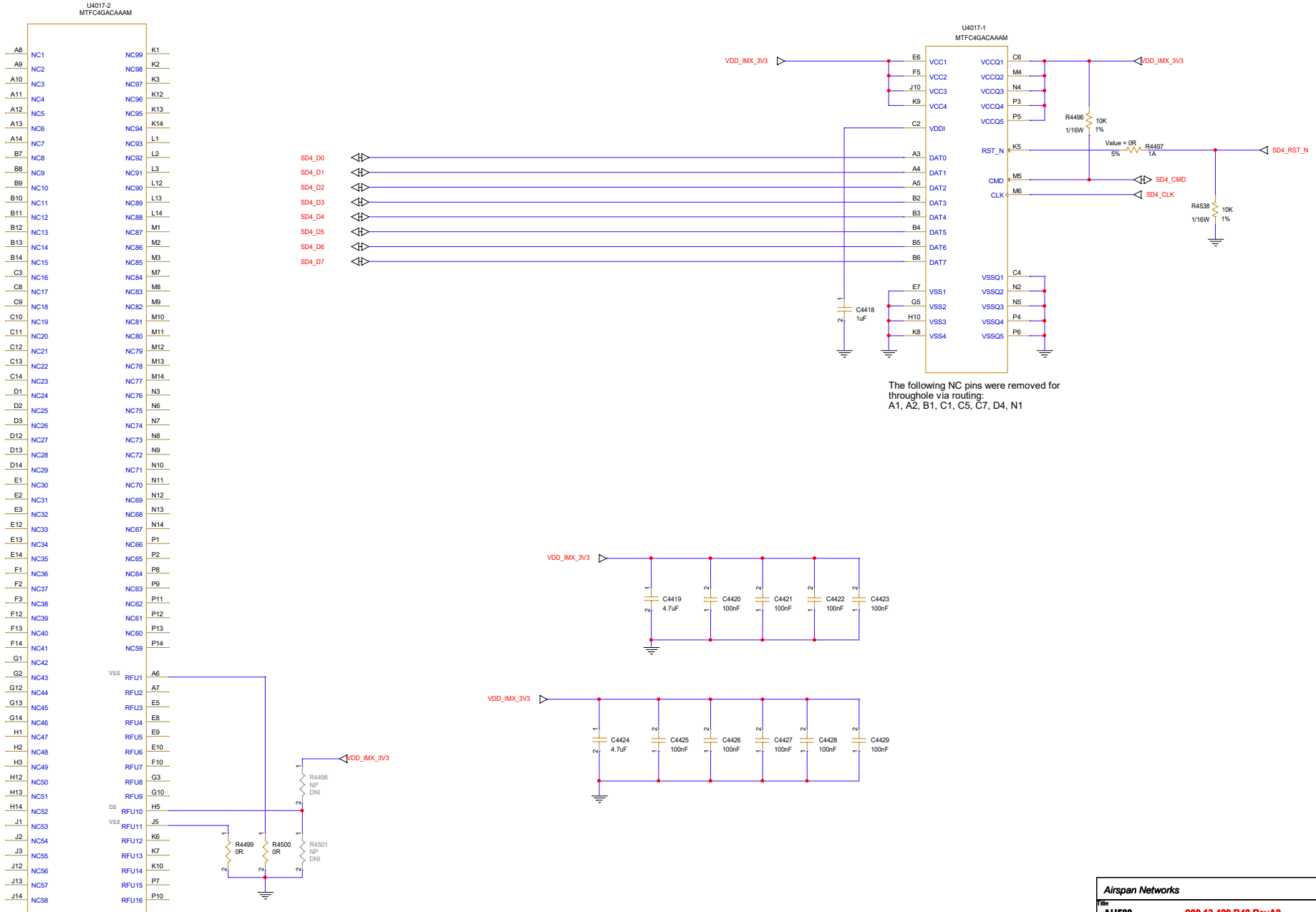
Pins in reverse order due to mechanical alignment



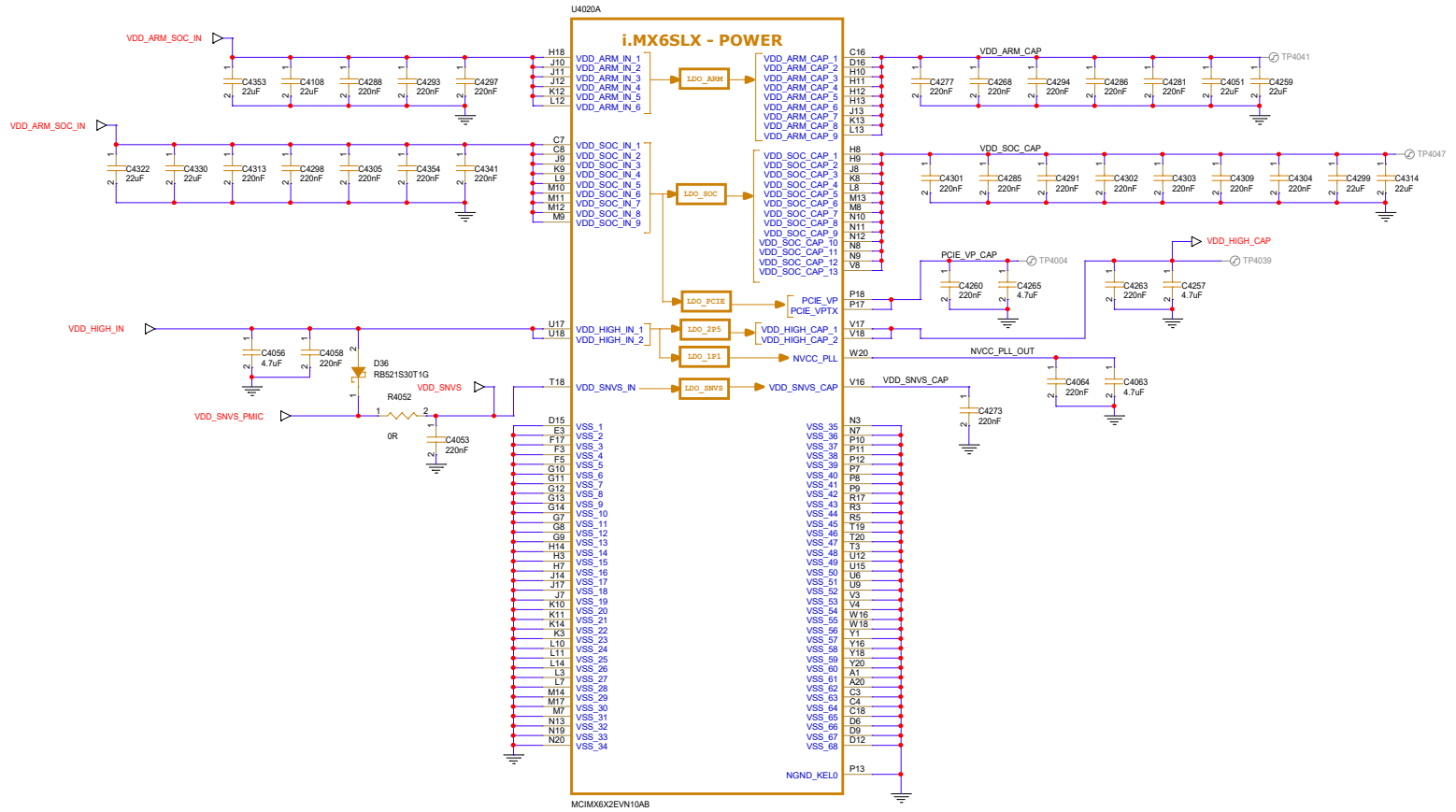
Supports both LCD versions  
 Touch + disp on 1 connector  
 Touch and disp on separate connectors

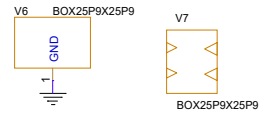
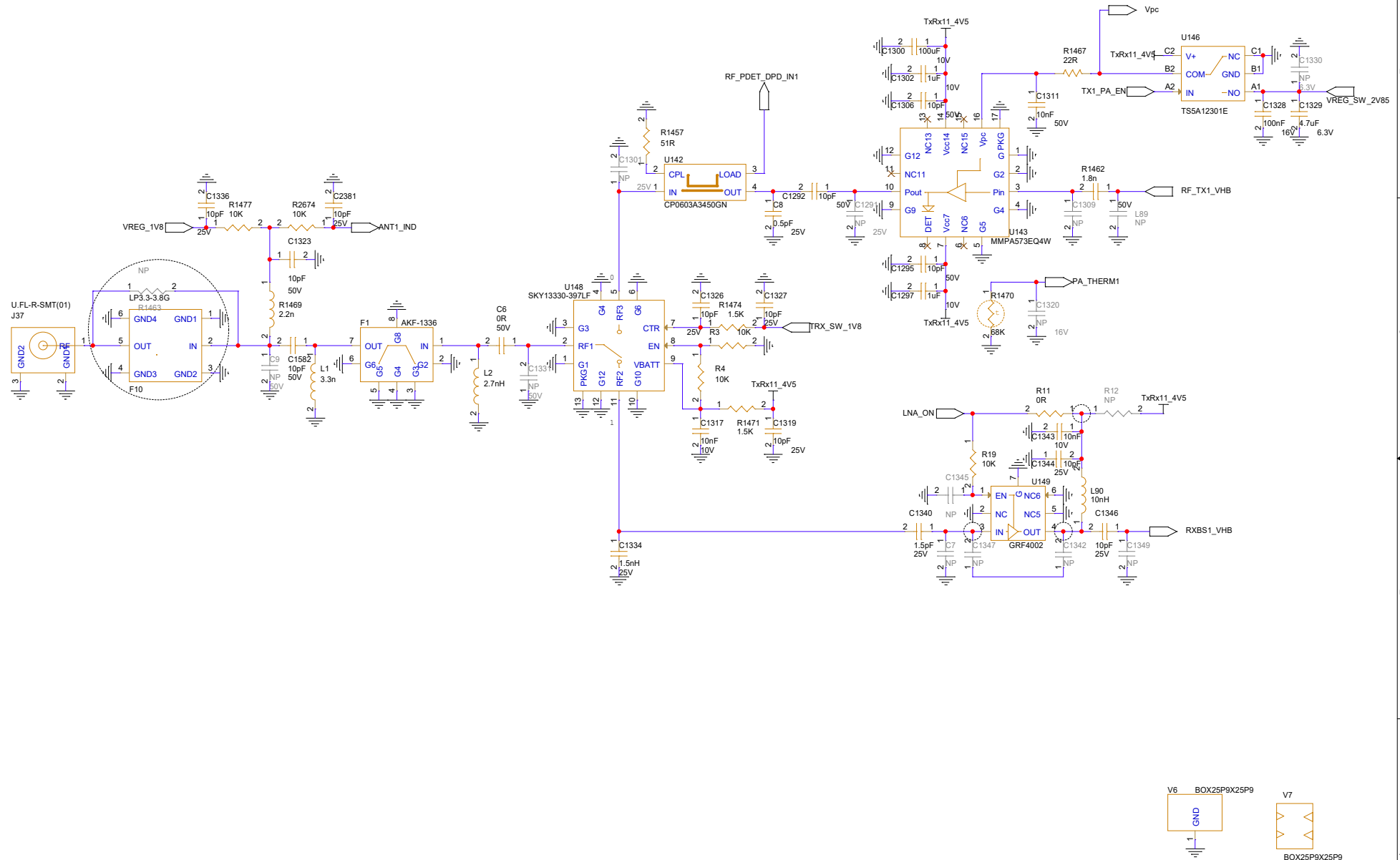


Used 201-50-039 footprint  
for better layout (same as in FSM eMMC)



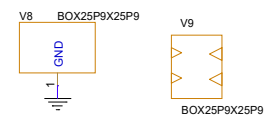
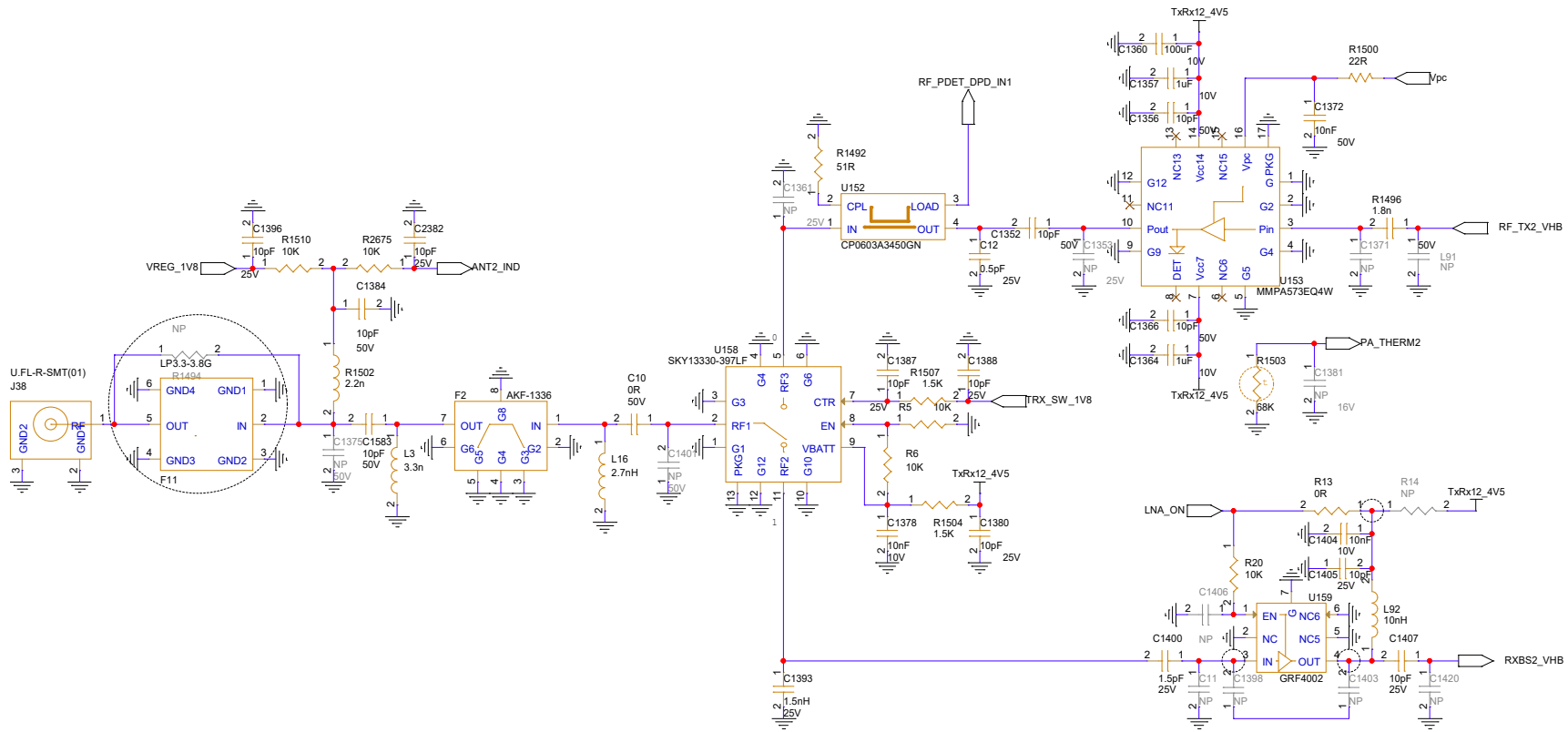
The following NC pins were removed for through-hole via routing:  
A1, A2, B1, C1, C5, C7, D4, N1



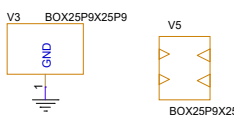
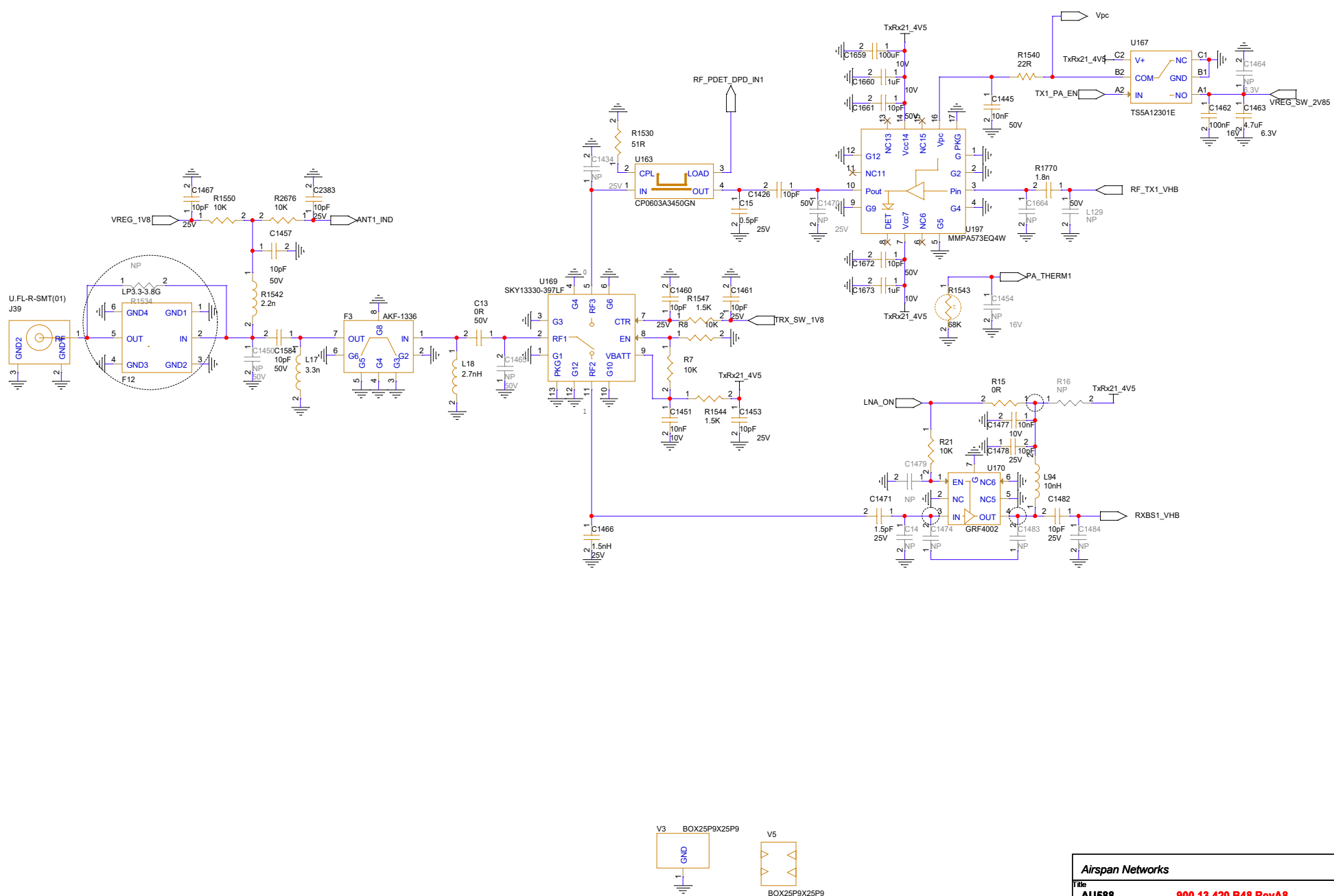


<b>Airspan Networks</b>			
Title			
<b>AU588</b>		<b>900 13 420 B48 RevA8</b>	
Size	Page Name	Schematic Name	Ver
A3	FE1	FE11	A
Date:	Sunday, December 11, 2022	Sheet 56	of 62

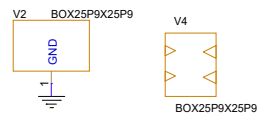
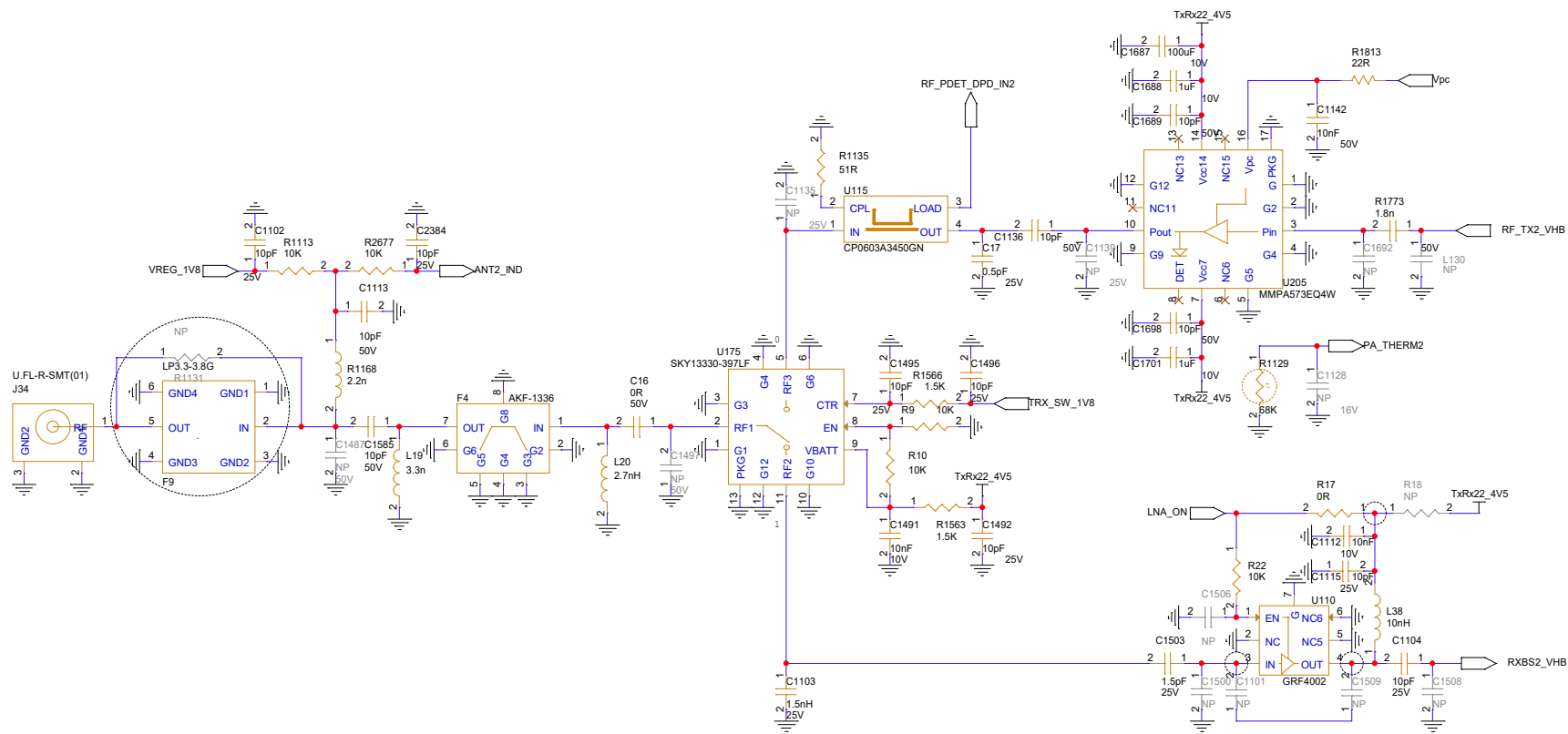




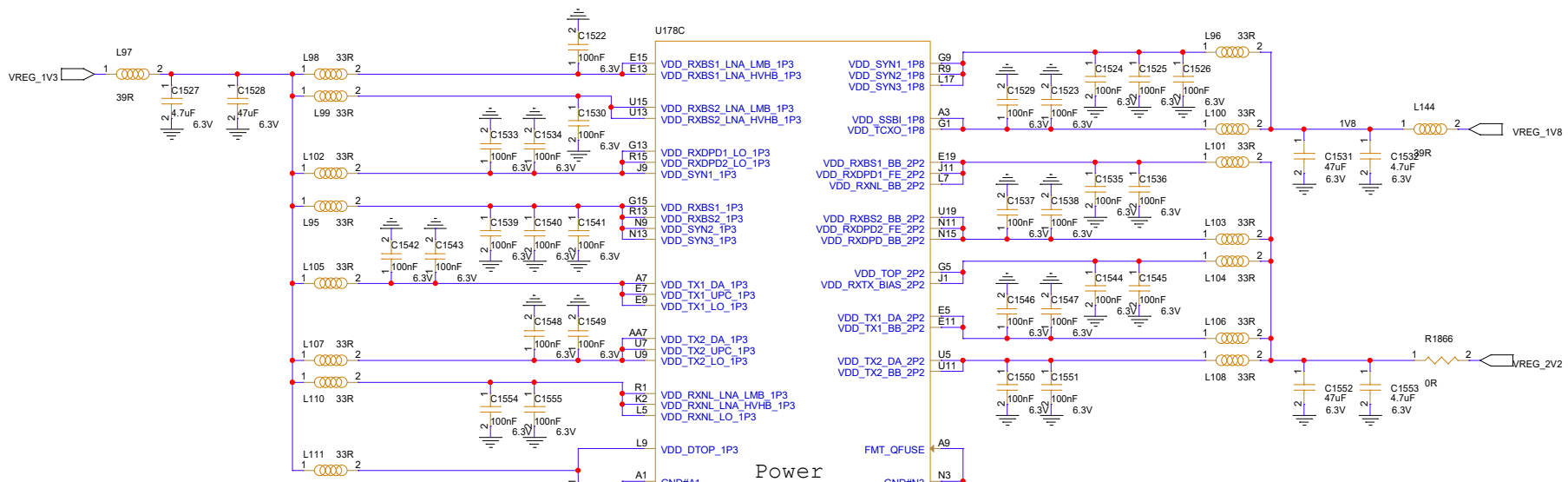
<b>Airspan Networks</b>			
File		<b>AU588 900 13 420 B48 RevA8</b>	
Size	Page Name	Schematic Name	Ver
A3	FE2	FE12	A
Date: Sunday, December 11, 2022		Sheet 57 of 62	



<b>Airspan Networks</b>			
Title			
<b>AU588</b>		<b>900 13 420 B48 RevA8</b>	
Size	Page Name	Schematic Name	Ver
A3	FE1	FE21	A
Date: Sunday, December 11, 2022		Sheet 58	of 62



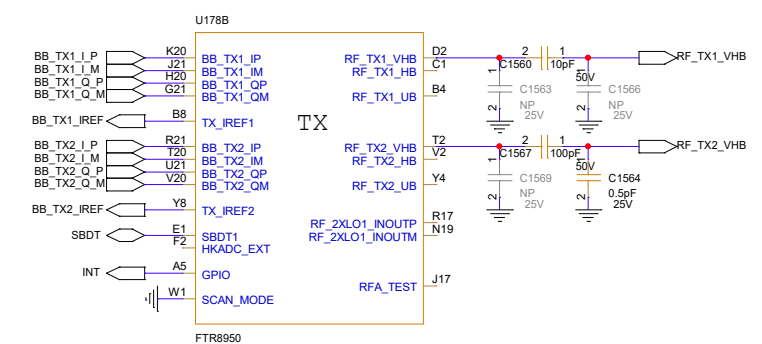
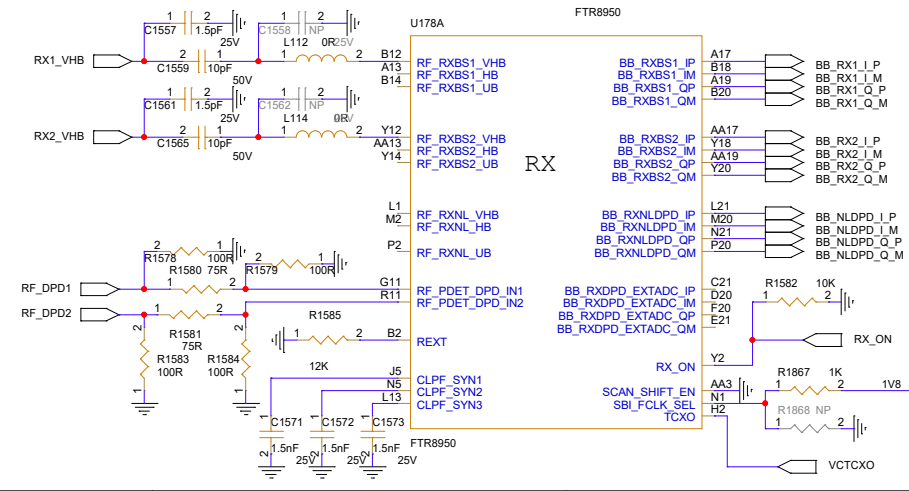
<b>Airspan Networks</b>			
Title			
<b>AU588</b>		<b>900 13 420 B48 RevA8</b>	
Size	Page Name	Schematic Name	Ver
A3	FE2	FE22	A
Date: Sunday, December 11, 2022		Sheet 59	of 62



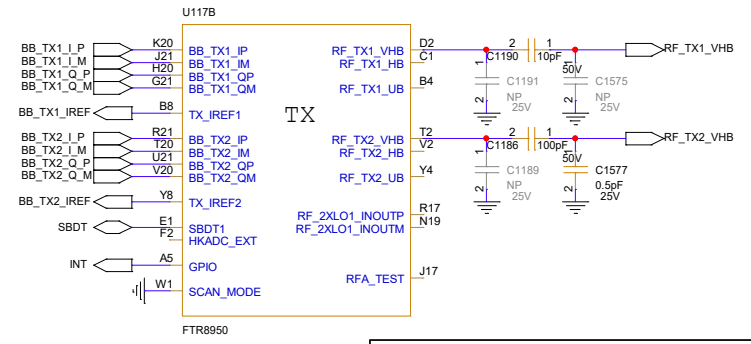
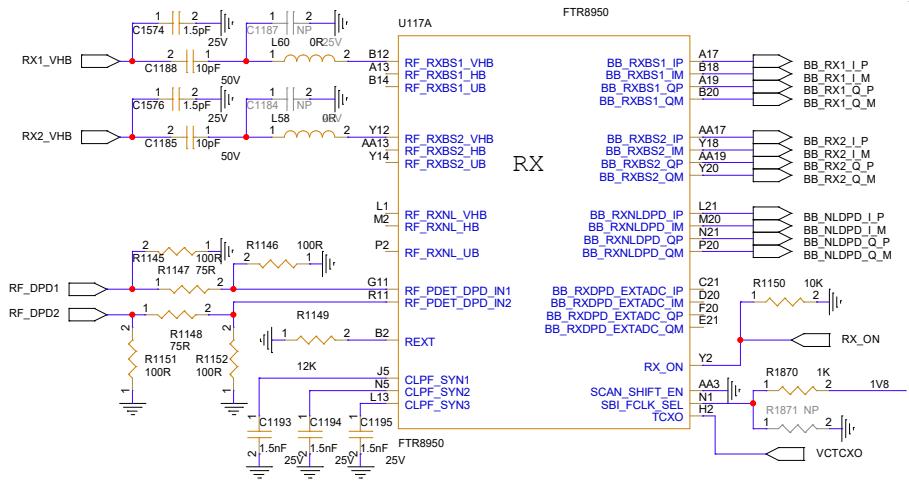
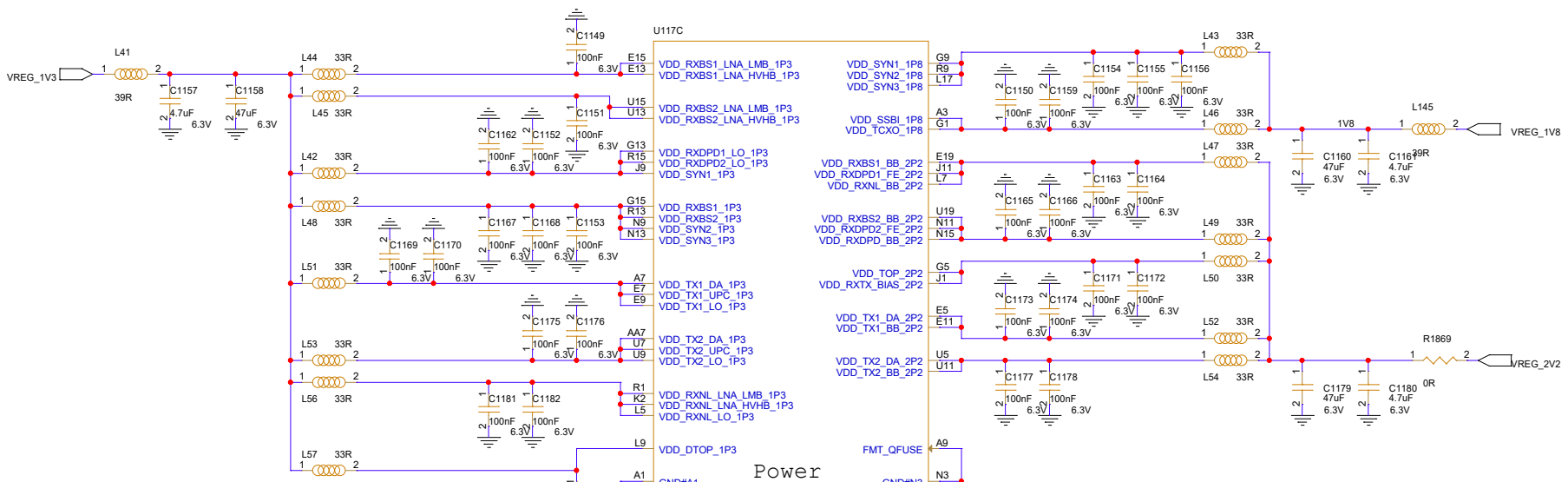
**Power**

VDD_RXBS1_LNA_LMB_1P3	VDD_SYN1_1P8
VDD_RXBS1_LNA_HVHB_1P3	VDD_SYN2_1P8
VDD_RXBS2_LNA_LMB_1P3	VDD_SYN3_1P8
VDD_RXBS2_LNA_HVHB_1P3	VDD_SSBI_1P8
VDD_RXDPD1_LO_1P3	VDD_TCXO_1P8
VDD_RXDPD1_FE_2P2	VDD_RXBS1_BB_2P2
VDD_SYN1_1P3	VDD_RXBS2_BB_2P2
VDD_RXBS2_1P3	VDD_RXNL_BB_2P2
VDD_SYN2_1P3	VDD_RXDPD2_FE_2P2
VDD_SYN3_1P3	VDD_RXDPD_BB_2P2
VDD_TX1_DA_1P3	VDD_TOP_2P2
VDD_TX1_UPC_1P3	VDD_RXTX_BIAS_2P2
VDD_TX1_LO_1P3	VDD_TX1_DA_2P2
VDD_TX2_DA_1P3	VDD_TX1_BB_2P2
VDD_TX2_UPC_1P3	VDD_TX2_DA_2P2
VDD_TX2_LO_1P3	VDD_TX2_BB_2P2
VDD_RXNL_LNA_LMB_1P3	
VDD_RXNL_LNA_HVHB_1P3	
VDD_RXNL_LO_1P3	
VDD_DTOP_1P3	FMT_QFUSE

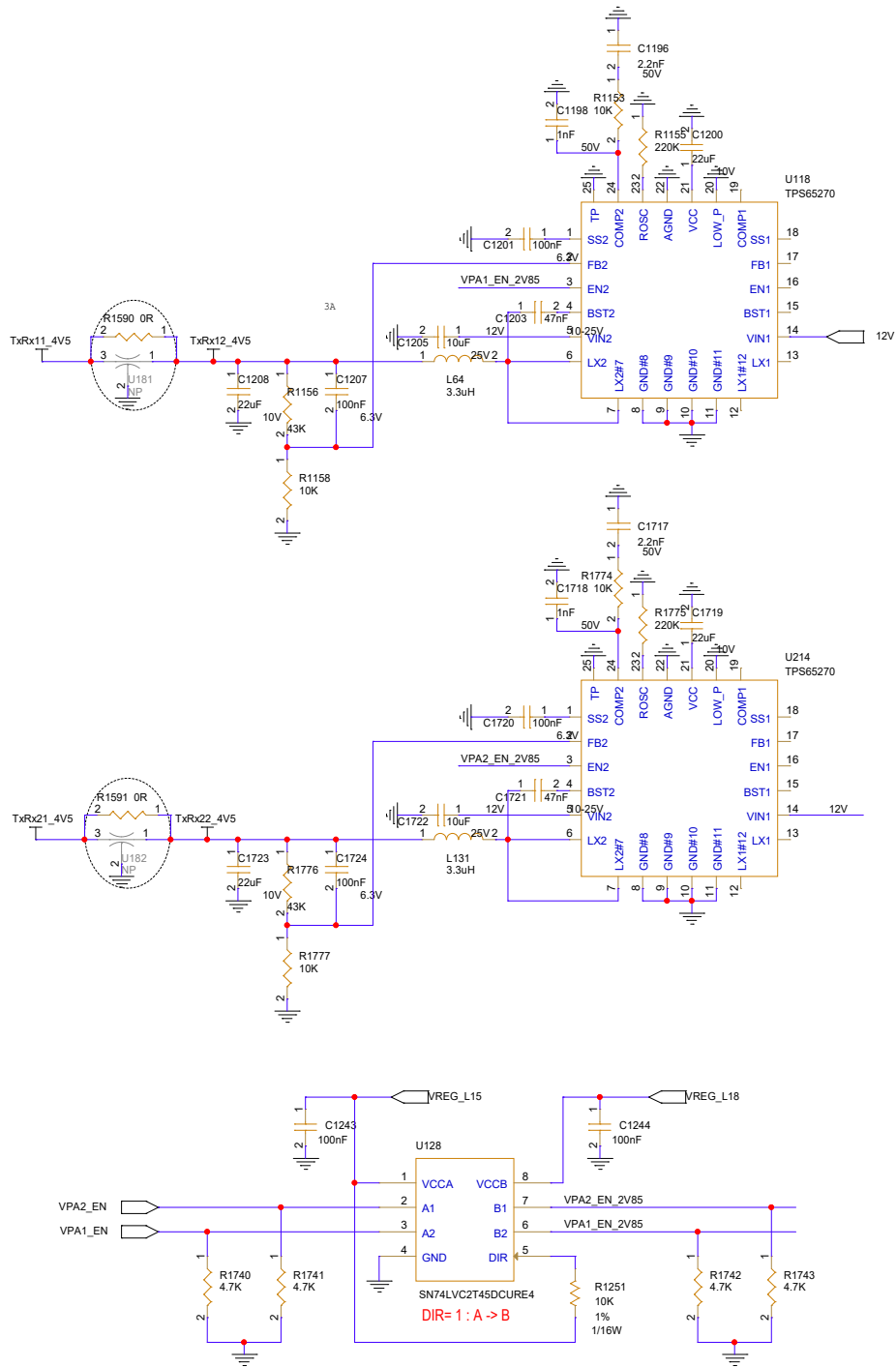
A1	GND#A1	N3	
A11	GND#A11	N7	
A21	GND#A21	N15	
B6	GND#B6	N17	
B16	GND#B16	R3	
C5	GND#C5	R5	
C3	GND#C3	R7	
C7	GND#C7	R19	
C9	GND#C9	AA9	
C11	GND#C11	U1	
C13	GND#C13	U3	
C15	GND#C15	U17	
C17	GND#C17	W3	
C19	GND#C19	W5	
E3	GND#E3	W7	
E17	GND#E17	W9	
G3	GND#G3	W11	
G7	GND#G7	W13	
J7	GND#J7	W15	
G19	GND#G19	W17	
J3	GND#J3	W19	
J13	GND#J13	W21	
J15	GND#J15	Y6	
J19	GND#J19	Y16	
L3	GND#L3	AA1	
L11	GND#L11	AA5	
L19	GND#L19	AA11	
		AA21	
		A15	
		B10	
		GND#A15	
		GND#B10	
		GND#Y10	



<b>Airspan Networks</b>			
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FTR8900_1	FTR8900_1	FTR8900_1	A
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File	Page Name	Schematic Name	Ver
FTR8900_2	FTR8900_2	FTR8900_2	A
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<b>Size</b> A3	<b>Page Name</b> PA's REGULATOR	<b>Schematic Name</b> PA's REGULATOR	<b>Ver</b> A
<b>Date:</b>	Monday, October 31, 2022	<b>Sheet</b> 62	of 62